

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C
60V	65mΩ @ V _{GS} = 10V	27A
	79mΩ @ V _{GS} = 4.5V	24A

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP, and is ideal for use in:

- Backlighting
- Power management functions
- DC-DC converters

Features and Benefits

- Rated to +175°C—Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low Input Capacitance
- Wettable Flank for Improved Optical Inspections
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DIODES™ DMNH6065SPDWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

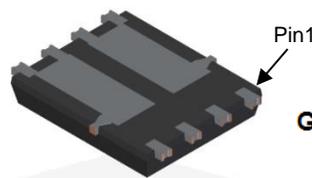
Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 Ⓔ3
- Weight: 0.097 grams (Approximate)

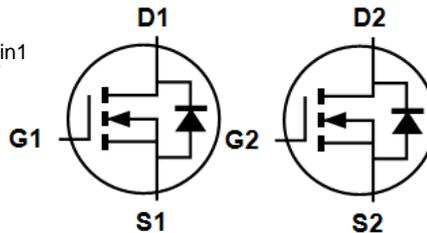
PowerDI5060-8 (SWP) (Type R)



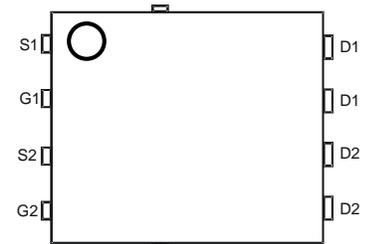
Top View



Bottom View



Equivalent Circuit



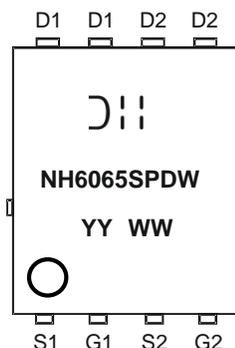
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMNH6065SPDWQ-13	PowerDI5060-8 (SWP) (Type R)	2500	Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



⌋⌋⌋ = Manufacturer's Marking
 NH6065SPDW = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 23 = 2023)
 WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Note 6)	I _D	T _C = +25°C	27
		T _C = +100°C	19
Maximum Body Diode Forward Current (Note 6)	I _S	27	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	108	A
Pulsed Source Current (10µs Pulse, Duty Cycle = 1%)	I _{SM}	108	A
Avalanche Current, L = 1mH	I _{AS}	13.3	A
Avalanche Energy, L = 1mH	E _{AS}	89	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	62	°C/W
Total Power Dissipation	P _D	2.4	W
Thermal Resistance, Junction to Case (Note 6)	R _{θJC}	2.2	°C/W
Total Power Dissipation	P _D	68	W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +175	°C

Electrical Characteristics (@T_C = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	60	—	—	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	µA	V _{DS} = 60V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	1	—	3	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	53	65	mΩ	V _{GS} = 10V, I _D = 15A
		—	68	79		V _{GS} = 4.5V, I _D = 7.5A
Diode Forward Voltage	V _{SD}	—	0.7	1.3	V	V _{GS} = 0V, I _S = 2.6A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	466	—	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	124	—		
Reverse Transfer Capacitance	C _{rss}	—	9.9	—		
Gate Resistance	R _G	—	3.3	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	4.6	—	nC	V _{DS} = 30V, I _D = 20A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	9.5	—		
Gate-Source Charge	Q _{gs}	—	1.3	—		
Gate-Drain Charge	Q _{gd}	—	2.9	—		
Turn-On Delay Time	t _{D(ON)}	—	3.3	—	ns	V _{DD} = 30V, V _{GS} = 10V, R _G = 4.7Ω, I _D = 20A
Turn-On Rise Time	t _R	—	4.6	—		
Turn-Off Delay Time	t _{D(OFF)}	—	12.6	—		
Turn-Off Fall Time	t _F	—	4.3	—		
Body Diode Reverse Recovery Time	t _{RR}	—	24	—	ns	I _F = 20A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{RR}	—	20	—	nC	I _F = 20A, di/dt = 100A/µs

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate; measured with 1 channel active.
 - Thermal resistance from junction to solder point (on the exposed drain pin); measured with 1 channel active.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

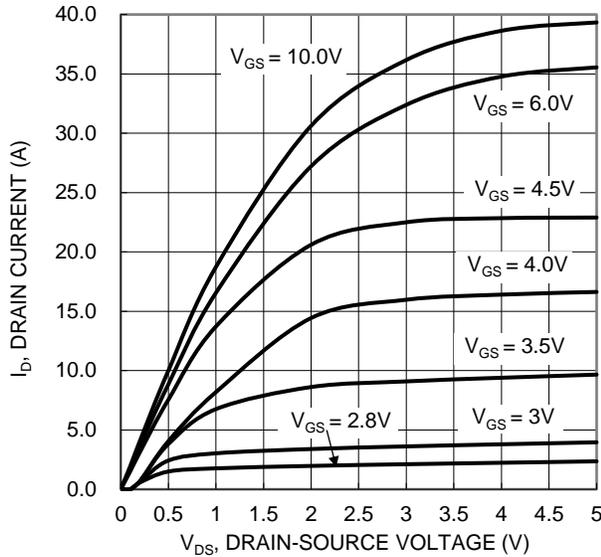


Figure 1. Typical Output Characteristic

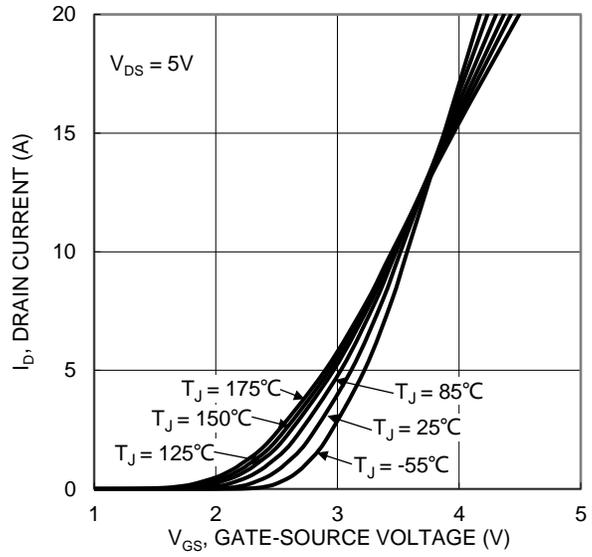


Figure 2. Typical Transfer Characteristic

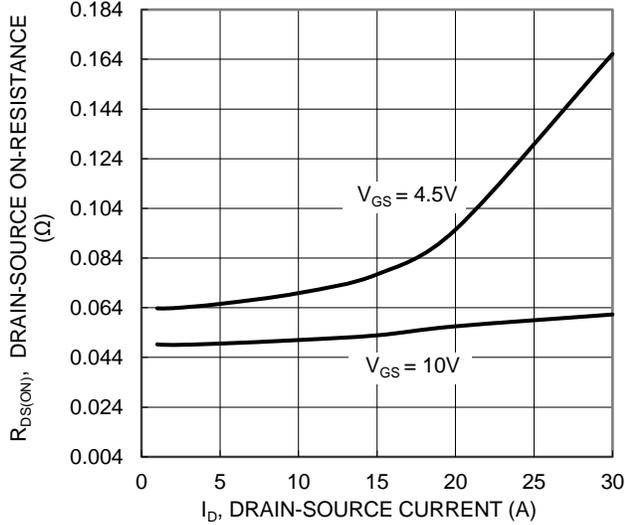


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

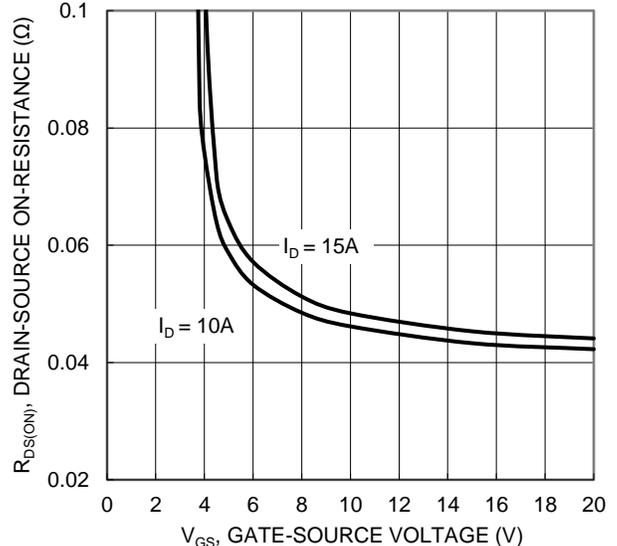


Figure 4. Typical Transfer Characteristic

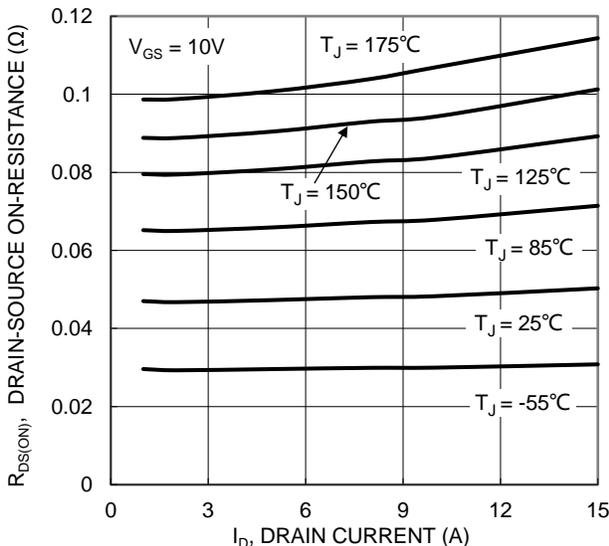


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

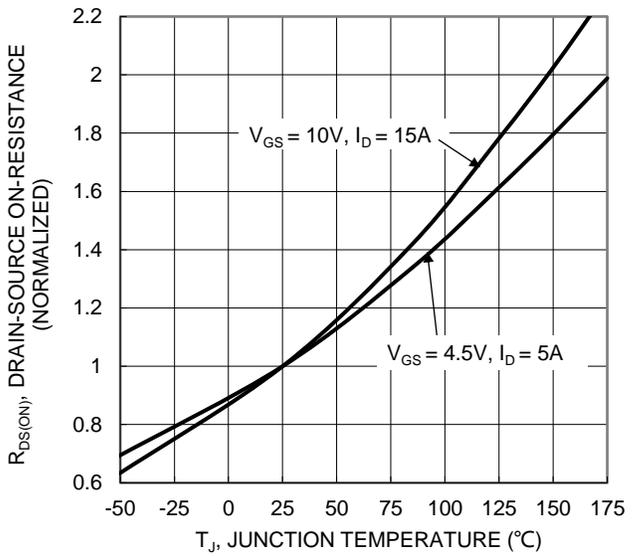


Figure 6. On-Resistance Variation with Junction Temperature

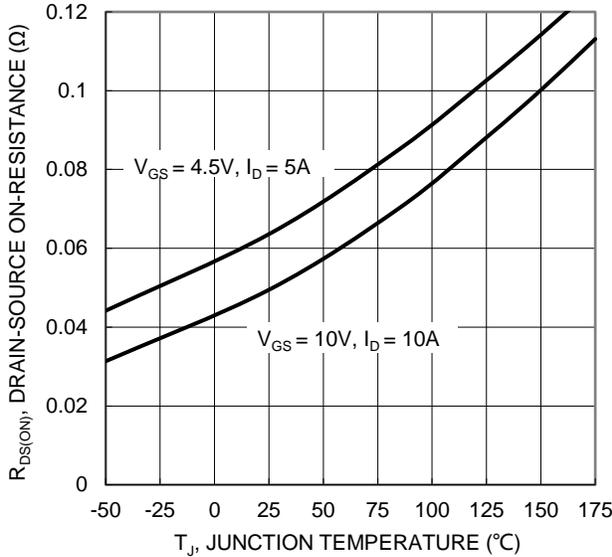


Figure 7. On-Resistance Variation with Junction Temperature

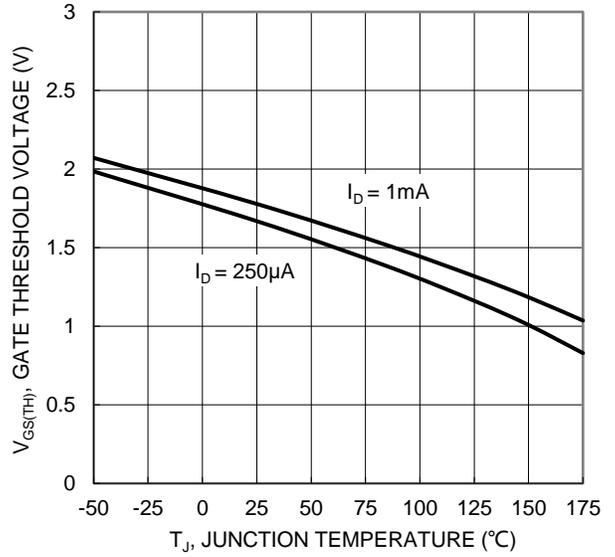


Figure 8. Gate Threshold Variation vs. Junction Temperature

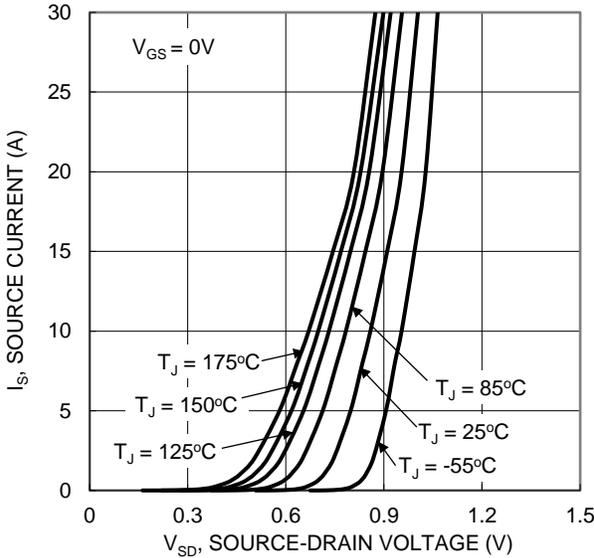


Figure 9. Diode Forward Voltage vs. Current

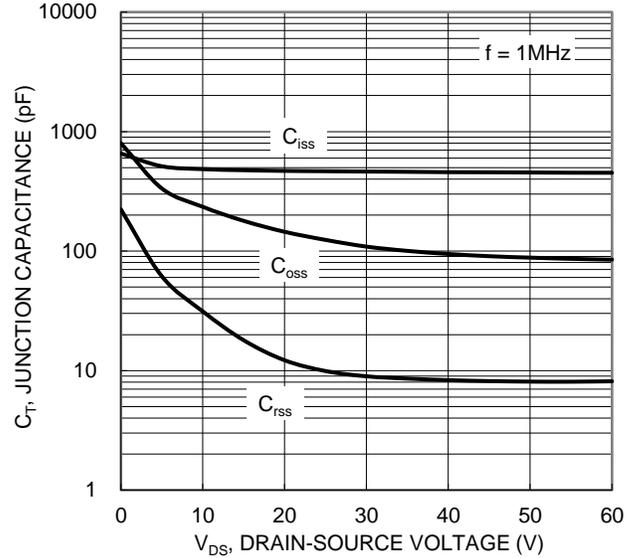


Figure 10. Typical Junction Capacitance

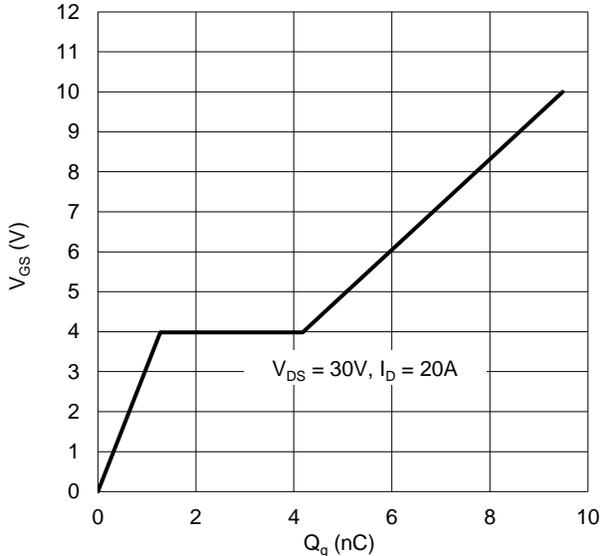


Figure 11. Gate Charge

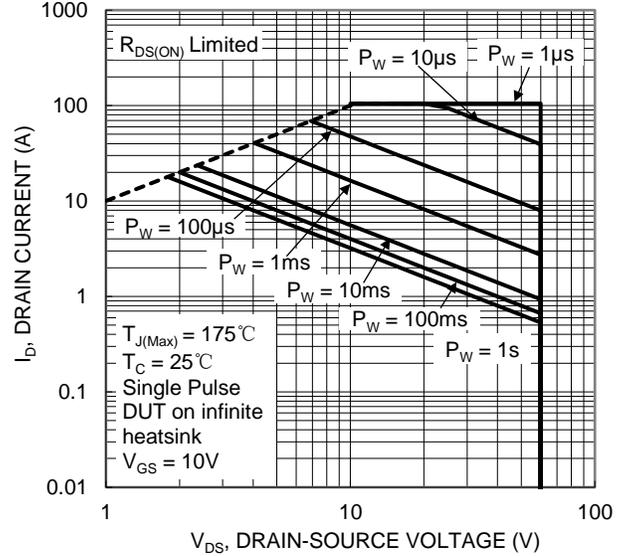


Figure 12. SOA, Safe Operation Area

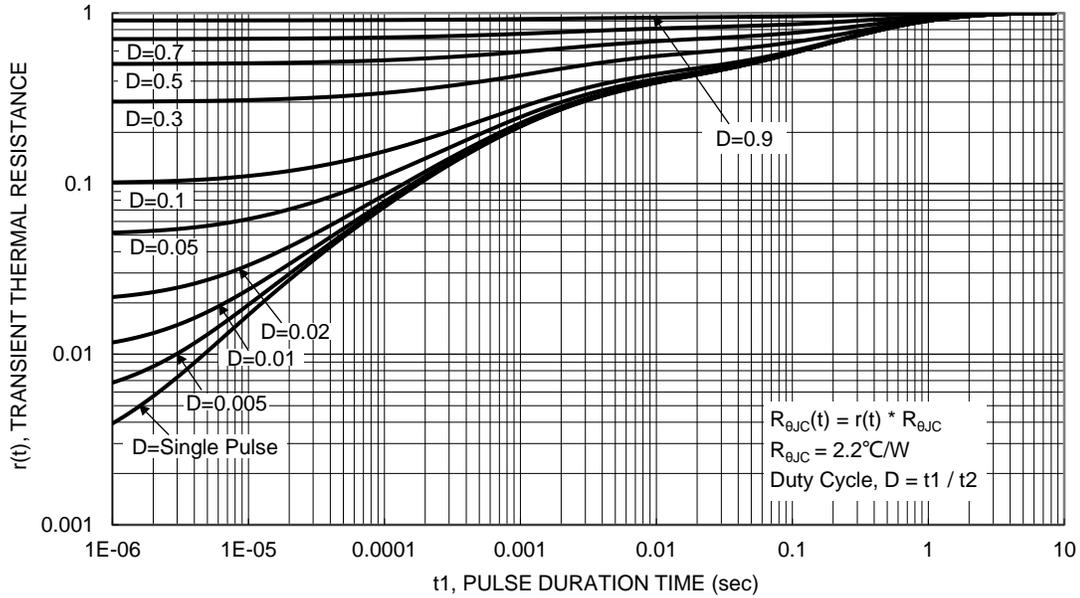


Figure 13. Transient Thermal Resistance

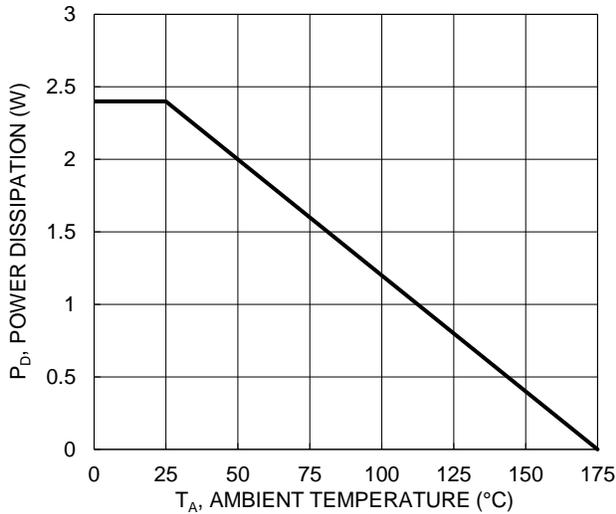


Figure 14. DC Power Derating

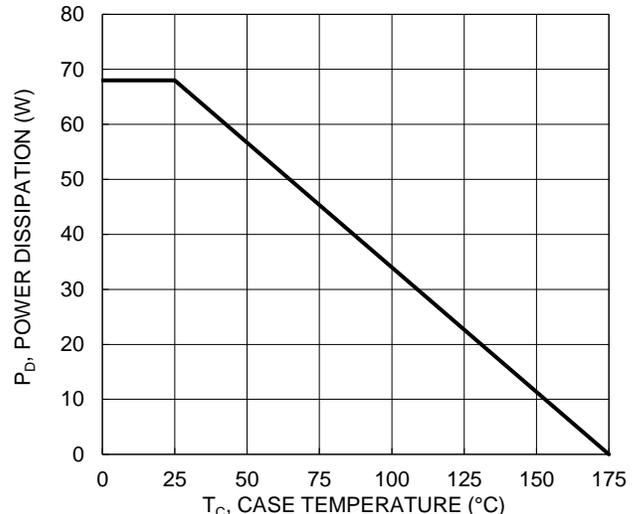


Figure 15. DC Power Derating

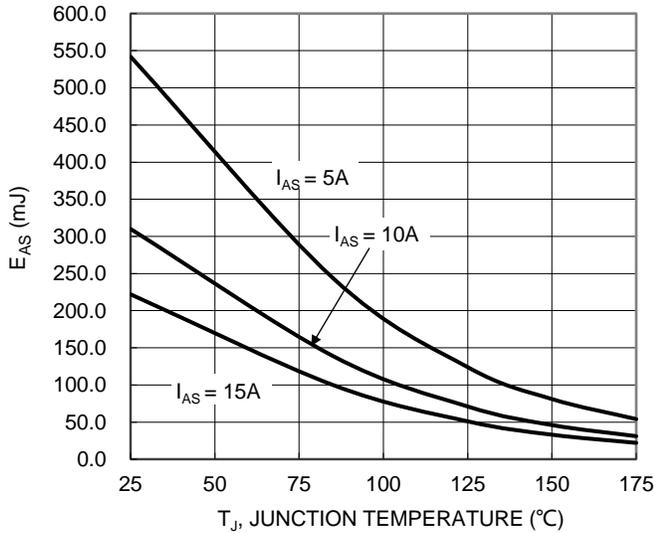
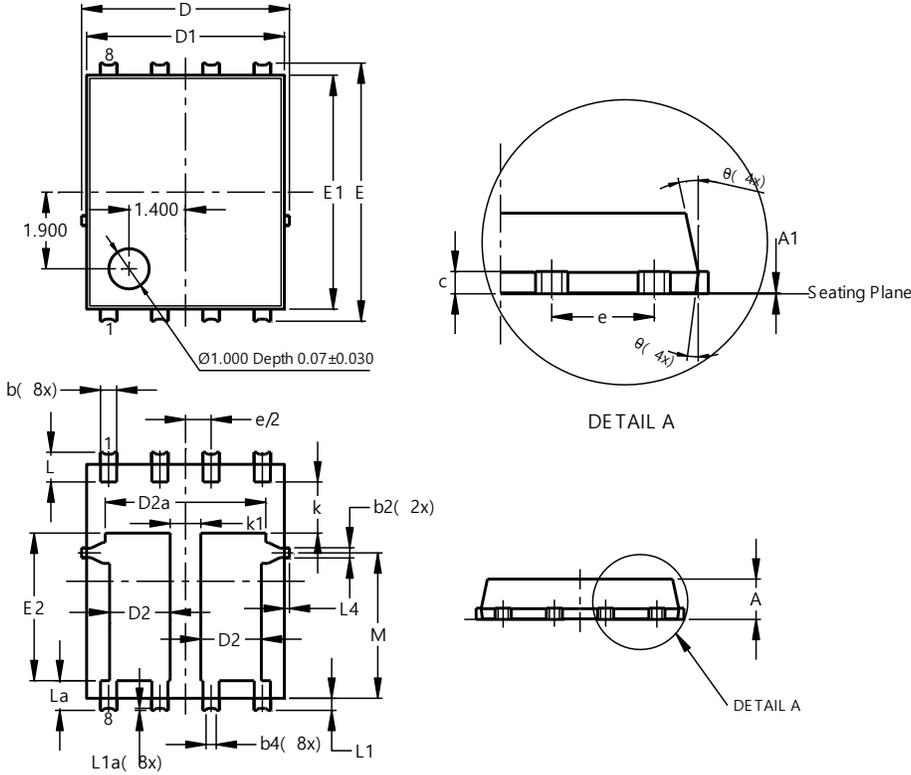


Figure 16. E_{AS} vs T_J

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (SWP) (Type R)

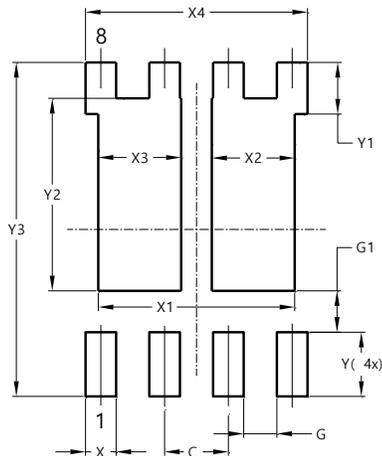


PowerDI5060-8 (SWP) (Type R)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	1.40	1.60	1.50
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
e	1.27BSC		
k	1.05	--	--
k1	0.56	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
$\theta 1$	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (SWP) (Type R)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	1.650
X3	1.650
X4	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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