

DM74LS86

Quad 2-Input Exclusive-OR Gate

General Description

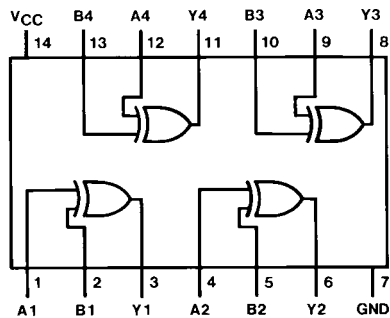
This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

DM74LS86 Quad 2-Input Exclusive-OR Gate

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			–0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –18 mA			–1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min I _{OL} = 4 mA, V _{CC} = Min		0.35 0.25	0.5 0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.2	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			40	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			–0.6	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	–20		–100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max (Note 4)		6.1	10	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

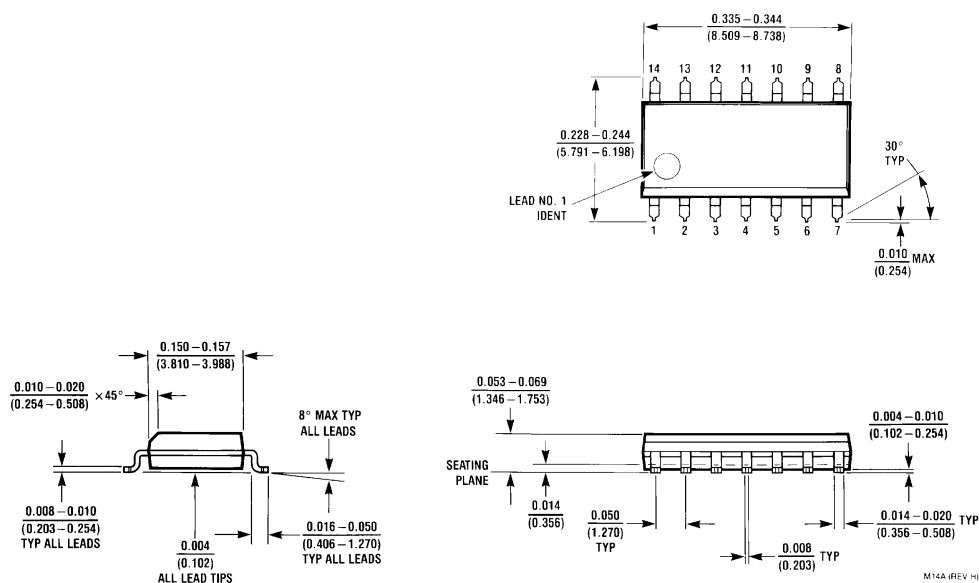
Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

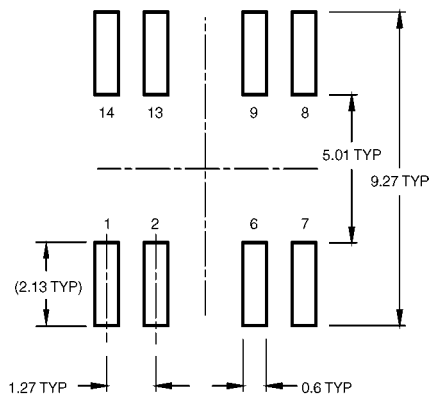
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

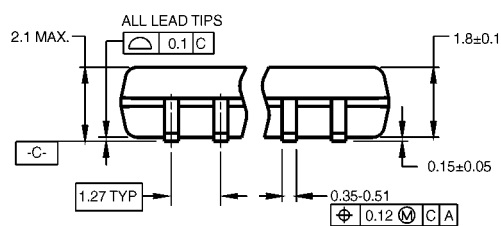
Symbol	Parameter	Conditions	R _L = 2 kΩ				Units
			C _L = 15 pF		C _L = 50 pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		18		23	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Low		17		21	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		10		15	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	High		12		15	ns



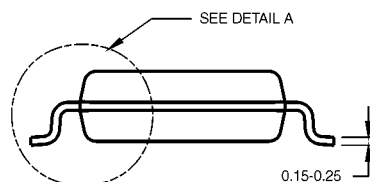
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A**



LAND PATTERN RECOMMENDATION



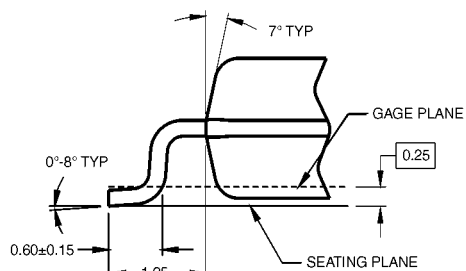
DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

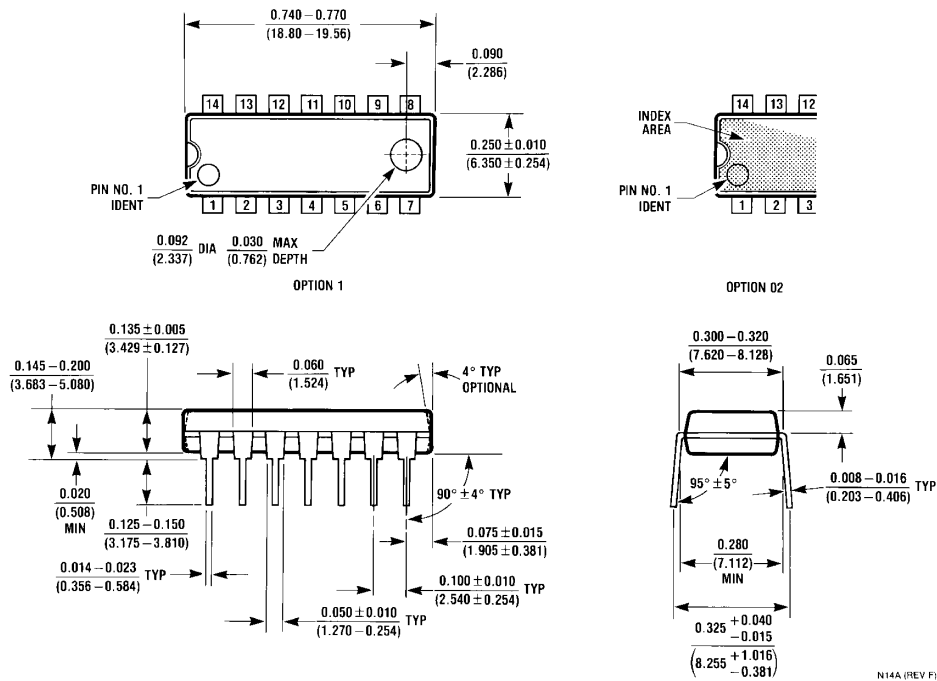
M14DRevB1



DETAIL A

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

N14A (REV F)

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