DM336P

V.34 Integrated Data/ Fax/Voice/Speakerphone Modem Device Set

General Description

The DM336P integrated modem is a four chipset design that provides a complete solution for state-of-the-art, voice-band Plain Old Telephone Service (POTS) communication. The modem provides for Data (up to 33,600bps), Fax (up to 14,400bps), Voice and Full Duplex Speaker-phone functions to comply with various international standards.

The design of the DM336P is optimized for desktop personal computer applications and it provides a low cost, highly reliable, maximum integration, with the minimum amount of support required. The DM336P modem can operate over a dial-up network (PSTN) or 2 wire leased lines.

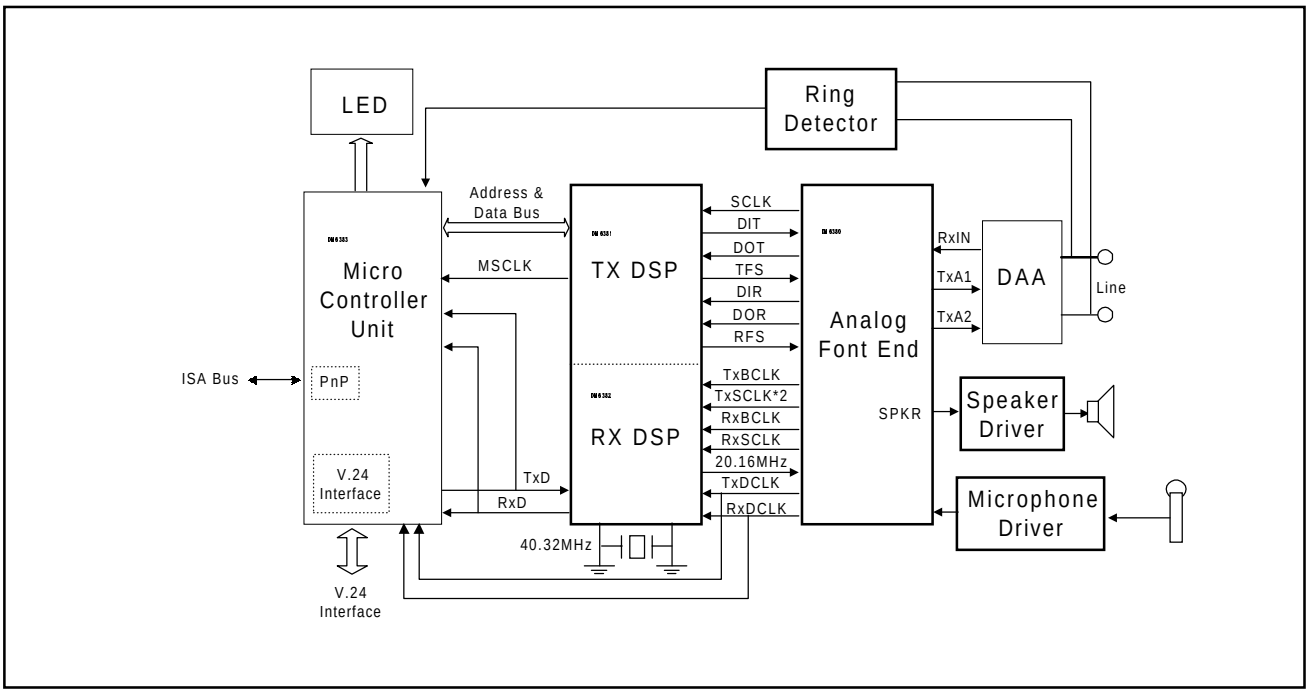
The modem integrates auto dial and answer capabilities, synchronous and asynchronous data transmissions, serial and parallel interfaces, various tone detection schemes and data test modes.

The DM336P modem's reference design is pre-approved for FCC part 68 and provides minimum design cycle time, with minimum cost to insure the maximum amount of success.

The simplified modem system, shown in figure below, illustrates the basic interconnection between the MCU, DSP, AFE and other basic components of a modem. The individual elements of the DM336P are:

- DM6380 Analog Front End (AFE). 28-pin PLCC package
- DM6381 ITU-T V.34 Transmit Digital Signal Processor (TX DSP). 100-pin QFP package
- DM6382 ITU-T V.34 Receive Digital Signal Processor (RX DSP). 100-pin QFP package
- DM6383 Modem Controller (MCU) built in Plug & Play (PnP). 100-pin QFP package

Block Diagram



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  - CCITT V.22bis (2400, 1200bps)
  - CCITT V.22 (1200bps)
  - CCITT V.23 (1200/75bps)
  - Bell 212A (1200bps)
  - Bell 103 (300bps)
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  - 2 and 4 bit ADPCM voice compression
- DTE Interface
  - DTE speed up to 115200bps
  - Serial V.24 (EIA-232-D)
- Enhanced “AT” command set and S registers
- Caller identification (Caller ID) support
- Full duplex speakerphone (Telephone Emulation)
- 16 Bits over-sampling codec
- Selectable world wide call progress tone detection
- Compromise and adaptive equalizer providing channel impairment compensation
- The channel impairment compensation
- Plug and Play (PnP) support
- Integrated UART 16550
- Enhanced 8031 compatible micro-controller
- 8 selectable interrupts
- Parallel and serial interfaces supported
  - 6-, 7- and 8- bit character support
  - Even, odd, mark and none parity detection and generation
  - 1 and 2 stop bit support
  - Auto DTE data speed detection through ”AT”
- Access up to 128K bytes external program memory
- Access up to 64K bytes external data memory
- NVRAM to store two user configurable, switchable profiles and three programmable telephone numbers
- Full duplex data mode test capabilities
  - Analog loop test

Chipset

The DM336P integrated modem device set contains 4 VLSI devices as described below:

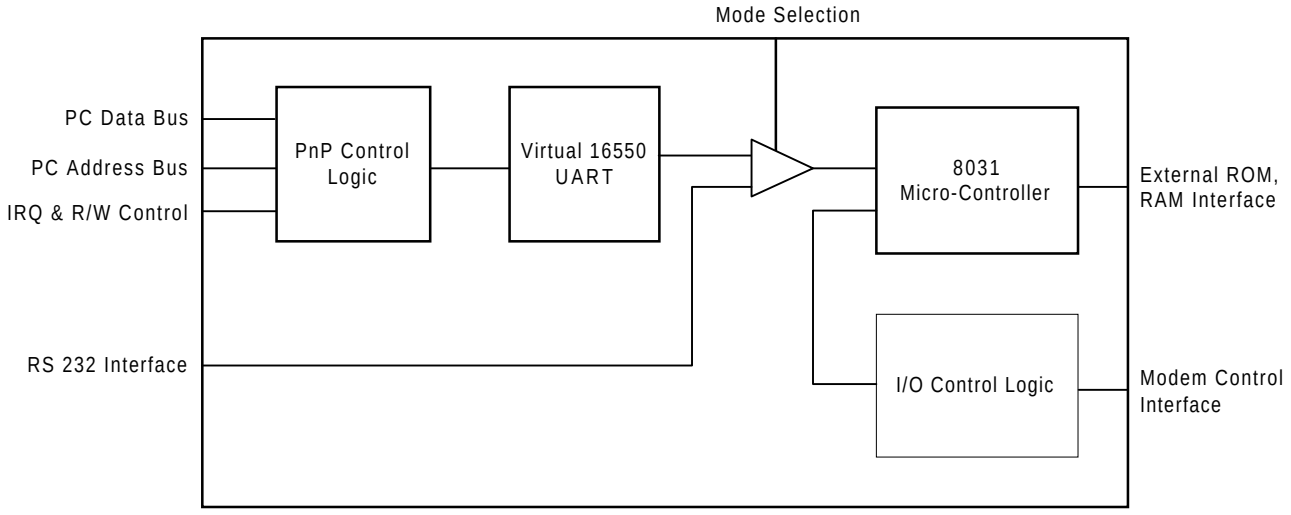
- DM6383 Modem Controller Unit with PnP for ISA (MCU)
- DM6380 Analog Front End (AFE)
- DM6381 ITU-T V.34 Transmit Digital Signal Processor (TX DSP)
- DM6382 ITU-T V.34 Receive Digital Signal Processor (RX DSP)

• Chip 1 : DM6383 Modem Controller Unit With PnP For ISA (MCU)

DM6383 Description

The DM6383 Modem Control Unit (MCU) is designed for use in high speed internal and external modem applications. Its interface is compatible with the DM6381/DM6382 Transmit and Receive Digital Signal Processor Chipset. The DM6383 incorporates a micro-controller 80C31, virtual 16550A UART (with FIFO mode), I/O and Plug & Play control logic. The DM6383 MCU performs the general modem control functions. It is also designed to provide Plug and Play capability for ISA bus systems by implementing PnP control logic. The PnP logic supports hardware & software selectable options to allow users to configure the internal modem card without jumpers.

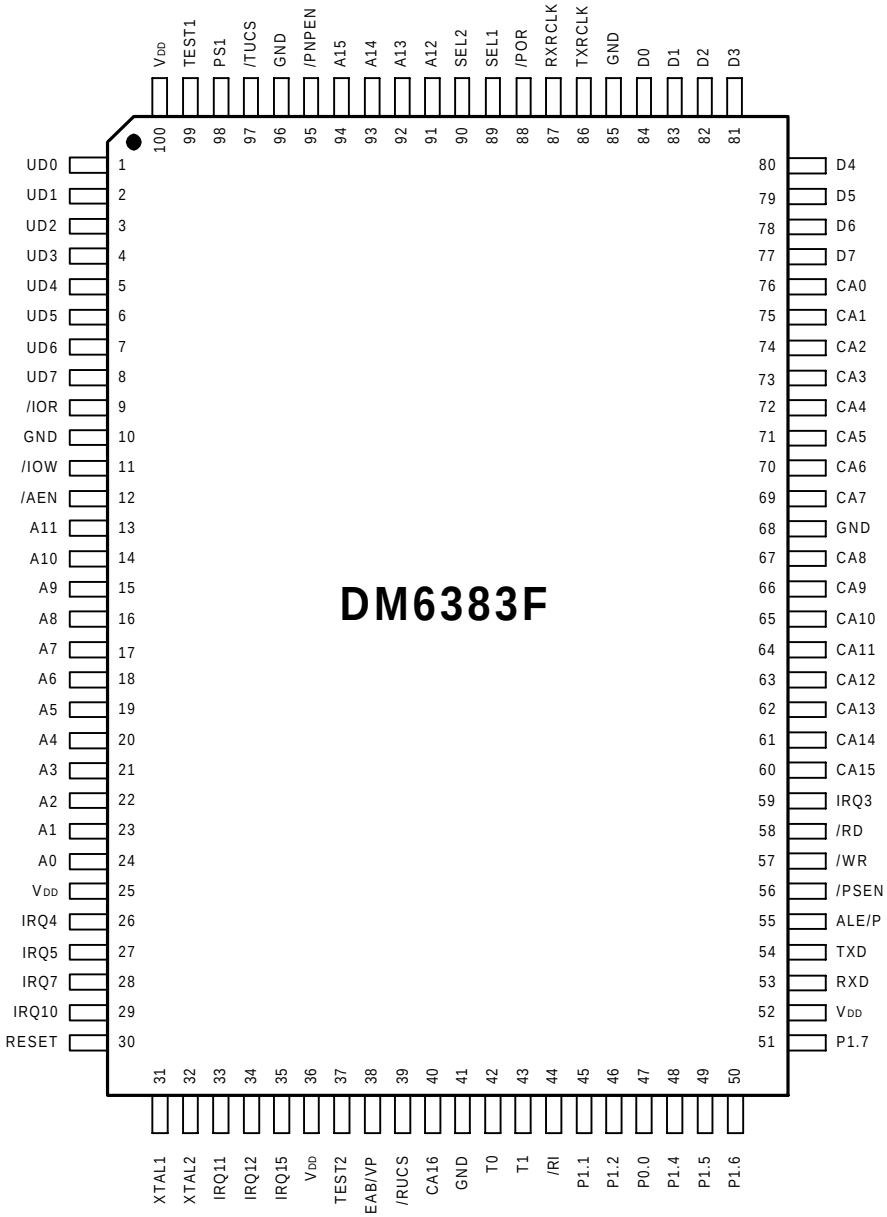
DM6383 Block Diagram



DM6383 Features

- Control interface support
- Supports parallel and serial interfaces
- Includes a micro-controller 80C31
- Maximum access 128K bytes external program memory
- Maximum access 64K bytes external data memory
- Provides automatic configuration capability to Industry
- Configuration selectable by software
- Interrupt lines selectable
- I/O base conflict avoidable
- Includes a virtual 16550A UART compatible parallel interface
- Fully programmable serial interface:
  - 6-, 7- or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1 and 2 stop bit generation
  - Baud rate generation
- Includes I/O control logic for modem control interface

DM6383 Pin Configuration



DM6383 Pin Description

Pin No.	Pin Name	I/O	Description
1 - 8	UD0 - UD7	I/O	**Data Bus Signal**, in internal modem: These signals are connected to the data bus of the PC I/O slot. They are used to transfer data between the PC and the DM6383. **Modem Control Output**, in external Modem: Memory address mapping of the controller is E800H.
9	/IOR	I	**I/O Read**: An active low signal used to read data from the DM6383.
10	GND	P	**Ground**
11	/IOW	I	**I/O Write:** An active low signal used to write data to DM6383.
12	/AEN	I	**Address Enable:** This is an active low signal to enable the system address for DM6383.
13 - 24	A11 - A0	I	**System Address:** These signals are connected to the bus of PC I/O slot. They are used to select DM6383 I/O ports.
25, 36, 52, 100	VDD	P	**+5V Power Supply**
26, 27, 28, 29, 33 - 35	IRQ4, IRQ5, IRQ7, IRQ10, IRQ11, IRQ12, IRQ15	O	**Interrupt Request:** These are 8 interrupt request pins. Only one pin, which is decoded from Configuration Register, can be activated, the other pins are left floating. The active pin will go high when an interrupt request is generated from the DM6383.
30	RESET	I	**Reset:** An active high signal used to power-on reset the DM6383.
31	XTAL1	I	**Crystal Oscillator Input**
32	XTAL2	O	**Crystal Oscillator Output**
37	TEST2	I	**Test Pin** (see description of pin 99)
38	EAB/VP	I	**External ROM Select:** Should be connected to low state.
39	/RUCS	O	**RX DSP Register Select Output:** Memory address mapping of the controller is E400H.
40	CA16	O	**Bank Switch Control:** This signal is used to switch external program memory between bank 0 (lower 64K bytes) and bank 1 (upper 64K bytes) when the EPROM for system use is 27010 (128Kx8 bits). Otherwise, this pin is not connected.
41, 68, 85, 96	GND	P	**Ground**
42	T0	I	**Controller Counter 0 Input**
43	T1	I	**Controller Counter 1 Input**
44	/RI	I	**Ring Signal Input**
45, 46, 48 - 51	P1.1, P1.2, P1.4 - P1.7	I/O	**Controller Port 1 I/O**

DM6383 Pin Description (continued)

Pin No.	Pin Name	I/O	Description
47	P0.0	O	**Modem Control Output** (memory map is bit 4 of DAA)
53	RXD	I	**Controller Serial Port Data Input**
54	TXD	O	**Controller Serial Port Data Output**
55	ALE/P	O	**Controller Address Latch Enable:** Output pulse for latching the low byte of the address during accesses to the external memory.
56	/PSEN	O	**Controller Program Store Enable:** This output goes low during a fetch from external program memory.
57	/WR	O	**Controller External Data Memory Write Control**
58	/RD	O	**Controller External Data Memory Read Control**
59	IRQ3	O	**Interrupt Request** (see description of pin 26)
60 - 67	CA15 - CA8	O	**Controller Address Bus**
69 - 76	CA7 - CA0	O	**Controller Address Bus**
77 - 84	D7 - D0	I/O	**Controller Data Bus**
86	TXRCLK	I	**Transmitter Baud Rate Clock Input** (Controller INT 0)
87	RXRCLK	I	**Receiver Baud Rate Clock Input** (Controller INT 1)
88	/POR	O	**DSP Reset Output**
89, 90	SEL1, SEL2	O	**Modem Control Output** (Memory map is bit 1-2 of DAA at memory address D000H)
91 - 94	A12 - A15	I	**System Address:** These signals are connected to the bus of the PC I/O slot. They are used to select the DM6383 I/O ports.
95	/PNPEN	I	**PnP Mode Enable:** This pin will be detected to enable/disable the PnP mode. When it is pulled down by a resistor (3.3K ~ 4.7K), the DM6383 can enter the PnP mode when it receives the PnP initial key sequence. When disconnected, an internal pull up will disable the Plug and Play function.
97	/TUCS	O	**TX DSP Register Select Output:** Memory address mapping of the controller is F000H.
98	PS1	O	**Modem Control Port Select Output:** Memory address mapping of the controller is D800H.
99	TEST1	I	**Test Pin:** Used for system configuration and test mode **TEST2** / **TEST1** / **System Configuartion** 0 / 0 / Internal mode 0 / 1 / External mode 1 / 0 / Test mode 1 / 1 / Test mode

DM6383 Functional Description

1. Operating Mode Selection

The DM6383 MCU can be used with both internal and external modems. When it works within an internal modem, pin TEST2 and TEST1 must be in a low state. The DM6383 includes a virtual UART and supports a parallel interface.

When DM6383 works within an external modem, pin TEST2 must be in a low state, and pin TEST1 must be in high. The virtual UART will be disabled and the RS232 serial interface, enabled.

TEST2	TEST1	System Configuration
LOW	LOW	Internal Modem
LOW	HIGH	External Modem
HIGH	X	Test Mode

2. Micro-controller (80C31) Reference

DM6383 supports a bank switch control pin to switch external program memory between lower 64K bytes (bank 0) and upper 64K bytes (bank 1) of 27C010. In this mode, two instructions must be included in software to switch bank 0 to bank 1:
i.e.,

```
CLR     P1.3
JMP     BANK 1 ADDRESS
```

With the same way, it can also switch back to bank 0 by

```
SETB    P1.3
JMP     BANK 0 ADDRESS
```

* For detailed information about micro-controller, please see *Programmer's Guide to 8031.*

3. Micro-controller Register Description

a. UART Clock Register :
Address D4000H Reset State: 06H

Write Only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	dat6	dat5	dat4	dat3	dat2	dat1	0

The clock source of the virtual UART logic is fixed at 1.8432MHz. The clock is derived from the external crystal used by the DM6383 controller. Therefore, the UART 1.8432MHz clock must be obtained through division. When the operating frequency of the DM6383 controller changes, the divider should be changed accordingly. This divider is specified by the Configuration Register which can be written by the DM6383 controller. The address mapping of the register is D4000H: (DM6383 controller memory mapping)

Bit 0: Always 0.

Bit 6-1: B6 - B1 define the clock divider range from 2 to 64 (even number).

Bit 7: Not used.

b. UART Baud Generator Divisor Latch Register:
Address EC00H

Read only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
dat7	dat6	dat5	dat4	dat3	dat2	dat1	dat0

By reading this register, the micro-controller can monitor the value of the low byte divisor latch of the virtual UART baud generator (see DLL in next section) and determine the baud rate clock itself.

c. Modem Status Controller Register (MSCR):
Address E000H

Write only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit 0
0	0	0	0	/CTS	/DSR	/DCD	/RI

The advantage of this register is that the modem line status information can be passed to the virtual UART by the micro-controller. The resulting signals are Ring Detect (/RI), Carrier Detect (/DCD), Data Set Ready (/DSR) and Clear To Send (/CTS).

d. Modem Output Port Register: Address D000H

Write only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				PO0	SEL2	SEL1	/POR

These 4 bits work as output ports in response to the 88th, 89th, 90th and 47th pins of this chip (see pin description).

e. PnP Isolation & Resource Data Port: Address F800H

Write only
The PnP isolation and resource data can be byte-sequentially written to the corresponding memory (built-in SRAM) through this register.

f. Auto-configuration Register: Address F400H

bit2	bit1	bit0	IRQ	bit5	bit4	bit3	I/O
0	0	0	3	0	0	0	03F8-03FF(COM1)
0	0	1	4	0	0	1	02F8-02FF(COM2)
0	1	0	5	0	1	0	03E8-03EF(COM3)
0	1	1	7	0	1	1	02E8-02EF(COM4)
1	0	0	10	1	0	0	03F0-03F7(COM5)
1	0	1	11	1	0	1	02F0-02F7(COM6)
1	1	0	12	1	1	0	03E0-03E7(COM7)
1	1	1	15	1	1	1	02E0-02E7(COM8)

The default I/O base and IRQ data stored in 94C46 should be loaded to this register by micro-controller, and then enable the default configuration. Micro-controller can also get the current I/O base and IRQ information by a read from this register.

The configuration determined by this register should be disabled when the register detects the Initiation Key described in the next section.

Bit 6: When this bit is set to inform micro-controller that the current I/O base and IRQ data should be stored to 93C46 as the default setting at the next power-on reset through programming the Auto-configuration Register, this bit should be cleared by micro-controller.

Bit 7: When bit 7 is set, it enables hardware configuration set according to bit 0-bit 5 (Jumper mode) and load the proper value of PnP Registers including I/O and Interrupt Configuration Registers. This bit will be reset, when it receives PnP Initial Key sequence.

* When reset condition occurred, the I/O and Interrupt configuration registers must be reset to default value according to bit 0 - bit 5.

4. UART(16550A) Emulation Registers

a. Receiver Buffer (Read), Transmitter Holding Register (Write)

Address: 0 (DLAB=0) Reset State 00h

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
dat7	dat6	dat5	dat4	dat3	dat2	dat1	dat0

When this register address is read, it contains the parallel received data. Data to be transmitted is written to this register.

b. Interrupt Enable Register (IER): Address 1

Reset State 00h, Write Only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	Enable Mode mStatus Intr	Enable Line Status Intr	Enable TX Holding Register Intr	Enable RX Data Intr

This 8-bit register enables the four types of interrupts as described below. Each interrupt source can activate the INT output signal if enabled by this register. Resetting bits 0 through 3 will disable all UART interrupts.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4-7: Not used

c. Interrupt Identification Register (IIR): Address 2

Reset State 01h, Read only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
FIFO Enable	0	0	0	D3: INTD2	D2: INTD1	D1: INTD0	D0: int Pending

In order to provide minimum software overhead during data transfers, the virtual UART prioritizes interrupts into four levels as followed: Receiver Line Status (priority 1), Receiver Data Available (priority 2), Character Timeout Indication (priority 2, FIFO mode only), Transmitter Holding Register Empty (priority 3), and Modem Status (priority 4).

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR indicates the highest priority interrupt that is pending, as indicated by bits INTD(2-0).

Bit 0: This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When this bit is a logic 0, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending, and polling (if used) continues.

Bit 1-2: These two bits of the IIR are used to identify the highest priority interrupt pending, as indicated in the table below.

Bit 3: In character mode, this bit is 0. In FIFO mode, this bit is set, along with bit 2, when a timeout interrupt is pending.

Bit 4-6: Not used

Bit 7: This bit is set when FCR0 = 1.

D3	D2	D1	D0	Priority Level	Interrupt Type	Condition	Reset
0	0	0	1	-	-	-	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reads the Line Status Register
0	1	0	0	Second	Receiver Data Available	Receiver Data Available or Trigger Level Reached	Reads the Receiver Buffer Register or the FIFO Drops Below The Threshold Value
1	1	0	0	Second	Character Timeout Indication	No characters have been read from or written to the Rx FIFO during programming time interval, and the Rx FIFO is not empty	Reads The Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reads the IIR Register or (if source of interrupt) Writes To The Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send, Data Set Ready, Ring Indicator or Data Carrier Detected	Reads the Modem Status Register

d. FIFO Control Register (FCR): Address 2

Reset State 00h , write only

bit7	bit6	bit 5	bit 4	bit3	bit2	bit1	bit0
RCVR Trig (MSB)	RCVR Trig (LSB)	0	0	DMA Mode	TxFIFO Reset	RxFIFO Reset	FIFO Enable

This is a write only register at the same location as the IIR, which is a read only register. This register is used to enable the FIFOs, clear the the FIFOs, set the RxFIFO trigger level, and select the type of DMA signal.

Bit 0: Writing a 1 to FCR0 enables both transmit and receive FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO mode to Character mode (and vice versa), data is automatically cleared from the FIFOs.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RxFIFO and resets its counter logic to 0.

Bit 2: Writing a 1 to FCR2 clears all bytes in the TxFIFO and resets its counter logic to 0.

Bit 3: Setting FCR3 to 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1.

Bit 4-5: Reserved

Bit 6-7: FCR6, FCR7 are used to set the trigger level for the RxFIFO interrupt.

FCR6	FCR7	RxFIFO Trigger Level
0	0	01
0	1	04
1	0	08

e. Line Control Register (LCR): Address 3

Reset State 00h, Write Only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DLAB	SBRK	STP	EPS	PEN	STB	WLS1	WLS0

This register is available to maintain compatibility with the standard 16550 register set, and provides information to the internal hardware that is used to determine the number of bits per character.

WLS1	WLS2	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 0-1: WLS0-1 specifies the number of bits in each transmitted and received serial character.

Bit 2: This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stops are generated. If bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: Logic 1 indicates that the PC has enabled the parity generation and checking.

Bit 4: Logic 1 indicates that the PC is requesting an even number of logic 1s to be transmitted or checked. Logic 0 indicates that the PC is requesting odd parity generation and checking.

Bit 5: When bit 3, 4 and 5 are logic 1, the parity bit is transmitted and checked by the receiver as logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0, then the parity is transmitted and checked as logic 1.

Bit 6: This is a Break Control bit. When it is set to logic 1, a break condition is indicated.

Bit 7: The Divisor Latch Access bit must be set to logic 1 to access the Divisor Latches of the baud generator during a read or write operation. It must be set to logic 0 to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

f. Modem Control Register (MCR): Address 4

Reset State 00h

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	RTS	DTR

Bit 0: This bit asserts a Data Terminal Ready condition that is readable via port P1.1 of micro-controller 8031. When bit 0 is set to logic 1, the P1.1 is forced to logic 0. When bit 0 is reset to logic 0, the P1.1 is forced to logic 1.

Bit 1: This bit asserts a Request To Send condition that is readable via port P3.4 of the micro-controller 8031. Bit 1 affects P3.4 in a manner identical to that described above for bit 0.

g. Line Status Register (LSR): Address 5

Reset State 60h, Read only

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RCV	ETEMT	THRE	BI	FE	PE	OE	DR

This register provides status information to the host PC concerning the data transfer. Bit 1-4 indicate the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operations only.

Bit 0: Set to logic 1 when a received character is available in the RxFIFO. This bit is reset to logic 0 when the RxFIFO is empty.

Bit 1: An Overrun error will occur only after the RxFIFO is full and the next character has overwritten the unread FIFO data. This bit is reset upon reading the Line Status Register.

Bit 2: A value of logic 1 indicates that a received character does not have the correct even or odd parity as selected by the Even Parity Select bit. This error is set when the corresponding character is at the top of the RxFIFO. It will remain set until the CPU reads the LSR. This Parity Error indication is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE bit is reset whenever the CPU reads the contents of the Line Status Register. The FE error condition is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.h. Modem Status Register (MSR): Address 6 Reset State, bit 0-3: low, bit 4-7: input signal.

Bit 4: This bit is a Break Interrupt (BI) indicator. Bit 4 is set to logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. The BI error condition is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 5: This bit is a Transmitter Holding Register Empty indicator. Bit 5 indicates that UART is ready to accept a new character for transmission. In addition, this bit causes UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high. The THRE bit is reset to logic 0 when the host CPU loads a character into the Transmit Holding register. In the FIFO mode, this bit is set when the TxFIFO is empty, and is cleared when at least 1 byte is written to the TxFIFO.

Bit 6: This bit is the Transmitter Empty indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) is empty, and is reset to a logic 0 whenever the THR contains a character. In FIFO mode, this bit is set to 1 whenever the transmitter FIFO is empty.

Bit 7: In character mode, this bit is 0. In FIFO mode, this bit is set when there is at least one parity error, framing error, or break indication in the FIFO. If there are no subsequent errors in the FIFO, LSR7 is cleared when the CPU reads the LSR.

h. Modem Status Register (MSR): Address 6

Reset State bit 0-3 : low , bit 4-7: Input Signal

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

This 8-bit register provides the current state of the control lines from the Modem to the CPU. In addition, four bits of the Modem Status Register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem Status Register.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS (MSCR3) has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR (MSCR2) has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring indicator. Bit 2 indicates that the RI (MSCR0) has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD (MSCR1) has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to a logic 1, a Modem Status Interrupt is generated.

Bit 4: This bit reflects the value of MSCR3 (CTS).

Bit 5: This bit reflects the value of MSCR2 (DSR).

Bit 6: This bit reflects the value of MSCR0 (RI).

Bit 7: This bit reflects the value of MSCR1 (DCD).

i. Scratch Register (SCR): Address 7

Reset State 00h
This 8-bit Read/Write Register does not control the UART in any way. It is intended as a Scratch Pad Register to be used by the programmer to hold data temporarily.

j. Divisor Latch (DLL): Address 0 (DLAB = 1)

Reset State 00h

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains baud rate information from the host PC. The PC sets the Divisor Latch Register values.

k. Divisor Latch (DLM): Address 1 (DLAB = 1)

Reset State 00h

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

This register contains baud rate information from the host PC.

Note: Two 8-bit latches (DLL-DLM) store the divisor in 16-digit binary format. The desired baud rate can be obtained by dividing the 115200Hz clock by the divisor.

Desired Baud Rate	Divisor Value
50	2304
75	1536
110	1047
150	768
300	384
600	192
1200	96
2400	48
4800	24
9600	12
19200	6
38400	3
57600	2
115200	1

5. Plug and Play (PnP) Module

a. Auto-configuration Ports

Three 8-bit I/O ports are defined for the PnP read/write operations. They are called Auto-configuration ports as listed below.

Port	Type	Location
ADDRESS	W	0279H (Printer status port)
WRITE_ DATA	W	0A79H (Printer status port + 0800H)
READ_ DATA	R	Relocatable in range 0203H to 03FFH

To access the Plug and Play Register, a host should follow this procedure: Write a target register address (Register Index), choose a port (WRITE_DATA or READ_DATA), then enter data. But Plug & Play Register could be directly accessed without the need to write to the ADDRESS port before each access. The ADDESS port is also the write destination of the initiation key, which will be described later.

b. Plug and Play Registers

The Plug and Play Registers may be divided into Card Registers and Logical Device Registers. According to the Plug & Play specification, if a PnP card contains more than one logical device, there are one more copies of Logical Device Registers in the PnP card. However, the DM6383A contains only one logical device, the Card Register and Logical Device Registers are unique for each card. Those PnP registers or bits not defined below are all read with value = 0.

(1) Card Control Registers

Index	Name	Type	Definition
00H	Set RD_DATA port	W	The location of the READ_DATA port is determined by writing to this register. Bits [7:0] become ISA I/O read port address bits [9:2]. Address bits [1:0] of the READ_DATA port are always 1.
01H	Serial Isolation	R	A read to this register causes a PnP card in the Isolation state to compare one bit of the card serial ID. This process is described in more detail in the next section.
02H	Config Control	W	**Bit [0] - Reset Command Setting** This bit will reset all logical devices and restore configuration registers to their power-up values. The CSN is preserved. **Bit [1] - Wait for Key Command Setting** This bit makes the PnP card return to the Wait for Key state. The CSN is preserved. **Bit [2] - PnP Reset CSN Command Setting** This bit will reset the card CSN to 0. Note that the hardware will automatically clear the bits without any need for software to clear them.
03H	Wake [CSN]	W	A write to this register will cause all cards that have a CSN that matches the write data [7:0] to go from the Sleep state to either the 1) Isolation state if the write data for this command is zero, or 2) Configuration state if the write data is not zero.
04H	Resource Data	R	A read from this register reads the next byte of resource data. The Status Register must be polled until bit[0] is set before this register may be read.
05H	Status	R	Bit [0], when set, indicates it is ready to read the next data byte from the Resource Data Register.
06H	Card Select Number (CSN)	R/W	A write to this register sets a card CSN. After a serial identification process, the CSN value (CSN) is uniquely assigned to each ISA PnP card so that each card may be individually selected during a Wake[CSN] command.

(1) Card Control Registers (continued)

Index	Name	Type	Definition
07H	Logical Device	R	00H (Only one logical device in DM6383A)

(2) Logical Device Control Registers

Index	Name	Type	Definition
30H	Activate	R/W	For each logical device, there is one Activate register that controls whether or not the device is active on the ISA bus. Bit[0], if set, activates the logical device. Before a logical device is activated, I/O range check must be disabled.
31H	I/O Range Check	R/W	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device. **Bit[1]** - This bit, when set, enables I/O range check. I/O port range check is only valid when the logical device is inactive. **Bit[0]** - If set, this bit forces logical device to respond to I/O reads within logical device assigned I/O range with a 55H when I/O range check is in operation. If clear, the logical device drives AAH.

c. Logical Device Configuration Registers

(1) I/O Configuration Registers

Index	Name	Type	Definition
60H	I/O base address bits[15:8]	R/W	Read/write value indicating the selected I/O Lower Limit Address Bits [15:8] for I/O descriptor 0. If a logical device indicates it uses only 10 bits for decoding, then bits [15:10] need not to be supported.
61H	I/O base address bits[7:3]	R/W	Read/write value indicating the selected I/O Lower Input Address Bits [7:3] for I/O descriptor 0.

(2) Interrupt Configuration Registers

Index	Name	Type	Definition
70H	IRQ level	R/W	Read/write value indicating a selected Interrupt Level Bits[3:0] Select which ISA interrupt level is used. A value of 1 selects IRQ1, 15 selects IRQ15, etc. IRQ0 is not a valid interrupt selection.
71H	IRQ type bits [7:0]	R	Read/write value indicating which type of interrupt is used for the IRQ selected above Bit[1] - Level, 1 = high, 0 = low Bit[0] - Type, 1= level, 0 = edge for DM6383A, this register is read only with value = 02H.

(3) Vender Define Register

Index	Name	Type	Definition
F0H	Auto Configuration	R/W	The I/O base address and IRQ can be configured by CPU through this register. (It can also be configured by micro-controller. See previous section).
F1H	IRQ Status Enable	W	Before reading IRQ lines status, bit 0 must be set in order to load IRQ lines status to IRQ Status register, bit 1 enable Pull Low resistor.
F2H	IRQ Status	R	This register responds to IRQ lines status to determine which interrupt has been used by PC system. bit 0: IRQ 3 bit 1: IRQ 4 bit 2: IRQ 5 bit 3: IRQ 7 bit 4: IRQ 10 bit 5: IRQ11 bit 6: IRQ12 bit 7: IRQ15.

d. DM6383 Configuration Modes

The DM6383A is power-on in jumpless mode. The default configuration is set by loading the default value stored in 93C46 to Auto-configuration register. These values can be modified by software via the logical device configuration registers in DM Jumpless mode. This update value of new configuration is only valid temporarily and will be lost after an active PC Hardware Reset. Permanent changes of default configuration will be done by informing micro-controller to modify the content of 93C46 via Auto-configuration Register.

The Plug and Play logic can operate through two configuration modes: One is DM Jumpless mode, the other, PnP mode. There are two operating methods between the two modes: First, setting hard configuration through Initiation Key sequences, second, setting hard configuration according to the register that is used, I/O Configuration Register or Auto-configuration Register.

(1) The Initiation Key for Plug and Play

The Plug and Play logical is in sequence on powering up and must be enabled by softwares. This is achieved by a predefined series of writes (32 I/O writes) to the Address port, which is called the Initiation Key. The proper series of the I/O writes is detected, then the Plug and Play read/write data ports are enabled. The Write sequence will be reset and must be issued from the beginning if any data mismatch occurs. The exact sequence for Initiation Key is listed below in hexadecimal notion.

(2) PnP Initiation Key

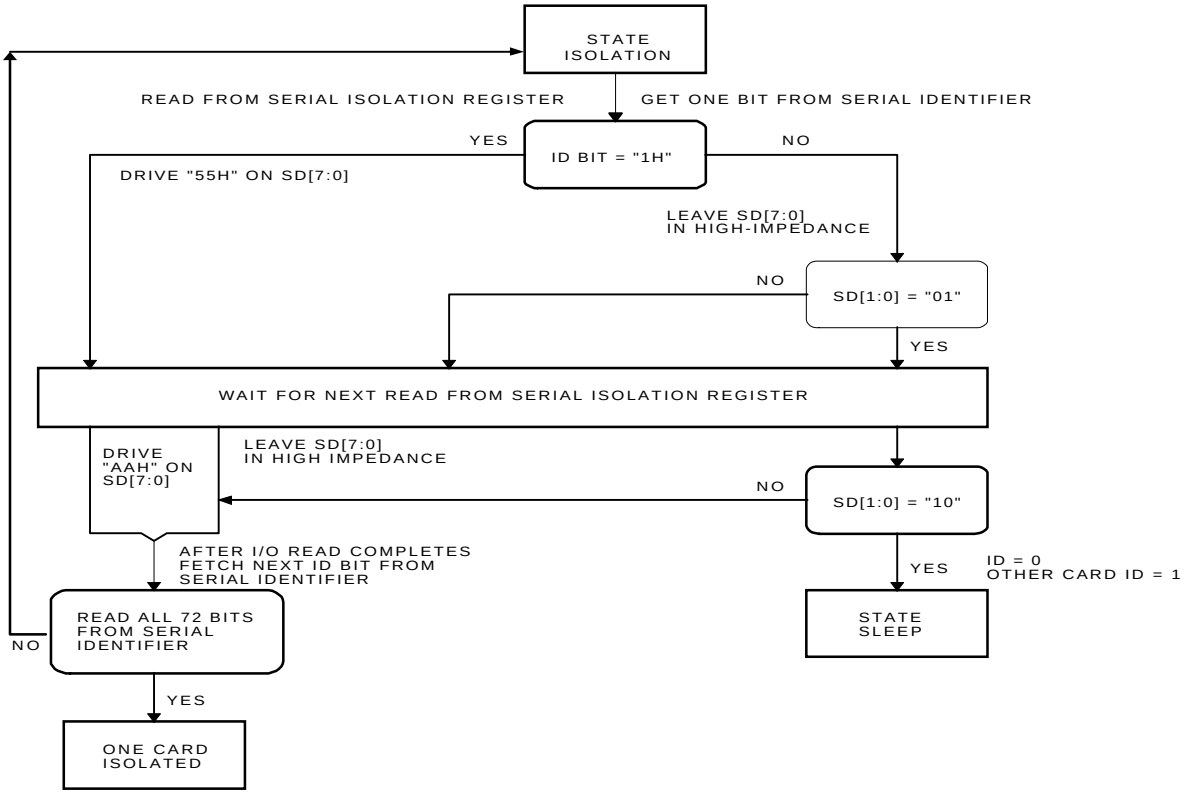
6A, B5, DA, ED, F6, FB, 7D, BE, DF, 6F, 37, 1B, 0D, 86, C3, 61, B0, 58, 2C, 16, 8B, 45, A2, D1, E8, 74, 3A, 9D, CE, E7, 73, 39

(3) DM Initiation Key

68, 34, 1A, 8D, CB, E3, 71, B8, 5C, 2E, 97, 4B, 25, 92, C9, E4, 72, B9, DC, 6E, B7, 5B, 2D, 96, CB, 65, B2, D9, EC, 76, BB, 5D

(4) Isolation Protocol

A simple algorithm is used to isolate each Plug and Play card. This algorithm uses the signals on the ISA bus and requires lock-step operation between the Plug and Play hardware and the isolation software.



(5) Serial Identifier

The key element of the Plug and Play isolation protocol is that each card contains a unique number called a serial identifier. The serial identifier is a 72-bit unique, non-zero number composed of two 32 bit fields and 8-bit checksum. The first 32-bit field is a vendor identifier. The other 32-bits can be any value, such as a serial number, part of a LAN address, or a static number, as long as no two cards in a single system will ever have the same 64-bit number. The serial identifier is accessed bit-serially by isolation logic, and is used to differentiate the cards.

Checksum	Serial Number				Vendor ID				
BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	BYTE	
7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0	SHIFT

Table 2. Shifting of Serial Identifier

The shift order for all Plug and Play serial isolation and resource data is defined as bit [0], bit [1], and so on through bit [7].

(6) Hardware Protocol

The isolation protocol can be invoked by the Plug and Play software at any time. The previously described Initiation Key puts all cards into configuration mode. The hardware on each card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value of each bit of the serial identifier, which is examined one bit at a time, as shown in Table 2.

If the current bit of the serial identifier is a "1," then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is a "0," then the card puts its data bus driver into high impedance. All cards in high impedance will check the data bus during the I/O read cycle to sense if another card is driving SD[1:0] to "01." During the second I/O read, the card(s) that drove the 55H will now drive a AAH. All high impedance cards will check the data bus to sense if another card is driving SD [1:0] to "10."

If a high impedance card senses another card driving the data bus with the appropriate data during both cycles, it ceases to participate in the current iteration of card isolation. Such cards, which lose out, will participate in future iterations of the isolation protocol.

Note: During each read cycle, the Plug and Play hardware drives the entire 8-bit data bus, but checks only the lower 2 bits.

If a card is driving the bus or is in high impedance state and does not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit, using the shifted bit to decide its response. The above sequence is repeated for the entire 72-bit serial identifier.

At the end of this process, one card remains. This card is assigned a handle referred to as the Card Select Number (CSN) that will be used later to select the card. Cards that have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. Cards must be assigned a CSN before they will respond to the other PnP commands.

(7) Software Protocol

The Plug and Play software sends the Initiation Key to all Plug and Play cards to place them into configuration mode. The software is then ready to perform the isolation protocol.

The Plug and Play software generates 72 pairs of I/O read cycles from the READ_DATA port. The software checks the data returned from each pair of I/O reads for the 55H or AAH driven by the hardware. If both 55H or AAH are read back, then the software assumes that the hardware has a "1" bit in that position. All other bits are assumed to be a "0."

During the first 64 bits, software generates a checksum using the received data. The checksum is compared with the checksum read back in the last 8 bits of the sequence.

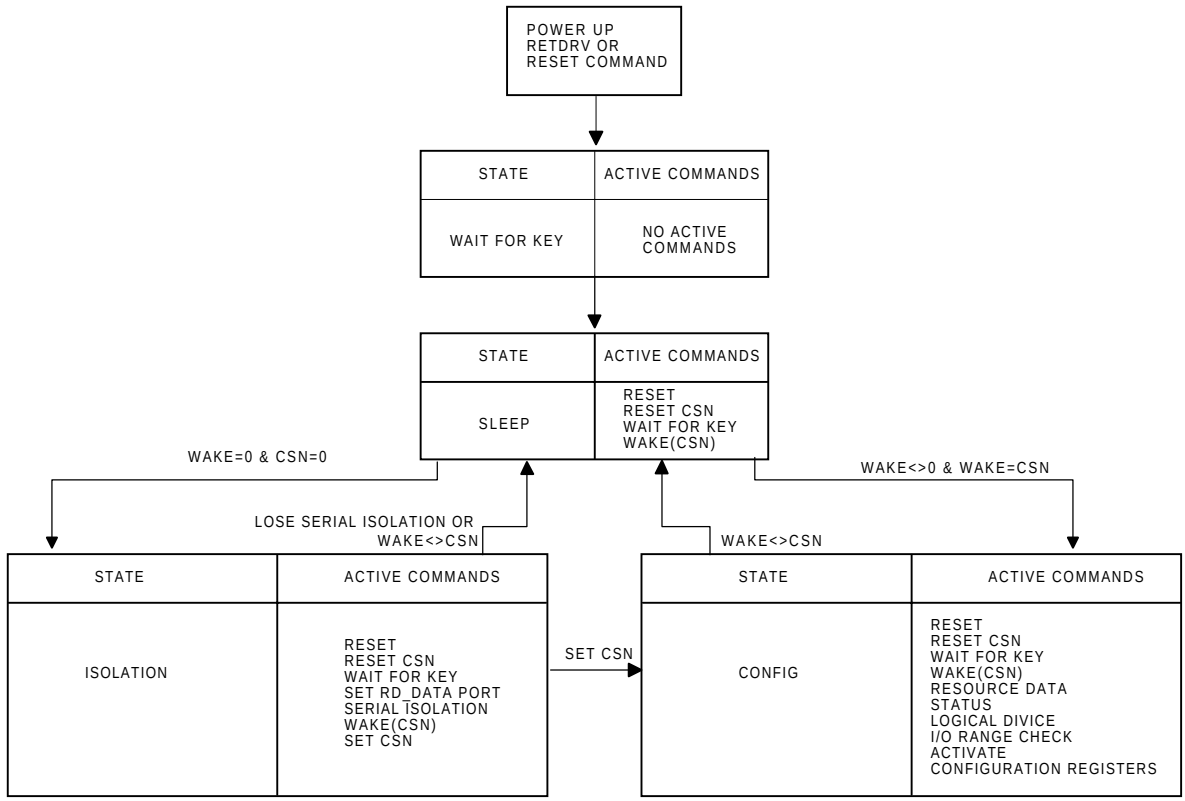
There are two other special considerations for software protocol. During an iteration, it is possible that the 55H and AAH combination is never detected. It is also possible that the checksum does not match. If either of these cases occurs on the first iteration, it must be assumed that the READ_DATA port is in conflict. If a conflict is detected, then the READ_DATA port will be relocated. The above process is repeated until a non-conflicting location for the READ_DATA port is found. The entire range between 203H and 3FFH is available; however, in practice, it is expected that only a few locations will be tried before software determines that no Plug and Play cards are present.

During subsequent iterations, the occurrence of either of these two special cases should be interpreted as the absence of any further Plug and Play cards (i.e. the last card was found in the previous iteration). This terminates the isolation protocol.

Note: The software must delay 1 msec prior to starting the first pair of isolation reads, and wait 250 msec between each sub-sequence pair of isolation reads. This delay gives the ISA card time to access information from very slow storage devices.

(8) Plug and Play Isolation Sequence

The Plug and Play isolation sequence is divided into four states: Wait for Key, Sleep, Isolation, and Configuration. The state transitions for the Plug and Play ISA card are shown below:



Note: 1. CSN = Card Select Number.
2. RSTDRV causes a state transition from the current state to Wait for Key and sets all CSNs to zero.
3. The Wait for Key command causes a state transition from the current state to Wait for Key.
4. The Reset CSN commands include PnP Reset CSN and DM Reset CSN commands. The former sets all ISA PnP cards CSNs to zero, while the latter only sets DM6383 PnP cards CSNs to zero. command will cause a state transition.

Plug and Play ISA Card State Transitions

(9) Isolation and Resource Data

DM6383 built in 64-bytes SRAM that can be accessed by micro-controller an PnP Isolation and Resource Data Registers. Through port F800H, micro-controller can load serial data and part of resource data to SRAM byte by byte. It is important to note that the length of the data frame to be programmed should be loaded first, next, isolation data, and then resource data port.

When a read from PnP resource data register occurs, the data stored in SRAM will be sent to ISA data bus, and then the data pointer will be added by 1. Once the data pointer is equivalent to the data length, the next data read will change the pointer value to the beginning of resource data block and describe the other fixed resource data.

```
Resource Data Block ={ 30, 47, 01, f8,  02, f8,  02,     08, 08,  22, 08,  00
                       30, 47, 01, f8,  03, f8,  03,     08, 08,  22, 10,  00
                       30, 47, 01, e8, 03, e8, 03,       08, 08,  22, 10,  00
                       30, 47, 01, e8, 02, e8, 02,       08, 08,  22, 08,  00
                       30, 47, 01, e8, 03, e8, 03,       08, 08,  22, 20,  00
                       30, 47, 01, e8, 02, e8, 02,       08, 08,  22, 20,  00
                       30, 47, 01, e8, 03, e8, 03,       08, 08,  22, b8,  9c
                       30, 47, 01, e8, 02, e8, 02,       08, 08,  22, b8,  9c
                       30, 47, 01, f8,  03, f8,  03,     08, 08,  22, b8,  9c
                       30, 47, 01, f8,  02, f8,  02,     08, 08,  22, b8,  9c
                       30, 47, 01, 00, 02, f8,  03,      08, 08,  22, b8,  9c
                       38, 79}
```

* The data pointer will return to 1 when a Hardware Reset or Software Wake[CSN] is occurred.

On powering up, modem card detects RSTDRV, sets CSN to 0, loads isolation data and resource data to built-in 64-bytes SRAM, programs Auto-configuration Register, configures hardware from Auto-configuration Register, and then enters the Wait for Key state. There is a required 2 msec delay from either a RSTRDV or a PnP Reset command to any Plug and Play access to allow a card to load these information via internal micro-controller.

Cards in the Wait For Key state will not acknowledge any access to their auto-configuration ports until the Initiation Key is detected and they ignore all ISA access to their Plug and Play interface. When the cards have received the initiation key, they enter the Sleep state. In this state, the cards listen for a Wake [CSN] command with the write data set to 00H. This Wake[CSN] command will send all cards to the Isolation state and reset the serial identifier/resource data pointer to the beginning.

The first time the cards enter the Isolation state, it is necessary to set the READ_DATA port address using the Set RD_DATA port command. The software should then use isolation protocol to check the selected READ_DATA port address and to see if it is in conflict with any other device.

Next, 72 pairs of reads are performed to the Serial Isolation Register to isolate a card, as previously described. When the checksum read from the card is valid, it means the card is already isolated. The isolated card remains in the Isolation state, while all other cards fail the isolation protocol and are returned to the Sleep state. The CSN on the isolated card is set to a unique number, causing this card to change to the Configuration state. Sending a Wake[0] command causes this card to change back to Sleep state, and all cards with a CSN value of zero to change to the Isolation state. This entire process will repeat until no Plug and Play cards are detected.

(10) Reading Resource Data

Each PnP card supports a resource data structure stored in a non-volatile device (e.g. 9346) that describes the resources requested by the card. The Plug and Play resource management software will arbitrate resources and setup the logical device configuration registers according to the resource data.

Card resource data may only be read from cards in the Configuration state. A card may get to the Configuration state by one of two different methods: 1) A card enters the Configuration state in response to the card "winning" the serial isolation protocol and having a CSN assigned, or 2) the card receives a Wake[CSN] command that matches the card CSN.

As described above, all Plug and Play cards function as if both of their serial identifiers and resource data come from the same serial device. Similarly, the pointer to the serial device is reset in response to any Wake[CSN] command. This implies that if a card enters the Configuration state directly from Sleep state in response to a Wake[CSN] command, the 9-byte serial identifier must be read first before the card resource data is accessed. Then the Vendor ID and Unique Serial Number is valid. however, the checksum byte, when read in this way, is not valid. For a card that enters Configuration state / Isolation state, the first read of the Resource Data Register will report resource data.

Card resource data is read by first polling the Status register and waiting for bit[0] to be set. When this bit is set, one byte of resource data is ready to be read from the Resource Data Register. After the Resource Data Register is read, the Status Register must be polled before reading the next byte of resource data. This process will repeat until all resource data is read.

The above operation implies that the hardware is responsible for accumulating 8 bits of data in the Resource Data Register. When this operation is complete, the status bit [0] is set. When a read is performed on the Resource Data Register, status bit [0] is cleared, eight more bits are shifted into the Resource Data Register, and the status bit[0] is set again.

DM6383 Absolute Maximum Ratings*

Power Supply Voltage..... -0.5V to +7.0V

Case Operating Temperature..... 0 ^{o}C to 85 ^{o}C

Storage Temperature..... -65 ^{o}C to 150 ^{o}C

Applied Voltage On Any Pin.....
..... - 0.5V ≤ VIN ≤ VDD+0.5V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DM6383 DC Electrical Characteristics (VDD = 5V, GND = 0V; Tc = 0 ^{O}C to 85 ^{O}C)

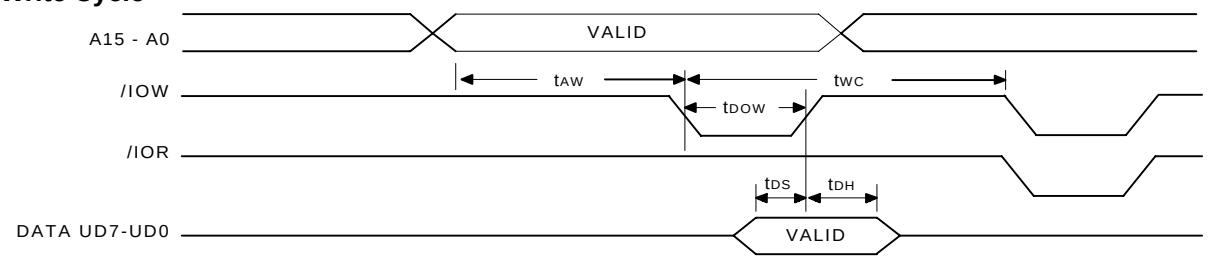
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	4.75	5.0	5.25	V	
IDD	Operating Current		30		mA	
VIH	Input High Voltage	2.0			V	
VIL	Input Low Voltage			+0.8	V	
ILI	Input Leakage Current	-10		10	• A	VIN = 0, 5.25V
VOH	Output High Voltage	2.4			V	IOH = -0.5mA
VOL	Output Low Voltage			+0.4	V	IOL = 1.5mA
CIN	Input Capacitance		10.0		pF	
VILRESET	Reset Schmitt VIL			0.8	V	
VIHRESET	Reset Schmitt VIH	2.8			V	
IOH	UD Data Bus Output High Current			-15.0	mA	VOH = 2.4V
IOL	UD Data Bus Output Low Current	24.0			mA	VOL = 0.4V

DM6383 AC Electrical Characteristics (VDD = 5V, GND = 0V; Tc = 0 ^{O}C to 85 ^{O}C)

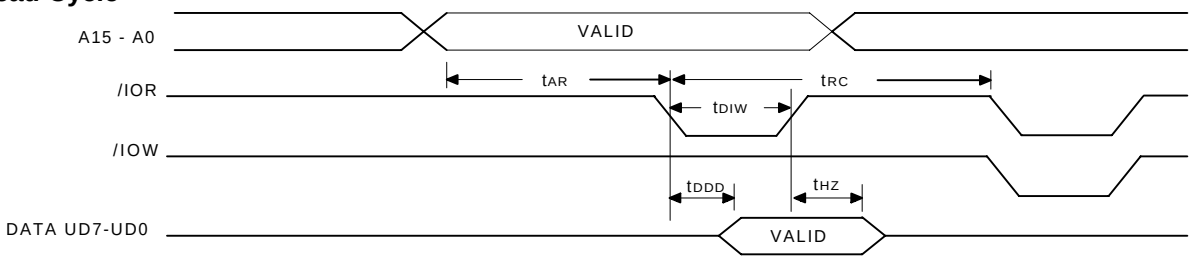
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tAW	IOW Delay from Address	30			ns	
tWC	Write Cycle	280			ns	
tDOW	IOW Strobe Width	100			ns	
tDS	Data Setup Time	30			ns	
tDH	Data Hold Time	30			ns	
tAR	IOR Delay from Address	30			ns	
tRC	Read Cycle	280			ns	
tDIW	IOR Strobe Width	125			ns	
tDDD	Delay from IOR to Data Valid			125	ns	100pF loading
tHZ	IOR to Floating Data Delay	0		100	ns	100pF loading

DM6383 Timing Waveforms

Write Cycle



Read Cycle

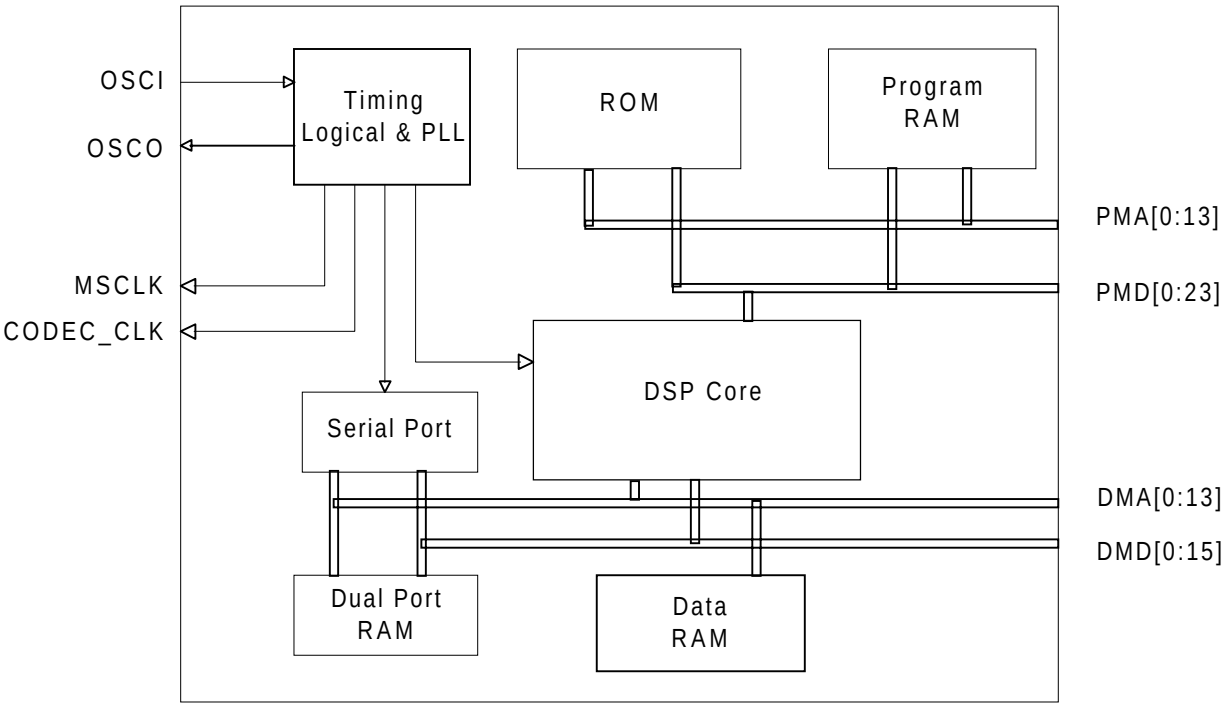


- **Chip 2: DM6381/DM6382 ITU-T V.34 TX and RX Digital Signal Processor (TX DSP and RX DSP) Description**

DM6381/82 Description

The DM6381/DM6382 are application specific Digital Signal Processors (DSP) dedicated to V.34 modem operation. They are used in pairs. The primary component of these devices is a 22.43Mips DSP core processor. The basic clock frequency of this device is 40.32MHz. An internal built PLL circuit is used to boost the clock from 40.32MHz to 80.64MHz or 89.74MHz. This 80.64MHz/89.74MHz clock is used as the clock source of DSP core processor. A 16-byte dual port SRAM is utilized to provide the communication between DSP and the DM6383. There are two dedicated serial ports that provide the link between the DSP and the DM6380. The DM6381/DM6382 are bonded-out in a 100-pin QFP package for mass production, and provide the most economical package.

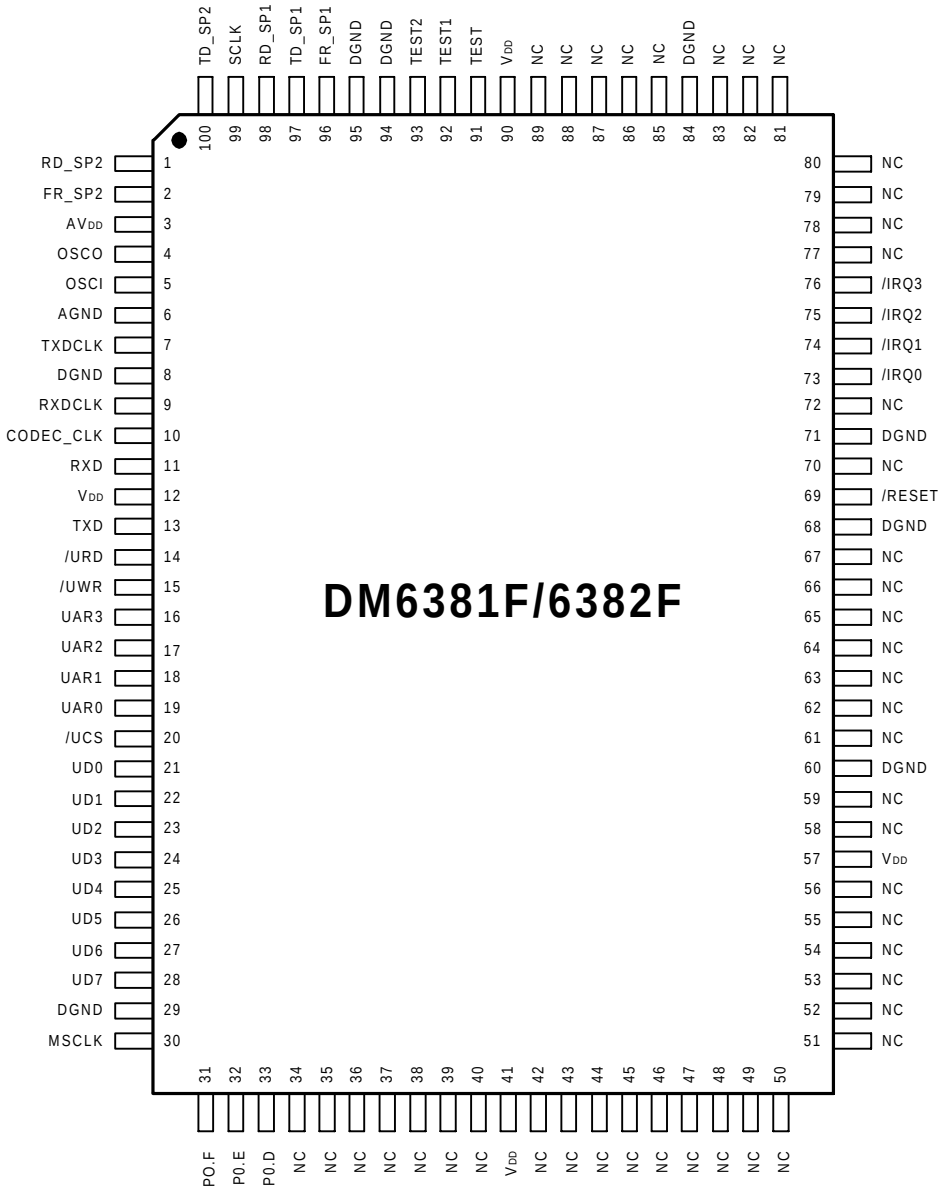
DM6381/82 Block Diagram



DM6381/82 Features

- DM6381 for TX data-pump, DM6382 for RX data-pump
- Build in program ROM
- 2 serial ports to interface with codec
- 16 byte dual port RAM
- Clock Generator for codec chip and controller chip
- Build in PLL

DM6381/82 Pin Configuration



DM6381/82 Pin Description

Pin No.	Pin Name	I/O	Description
1	RD_SP2	I	**Data Input Pin Of Serial Port 2:** The serial data is sampled at the falling edge of the SCLK. The MSB is coming immediately after falling of FR_SP2 signal.
2	FR_SP2	I/O	**Frame Signal For Serial Port 2:** This pin keeps at the low state normally and changes it's state according to the rising edge of the SCLK clock. A high to low transition initiates a data transfer.
3	AVDD	P	**Analog Power For PLL Circuit**
4	OSCO	O	**Oscillator Output Pin**
5	OSCI	I	**Oscillator Input Pin:** A 40.32MHz crystal and feedback resister should be connected between OCSI and OSCO.
6	AGND	P	**Analog Ground For PLL Circuit**
7	TXDCLK	I	**Transmit Data Rate Clock:** This pin is used as reference clock of TXD pin.
8, 29, 60, 68, 71, 84, 94, 95	DGND	P	**Digital Ground**
9	RXDCLK	I	**Receive Data Rate Clock:** This pin is used as reference clock of RXD pin.
10	CODEC_CLK	O	**20.16MHz Clock Output For DM6380 Chip**
11	RXD	O	**Modem Received Data** Shifted out to the EIA port through this pin according to the rising edge of RXDCLK.
12, 42, 57, 90, 93	VDD	P	**Digital Power**
13	TXD	I	**Modem Transmit Data** Shifted into DM6381/DM6382 from EIA port through this pin at the rising edge of TXDCLK.
14	/URD	I	**Read Indication Of Dual Port RAM**, low active.
15	/UWR	I	**Write Indication Of Dual Port RAM**, low active.
16 - 19	UAR3 - UAR0	I	**Dual Port RAM Address Bus Input** This address bus can access 16 bytes dual port RAM.
20	/UCS	I	**Dual Port RAM Chip Select Pin**, low active.
21 - 28	UD0 - UD7	I/O	**Data Bus Of The Dual Port RAM**
30	MSCLK	O	**Clock Output Pin For DM6383** The frequency of this clock can be programmed to be either 22.43MHz or 44.87MHz.
31	P0.F	O	**Output Port Bit F**
32	P0.E	O	**Output Port Bit E**
33	P0.D	O	**Output Port Bit D**
34	P0.C	O	**Output Port Bit C**
35 - 41, 43 - 56, 58, 59, 61 - 67, 70, 72, 77 - 83, 85 - 89	NC	-	**No Connection**

DM6381/82 Pin Description (continued)

Pin No.	Pin Name	I/O	Description
69	/RESET	I	**Reset Pin Of DSP Chip**, low active.
73	/IRQ0	I	**Interrupt 0 Input**
74	/IRQ1	I	**Interrupt 1 Input**
75	/IRQ2	I	**Interrupt 2 Input**
76	/IRQ3	I	**Interrupt 3 Input**
91 - 92	TEST, TEST1	I	These three pins define the testing mode operation of DM6381/DM6382 as followed: When Test=0 Test1 0, PLL output clock is 89.74MHz. 1, PLL output clock is 80.64MHz. When Test=1: Reserved for mass production testing mode. All these 2 pins are pulled low internally.
96	FR_SP1	I/O	**Frame Signal Of Serial Port 1**
97	TD_SP1	O	**Data Output Pin Of Serial Port 1** The serial data is clocked out through this pin according to the rising edge of SCLK. The MSB is sent immediately after the falling edge of the FR_SP1 signal.
98	RD_SP1	I	**Data Input Pin Of The Serial Port 1** The serial data is sampled at the falling edge of the SCLK. The MSB is coming immediately after the falling of FR_SP1 signal.
99	SCLK	I	**Reference Clock For Serial Port 1 And Serial Port 2**
100	TD_SP2	O	**Data Output Pin Of Serial Port 2** The serial data is clocked out through this pin according to the rising edge of SCLK. The MSB is sent immediately after the falling edge of the FR_SP2 signal.

DM6381/82 Functional Description

1. System Clock

a. Reference Oscillator Clock

The reference oscillator is provided by an external 40.32 MHz crystal, this is the clock source of the Data Pump chipset.

b. DSP Clock

This DSP clock is the output of the PLL frequency synthesizer and its frequency can be selected by Test1 pin. (see pin description)

c. CODEC Clock

This clock is output via the CODEC_CLK Pin as the reference clock of the codec chip. This clock is derived from dividing reference oscillator clock by two.

d. MSCLK Clock

This clock is derived from dividing the DSP clock by 2 or 4, the divider is programmed by DIV bit (configuration register bit 14) as followed:

Config Reg bit 14	Divider
0	2
1	4

2. Serial Port

There are two serial ports to provide the interface with CODEC chip. The serial port 1 (SP1) transfer 32 bits in each frame while the serial port 2 can transfer 64 bits in each frame. The frame signal of each serial port can be configured as either input signal or output signal by the Serial Port Control Register (SPC).

3. Dual Port RAM

The 16 X 8 dual port RAM allows easy system expansion by adding another DSP or micro-processor. Address 2000h ~ 200Fh are reserved for this dual port RAM. The 8 bits dual port RAM data correspond to the MSBs of the data bus (bit 15 ~ bit 8) of the DSP core. Upon reading the dual port RAM, the 8 lsb contents (bit 7 to bit 0) are all 0. For the convenience of description, the micro-controller port is referred to as B port and the DSP port is referred to as A port.

4. Interrupt

The DSP core provides 4 nested interrupt inputs: IRQ3, IRQ2, IRQ1, IRQ0. IRQ3 is the highest priority input and IRQ0, the lowest. In the V.34 and V.32 application, the IRQ3, IRQ2 and IRQ1 are defined as external interrupt triggered from the pin IRQ3B, IRQ2B, IRQ1B respectively.

DM6381/82 Absolute Maximum Ratings*

Power supply voltage ..... -0.5V to +7.0V

Case operating temperature ..... 0 ^{o}C to 85 ^{o}C

Storage temperature ..... -65 ^{o}C to 150 ^{o}C

Applied voltage on any pin .....
..... -0.5V ≤ VIN ≤ VDD+0.5V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DM6381/82 DC Electrical Characteristics (VDD = 5V, GND = 0V; Tc = 0 ^{O}C to 85 ^{O}C)

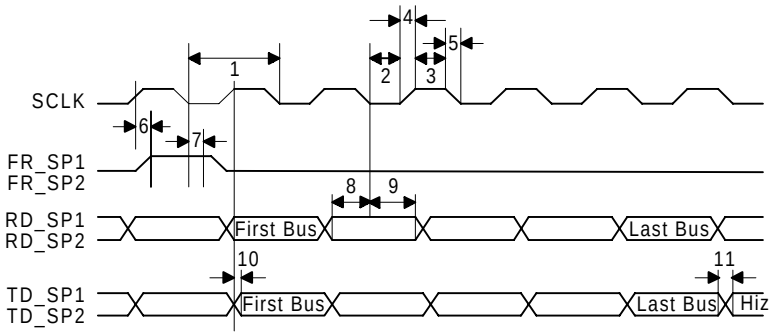
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	4.75	5.0	5.25	V	
IDD	Operating Current		85	100	mA	
VIH	Input High Voltage	2.2			V	
VIL	Input Low Voltage			+0.8	V	
ILI	Input Leakage Current	-10		10	uA	VIN = 0, 5.25V
VOH	Output High Voltage	2.4			V	IOH = 2.5mA
VOL	Output Low Voltage			+0.4	V	IOL = 2.5mA

DM6381/82 AC Electrical Characteristics

(VDD = 5V, GND = 0V; Tc = 0 ^{O}C to 85 ^{O}C, PLL out frequency = 90MHz, CL = 50pF)

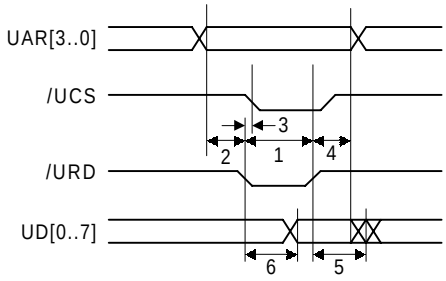
a. Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
1	SCLK Period	49			ns	
2	SCLK Low Width	20			ns	
3	SCLK High Width	20			ns	
4	SCLK Rise Time			5	ns	
5	SCLK Fall Time			5	ns	
6	Frame Delay Time			20	ns	
7	Frame To SCLK Hold	17			ns	
8	RD Valid Before SCLK Low	5			ns	
9	RD Hold Time	15			ns	
10	TD Delay Time			20	ns	



b. Dual Port RAM Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
1	/URD Read Period	100			ns	
2	Address Valid Before /URD Low	50			ns	
3	/URD to /UCS Delay Time			7	ns	
4	Data Hold Time After /URD High	4			ns	
5	Data Bus High Z After /URD High			20	ns	
6	/URD Low To Data Valid			25	ns	
7	/UWR Period	100			ns	
8	Data Setup Time /UWR High	50			ns	
9	Address Valid Before /UWR Low	50			ns	
10	/UWR To /UCS Delay			7	ns	
11	Data Hold Time After /UWR High	0			ns	

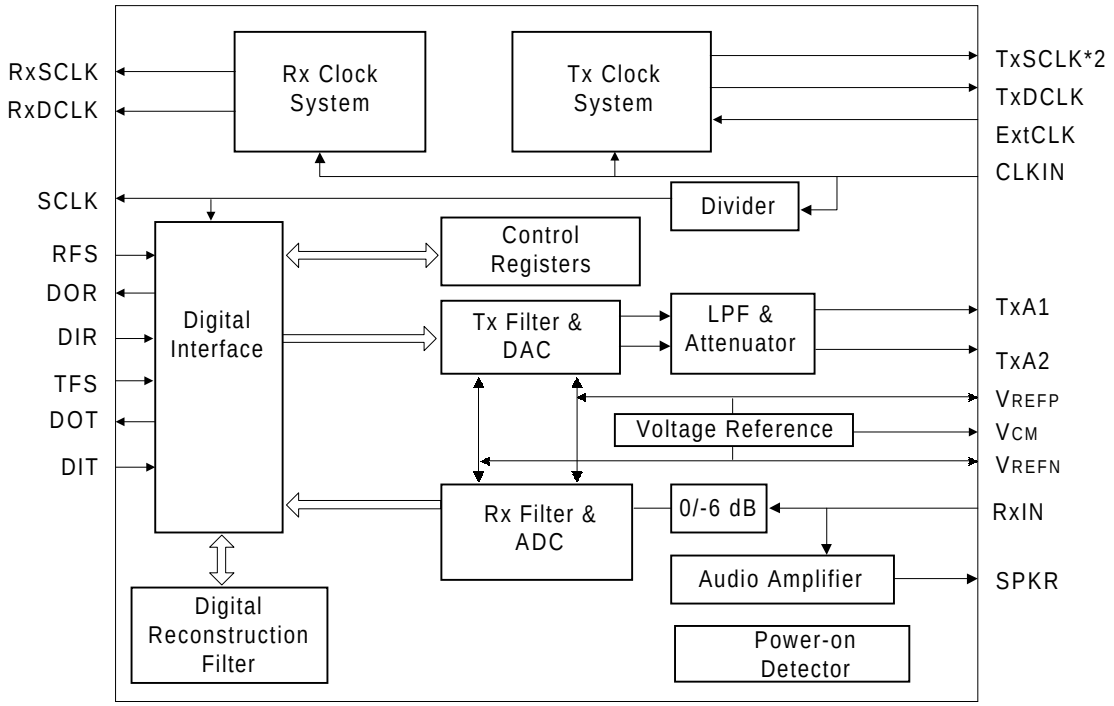


• Chip 3 : DM6380 Analog Front End (AFE) Description

DM6380 Description

The DM6380 is a single chip Analog Front End (AFE) designed to implement voice grade modem up to 33600bps. It is used as a portion of a complete modem device set. The AFE converts the analog signal into digital form and transfers the digital data to the DSP through the serial port. All the clock information needed in a modem device is also generated in this device. The differential analog outputs are provided to acquire the maximum output signal level. An audio monitor whose volume is programmable is built in to monitor the on-line signal. Inside the device, a 16-bit ADC and a 16-bit DAC with over-sampling and noise-shaping techniques is implemented to maximize performance for high speed modem. It offers wide-band transmit and receive filters so that the voice band signal is transmitted or received without amplitude distortion and with minimum group delay. In order to support the multi-mode modem standards, such as V.34, V.32bis, V.32, V.22bis, V.22, V.23, V.21, Bell 212A, Bell 103, V.17, V.29, V.27ter, the programmable baud and data rate clock generators are provided. For the asymmetric channel usage, the transmit and receive clock generators are independent. In order to provide the echo-cancel capability, the receive clock is synchronized with the transmit clock and the best receive timing sample is reconstructed by a reconstruction filter. Transmit Digital Phase Lock Loop (DPLL) is self-tuning to provide the master, slave or free-running mode for the data terminal interface. A software programmable receive DPLL that is step-controllable by the host DSP is implemented to get the best samples for the relevant signal processing.

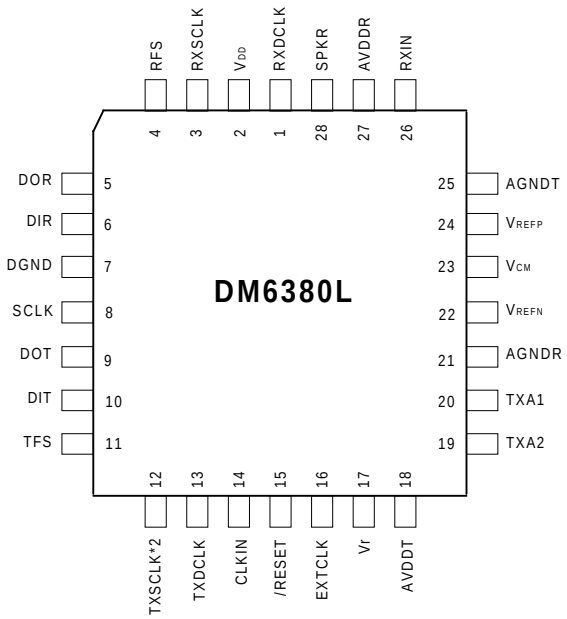
DM6380 Block Diagram



DM6380 Features

- 16-bit • -△ A/D and D/A converters
- Dynamic range : 86dB
- Total harmonic distortion : -86dB
- Separate transmit and receive clocks
- Symbol rate : 75, 300, 600, 1200, 1600, 2400, 2743, 2800, 3000, 3200, 3429Hz
- Data rate : 75, 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 33600bits per second
- Dual synchronous serial interface to host Digital Signal Processor (DSP)
- Separate transmit digital phase lock loop and receive digital phase lock loop
- Full echo cancellation capability
- Differential analog output
- Single-ended analog input
- Single power supply voltage : +5V
- Low power consumption

DM6380 Pin Configuration



DM6380 Pin Description

Pin No.	Pin Name	I/O	Description
1	RXDCLK	O	Receive Data Clock
2	VDD	P	Digital Power
3	RXSCLK	O	Receive Sample Clock
4	RFS	I	Receive Frame Synchronization
5	DOR	O	Data Output For Receiver
6	DIR	I	Data Input For Receiver
7	DGND	P	Digital Ground
8	SCLK	O	Serial Clock Synchronized With All Serial Data
9	DOT	O	Data Output For Transmitter
10	DIT	I	Data Input For Transmitter
11	TFS	I	Transmit Frame Synchronization
12	TXSCLK*2	O	Transmit Sample Clock * 2
13	TXDCLK	O	Transmit Data Clock
14	CLKIN	I	Master Clock Input (20.16MHz = 40.32MHz / 2)
15	/RESET	I	Codec Reset Input
16	EXTCLK	I	External Transmit Data Clock
17	Vr	O	Internal Reference Voltage. Connect 0.1uF to DGND
18	AVDDT	I	Analog VDD For The Transmitter Analog Circuitry (+5VDC)
19	TXA2	O	Transmit Negative Analog Output
20	TXA1	O	Transmit Positive Analog Output
21	AGNDR	P	Analog Receiver Circuitry Signal Return Path
22	VREFN	O	Negative Reference Voltage, VCM - 1V
23	VCM	O	Common Mode Voltage Output, 2.5V
24	VREFP	O	Positive Reference Voltage, VCM + 1V
25	AGNDT	P	Analog Transmitter Circuitry Signal Return Path
26	RXIN	I	Receive Analog Input
27	AVDDR	I	Analog VDD For The Receiver Analog Circuitry (+5VDC)
28	SPKR	O	Speaker Driver

DM6380 Functional Description

In this chip, we could roughly divide it into two major parts : digital portion and analog portion. The functional blocks are described separately in this section. The analog circuits include a sigma-delta modulator/demodulator, decimation/interpolation filters, a speaker driver, low-pass filter and certain logic circuits. The digital circuits is composed of Tx/Rx clock generator/PLL, serial port, serial/parallel conversions and control registers. All the clock information the analog circuits need should be provided by the digital clock system since the best sampling instant of A/D and D/A depends on the received signal and transmit signals. The data format of A/D and D/A is 2's complement.

Master clock (FQ) is obtained from an external signal connected to CLKIN. The different transmit and receive clocks are obtained by master clock frequency division in several programmable counters. The Tx and Rx clocks can be synchronized on external signals by performing the phase shifts in the frequency division process. Two independent digital phase locked loops are implemented using this principle, one for transmit clock system, the other, receive clock. The tracking of the transmit clock is automatically done by the transmit DPLL circuit. The receive DPLL circuit is controlled by the host processor and it is actually an adjustable phase shifter.

DM6380 Absolute Maximum Ratings*

Power supply voltage ..... -0.5V to +7.0V

Case operating temperature..... 0 ^{O}C to 85 ^{O}C

Storage temperature ..... -65 ^{O}C to 150 ^{O}C

Applied voltage on any pin .....
..... -0.5V ≤ VIN ≤ VDD+0.5V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational section of this specification is not implied or intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

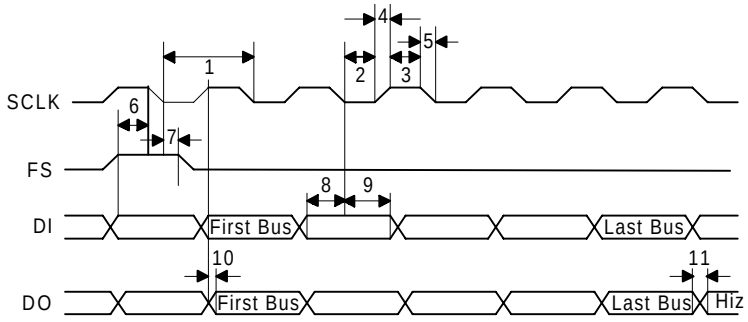
DM6380 DC Electrical Characteristics (VDD = 5V, Tc = 0 ^{O}C to 85 ^{O}C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	4.75	5	5.25	V	
VCM	Output Common Mode Voltage		2.5		V	
IDD	Supply Current		25		mA	
VIL	Input Low Voltage			0.8	V	
VIH	Input High Voltage	2.2			V	
VOL	Output Low Voltage			0.4	V	
VOH	Output High Voltage	2.4			V	
II	Input Current	-10	±1	10	μA	VI=VDD or VI=GND
CIN	Input Capacitance		5		pF	
VREF	Differential Reference Voltage Output	1.9	2	2.1	V	
VCMD_OUT	Output Common Mode Offset	-200		200	mV	=(TxA1+TxA2)/2-VCM
VDIF_OUT	Differential Output Voltage	3 *VREF		3 *VREF	V	TxA1-TxA2 ≤ 3*VREF
VOFF_OUT	Differential Output DC Offset Voltage	-100		100	mV	VDC (TXA1)-VDC (TXA2)
RIN	Input Resistance RxIN	100			kΩ	
ROUT	Output Resistance TxA1, TxA2, SPKR		1	2	kΩ	
RL	Load Resistance TxA1, TxA2, SPKR	20			kΩ	
CL	Load Capacitance TxA1, TxA2, SPKR			50	pF	

DM6380 AC Characteristics (VDD = 5V, Tc= 0 °C to 85 °C)

Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
1	SCLK Period	49			ns	
2	SCLK Low Width	24			ns	
3	SCLK High Width	24			ns	
4	SCLK Rise Time			5	ns	
5	SCLK Fall Time			5	ns	
6	FS To SCLK Setup	17			ns	
7	FS To SCLK Hold	17			ns	
8	DI To SCLK Setup	5			ns	
9	DI To SCLK Hold	5			ns	
10	SCLK High To DO Valid			8	ns	
11	SCLK To DO Hiz			8	ns	

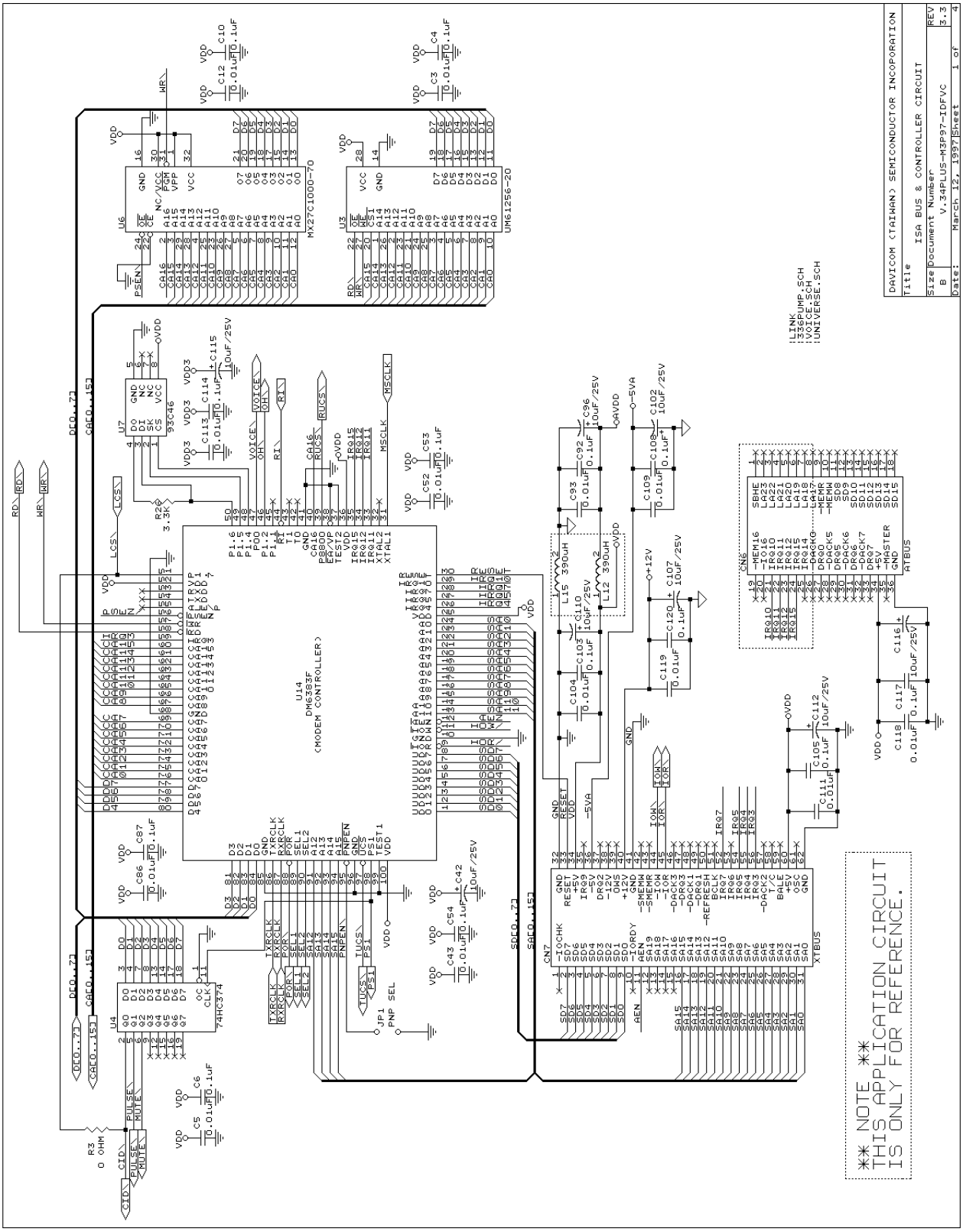


DM6380 Performance

(VDD= 5V, Tc= 0 °C to 85 °C, FQ= 20.16MHz, Measurement Band= 220Hz to 3.6KHz, RX DPLL Free Running)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Gabs	Absolute Gain At 1KHz	-0.5		0.5	dB	RX signal: VIN= 2.5 VPP, f = 1KHz
THD	Total Harmonic Distortion		-84		dB	Tx signal: VOUT (diff)= 5 VPP, f = 1KHz
DR	Dynamic Range		86		dB	f = 1KHz
PSRR	Power Supply Rejection Ratio		50		dB	f = 1KHz, VAC = 200m VPP
CTxRx	Crosstalk		95		dB	Transmit channel to receive channel

Application Circuit (For Reference Only)



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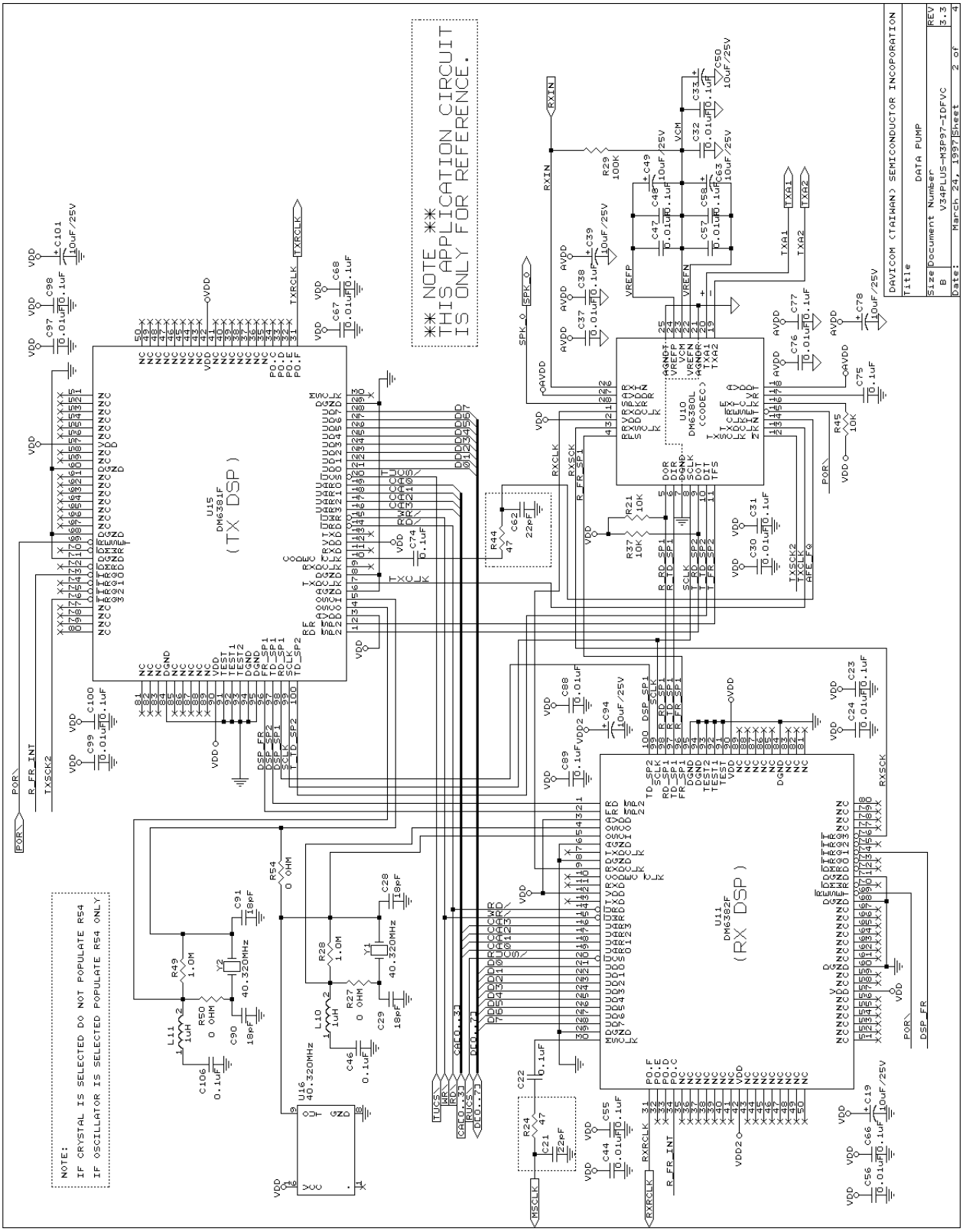
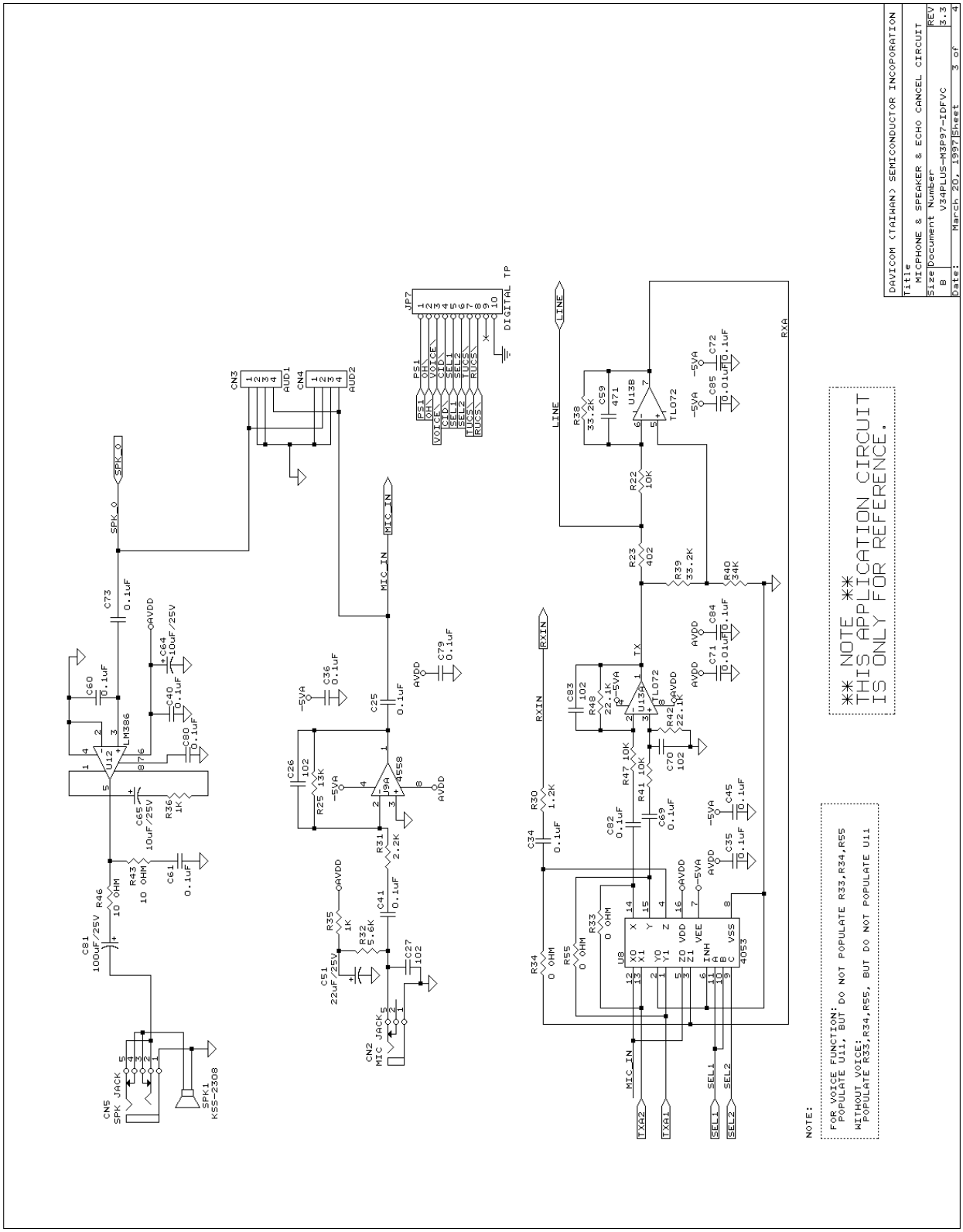
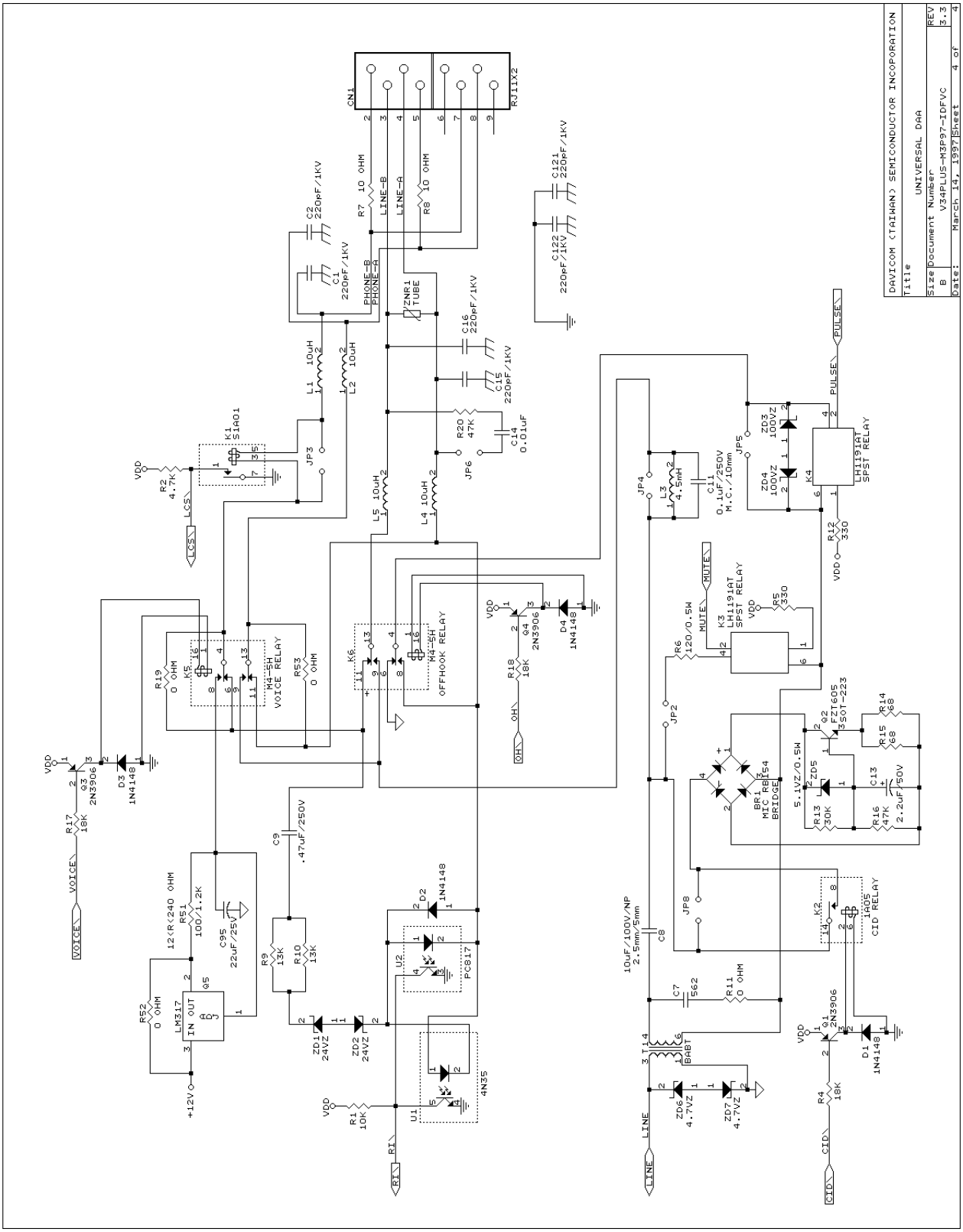


Application Circuit (For Reference Only)



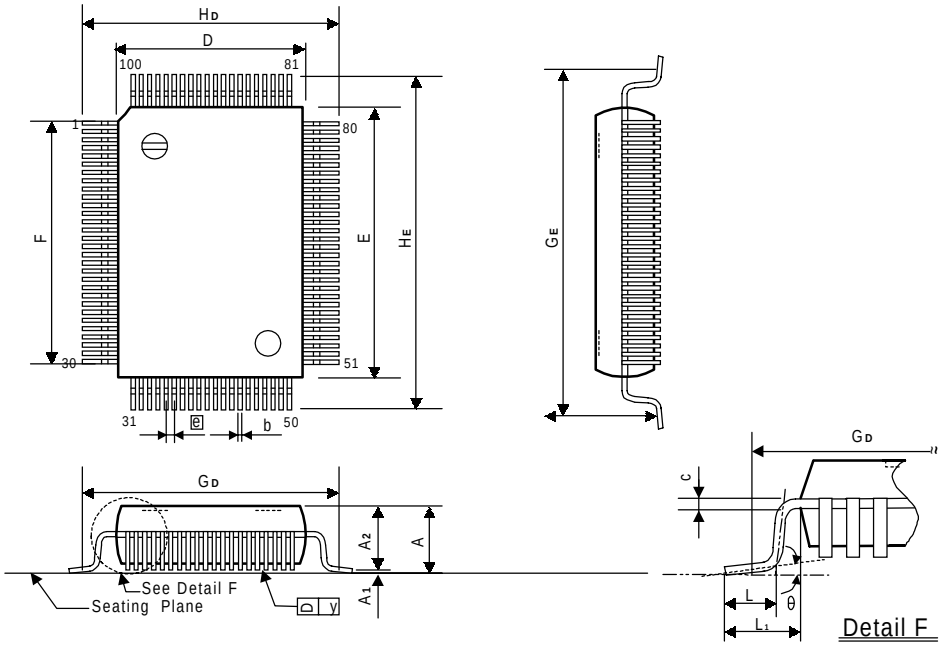
Application Circuit (For Reference Only)



Package Information

QFP 100L Outline Dimensions

unit: inches/mm



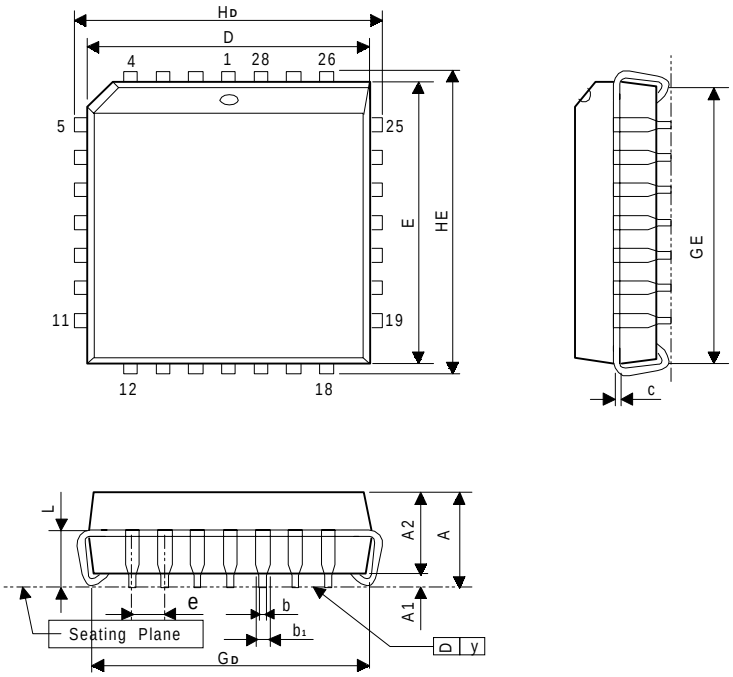
Symbol	Dimensions In Inches	Dimensions In mm
A	0.130 Max.	3.30 Max.
A**1**	0.004 Min.	0.10 Min.
A**2**	0.112± 0.005	2.85± 0.13
b	0.012 +0.004 -0.002	0.31 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.551± 0.005	14.00± 0.13
E	0.787± 0.005	20.00± 0.13
e	0.026 ± 0.006	0.65± 0.15
F	0.742 NOM.	18.85 NOM.
G**D**	0.693 NOM.	17.60 NOM.
G**E**	0.929 NOM.	23.60 NOM.
H**D**	0.740± 0.012	18.80± 0.31
H**E**	0.976± 0.012	24.79± 0.31
L	0.047± 0.008	1.19± 0.20
L_1	0.095± 0.008	2.41± 0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Note:

1. Dimensions D&E do not include resin fins.
2. Dimensions G**D** & G**E** are for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

PLCC 28L Outline Dimensions

unit: inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.185 Max.	4.70 Max.
A**1**	0.020 Min.	0.51 Min.
A**2**	0.150± 0.005	3.81± 0.13
b**1**	0.028 +0.004 -0.002	0.71 +0.10 -0.05
b	0.018 +0.004 -0.002	0.46 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.453± 0.010	11.51± 0.25
E	0.453± 0.010	11.51± 0.25
e	0.050± 0.006	1.27± 0.15
G**D**	0.410± 0.020	10.41± 0.51
G**E**	0.410± 0.020	10.41± 0.51
H**D**	0.490± 0.010	12.45± 0.25
H**E**	0.490± 0.010	12.45± 0.25
L	0.100± 0.010	2.54± 0.25
y	0.006 Max.	0.15 Max.

Note:

1. Dimensions D and E do not include resin fins.
2. Dimensions G**D** & G**E** are for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM6380L	28	PLCC
DM6381F	100	QFP
DM6382F	100	QFP
DM6383F	100	QFP

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