DAVICOM Semiconductor, Inc.

DM130036

15V / 30V Selectable Output & 40 Hi-V Channels Driver IC

DATA SHEET

PRELIMINARY

Preliminary

Version: DM130036-11-MCO-DS-P01

July 11, 2016

Content

PRELIMINARY

1 General Description

The DM130036 consists of Hi-V DC-DC charge pump for EPD (Electrophoretic display) application. User can choose 0V,15V or 30V to drive EPD. All the functions are controlled by 2-wire serial interface. DM130036 supports synchronous serial signal interface (Maximum 4 chips cascadable).

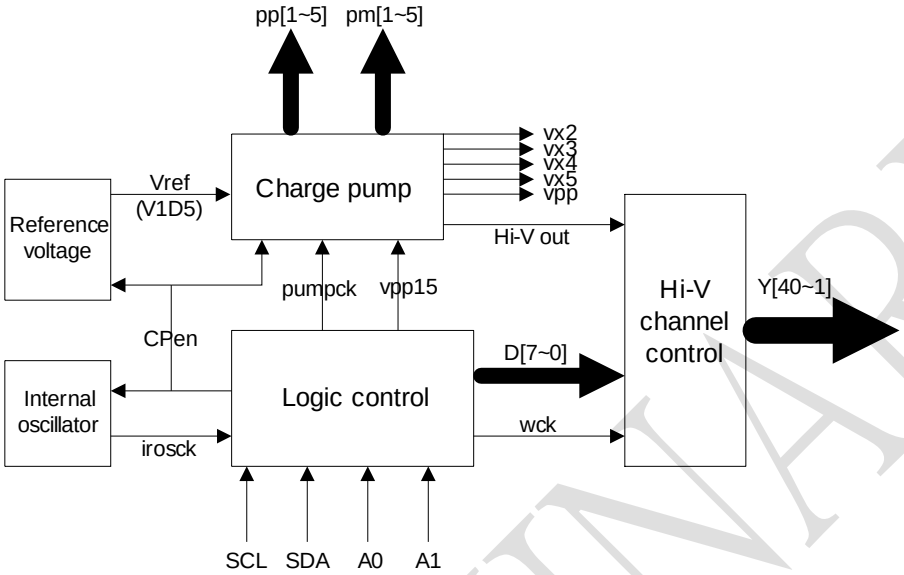
PRELIMINARY

2 Features

- Operating voltage 2.2V ~ 5.5V
- Selectable 0V,15V or 30V driving voltage for EPD
- EPD driver can also perform 3V ~ 5V application by external driven power
- 36 SEG + 2 COM + 2 Background
- DC-DC charge pump circuit
- ON chip RC oscillator
- 2-wire serial interface
- Voltage regulator
- Synchronous serial signal (Maximum 4 chips cascadable)

PRELIMINARY

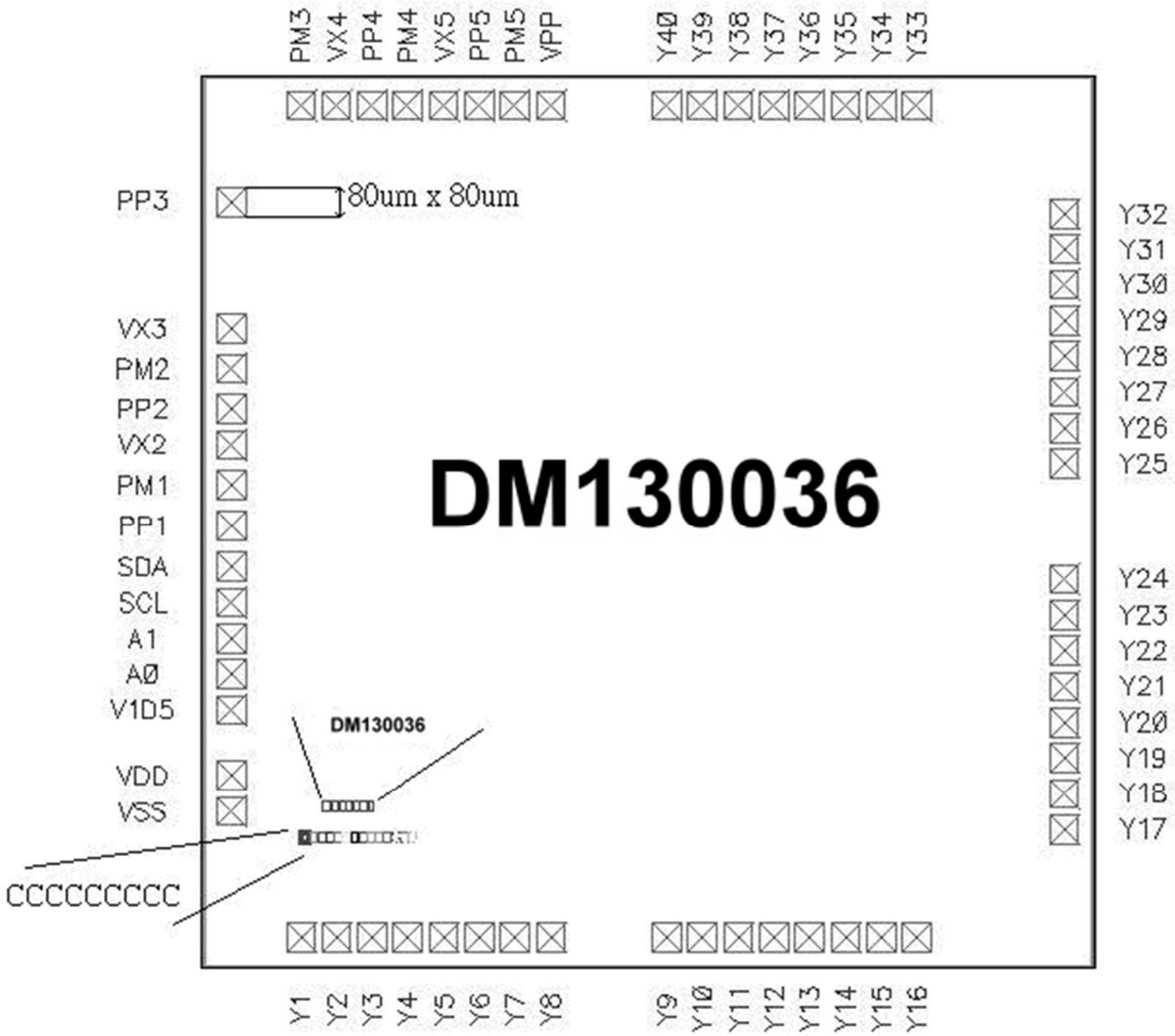
3 Block Diagram



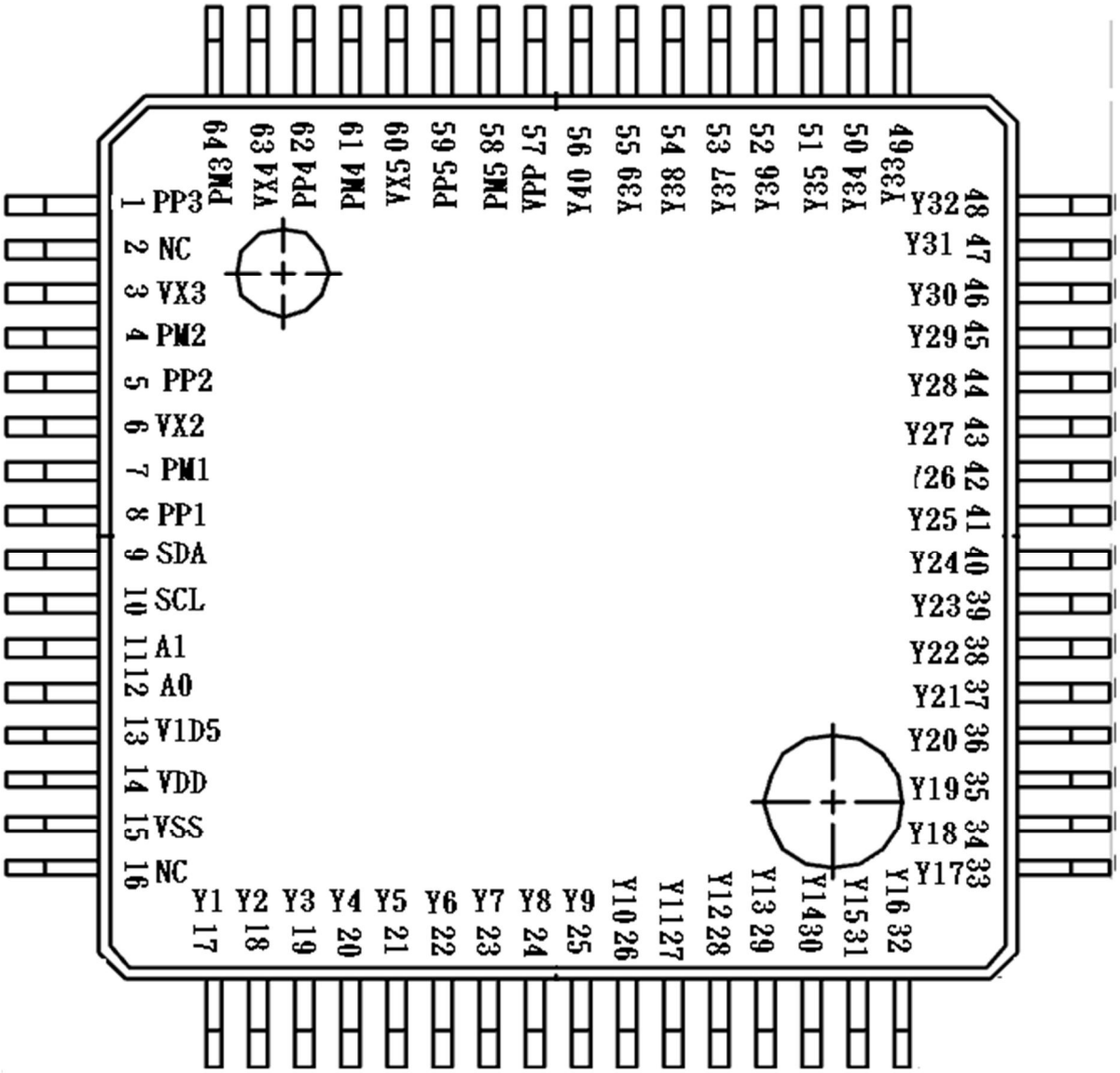
PRELIMINARY

4 Pin Out Diagram

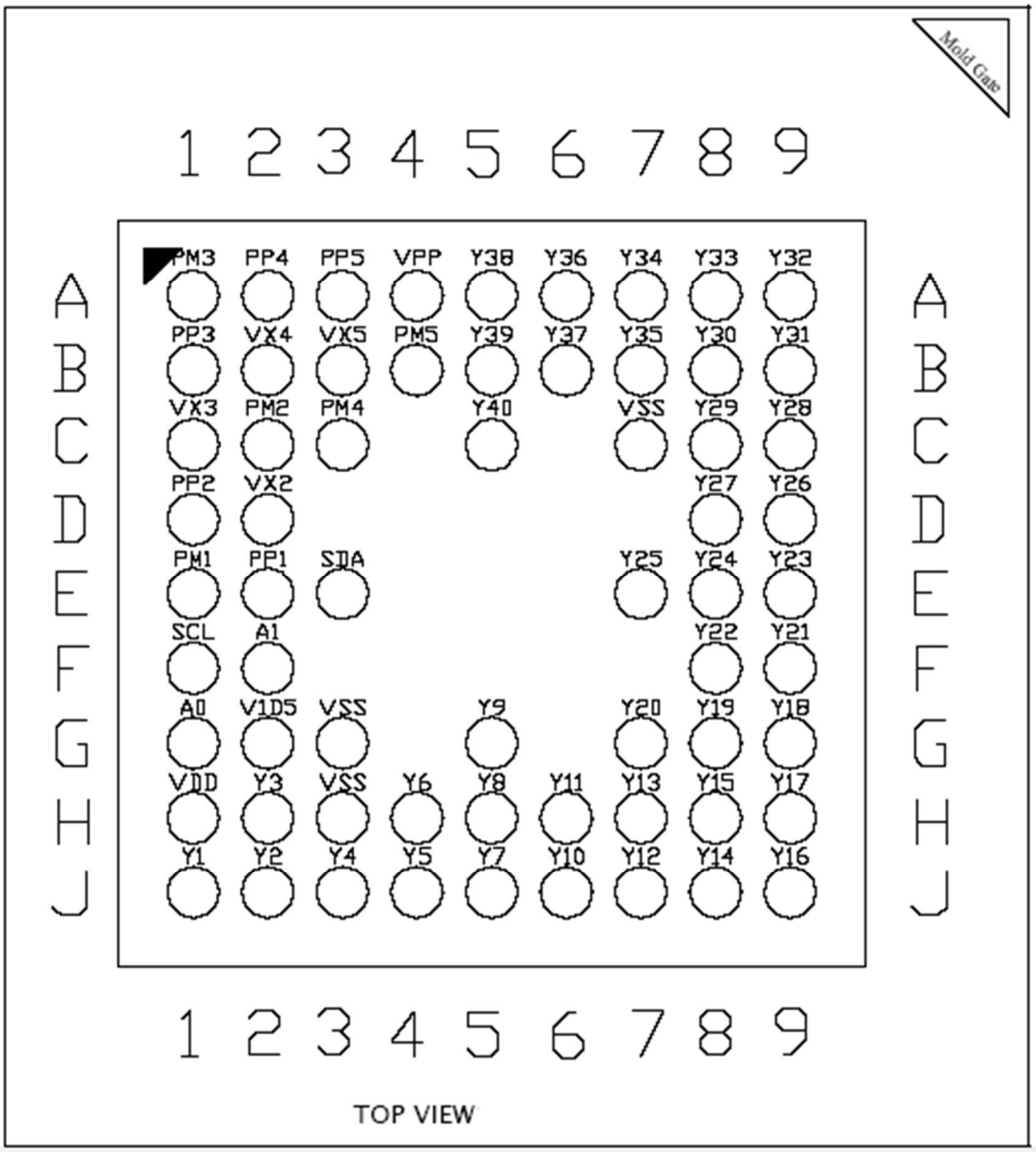
4.1 IC PAD Diagram



4.2 LQFP 64 Pin Out Diagram



4.3 LFBGA 64 Pin out Diagram (Top View)



5 Pin Description

PIN NAME	Description
SCL	2-wire serial signal clock input
SDA	2-wire serial signal data input
A1	Device ID code
A0	Device ID code
VPP	Charge pump output pin about 30V
VX5	Charge pump output pin about 15 V
VX4	Charge pump output pin about 7.5 V
VX3	Charge pump output pin about 5 V
VX2	Charge pump output pin about 2.5 V
PP[1:5]	Positive terminal for charge pump capacitor
PM[1:5]	Negative terminal for charge pump capacitor
Y[1:40]	EPD Hi-V channels
VDD	Positive power source
VSS	Negative power source
V1D5	Charge pump reference voltage

Note：SCL & SDA need pull high resistor 4.7KΩ to VDD
VID5 needs connect to 0.1uF to VSS

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LQFP 64	LFBGA 64	IC 62	Pin Name	Pin Type	Description
Control PIns					
10	F1	9	SCL	I	2-wire serial signal clock input
9	E3	8	SDA	I/O	2-wire serial signal data input
11	F2	10	A1	I	Device ID code
12	G1	11	A0	I	Device ID code
Charge Pump Pins					
57	A4	55	VPP	O	Charge pump output pin about 30V
60	B3	58	VX5	O	Charge pump output pin about 15 V
63	B2	61	VX4	O	Charge pump output pin about 7.5 V
3	C1	2	VX3	O	Charge pump output pin about 5 V
6	D2	5	VX2	O	Charge pump output pin about 2.5 V
8	E2	7	PP1	O	Positive terminal for charge pump capacitor
5	D1	4	PP2	O	Positive terminal for charge pump capacitor
1	B1	1	PP3	O	Positive terminal for charge pump capacitor
62	A2	60	PP4	O	Positive terminal for charge pump capacitor
59	A3	57	PP5	O	Positive terminal for charge pump capacitor
7	E1	6	PM1	O	Negative terminal for charge pump capacitor
4	C2	3	PM2	O	Negative terminal for charge pump capacitor
64	A1	62	PM3	O	Negative terminal for charge pump capacitor
61	C3	59	PM4	O	Negative terminal for charge pump capacitor
58	B4	56	PM5	O	Negative terminal for charge pump capacitor
Reference and Power Pins					
14	H1	13	VDD	Power	Positive power source
15	C7,G3,H3	14	VSS	Power	Negative power source
13	G2	12	V1D5	O	Charge pump reference voltage
EPD High Voltage Pins					
17	J1	15	Y1	O	EPD Hi-V channels, SEG1
18	J2	16	Y2	O	EPD Hi-V channels, SEG2
19	H3	17	Y3	O	EPD Hi-V channels, SEG3
20	J3	18	Y4	O	EPD Hi-V channels, SEG4
21	J4	19	Y5	O	EPD Hi-V channels, SEG5
22	H4	20	Y6	O	EPD Hi-V channels, SEG6
23	J5	21	Y7	O	EPD Hi-V channels, SEG7
24	H5	22	Y8	O	EPD Hi-V channels, SEG8
25	G5	23	Y9	O	EPD Hi-V channels, SEG9
26	J6	24	Y10	O	EPD Hi-V channels, SEG10
27	H6	25	Y11	O	EPD Hi-V channels, SEG11
28	J7	26	Y12	O	EPD Hi-V channels, SEG12
29	H7	27	Y13	O	EPD Hi-V channels, SEG13
30	J8	28	Y14	O	EPD Hi-V channels, SEG14
31	H8	29	Y15	O	EPD Hi-V channels, SEG15
32	J9	30	Y16	O	EPD Hi-V channels, SEG16
33	H9	31	Y17	O	EPD Hi-V channels, SEG17
34	G9	32	Y18	O	EPD Hi-V channels, SEG18
35	G8	33	Y19	O	EPD Hi-V channels, SEG19
36	G7	34	Y20	O	EPD Hi-V channels, SEG20
37	F9	35	Y21	O	EPD Hi-V channels, SEG21
38	F8	36	Y22	O	EPD Hi-V channels, SEG22
39	E9	37	Y23	O	EPD Hi-V channels, SEG23
40	E8	38	Y24	O	EPD Hi-V channels, SEG24
41	E7	39	Y25	O	EPD Hi-V channels, SEG25
42	D9	40	Y26	O	EPD Hi-V channels, SEG26
43	D8	41	Y27	O	EPD Hi-V channels, SEG27

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44	C9	42	Y28	O	EPD Hi-V channels, SEG28
45	C8	43	Y29	O	EPD Hi-V channels, SEG29
46	B8	44	Y30	O	EPD Hi-V channels, SEG30
47	B9	45	Y31	O	EPD Hi-V channels, SEG31
48	A9	46	Y32	O	EPD Hi-V channels, SEG32
49	A8	47	Y33	O	EPD Hi-V channels, SEG33
50	A7	48	Y34	O	EPD Hi-V channels, SEG34
51	B9	49	Y35	O	EPD Hi-V channels, SEG35
51	A6	50	Y36	O	EPD Hi-V channels, SEG36
53	B6	51	Y37	O	EPD Hi-V channels, background
54	A5	52	Y38	O	EPD Hi-V channels, background
55	B5	53	Y39	O	EPD Hi-V channels, common
56	C5	54	Y40	O	EPD Hi-V channels, common
Others					
2,16			NC	N/A	

Note: O = output, I = input, I/O = bidirection

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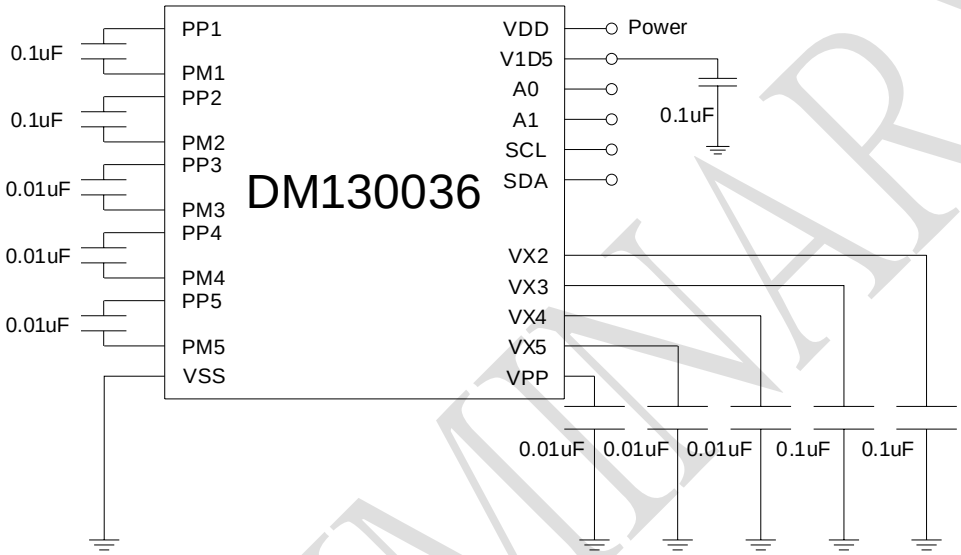
6 Function Description

6.1 Generate Hi-V Driving Bias Supply

6.1.1 Internal Charge Pump Supply

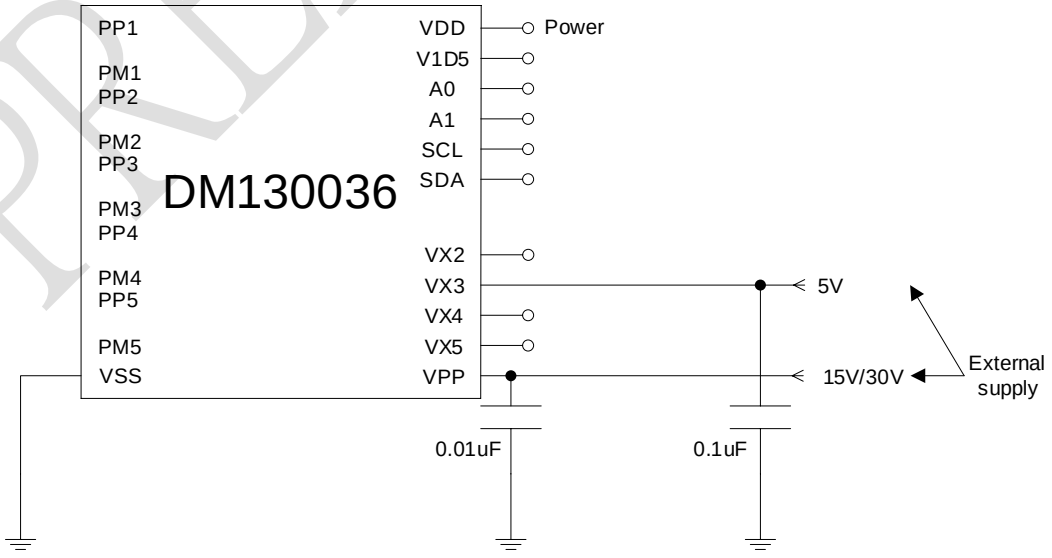
Internal charge pump can generate high voltage up to 30V. User also can select 0V,15V or 30V to drive EPD by setting control register.

The value of high voltage that pump can generate as following.
VPP=30V , VX5=15V , VSS= 0V, set register $05h bit5 VPP15=0



6.1.2 External Driving Bias Supply

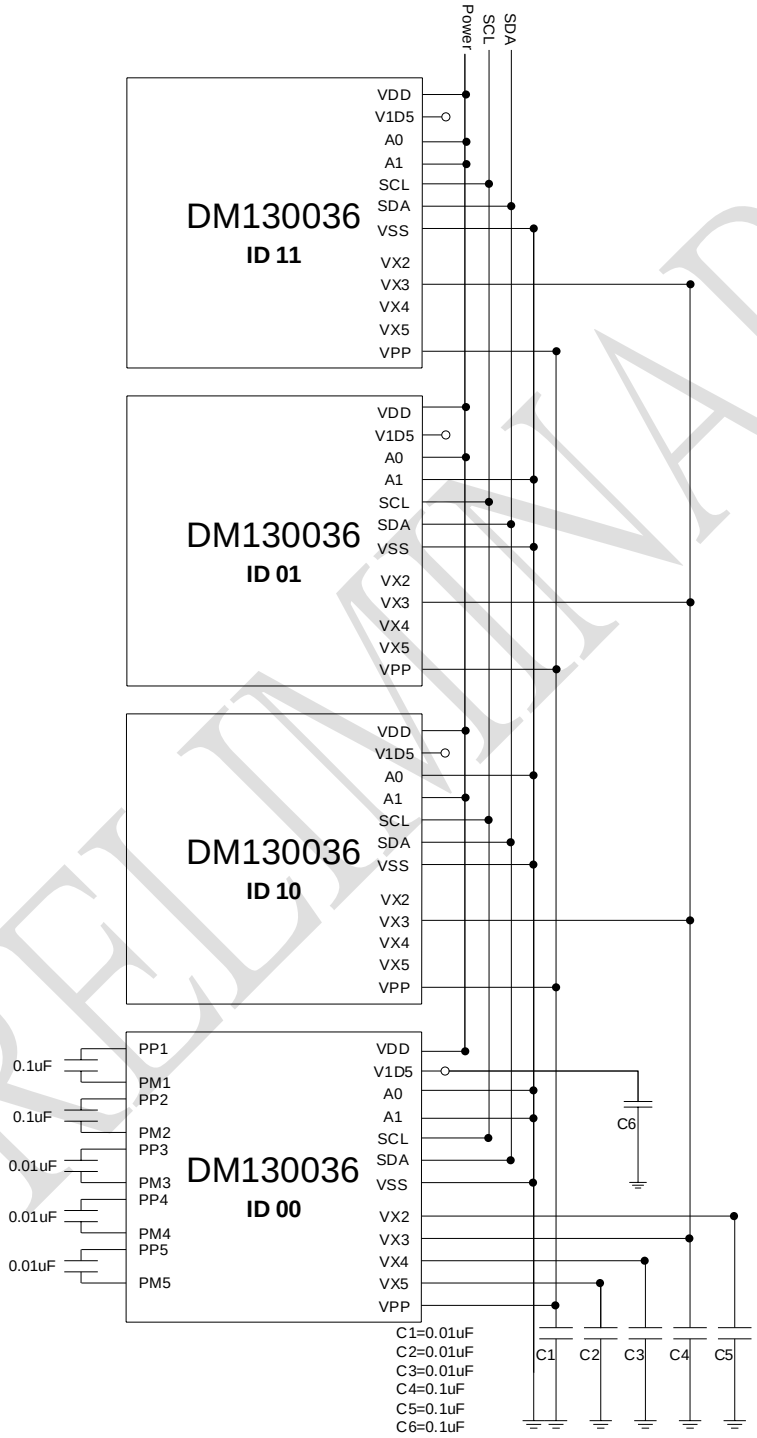
External driving bias supply to VPP & VX3, user need to turn off internal pump function first, and then supply 15V/30V to VPP, 5V to VX3.



PRELIMINARY

6.2 Multi-drivers Application

The host device with 2-wire serial interface can control DM130036. (A1,A0) pins correspond to the ID setting (Maximum support 4 chips). See the following figure for setting ID option.



PRELIMINARY

6.3 EPD Driver Control Register

Register Address	Data							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Y08	Y07	Y06	Y05	Y04	Y03	Y02	Y01
01H	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y09
02H	Y24	Y23	Y22	Y21	Y20	Y19	Y18	Y17
03H	Y32	Y31	Y30	Y29	Y28	Y27	Y26	Y25
04H	Y40	Y39	Y38	Y37	Y36	Y35	Y34	Y33
05H	CPEN	C3	VPP15	C2	Load	C1	VSEL1	VSEL0

Y1 ~ Y40 output setting：
Y1 ~ Y36 mapping to segments pins
Y37、Y38 correspond to BG1、BG2 (Background) pin
Y39、Y40 correspond to COM1、COM2 (Common) pin

The output voltage (0V,15V,30V) for Y[1:40] are selectable.
If user selects Y[1:40] to output 30V or 15V, setting the correspond bit to “1”.
If user selects Y[1:40] to output 0V, setting the correspond bit to “0”.

Example：
If user selects Y9, Y11, Y13, Y15 to output “VPP” and Y10, Y12, Y14,Y16 to output “0V”,
Register $01H = 01010101

Register”$05h” bit7 “CPEN”：Charge pump on / off
CPEN=1, charge pump enable
CPEN=0, charge pump disable

Register”$05h” bit6 “C3”：Internal test parameter “C3”. Here user have to set “0”

Register”$05h” bit5 “VPP15”： Half VPP output switch
VPP15=1：Hi-V channels logic high will output VX5, the voltage equal to half VPP
VPP15=0：Hi-V channels logic high will output VPP

Register”$05h” bit4 “C2”： Internal test parameter “C2”. Here user have to set “0”

Register”$05h” bit3 “Load”：Load data from Y[1~40] and then latch out for synchronous
Load=1：Load data from Y[1~40] to output buffer
Load=0：Latch the buffer and output

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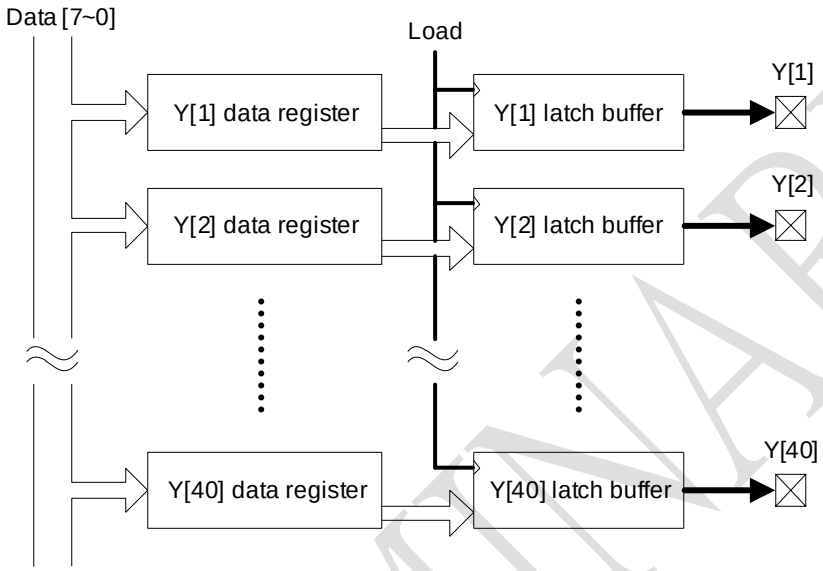
Output synchronous

For the reason of output synchronous that user has to set up $05h, bit3=1 first. This step will load the data Y[1~40] from register[$00h~$05h] into each buffer. And then set up $05h, bit3=0 for the next step. Y[1~40] latch buffers will latch and output the data synchronous.



Note: The data hold time for this bit should be over “1us”. That means, customer sets up register $05h.bit3=1 for latching output then waiting over 1us that will be available for next data

.

Register”$05h” bit2 “C1”：Internal test parameter “C1”. Here user has to set “0”

Register”$05h” bit0~1 “VSEL0~1”：Adjustable internal reference voltage
All the selections are shown as below:

VSEL[1：0]	V1D5
00	1.5V
01	1.6V
10	1.7V
11	1.8V

Note:
1. All control registers don’t have initial value after power on. Users need to initialize all registers manually.
2. $xxH means address and represents in hexadecimal form.
3. “xxxxxxxxb” means 8-bits data of register and represents in binary form.
4. The “VPP” here means the highest pumped voltage, “VX5” means half VPP and “GND” means the most low voltage of system power.
5. Write by default value 00b.

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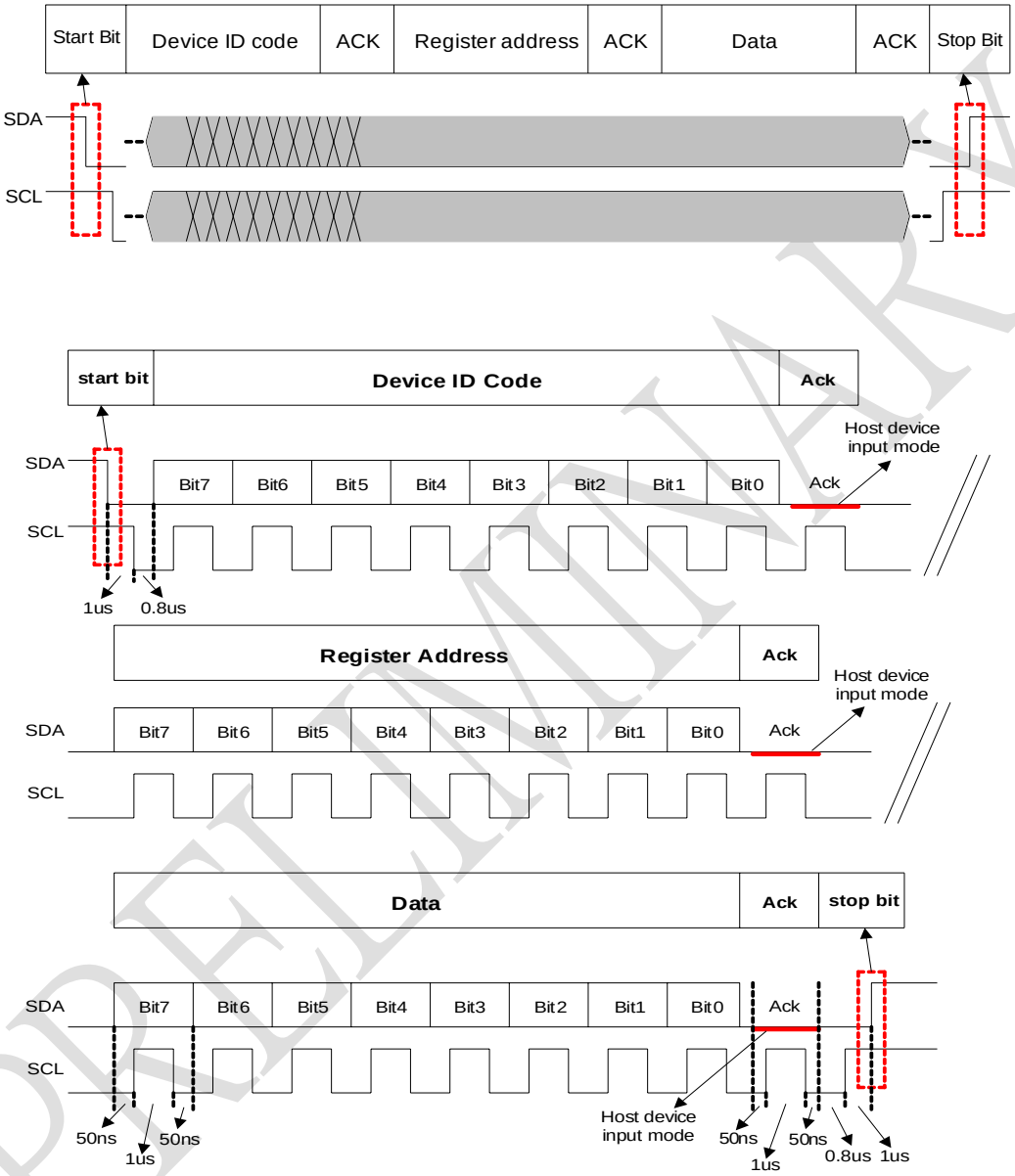
6.4 Control Signal Waveform

6.4.1 Format of One Byte

This byte can be 00H~05H, see 6.3 EPD driver control register



Note: Timing diagram above is when SCL=500KHz

Device ID code：
ID code defined by (A0&A1) pins. See P9 multi-driver application. Control signal input 8-bits “111100A1,A0” (A1,A0)=00 or 01 or 10 or 11 then only matched driver will operate.

Register address：
The control registers are from $00H~$05H. The control signal is after Device ID code.

Data of register：
Definition of all control registers, see 6.3 EPD driver control register.

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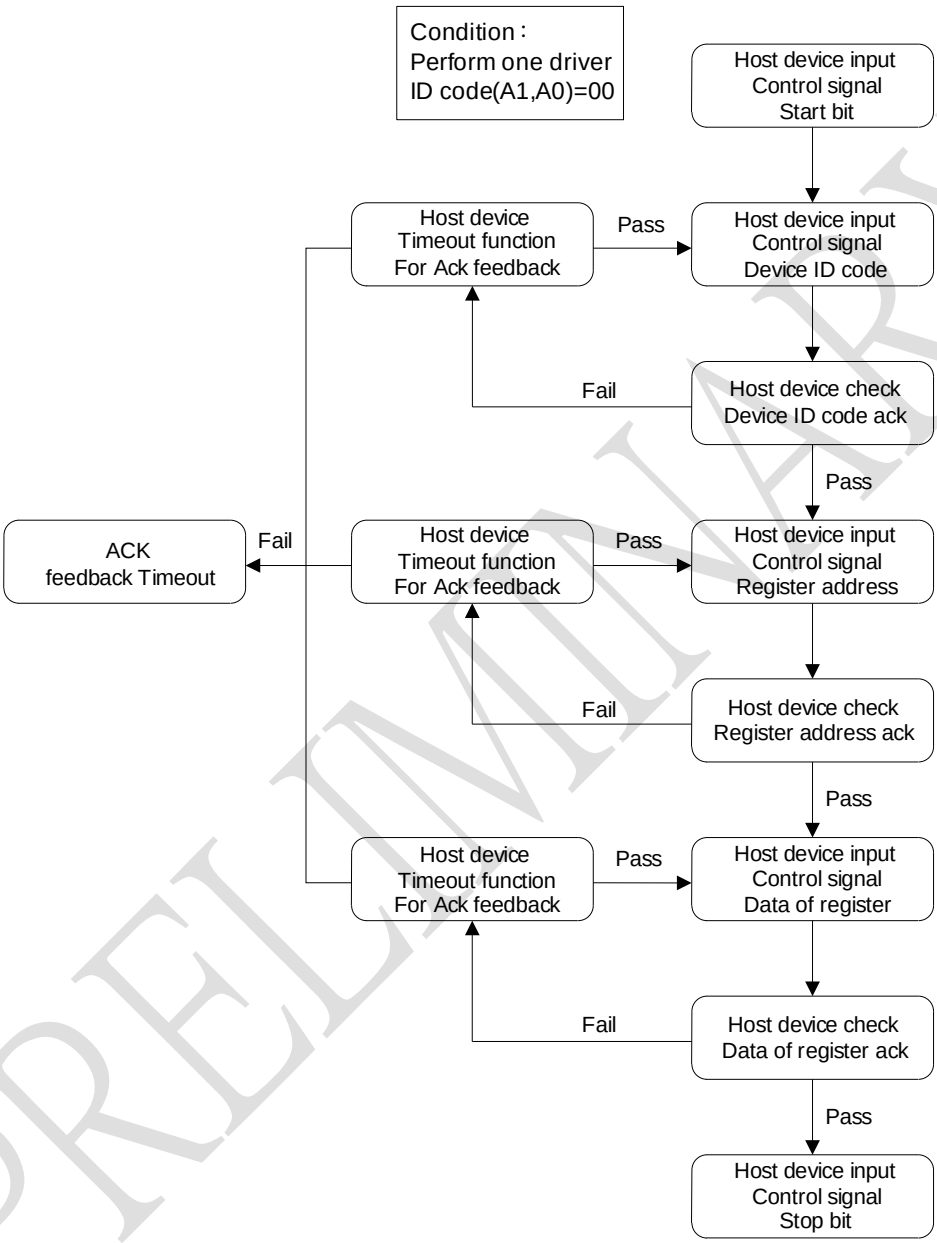
Condition setting
Perform with one driver IC and ID code (A1,A0)=00

Operating flow of one byte



Note：
1. According to operating flow above, host device needs to switch the pin to input-mode which connects to SDA while ACK feedback. Also check ACK feedback “Low” it means current byte transmission pass.
2. All the timing of pulse-width in operating flow above represents the minimum acceptable value.
3. Operating flow above is only for reference. For actual situation, please refer to E-paper spec.

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6.4.2 Com & Segment vs. Control Signal

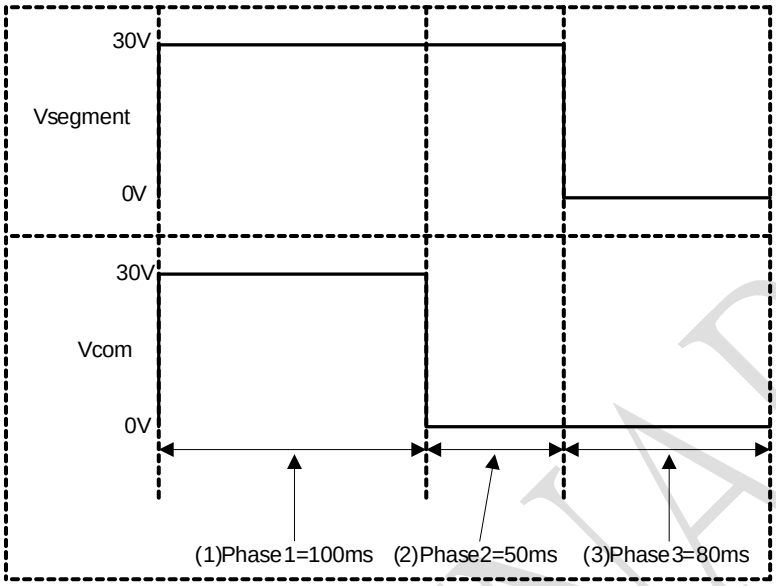


Figure 9

Condition1：One driver

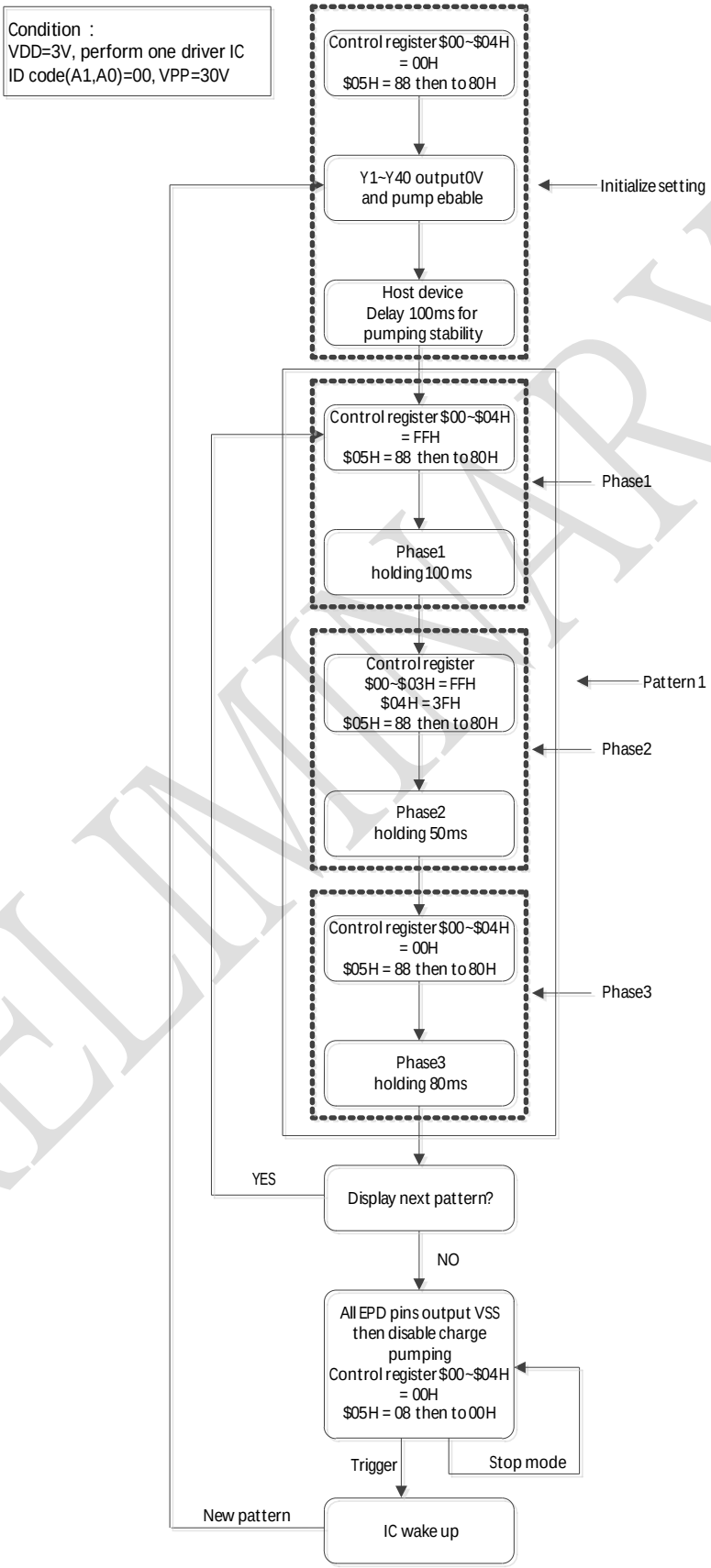
VDD=3V, use internal pumping function , perform with one driver IC, ID code (A1,A0)=00
Register $05H. bit5 VPP15=0 & bit6 PUMPH=0 → VPP=30V
Vsegment = Y1~Y36, Vbg = Y37~Y38 , Vcom = Y39~Y40

Condition1 operate flow

1. Control register $00H~$04H = “00000000b”, $05H = “10001000b”. This step Y1~Y40 will load data from data register and output “0V” to all EPD pins, simultaneously enable internal charge pump.
   After that $05H = “10000000b” here will latch all EPD pins to GND
   Note: $05H bit3 load = 0 → 1 will load all data to EPD pins and then latch output state.
2. Host device delay 100ms for internal pumping stable.
3. Control register $00H~$04H = “11111111b” , $05H = “10001000b”. Then $05H = “10000000b”.
   Here all EPD pins will output VPP.
4. Host device delay 100ms to display phase1 pattern.
5. Control register $00H~$03H = “11111111b” , $04H = “00111111b” , $05H = “10001000b”. Then $05H = “10000000b”. All segment & background will output VPP, Y39~Y40 output “0V”.
6. Host device delay 50ms to display phase2 pattern.
7. Control register $00H~$04H = “00000000b” , $05H = “10001000b”. Then $05H = “10000000b”. All EPD pins will output “0V”.
8. Host device delay 80ms to display phase3 pattern.
9. All EPD pins output “0V” and disable charge pumping if there’s no pattern will be display.

Note：$xxH means address represent in hexadecimal.
“xxxxxxxxb” means 8-bits data of register represent in binary.

PRELIMINARY



PRELIMINARY

Condition2：Cascade four drivers

VDD=3V , perform with four drivers, Set one driver to be the pumping source and others supply from this driver.

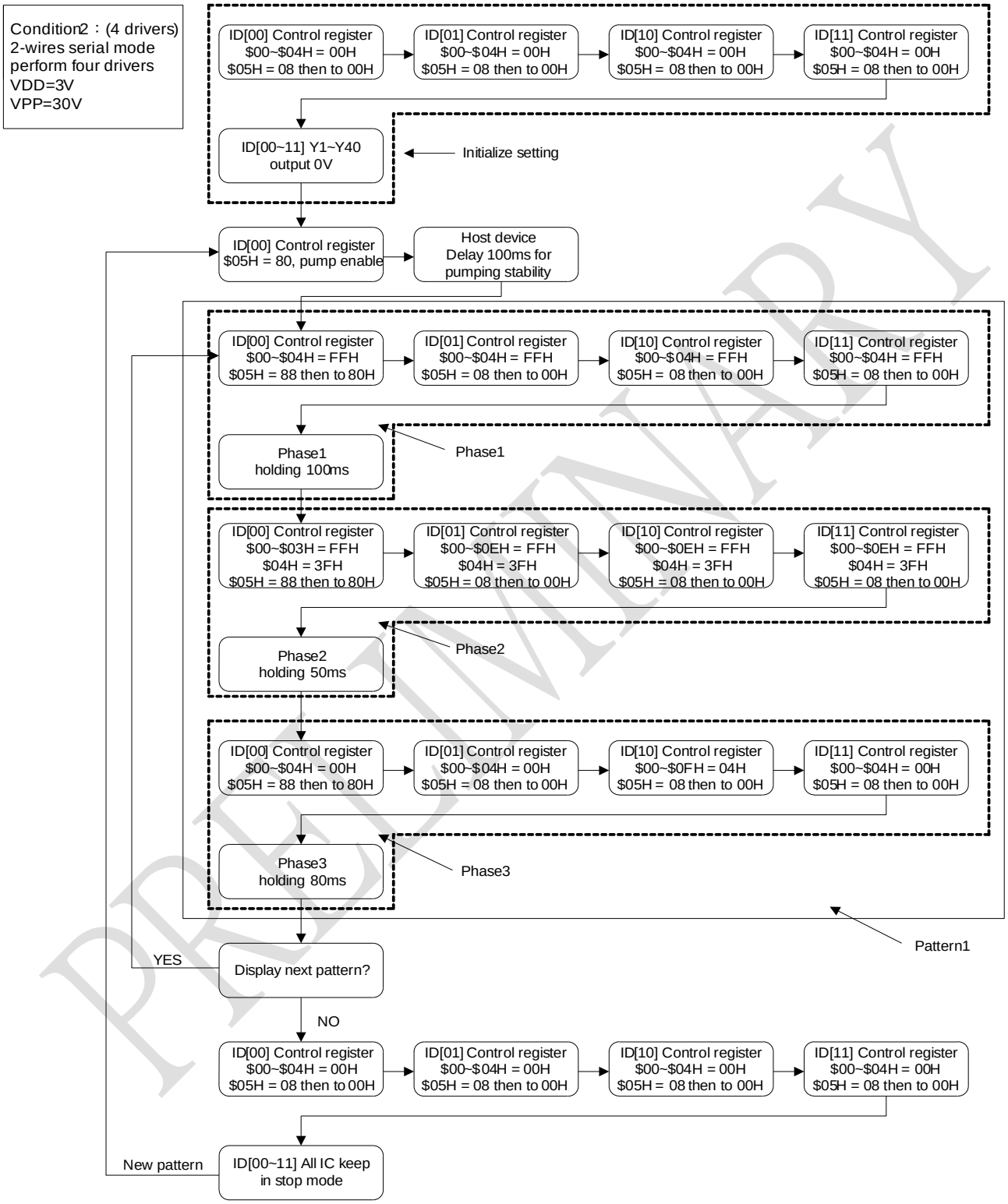
Register $05H. bit5 VPP15=0 , bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y36 , Vcom = Y37~Y38 , Vbg = Y39~Y40

Condition2 operate flow

1. ID[00] Control register $00H~$04H = “00000000b”, $05H = “00000000b”. This step Y1~Y40 will load data from data register and output “0V” to all EPD pins simultaneously.
   After that $05H = “00001000b” here will latch all EPD pins to “0V”.
   Note! $05H bit3 load = 1 → 0 will load all data to EPD pins and then latch output state.
2. ID[01~11] follow step1 to initialize all EPD pins to output “0V”
3. ID[00] register $05H = “10000000b” to enable charge pump and take ID[00] as pumping source others IC set up supply from external source.
4. Host device delay 100ms for internal pumping stability.
5. ID[00~11] Control register $00H~$04H = “11111111b” , *ID[00] $05H = “10001000b” , ID[01~11] $05H = “00001000b”. Then ID[00] $05H = “10000000b” ID[01~11] $05H = “00000000b”. Here all EPD pins will output VPP.
6. Host device delay 100ms to display phase1 pattern.
7. ID[00~11] Control register $00H~$03H = “11111111b” , $04H = “11111100b” , *ID[00] $05H = “10001000b” , ID[01~11] $05H = “00001000b”. Then ID[00] $05H = “10000000b” , ID[01~11] $05H = “00000000b”. All segment will output VPP, but Y39~Y40 output “0V”.
8. Host device delay 50ms to display phase2 pattern.
9. ID[00~11] Control register $00H~$04H = “00000000b” , *ID[00] $05H = “10001000b” , ID[01~11] $05H = “00001000b”. Then ID[00] $05H = “10000000b” , ID[01~11] $05H = “00000000b”. All EPD pins will output “0V”.
10. Host device delay 80ms to display phase3 pattern.
11. All EPD pins output “0V” and disable charge pumping if there’s no pattern will be display.

Note：$xxH means address and represent in hexadecimal form.
“xxxxxxxxb” means 8-bits data and represents in binary form.

PRELIMINARY



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7 Operating Rating

Description	Symbol	Value			Unit
		Min	Typ	Max	
Working voltage	VDD	2.2	3	5.5	V
Driver High-voltage capability	V_{DRV}		30	35	V
Ripple	V_{RIP}		200		mV
High-voltage1	VPP_{15}	3	15	18	V, (load =15M ohm)
High-voltage2	VPP_{30}	5	30		V, (load =15M ohm)
Stop mode current	I_{STOP}		0.1		uA
Pumping enable current	I_{CPEN}		350		uA
Input high voltage	V_{IH}		0.8*VDD		V
Input low voltage	V_{IL}		0.2*VDD		V
2wir speed (SCL&SDA)	F_{2wir}			1M	Hz
2wir load capacitance	C_{2wir}		15		pF

Note：
1. Symbol “2wir” represents SCL & SDA pins
2. Symbol “VPP_{15}” applies to Eink 15V film. For the better life time, customer has to tie each 40 channels to “0V” then turn off charge pumping.
3. Min of VPP_{15} = 3V and VPP_{30} = 5V all these supply from external

8 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
Vdd	Supply Voltage	-0.5 ~ +6	V
Vin	Input Voltage	-0.5 ~ VDD +0.5	V
Vout	Output Voltage	-0.5 ~ VDD +0.5	V
Topr	Operation Temperature	0 ~ 70	℃
Tstg	Storage Temperature	-40 ~ +125	℃

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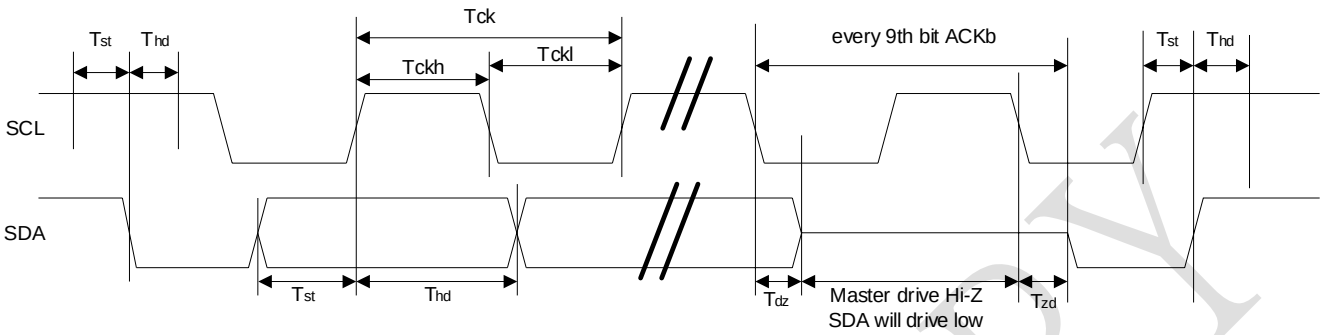
8.1 AC Characteristic



Parameter	Details	Min	Typ	Max	units
Tck	Clock cycle time	1			us
Tckl	Clock low time	400			ns
Tckh	Clock high time	400			ns
Tst	Setup time	100			ns
Thd	Hold time	100			ns
Tdz	Clock low to data Hi-z delay			80	ns
Tzd	Clock low to data drive delay			80	ns

8.2 HVPAD Driving

Parameter	Conditions	Vout	Min	Typ	Max	units
Roh	Y1 ~ Y36, VPP=16V	Vout=15V		7.1		K-ohm
Roh	Y37 ~ Y38, VPP=16V			4.6		K-ohm
Roh	Y39 ~ Y40, VPP=16V			4.4		K-ohm
Roh	Y1 ~ Y36, VPP=32V	Vout =30V		5.1		K-ohm
Roh	Y37 ~ Y38, VPP=32V			3.2		K-ohm
Roh	Y39~ Y40, VPP=32V			3.4		K-ohm

Note : *Roh* represents internal equivalent resistor at driving capability.

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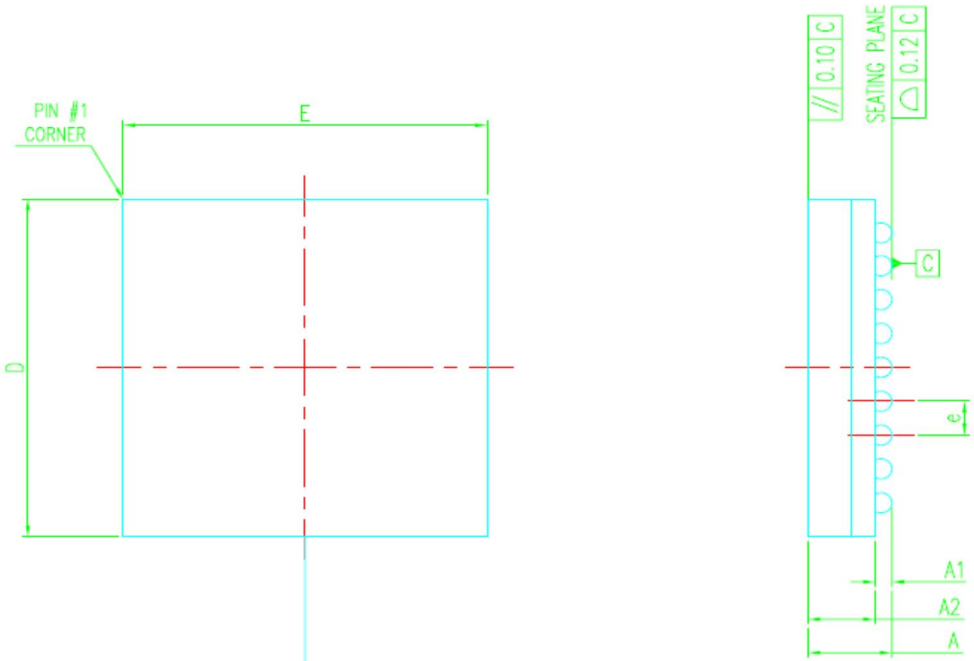
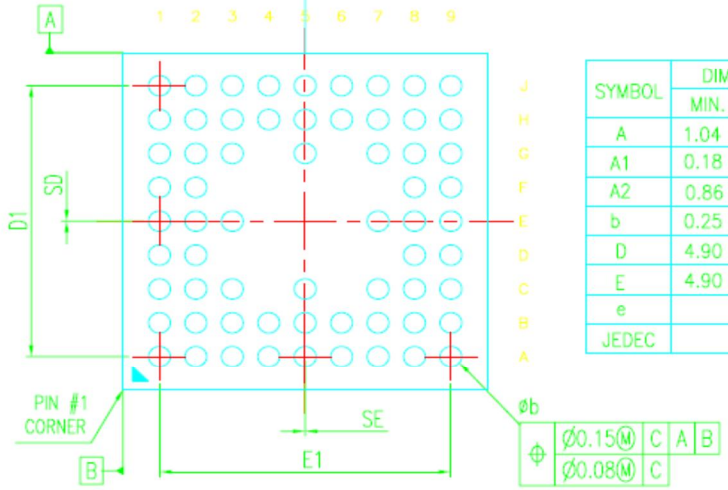
9 Package Information

9.1 LFBGA 64 Pins Detail Information

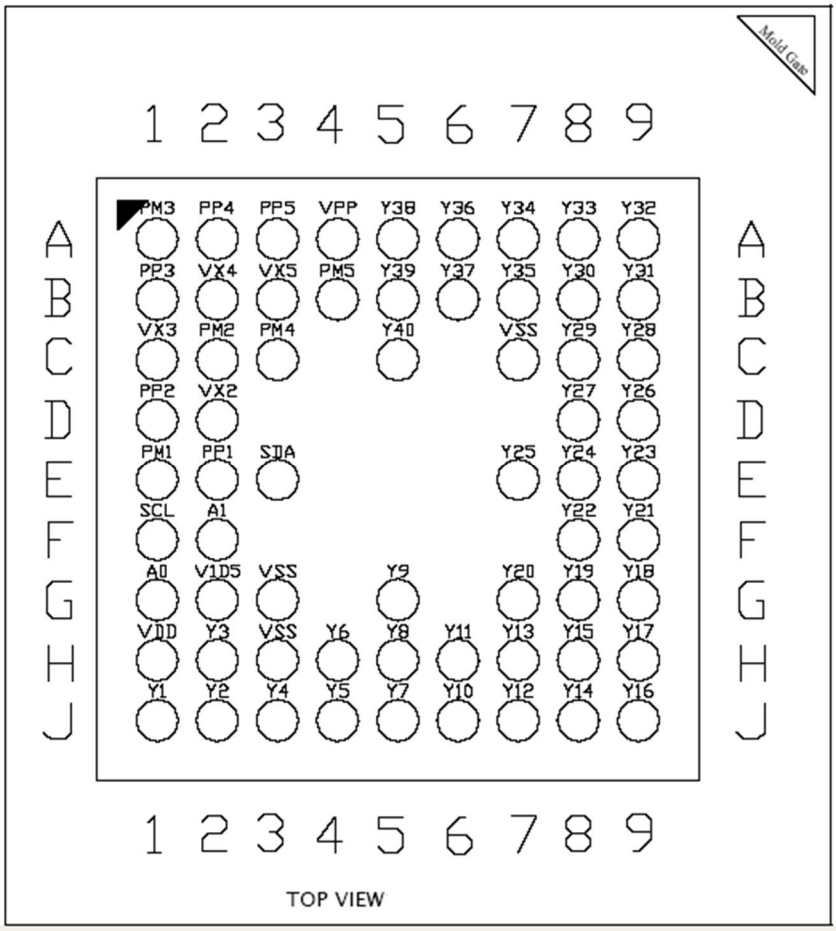




SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.04	1.15	1.26	0.041	0.045	0.050
A1	0.18	0.23	0.28	0.007	0.009	0.011
A2	0.86	0.92	0.98	0.034	0.036	0.039
b	0.25	0.30	0.35	0.010	0.012	0.014
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-205(REF.)					

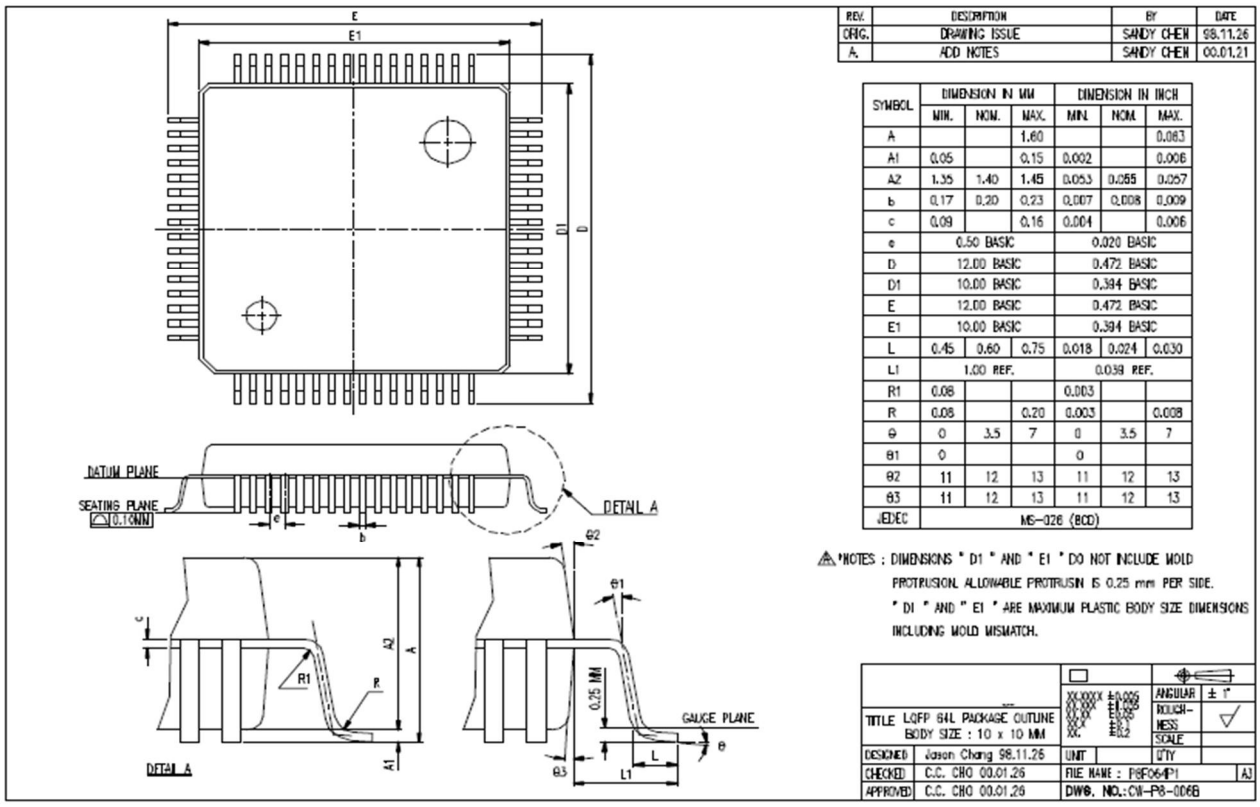
N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)	JEDEC(Ref.)
64L	0.0 BSC.	0.0 BSC.	4.00 BSC.	4.00 BSC.	

LFBGA 64 Pins PAD Top View



PRELIMINARY

9.2 LQFP 64 Pins Detail Information



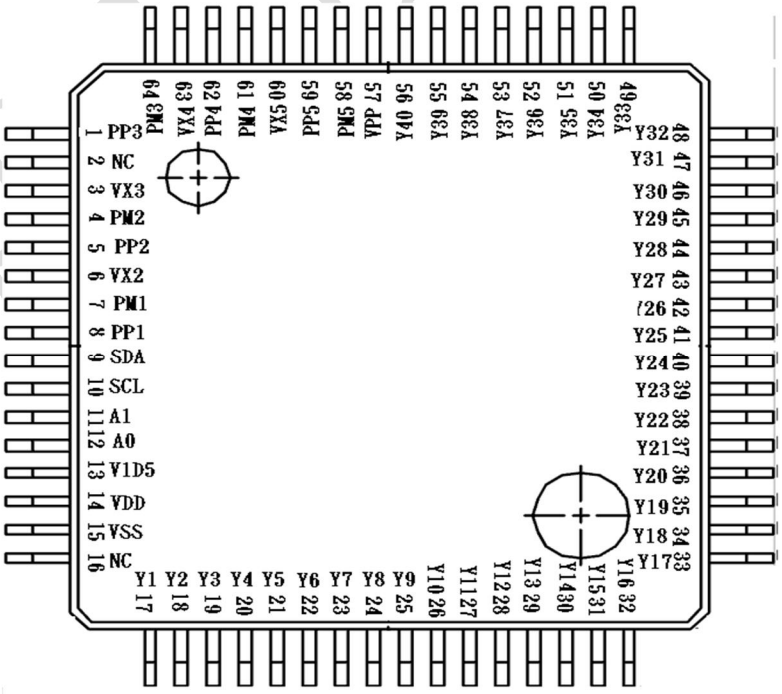
REV.	DESCRIPTION	BY	DATE
CHG.	DRAWING ISSUE	SANDY CHEN	98.11.26
A.	ADD NOTES	SANDY CHEN	00.01.21

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

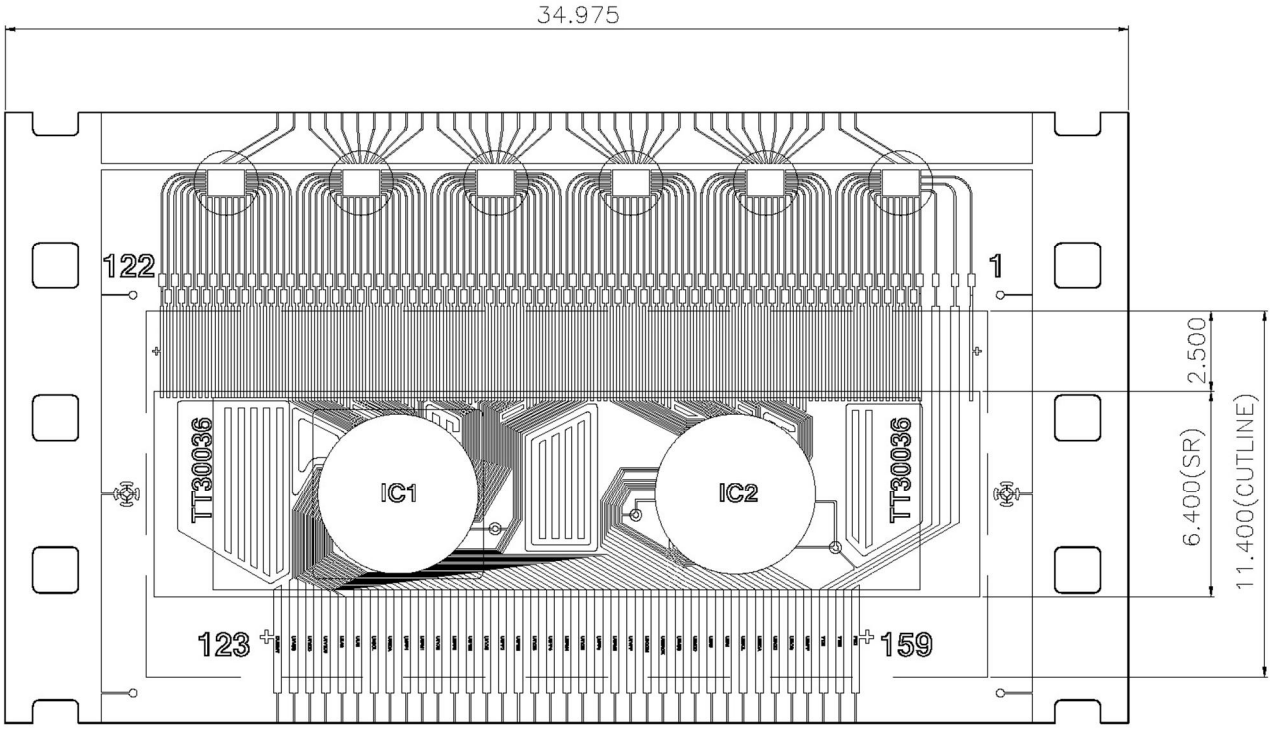
TITLE	LQFP 64L PACKAGE OUTLINE BODY SIZE : 10 x 10 MM	XX.XXXX ±0.005 XX.XXX ±0.025 XX.XX ±0.05 XX.X ±0.1 XX. ±0.2	ANGULAR ± 1° ROUGH-NESS SCALE
DESIGNED	Jason Chang 98.11.26	UNIT	DTY
CHECKED	C.C. CHO 00.01.26	FILE NAME : P8F064P1	A3
APPROVED	C.C. CHO 00.01.26	DWG. NO.:CW-P8-006B	

LQFP 64 Pins PAD Top View

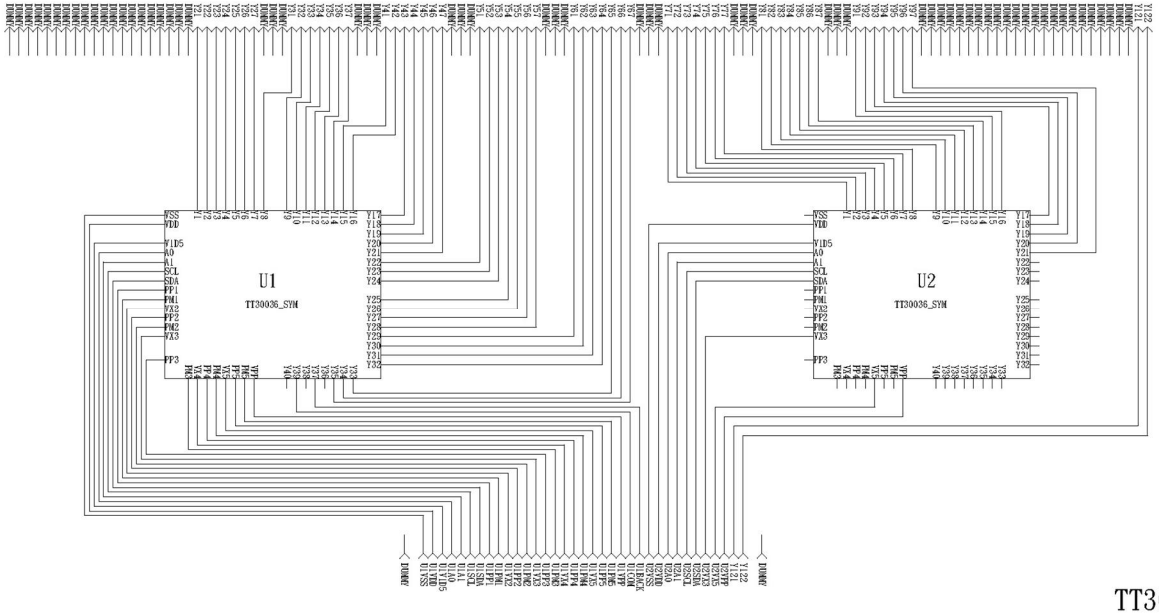


9.3 COF Information

DM130036 COF module



DM130036 COF layout



10 Ordering Information

Part Number	Pin Count	Package
DM130036W	-	Wafer (Pb-Free)
DM130036WB	-	Wafer + Gold bump (Pb-Free)
DM130036	64	Dice (Pb-Free)
DM130036B	64	Dice + Gold bump (Pb-Free)
DM130036GP	64	LFBGA 64L (Pb-Free)
DM130036EP	64	LQFP 64L (Pb-Free)
DM130036C	159	COF (Roll) (Pb-Free)
DM130036P	159	COF (Tray) (Pb-Free)

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We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards. ***For customized products, please contact to Davicom's sales***

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HTTP: http://www.davicom.com.tw

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Conditions beyond those listed for the absolute maximum rating may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (or permanently) affect and damage structure, performance and function.

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