DL031

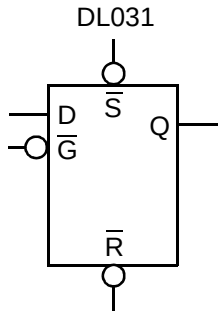
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL031 is a transparent, unbuffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0
RN	1.0

Equivalent Gates 5.0

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	8.4	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.48 0.57	0.52 0.63	0.63 0.78	0.73 0.92	0.78 1.00
GN	Q	t_{PLH} t_{PHL}	0.58 0.71	0.63 0.76	0.73 0.92	0.81 1.08	0.86 1.19
SN	Q	t_{PLH} t_{PHL}	0.14 0.20	0.18 0.25	0.28 0.41	0.37 0.55	0.43 0.64
RN	Q	t_{PLH} t_{PHL}	0.52 0.48	0.55 0.54	0.65 0.70	0.75 0.85	0.82 0.95

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

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Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.71
Min RN Width	Low	t_w	0.16
Min SN Width	Low	t_w	0.73
Min D Setup		t_{su}	0.55
Min D Hold		t_h	0.14
Min SN Setup		t_{su}	0.21
Min SN Hold		t_h	0.46
Min RN Setup		t_{su}	0.52
Min RN Hold		t_h	0.24

Logic Schematic