SPECIFICATION
FOR
LCD+CTP Module
DET040WVNMCMIS-2A

MODULE:	**DET040WVNMCMIS-2A**
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2015.07.08

DENSITRON	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Data	Rev. No.	Page	Summary
2014.07.08	V1.0	ALL	FIRST ISSUE

Contents

General Description

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.0'TFT-LCD contains 480*800 pixels, and can display up to 65K/262K/16.7M colors.

*** Features**

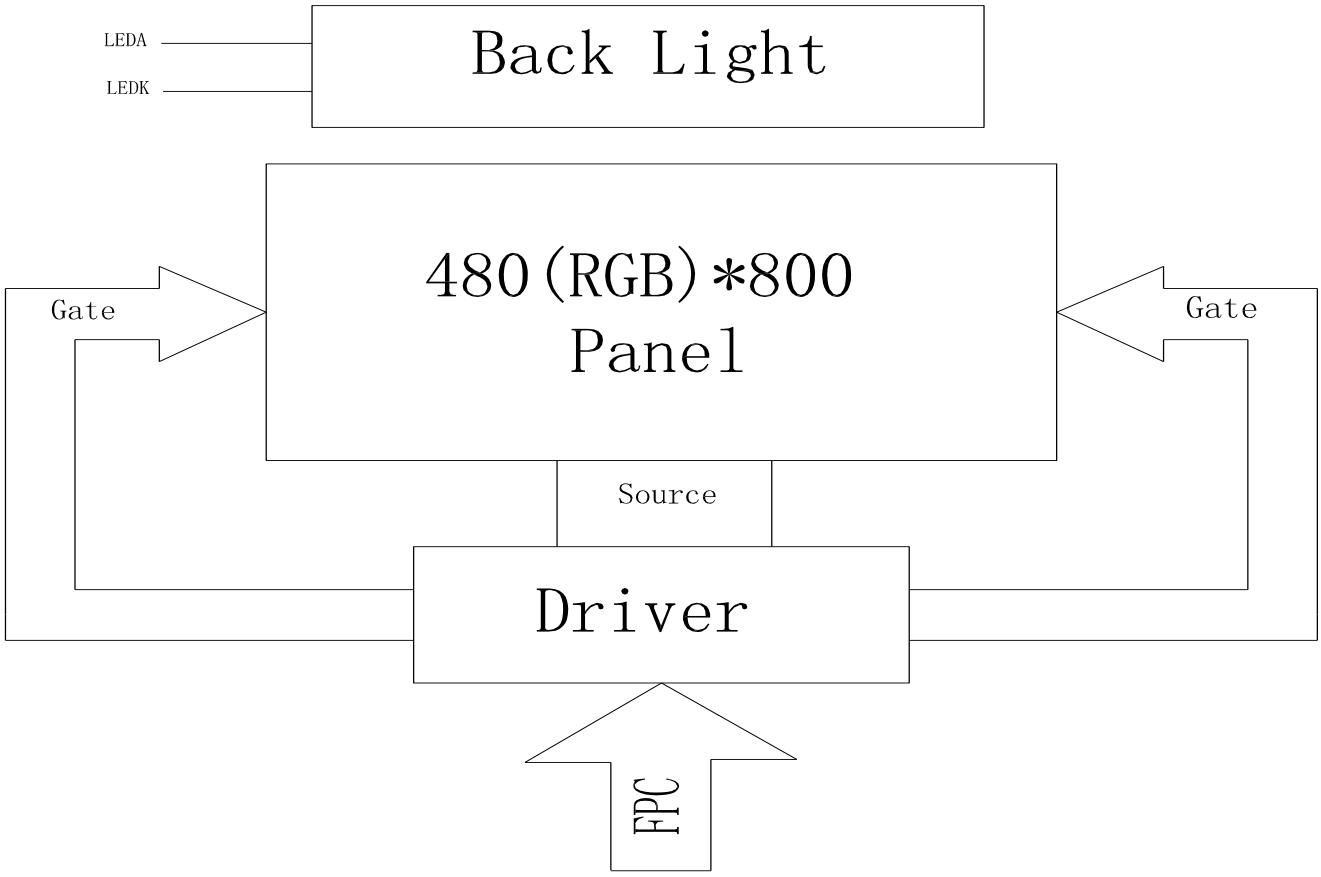
-Low Input Voltage: 3.3V (TYP)
-Display Colors of TFT LCD: 65K/262K/16.7M colors
- TFT Interface: 3SPI+16/18/24 bit RGB
-CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area(AA)	51.84(H)*86.40(V) (4.0inch)	mm	-
CTP View area	52.84(H)*87.40(V)	mm	
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*800	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.108(H)*0.108(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
CTP Driver IC	GT911		
Simultaneous Touch Points	5		
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

*** Mechanical Information**

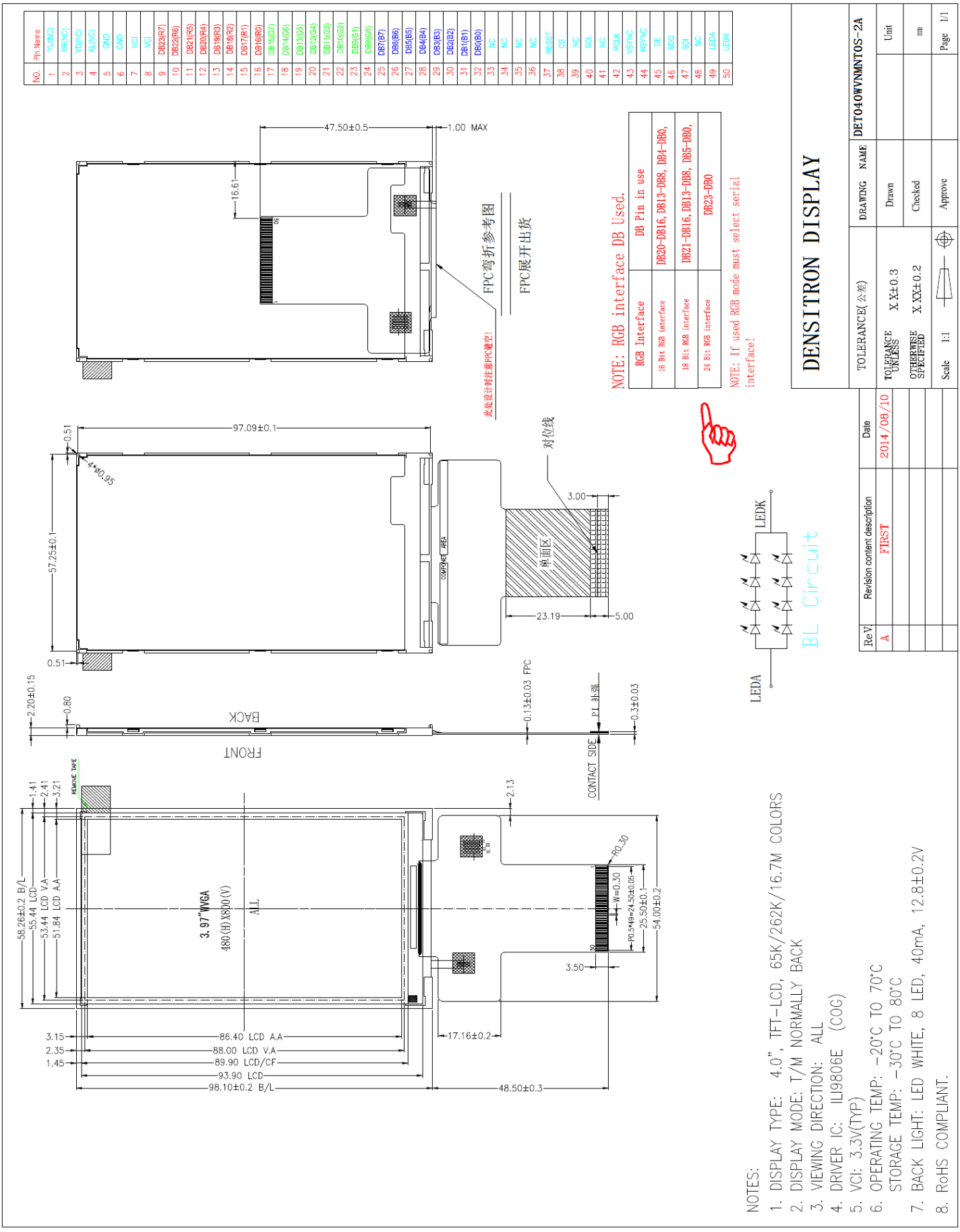
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		66.84		mm	-
	Vertical(V)		111.50		mm	-
	Depth(D)		4.13		mm	-
Weight			TBD		g	-

1. Block Diagram

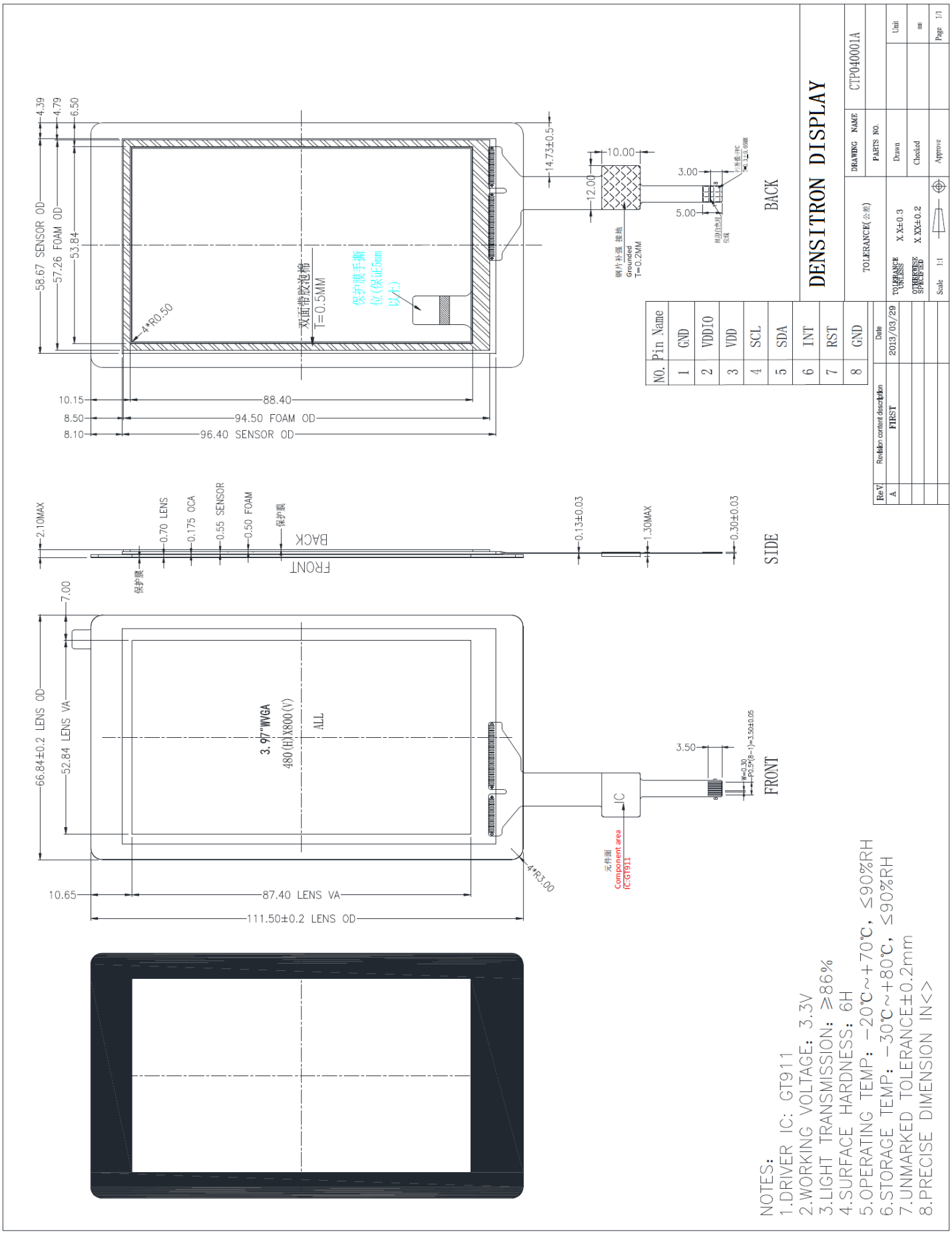


2. Outline dimension

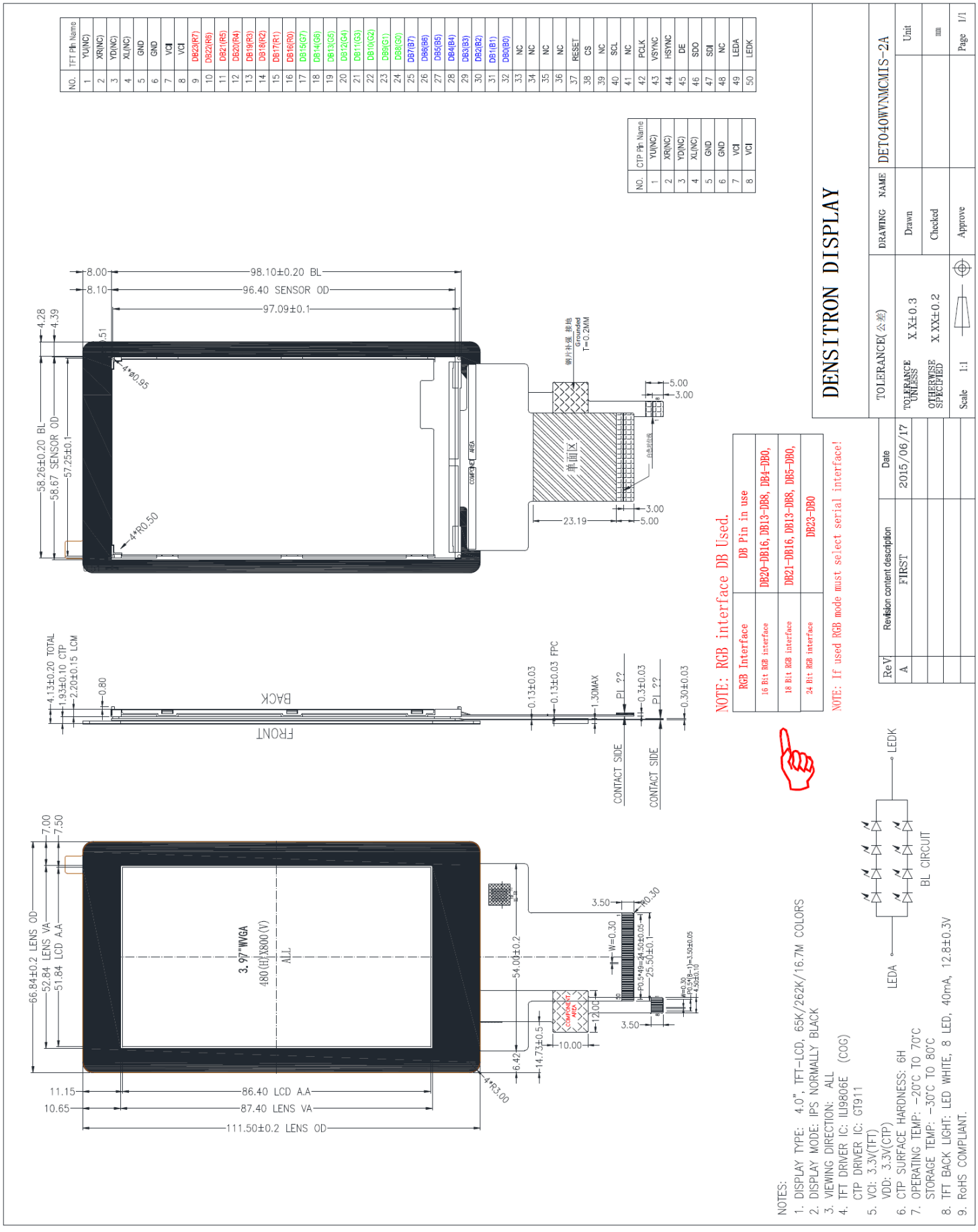
2.1 LCM



2.2 CTP


DENSITRON DISPLAY
CTP040001A
BACK
SIDE
FRONT
3.97"WVGA
480(H)X800(V)
ALL
88.40
94.50 FOAM OD
96.40 SENSOR OD
87.40 LENS VA
111.50±0.2 LENS OD
66.84±0.2 LENS OD
52.84 LENS VA
58.67 SENSOR OD
57.26 FOAM OD
53.84
NO. Pin Name
1 GND
2 VDDIO
3 VDD
4 SCL
5 SDA
6 INT
7 RST
8 GND
NOTES:
1.DRIVER IC: GT911
2.WORKING VOLTAGE: 3.3V
3.LIGHT TRANSMISSION: ≥86%
4.SURFACE HARDNESS: 6H
5.OPERATING TEMP: -20℃~+70℃, ≤90%RH
6.STORAGE TEMP: -30℃~+80℃, ≤90%RH
7.UNMARKED TOLERANCE±0.2mm
8.PRECISE DIMENSION IN<>

2.3 LCM+CTP



Part. No	DET040WVNMCMIS-2A	REV	V1.0	Page 8 of 35

3. Input terminal Pin Assignment

3.1 TFT

Pin NO.	Symbol	Function	I/O
1	YU(NC)		
2	XR(NC)		
3	YD(NC)		
4	XL(NC)		
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	VCI	Supply voltage (3.3V).	P
9-32	DB23-DB0	Data bus PINS. -RGB data bus used. 24-bitbus: use DB23-DB0 18-bit bus: use DB21-DB16,DB13-DB8,DB5-DB0. 16-bit bus: use DB20-DB16,DB13-DB8,DB4-DB0 If not used PINS, please must connect to GND.	I/O
33-36	NC		
37	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
38	CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.	I
39	NC		
40	SCL	Serial clock input.	I
41	NC		
42	PCLK	Dot clock signal.	
43	VSYNC	Frame synchronizing signal.	I

44	HSYNC	Line synchronizing signal.	I
45	DE	Data enable signal.	I
46	SDO	Serial data output pin used for the SPI Interface. Leave the pin to open when not in use.	O
47	SDI	Serial data input pin used for the SPI Interface.	I
48	NC		
49	LEDA	Anode pin of backlight.	P
50	LEDK	Cathode pin of backlight.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance 1lux and temperature = 25 2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0 . We refer to θØ=0 (=θ3) as the 3 o‟clock direction (the “right”), θØ=90 (= θ12) as the 12 o‟clock direction (“upward”), θØ=180 (= θ9) as the 9 o‟clock direction (“left”) and θØ=270(= θ6) as the 6 o‟clock direction (“bottom”). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. Optimum viewing angle direction is 6 „clock.

4.2 Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast ratio		CR	Θ = 0°	550	800	-		Note 2
Transmittance		Tr.		3.34	3.93	-	%	Without APF Note 3
White Chromaticity		x_w		0.277	0.292	0.307		Note 4 CF Glass Base on C Light
		y_w		0.318	0.333	0.348		
Reproduction of color (C light)	Red	R_x		0.650	0.665	0.680		
		R_y		0.308	0.323	0.338		
	Green	G_x		0.257	0.272	0.287		
		G_y		0.573	0.588	0.613		
	Blue	B_x		0.119	0.134	0.149		
		B_y		0.106	0.121	0.136		
Response Time (Rising + Falling)		$T_r + T_f$	Ta= 25° C Θ = 0°	-	35	-	ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer

4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. The Definition of Vth & Vsat

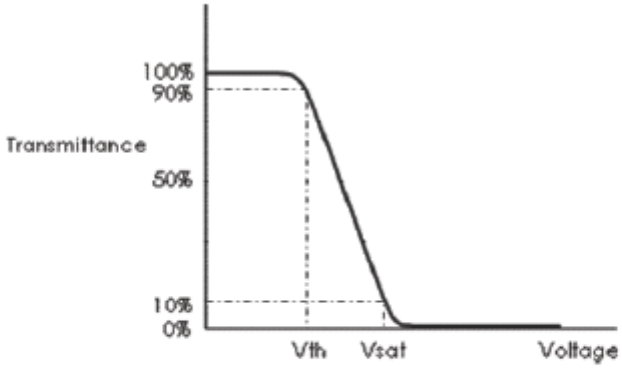


Figure 2. Measurement Set Up

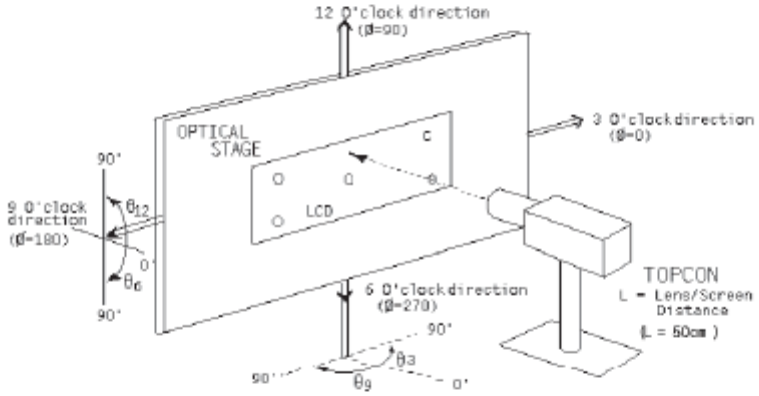
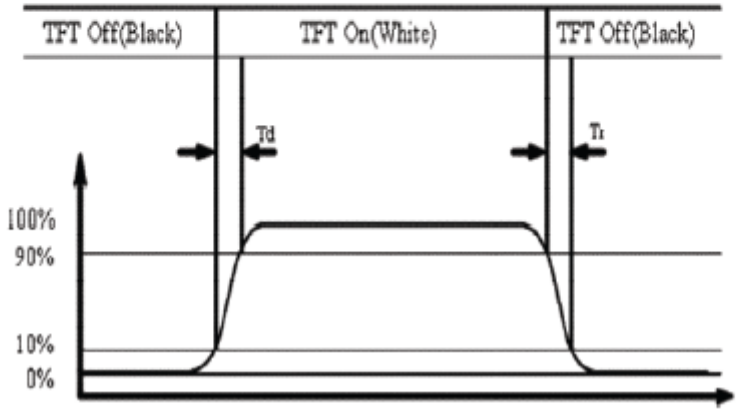


Figure 3. Response Time Testing



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	5.0	**V**
Digital interface supple Voltage	VDDIO	-0.3	4.0	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	3.0	3.3	4.2	V	--
Digital interface supple Voltage	VDDIO	1.65	3.3	4.2	V	--
Normal mode Current consumption	IDD	--	30	--	mA	--
Level input voltage	V_{IH}	$0.7V_{DDIO}$	--	V_{DDIO}	V	--
	V_{IL}	GND	--	$0.3V_{DDIO}$	V	--
Level output voltage	V_{OH}	V_{DDIO}-0.4	--	--	V	--
	V_{OL}	GND	--	GND+0.4	V	--

5.3 LED Backlight Characteristics

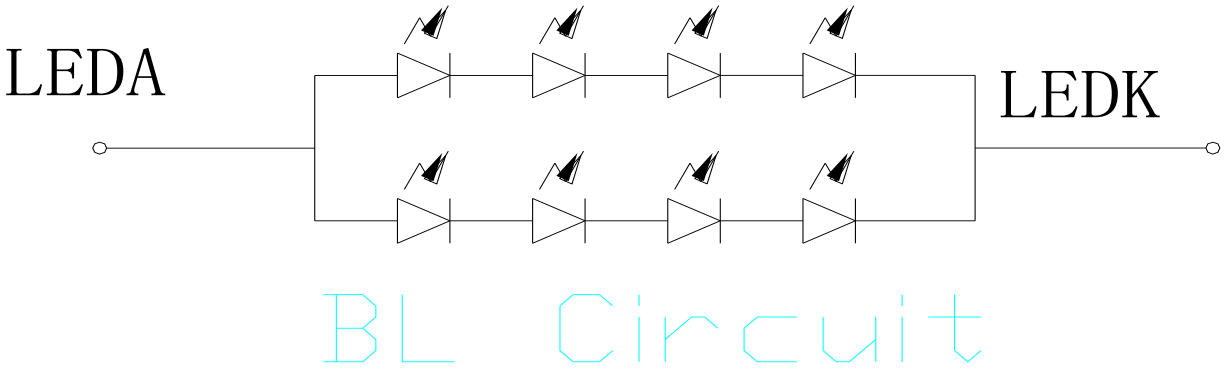
The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	--
Forward Voltage	V_F	--	12.8	--	V	--
LCM Luminance	L_V	400	--	--	cd/m2	I_F=40mA
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	--

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta= 25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25 ℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current

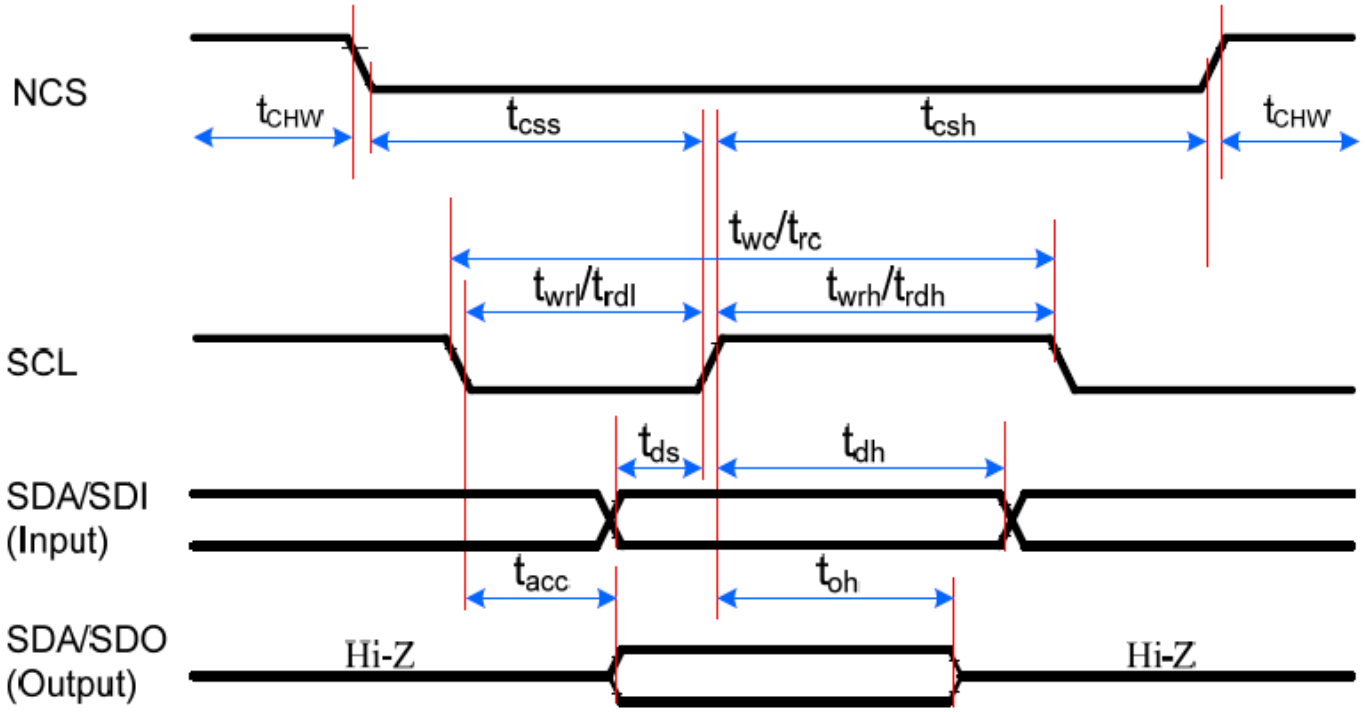
driving method is suggested.



BL Circuit

6. TFT AC Characteristic

6.1 Display Serial Interface Timing Characteristics (3-line SPI system)

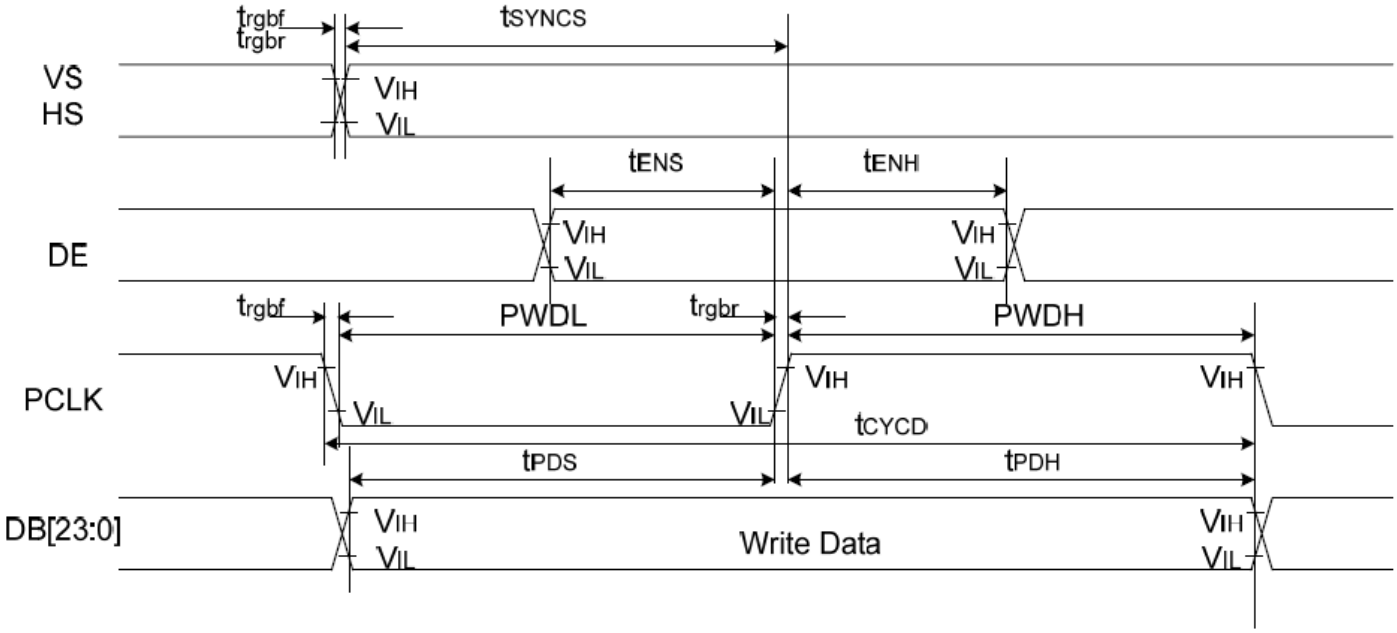


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

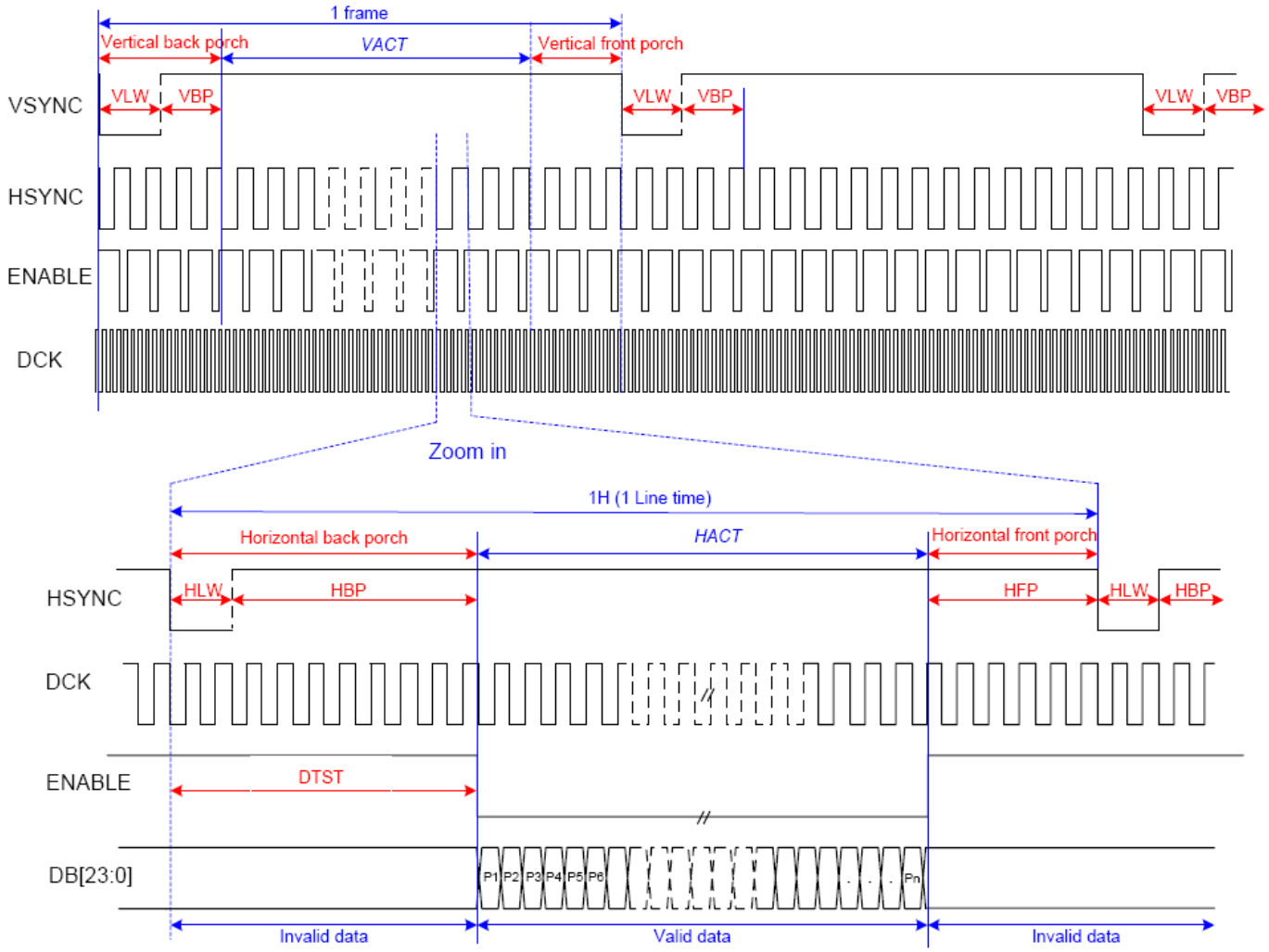
1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

6.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2⋯, pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		41.7	MHz

6.5 Reset input timing

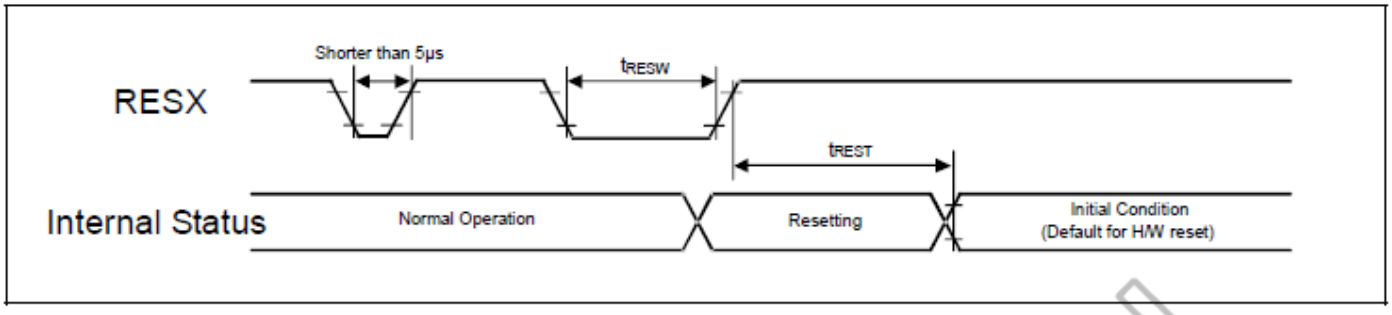


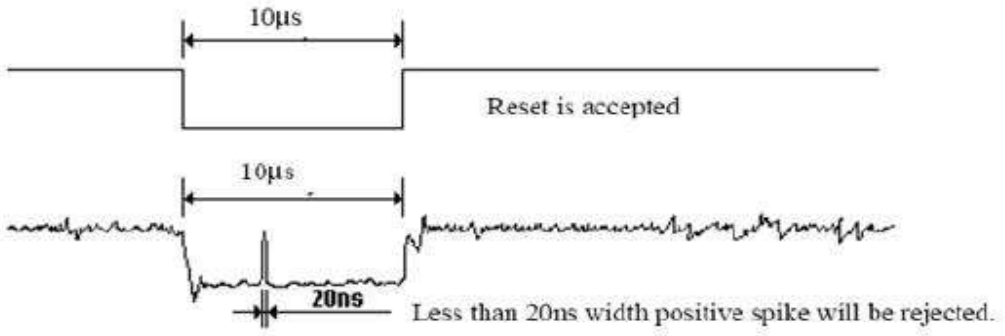
Figure 8.7: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	-	-	5	When reset is applied during Sleep In mode	ms
		-	-	-	120	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.10: Reset timing

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.47	V	1
I/O Digital Voltage	VDDIO	-0.3	3.47	V	1
Operating temperature	T_{OP}	-20	+70	℃	-
Storage temperature	T_{ST}	-30	+80	℃	-

NOTES:

1. *If used beyond the absolute maximum ratings, GT911 may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.*

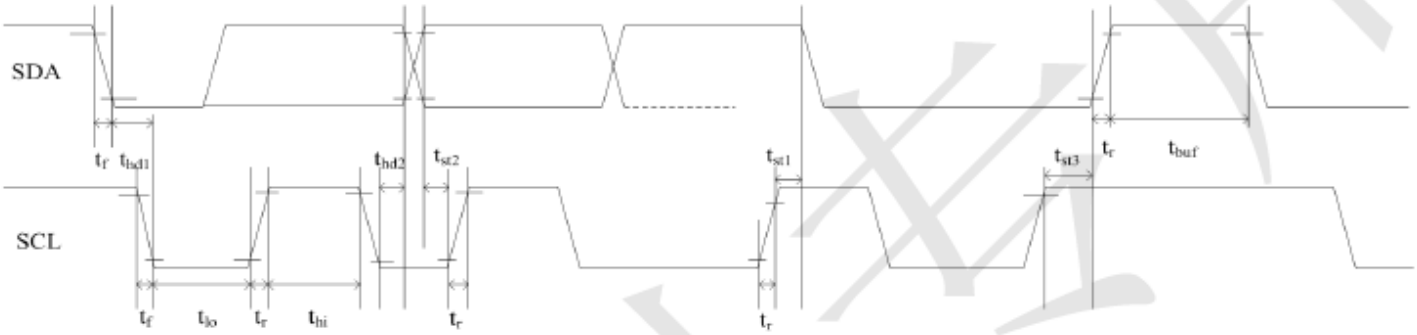
7.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD	2.8	-	3.3	V	
I/O Digital supply voltage	VDDIO	1.8	-	3.3	V	
Normal operation mode Current consumption	I_{opr}	-	8	14.5	mA	
Green mode Current consumption	I_{mon}	-	3.3	-	mA	
Sleep mode Current consumption	I_{slp}	70	-	120	uA	
Level input voltage	V_{IH}	$0.75V_{DDIO}$	-	$V_{DDIO}+0.3$	V	
	V_{IL}	-0.3	-	$0.25V_{DDIO}$	V	
Level output voltage	V_{OH}	$0.85V_{DDIO}$	-	-	V	
	V_{OL}	-	-	$0.15V_{DDIO}$	V	

7.2 AC Characteristics

7.2.1 I2C Interface

GT911 provides a standard I²C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I²C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

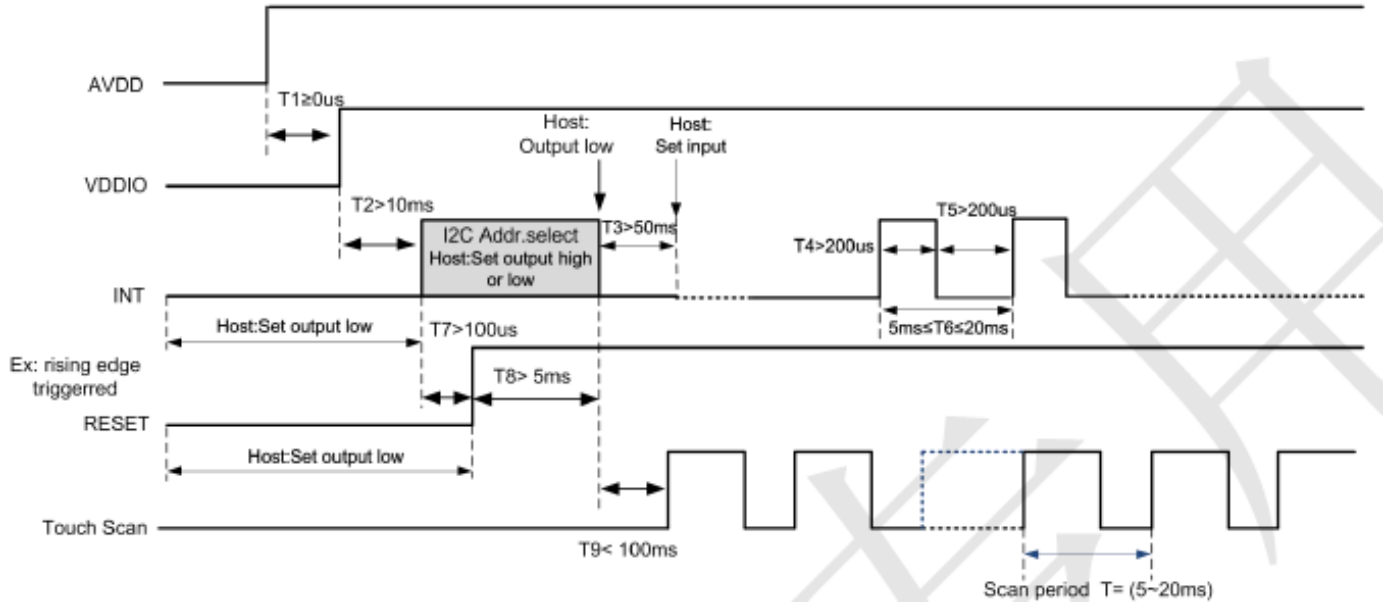
Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

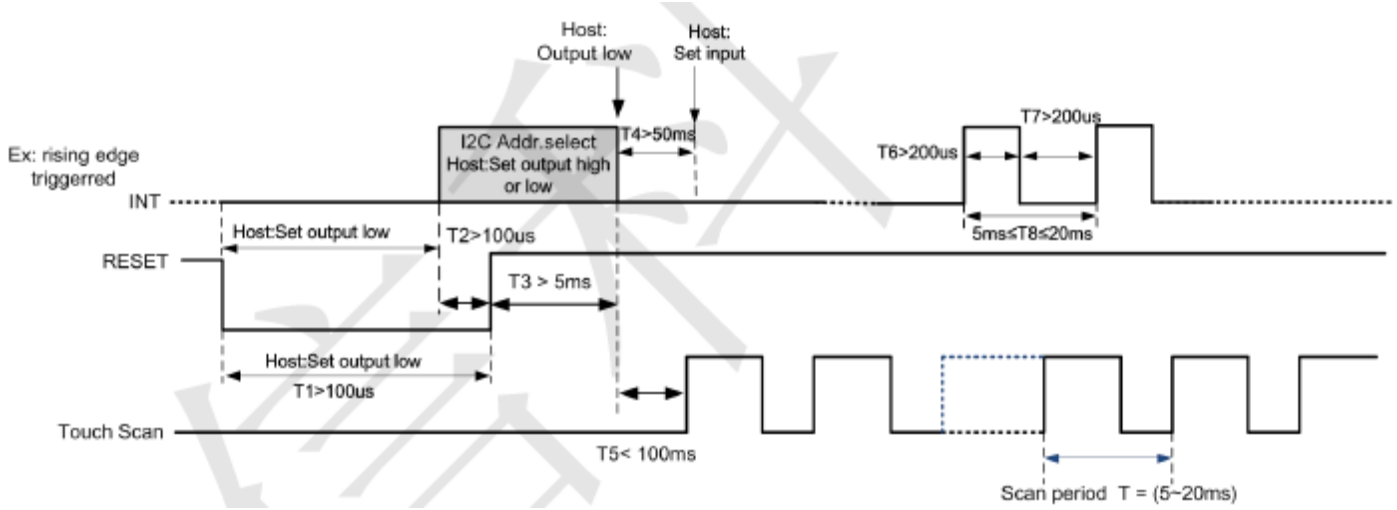
GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the

address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

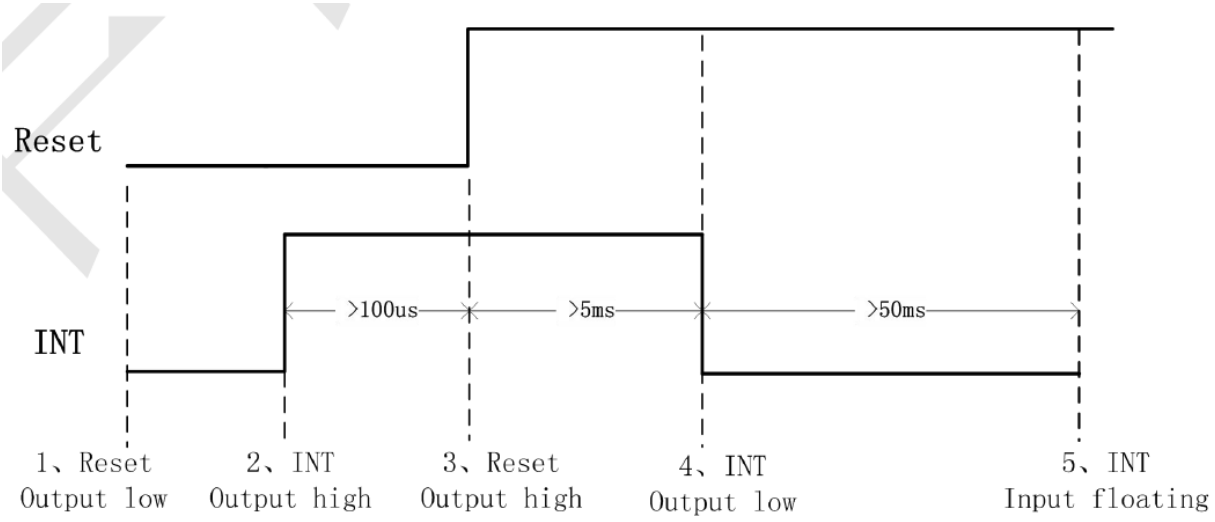
Power-On Timing:



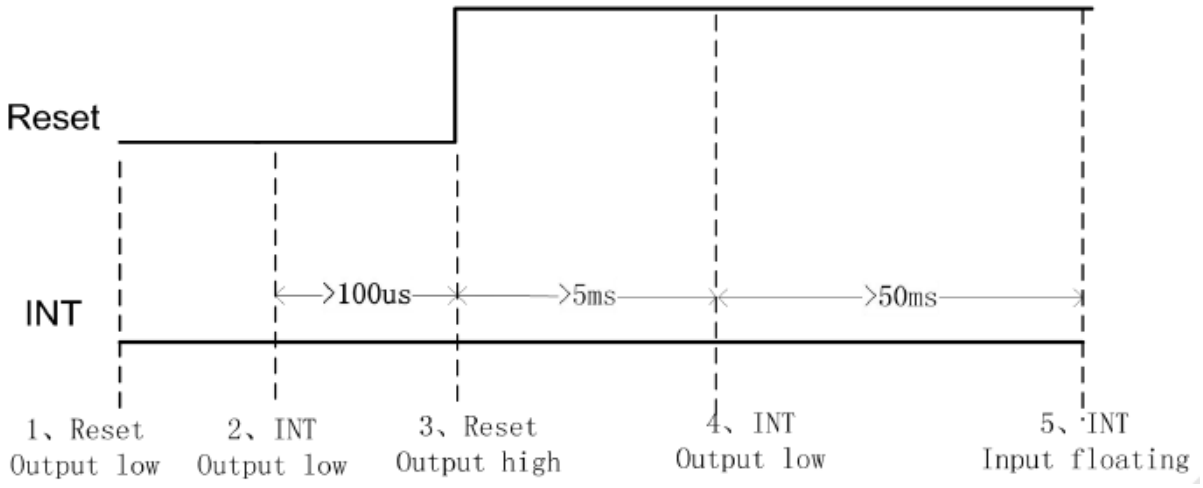
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

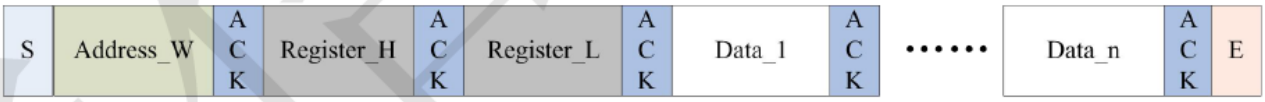
All slave devices connected to I^2C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)



Timing for Write Operation

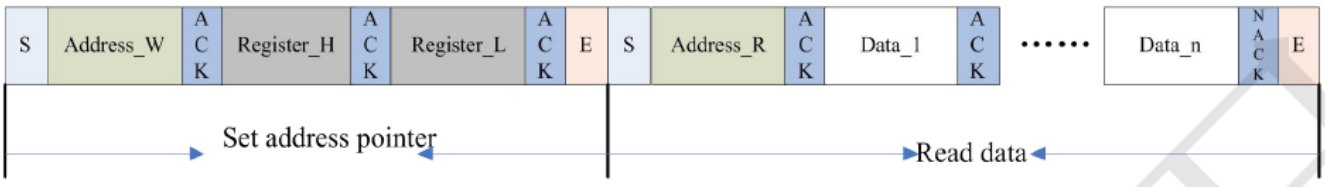
The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

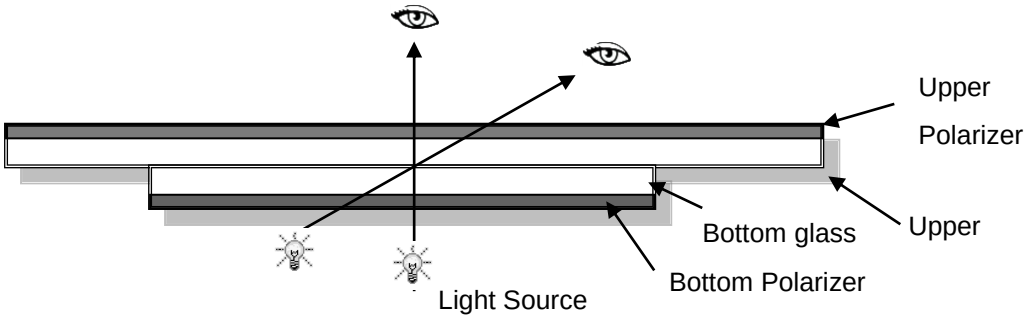
Temperature : 25±5℃

Humidity : 65%±10%RH

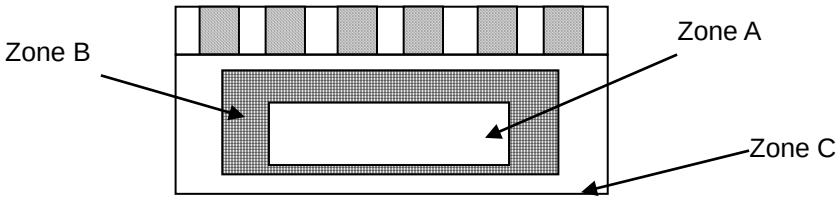
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

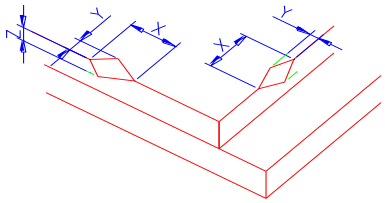
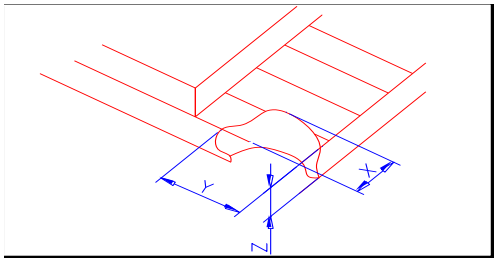
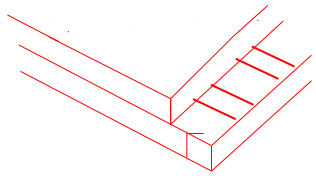
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

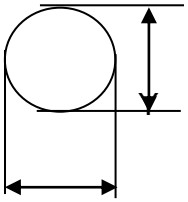
8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken

NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

Number	Items	Criteria (mm)

2.0 Spot defect



X

Φ=(X+Y)/2

① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ＞0.25	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.30	2		
Φ＞0.30	0		

③ Polarizer accidented spot

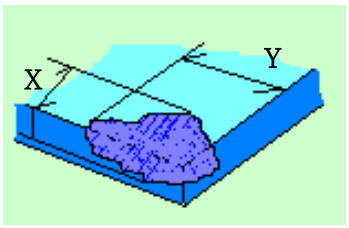
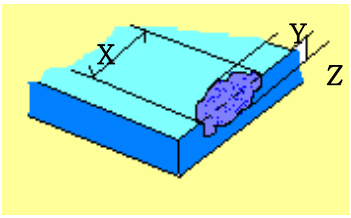
Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

Line defect (LCD/TP /Polarizer black/white line, scratch, stain)

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
Φ≤0.03	Ignore	Ignore		Ignore
0.03<W≤0.05	L≤3.0	N≤2		
0.05<W≤0.08	L≤2.0	N≤2		
0.08<W	Define as spot defect			

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
</table>

<table>
<tr><td rowspan="3">5.0</td><td rowspan="3">TP Related</td><td>TP bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2">3（distance≧</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.15mm</td></tr>
<tr><td>Newton Ring</td><td>Newton Ring area>1/3 TP area NG
Newton Ring area≤1/3 TP area OK</td><td> 
</td></tr>
</table>

<table>
<tr>
<td></td>
<td></td>
<td>TP corner broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TP edge broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11.Packing

----TBD----------