DCR4500A42

Phase Control Thyristor

Replaces DS5942-7 DS5942-8 March 2022 (LN41637)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Crowbar
- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	**4200V**
$I_{T(AV)}$	**4450A**
I_{TSM}	**60000A**
dV/dt*	**2000V/µs**
dI/dt	**500A/µs**

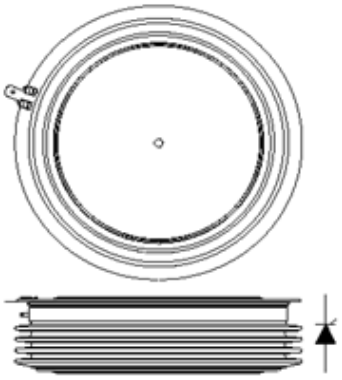
*** Higher dV/dt selections are available on request**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR4500A42* DCR4500A40 DCR4500A36	4200 4000 3600	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 300mA, V_{DRM}, V_{RRM} t_p = 10ms V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

*4100V @ -40°C, 4200V @ 0°C



Outline type code: A

(See Package Details for further information)

Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR4500A42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	4450	A
$I_{T(RMS)}$	RMS value	-	6990	A
I_T	Continuous (direct) on-state current	-	6270	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C V_R = 0	60.0	kA
I^2t	I^2t for fusing		18.0	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	6.0	°C/kW
		Single side cooled	Anode DC	-	10.4	°C/kW
			Cathode DC	-	14.9	°C/kW
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 83kN (with mounting compound)	Double side	-	1.0	°C/kW
			Single side	-	2.0	°C/kW
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			74	91	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C	-	300	mA
		At 50% V_{RRM}/V_{DRM}, T_{case} = 125°C	20	-	mA

Symbol	Parameter	Test Conditions		Min.	Max.	Units
V_{TM}	Instantaneous forward voltage	At 4000A peak, T_j = 125°C		1.30	1.45	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	2000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Repetitive 50Hz	-	200	A/µs
			Non-repetitive	-	500	A/µs
$V_{T(TO)}$	Threshold voltage - Low level	500A to 3400A at T_{case} = 125°C		-	0.81	V
	Threshold voltage - High level	3400A to 9000A at T_{case} = 125°C		-	0.98	V
r_T	On-state slope resistance - Low level	500A to 3400A at T_{case} = 125°C		-	0.17	mΩ
	On-state slope resistance - High level	3400A to 9000A at T_{case} = 125°C		-	0.12	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	I_T = 5000A, T_j = 125°C, V_R = 200V, dI/dt = 5A/µs, dV_{DR}/dt = 20V/µs linear		-	900	µs
Q_S	Stored charge	I_T = 1700A, T_j = 125°C, dI/dt = 1A/µs, V_R ~ 1700V, C_S = 1µF, R_S = 63Ω		2570	5350	µC
I_{RR}	Reverse recovery current			42	68	A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	400	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

CURVES

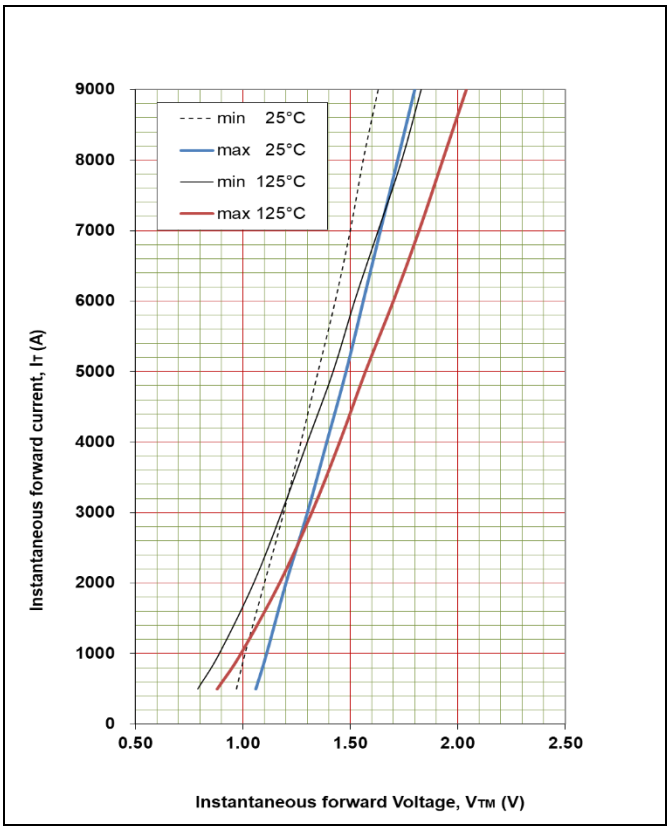


Fig. 2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.090451
B = 0.121408
C = 0.000109
D = -0.001368

These values are valid for T_j = 125°C for I_T 500A to 9000A

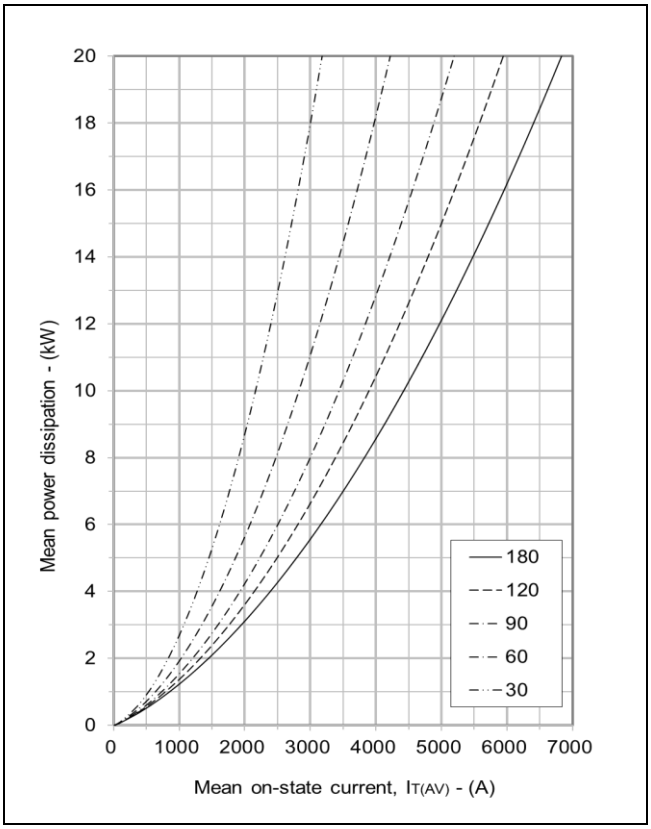


Fig. 3 On-state power dissipation - sine wave

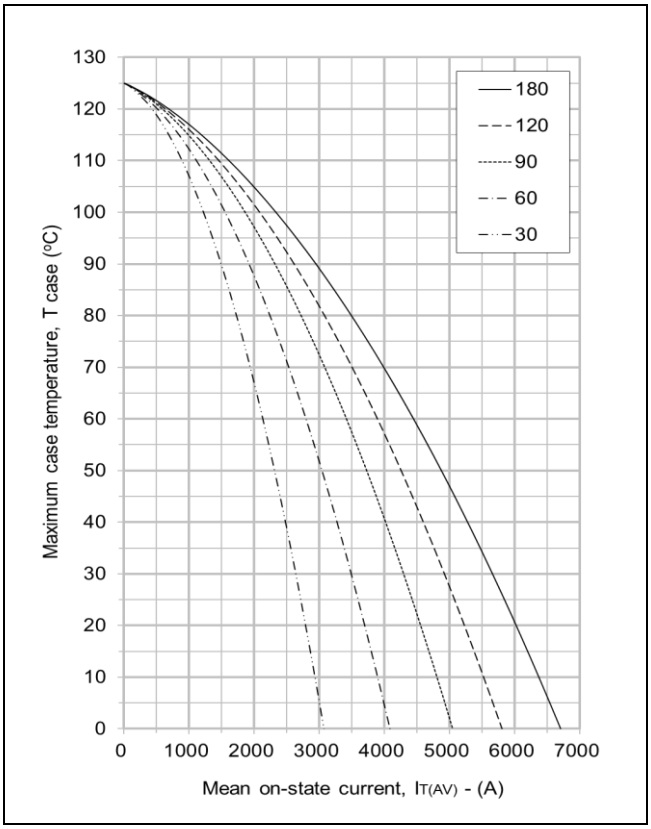


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

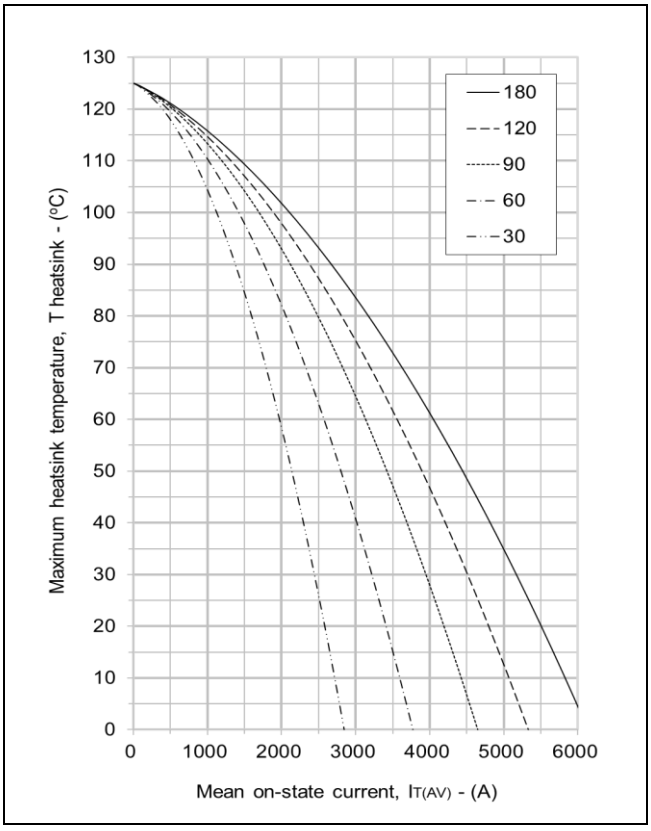


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

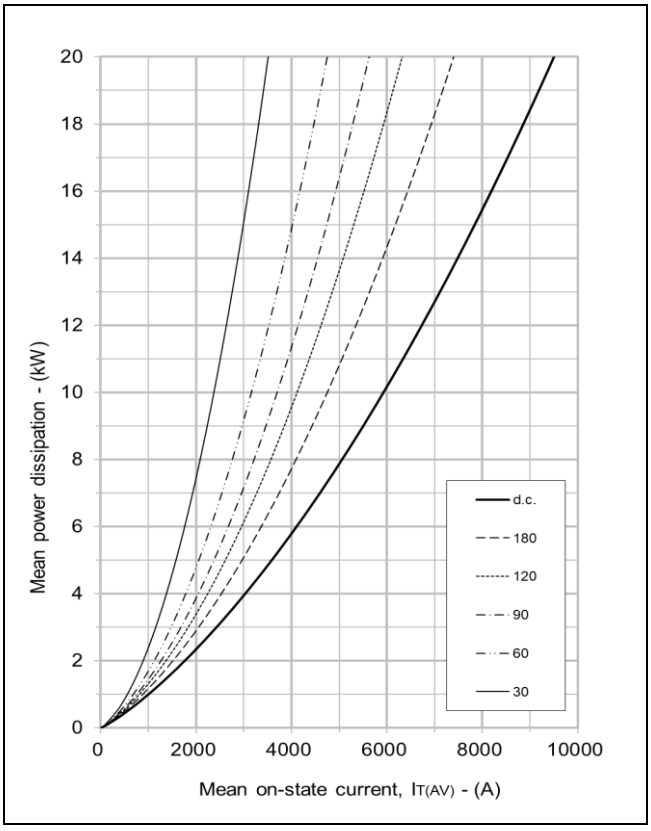


Fig. 6 On-state power dissipation - rectangular wave

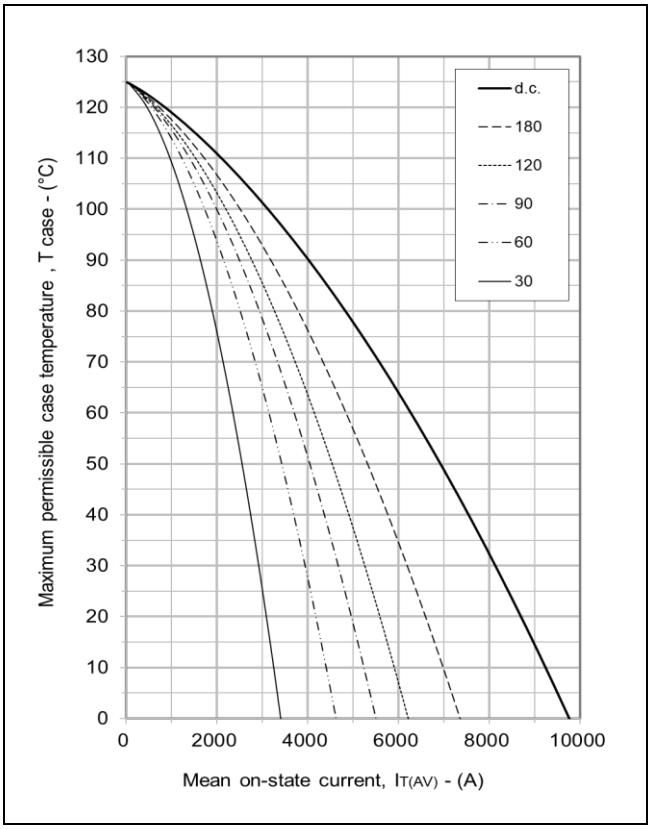


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

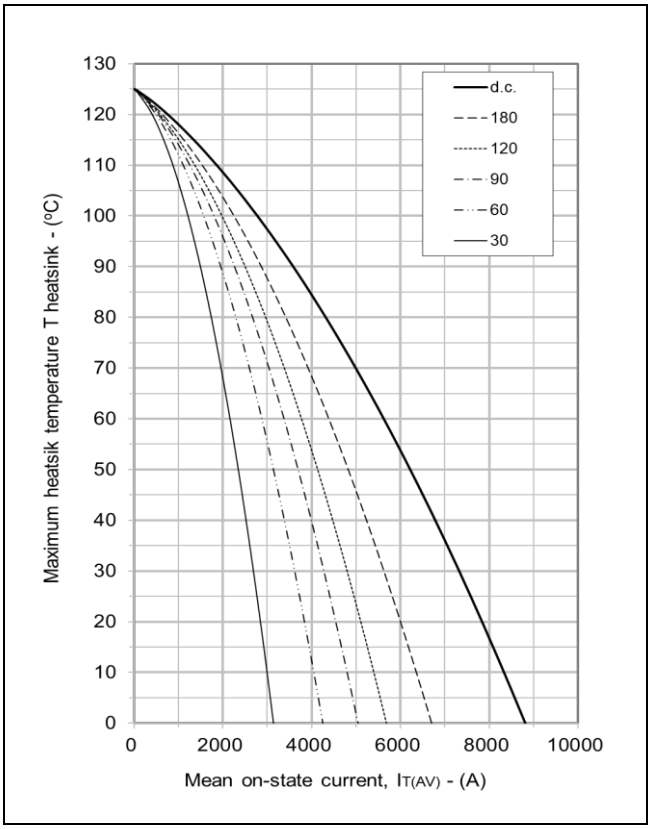
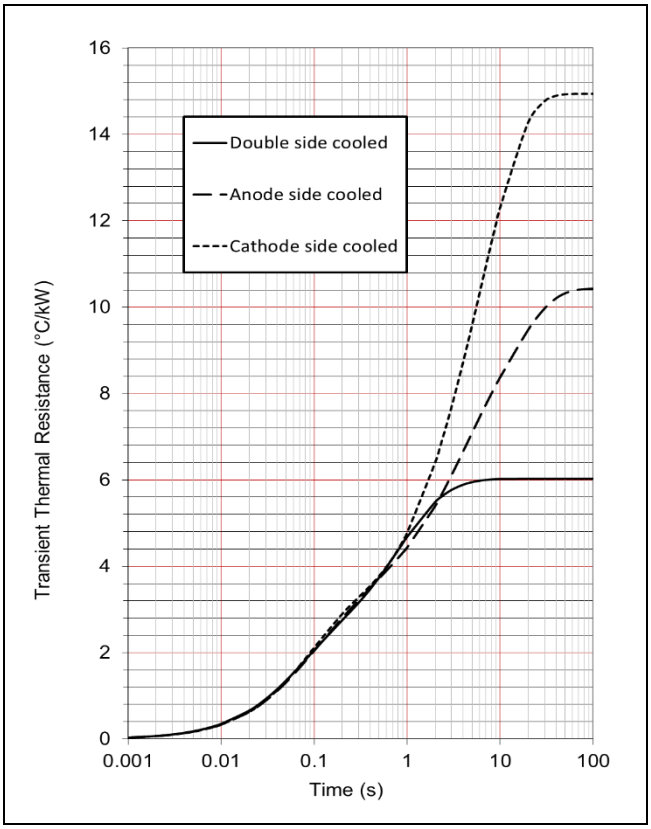


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	Ri(°C/kW)	3.015	1.049	0.984	0.984
	Ti(s)	0.704	1.905	0.059	0.059
Anode side cooled	Ri(°C/kW)	3.156	4.093	1.557	1.624
	Ti(s)	2.690	13.792	0.059	0.206
Cathode side cooled	Ri(°C/kW)	7.077	3.483	1.746	2.634
	Ti(s)	6.649	8.436	1.762	0.081

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.44	0.31
120	0.49	0.43
90	0.55	0.49
60	0.60	0.55
30	0.64	0.61
15	0.66	0.64

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.42	0.30
120	0.47	0.41
90	0.52	0.46
60	0.57	0.52
30	0.61	0.58
15	0.62	0.61

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.42	0.30
120	0.47	0.41
90	0.52	0.46
60	0.57	0.52
30	0.60	0.58
15	0.62	0.60

Fig.9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

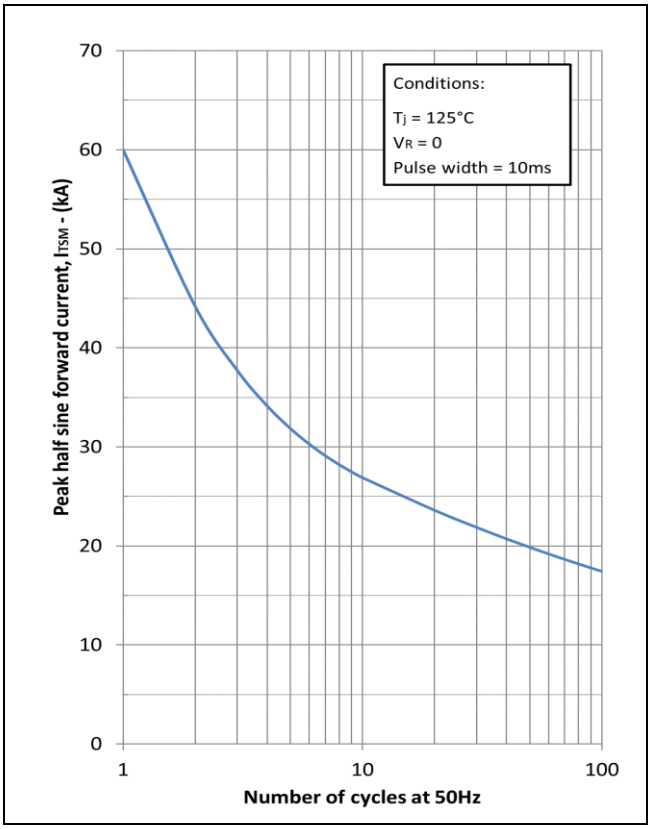


Fig. 10 Multi-cycle surge current

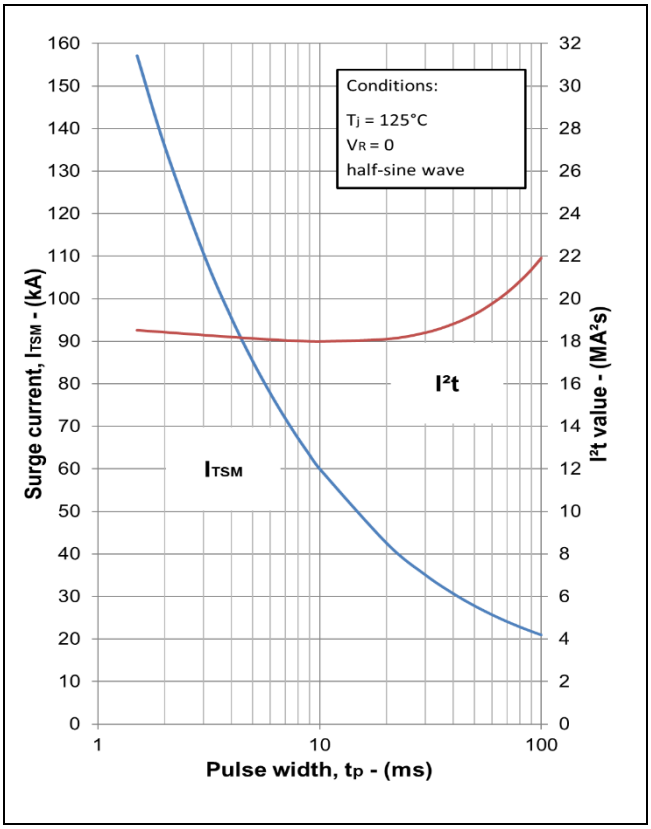


Fig. 11 Single-cycle surge current

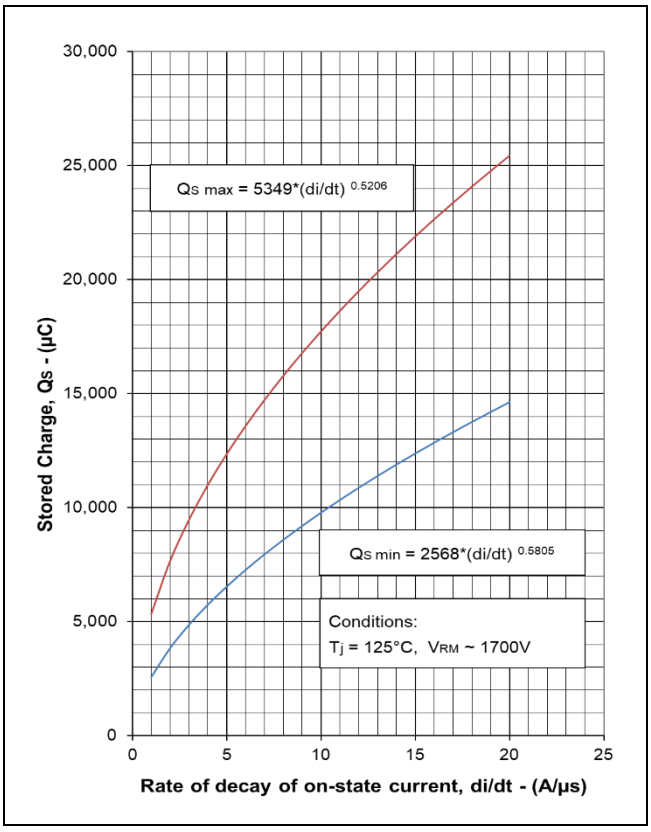


Fig. 12 Stored charge

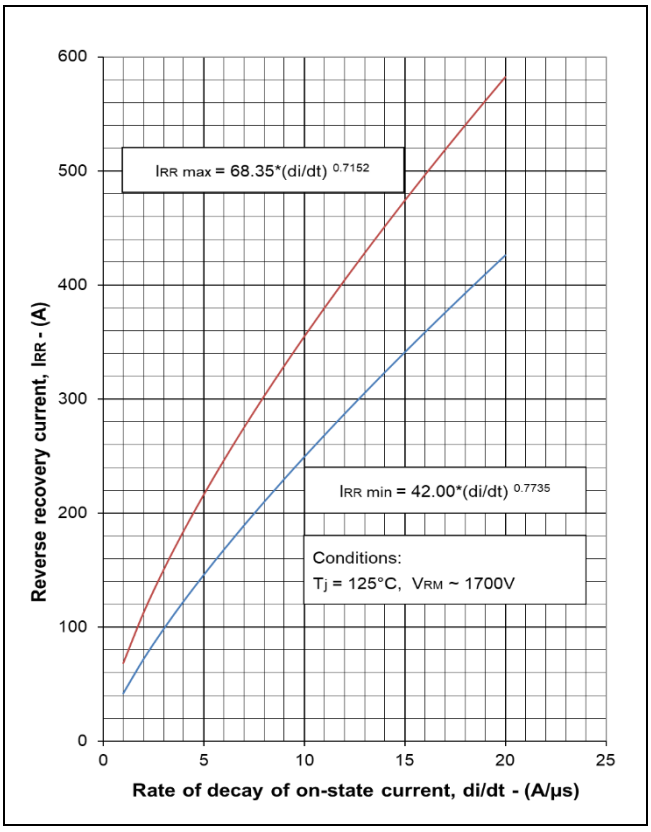


Fig. 13 Reverse recovery current

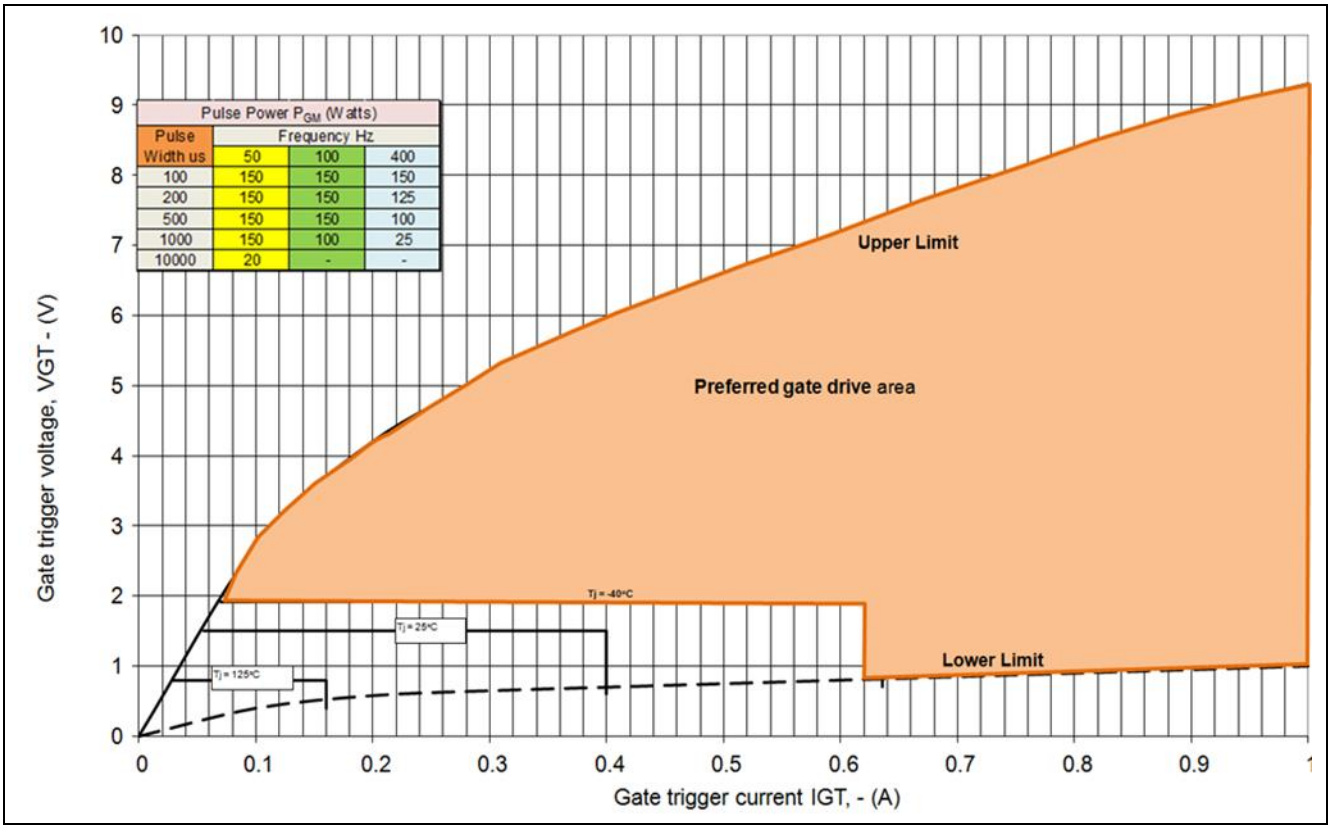


Fig.14 Gate characteristics

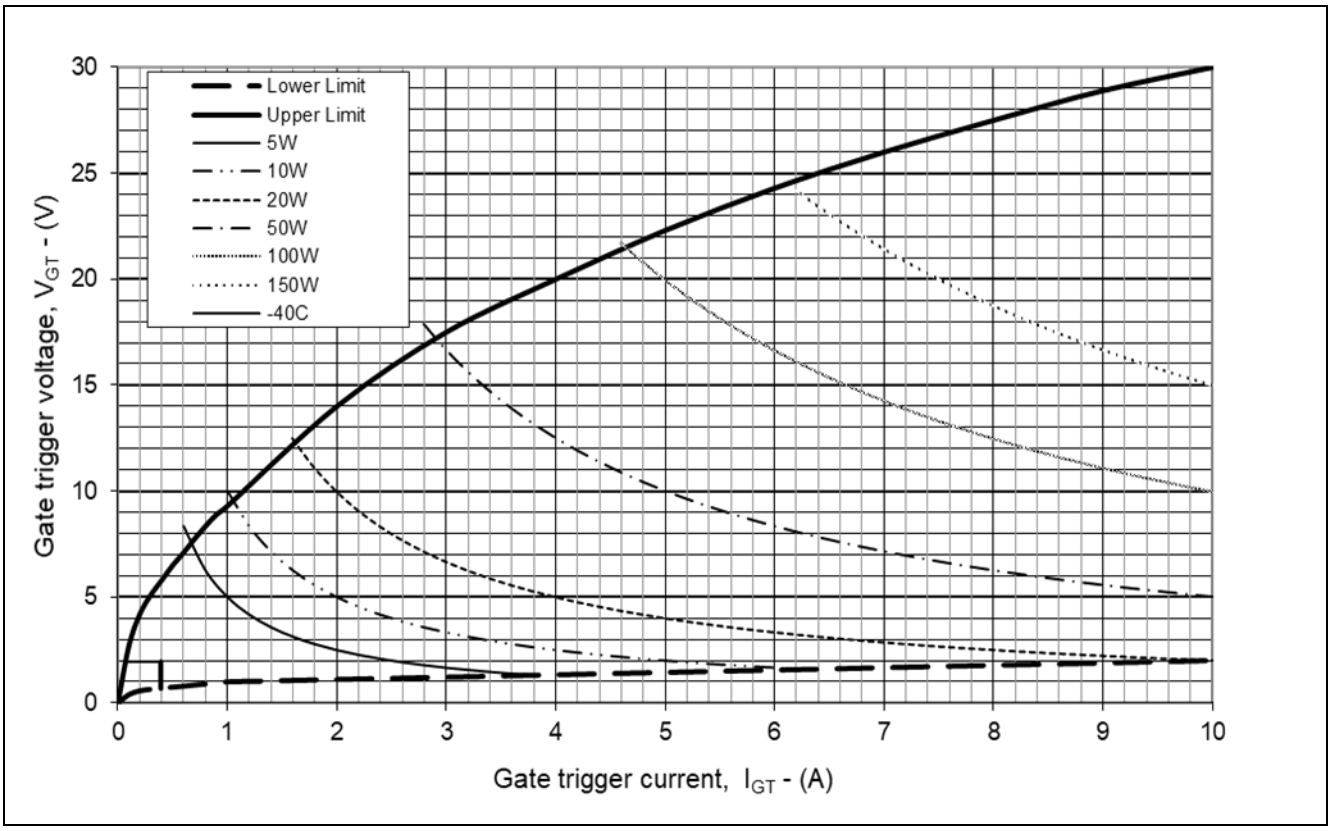


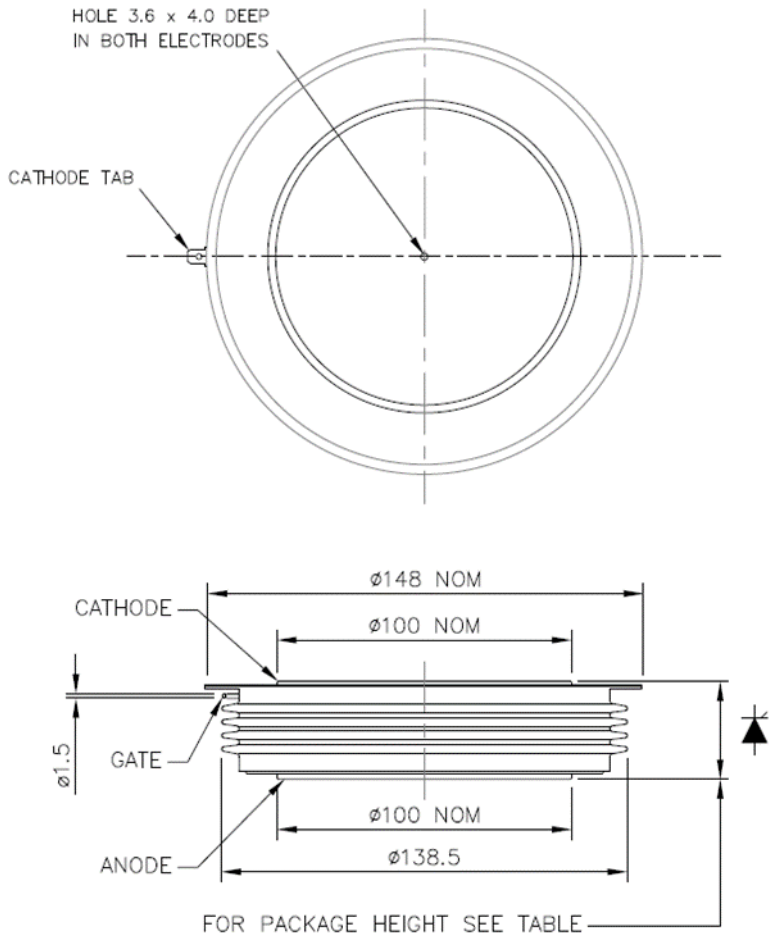
Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR2770A85	36.2	35.6
DCR2560A85	36.2	35.6
DCR3360A65	35.9	35.2
DCR3120A65	35.9	35.2
DCR3990A52	35.6	35.0
DCR3700A52	35.6	35.0
DCR4500A42	**35.5**	**34.8**
DCR4160A42	35.5	34.8
DCR5480A28	35.3	34.6

Clamping force: 82.5kN ± 10%

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: A

Fig. 16 Package outline

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