

## DACx0508 Octal, 16-, 14-, 12-Bit, SPI, Voltage Output DAC with Internal Reference

### 1 Features

- Performance
  - INL:  $\pm 1$  LSB Maximum at 16-Bit Resolution
  - TUE:  $\pm 0.1\%$  of FSR Maximum
- Integrated 2.5 V Precision Internal Reference
  - Initial Accuracy:  $\pm 5$  mV Maximum
  - Low Drift: 2 ppm/ $^{\circ}\text{C}$  Typical, DAC80508
- High Drive Capability: 20 mA with 0.5 V from Supply Rails
- Flexible Output Configuration
  - User Selectable Gain: 2, 1 or  $\frac{1}{2}$
  - Reset to Zero Scale or Midscale
  - Clear Output Function: DACx0508C
- Wide Operating Range
  - Power Supply: 2.7 V to 5.5 V
  - Temperature Range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- 50 MHz SPI Compatible Serial Interface
  - 1.7 V to 5.5 V Operation
  - Daisy Chain Operation
  - CRC Error Check
- Low Power: 0.6 mA/Channel at 5.5 V
- Small Packages:
  - 3 mm  $\times$  3 mm, 16-Pin WQFN
  - 2.4 mm  $\times$  2.4 mm, 16-Pin DSBGA

### 2 Applications

- Optical Networking
- Wireless Infrastructure
- Industrial Automation
- Data Acquisition Systems

### 3 Description

The DACx0508 is a pin-compatible family of low power, eight-channel, buffered voltage-output, digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx0508 includes a 2.5-V, 5-ppm/ $^{\circ}\text{C}$  internal reference, eliminating the need for an external precision reference in most applications. A user selectable gain configuration provides full-scale output voltages of 1.25 V (gain =  $\frac{1}{2}$ ), 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7-V to 5.5-V supply, is specified monotonic and provides high linearity of  $\pm 1$  LSB INL.

Communication to the DACx0508 is performed through a serial interface that operates at clock rates up to 50 MHz. The VIO pin enables serial interface operation from 1.7 V to 5.5 V. The DACx0508 flexible interface enables operation with a wide range of industry-standard microprocessors and microcontrollers.

The DACx0508 incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device. The device consumes low current of 0.6 mA/channel at 5.5 V, making it suitable for battery-operated equipment. A per-channel power-down feature reduces the device current consumption to 15  $\mu\text{A}$ .

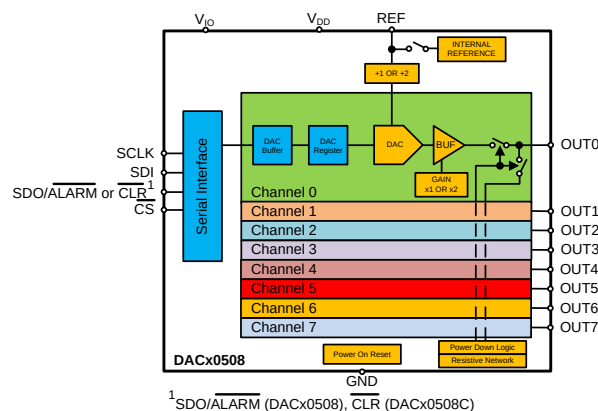
The DACx0508 is characterized for operation over the temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and is available in small packages.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)          |
|-------------|------------|--------------------------|
| DACx0508    | WQFN (16)  | 3.00 mm $\times$ 3.00 mm |
|             | DSBGA (16) | 2.40 mm $\times$ 2.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Block Diagram



## Table of Contents

|                                                |           |                                                      |           |
|------------------------------------------------|-----------|------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 8.5 Programming.....                                 | <b>28</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | 8.6 Register Map.....                                | <b>30</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | <b>9 Application and Implementation</b> .....        | <b>36</b> |
| <b>4 Revision History</b> .....                | <b>2</b>  | 9.1 Application Information.....                     | <b>36</b> |
| <b>5 Device Comparison Table</b> .....         | <b>4</b>  | 9.2 Typical Application .....                        | <b>38</b> |
| <b>6 Pin Configuration and Functions</b> ..... | <b>5</b>  | <b>10 Power Supply Recommendations</b> .....         | <b>40</b> |
| <b>7 Specifications</b> .....                  | <b>6</b>  | <b>11 Layout</b> .....                               | <b>41</b> |
| 7.1 Absolute Maximum Ratings .....             | <b>6</b>  | 11.1 Layout Guidelines .....                         | <b>41</b> |
| 7.2 ESD Ratings.....                           | <b>6</b>  | 11.2 Layout Examples.....                            | <b>41</b> |
| 7.3 Recommended Operating Conditions.....      | <b>6</b>  | <b>12 Device and Documentation Support</b> .....     | <b>43</b> |
| 7.4 Thermal Information .....                  | <b>7</b>  | 12.1 Related Links .....                             | <b>43</b> |
| 7.5 Electrical Characteristics.....            | <b>7</b>  | 12.2 Receiving Notification of Documentation Updates | <b>43</b> |
| 7.6 Typical Characteristics .....              | <b>10</b> | 12.3 Community Resources.....                        | <b>43</b> |
| <b>8 Detailed Description</b> .....            | <b>20</b> | 12.4 Trademarks .....                                | <b>43</b> |
| 8.1 Overview .....                             | <b>20</b> | 12.5 Electrostatic Discharge Caution.....            | <b>43</b> |
| 8.2 Functional Block Diagram .....             | <b>20</b> | 12.6 Glossary .....                                  | <b>43</b> |
| 8.3 Feature Description.....                   | <b>21</b> | <b>13 Mechanical, Packaging, and Orderable</b>       |           |
| 8.4 Device Functional Modes.....               | <b>25</b> | <b>Information</b> .....                             | <b>43</b> |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (April 2018) to Revision D                                                                                                                    | Page     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| • Changed TUE in Features from $\pm 0.14\%$ to $0.1\%$ .....                                                                                                          | <b>1</b> |
| • Changed Low Drift in Features from 5 ppm/°C to 2 ppm/°C and added DAC80508 .....                                                                                    | <b>1</b> |
| • Added Clear Output Function: DACx0508C to Features.....                                                                                                             | <b>1</b> |
| • Deleted 4-Wire Mode from Features .....                                                                                                                             | <b>1</b> |
| • Deleted 4-wire from second paragraph in Description .....                                                                                                           | <b>1</b> |
| • Deleted DAC80508 Product Preview footnote from Device Information .....                                                                                             | <b>1</b> |
| • Deleted Product Preview from DAC80508Z and DAC80508M in <a href="#">Device Comparison Table</a> .....                                                               | <b>4</b> |
| • Added DAC80508ZC and DAC80508MC to <a href="#">Device Comparison Table</a> .....                                                                                    | <b>4</b> |
| • Added DAC60508ZC and DAC60508MC to <a href="#">Device Comparison Table</a> .....                                                                                    | <b>4</b> |
| • Added DACx0508 to SDO/ALARM pin description in Pin Functions .....                                                                                                  | <b>5</b> |
| • Added $\overline{\text{CLR}}$ pin (DACx0508C) in Pin Functions .....                                                                                                | <b>5</b> |
| • Changed SCLK, SDI, SDO/ALARM and $\overline{\text{CS}}$ to Digital pins for Pin voltage in <a href="#">Absolute Maximum Ratings</a> .....                           | <b>6</b> |
| • Added Total unadjusted error, DAC80508. All Gains row in <a href="#">Electrical Characteristics</a> .....                                                           | <b>7</b> |
| • Added Offset error, DAC80508. WQFN and BGA packages. All gains. row in <a href="#">Electrical Characteristics</a> .....                                             | <b>7</b> |
| • Added Full-scale error, DAC80508. All gains row in <a href="#">Electrical Characteristics</a> .....                                                                 | <b>7</b> |
| • Added Gain error, DAC80508 row in <a href="#">Electrical Characteristics</a> .....                                                                                  | <b>7</b> |
| • Changed Short circuit current, DAC code = full scale. Output shorted to GND TYP from 35 mA to 30 mA in <a href="#">Electrical Characteristics</a> .....             | <b>8</b> |
| • Changed Short circuit current, DAC code = zero scale. Output shorted to $V_{\text{DD}}$ TYP from 30 mA to 35 mA in <a href="#">Electrical Characteristics</a> ..... | <b>8</b> |
| • Added Channel to Channel DC crosstalk, DAC80508. Measured channel at midscale. Adjacent channel at full scale in <a href="#">Electrical Characteristics</a> .....   | <b>8</b> |
| • Added Channel to Channel DC crosstalk, DAC80508. Measured channel at midscale. All other channels at full scale in <a href="#">Electrical Characteristics</a> ..... | <b>8</b> |
| • Added Reference output drift, DAC80508 in <a href="#">Electrical Characteristics</a> .....                                                                          | <b>9</b> |
| • Added Reference thermal hysteresis, DAC80508. First cycle in <a href="#">Electrical Characteristics</a> .....                                                       | <b>9</b> |

## Revision History (continued)

|                                                                                                                                                         |    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Added SDO/ $\overline{\text{ALARM}}$ to DIGITAL OUTPUTS heading in <a href="#">Electrical Characteristics</a> .....                                   | 9  |
| • Deleted $I_{DD}$ , Power-down max value in <a href="#">Electrical Characteristics</a> .....                                                           | 9  |
| • Changed <a href="#">Figure 1</a> to <a href="#">Figure 18</a> .....                                                                                   | 10 |
| • Changed <a href="#">Figure 20</a> to <a href="#">Figure 28</a> .....                                                                                  | 12 |
| • Changed <a href="#">Figure 34</a> .....                                                                                                               | 14 |
| • Changed <a href="#">Figure 35</a> .....                                                                                                               | 14 |
| • Changed <a href="#">Figure 37</a> .....                                                                                                               | 15 |
| • Changed <a href="#">Figure 38</a> .....                                                                                                               | 15 |
| • Added <a href="#">Figure 43</a> .....                                                                                                                 | 16 |
| • Added <a href="#">Figure 44</a> .....                                                                                                                 | 16 |
| • Changed <a href="#">Figure 58</a> .....                                                                                                               | 18 |
| • Deleted 4-wire from paragraph in <a href="#">Overview</a> section .....                                                                               | 20 |
| • Added paragraph to <a href="#">Overview</a> section .....                                                                                             | 20 |
| • Changed SDO/ $\overline{\text{ALARM}}$ to SDO/ $\overline{\text{ALARM}}$ or $\overline{\text{CLR}}$ in <a href="#">Functional Block Diagram</a> ..... | 20 |
| • Added <a href="#">CLEAR Operation (DACx0508C only)</a> section.....                                                                                   | 22 |
| • Added <a href="#">Figure 61</a> .....                                                                                                                 | 23 |
| • Deleted four-wire from <a href="#">Programming</a> section.....                                                                                       | 28 |
| • Added $\overline{\text{CLR}}$ pulse in <a href="#">Table 7</a> .....                                                                                  | 28 |
| • Added $\overline{\text{CLR}}$ delay and note in <a href="#">Table 7</a> .....                                                                         | 28 |
| • Changed table note for <a href="#">Table 8</a> .....                                                                                                  | 30 |
| • Added CLR-4TO7-MSK and CLR-0TO3-MSK bits for DACx0508C only to <a href="#">Figure 71</a> .....                                                        | 34 |
| • Added table note to <a href="#">Figure 71</a> .....                                                                                                   | 34 |
| • Added CLR-4TO7-MSK and CLR-0TO3-MSK bits for DACx0508C only to <a href="#">Table 13</a> .....                                                         | 34 |

## Changes from Revision B (January 2018) to Revision C

Page

|                                                                                                                                                      |   |
|------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| • Changed DAC80508Z, DAC70508Z, DAC60508Z, DAC80508M, DAC70508M, DAC60508M to DAC80508, DAC70508, DAC60508 in the data sheet header and footer ..... | 1 |
| • Changed DAC80508Z and DAC80508M to DAC80508 in Device Information table note.....                                                                  | 1 |

## Changes from Revision A (December 2017) to Revision B

Page

|                                                                                                         |    |
|---------------------------------------------------------------------------------------------------------|----|
| • Added 2.4 mm x 2.4 mm, 16-Pin DSBGA to Features .....                                                 | 1  |
| • Added DSBGA (16) package to Device Information .....                                                  | 1  |
| • Added DSBGA pinout.....                                                                               | 5  |
| • Added DSBGA package pin number column to Pin Functions table .....                                    | 5  |
| • Added DSBGA package pin number column to Pin Functions table .....                                    | 6  |
| • Added YZF column to Thermal Information .....                                                         | 7  |
| • Added Offset error test conditions and DSBGA package specific row to Electrical Characteristics ..... | 7  |
| • Added DSBGA Layout Example .....                                                                      | 42 |

## Changes from Original (June 2017) to Revision A

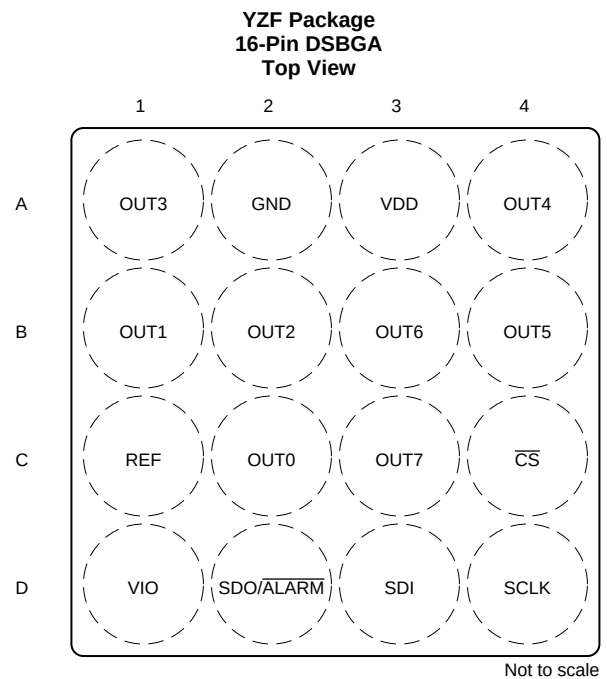
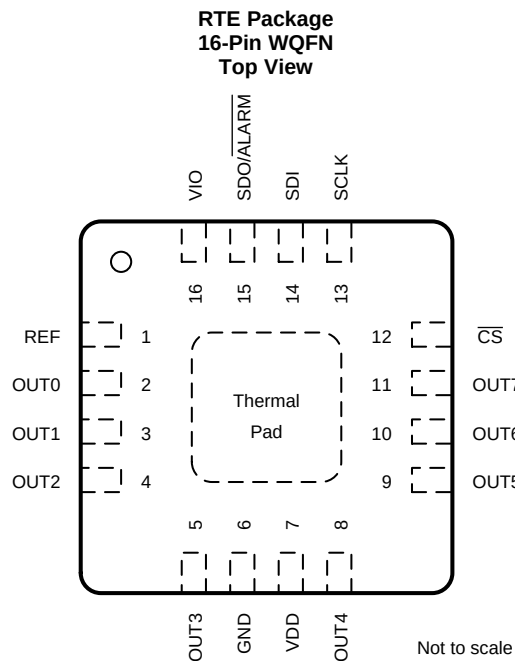
Page

|                                                         |   |
|---------------------------------------------------------|---|
| • Changed from Advance Information to Mixed Status..... | 1 |
|---------------------------------------------------------|---|

## 5 Device Comparison Table

| DEVICE     | RESOLUTION | REFERENCE                     | RESET    | SDO OR $\overline{\text{CLR}}$ OPERATION |
|------------|------------|-------------------------------|----------|------------------------------------------|
| DAC80508Z  | 16-Bit     | Internal (default) / External | Zero     | SDO                                      |
| DAC80508ZC |            |                               |          | $\overline{\text{CLR}}$                  |
| DAC80508M  |            |                               | Midscale | SDO                                      |
| DAC80508MC |            |                               |          | $\overline{\text{CLR}}$                  |
| DAC70508Z  | 14-Bit     | Internal (default) / External | Zero     | SDO                                      |
| DAC70508M  |            |                               | Midscale | SDO                                      |
| DAC60508Z  | 12-Bit     | Internal (default) / External | Zero     | SDO                                      |
| DAC60508ZC |            |                               |          | $\overline{\text{CLR}}$                  |
| DAC60508M  |            |                               | Midscale | SDO                                      |
| DAC60508MC |            |                               |          | $\overline{\text{CLR}}$                  |

## 6 Pin Configuration and Functions



### Pin Functions

| NAME                    | PIN      |           | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------------|----------|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                         | WQFN NO. | DSBGA NO. |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| REF                     | 1        | C1        | I/O  | When using internal reference, this is the reference output voltage pin (default). When using an external reference, this is the reference input pin to the device.                                                                                                                                                                                                                                                                                  |
| OUT0                    | 2        | C2        | O    | Analog output voltage from DAC 0.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT1                    | 3        | B1        | O    | Analog output voltage from DAC 1.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT2                    | 4        | B2        | O    | Analog output voltage from DAC 2.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT3                    | 5        | A1        | O    | Analog output voltage from DAC 3.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GND                     | 6        | A2        | GND  | Ground reference point for all circuitry on the device.                                                                                                                                                                                                                                                                                                                                                                                              |
| VDD                     | 7        | A3        | PWR  | Analog supply voltage (2.7 V to 5.5 V).                                                                                                                                                                                                                                                                                                                                                                                                              |
| OUT4                    | 8        | A4        | O    | Analog output voltage from DAC 4.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT5                    | 9        | B4        | O    | Analog output voltage from DAC 5.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT6                    | 10       | B3        | O    | Analog output voltage from DAC 6.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| OUT7                    | 11       | C3        | O    | Analog output voltage from DAC 7.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| $\overline{\text{CS}}$  | 12       | C4        | I    | Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, it enables the serial interface input shift register.                                                                                                                                                                                                                                                                   |
| SCLK                    | 13       | D4        | I    | Serial interface clock.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| SDI                     | 14       | D3        | I    | Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.                                                                                                                                                                                                                                                                                                                                    |
| SDO/ALARM               | 15       | D2        | O    | DACx0508. Serial interface data output (default). The SDO pin is in high impedance when CS pin is high. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit. Alternatively the pin can be configured as an ALARM open-drain output to indicate a CRC or reference alarm event. If configured as ALARM a 10 k $\Omega$ , pull-up resistor to V <sub>IO</sub> is required. |
| $\overline{\text{CLR}}$ |          |           | I    | DACx0508C. A low value on the $\overline{\text{CLR}}$ pin causes the DAC outputs of those channels configured for clear operation to update their registers and output to the reset value: zero scale (DACx0508Z) or midscale (DACx0508M). Bringing the CLR pin high causes the device to exit clear mode.                                                                                                                                           |

## Pin Functions (continued)

| PIN         |          |           | TYPE | DESCRIPTION                                                                                                                                                                               |
|-------------|----------|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | WQFN NO. | DSBGA NO. |      |                                                                                                                                                                                           |
| VIO         | 16       | D1        | PWR  | IO supply voltage (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the serial interface.                                                                                     |
| Thermal Pad | –        | –         | –    | The thermal pad is located on the bottom-side of the WQFN package. The thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance. |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                |                                             | MIN  | MAX                   | UNIT |
|----------------|---------------------------------------------|------|-----------------------|------|
| Supply voltage | V <sub>DD</sub> to GND                      | –0.3 | 6                     | V    |
|                | V <sub>IO</sub> to GND                      | –0.3 | 6                     |      |
| Pin voltage    | DAC outputs to GND                          | –0.3 | V <sub>DD</sub> + 0.3 | V    |
|                | REF to GND                                  | –0.3 | V <sub>DD</sub> + 0.3 |      |
|                | Digital pins to GND                         | –0.3 | V <sub>IO</sub> + 0.3 |      |
| Input current  | Input current to any pin except supply pins | –10  | 10                    | mA   |
| Temperature    | Operating free-air, T <sub>A</sub>          | –40  | 125                   | °C   |
|                | Junction, T <sub>J</sub>                    | –40  | 150                   |      |
|                | Storage, T <sub>stg</sub>                   | –60  | 150                   |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                                            |                                                                                             | VALUE | UNIT |
|--------------------------------------------|---------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per JEDEC Standard 22 Test Method A114-C.01 <sup>(1)</sup>          | ±3000 | V    |
|                                            | Charged-device model (CDM), per JEDEC Standard 22 Test Method C101, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                                  |                            | MIN | NOM | MAX                       | UNIT |
|-----------------------|----------------------------------|----------------------------|-----|-----|---------------------------|------|
| POWER SUPPLY          |                                  |                            |     |     |                           |      |
| V <sub>DD</sub>       | Analog supply voltage            |                            | 2.7 |     | 5.5                       | V    |
| V <sub>IO</sub>       | IO supply voltage                |                            | 1.7 |     | 5.5                       |      |
| DIGITAL INPUTS        |                                  |                            |     |     |                           |      |
| Digital input voltage |                                  |                            | 0   |     | V <sub>IO</sub>           | V    |
| REFERENCE INPUT       |                                  |                            |     |     |                           |      |
| V <sub>REFIN</sub>    | V <sub>DD</sub> = 2.7 V to 3.3 V | Reference divider disabled | 1.2 |     | (V <sub>DD</sub> – 0.2)/2 | V    |
|                       |                                  | Reference divider enabled  | 2.4 |     | V <sub>DD</sub> – 0.2     |      |
|                       | V <sub>DD</sub> = 3.3 V to 5.5 V | Reference divider disabled | 1.2 |     | V <sub>DD</sub> /2        |      |
|                       |                                  | Reference divider enabled  | 2.4 |     | V <sub>DD</sub>           |      |
| TEMPERATURE           |                                  |                            |     |     |                           |      |
| T <sub>A</sub>        | Operating free-air temperature   |                            | –40 |     | 125                       | °C   |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | DACx0508   |             | UNIT |
|-------------------------------|----------------------------------------------|------------|-------------|------|
|                               |                                              | RTE (WQFN) | YZF (DSBGA) |      |
|                               |                                              | 16 PINS    | 16 PINS     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 33.3       | 68.0        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 29.5       | 0.3         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 7.3        | 16.9        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2        | 0.2         | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 7.4        | 16.9        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 0.9        | n/a         | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

All minimum and maximum specifications at V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>IO</sub> = 1.7 V to 5.5 V, V<sub>REFIN</sub> = 1.25 V to 5.5 V, R<sub>LOAD</sub> = 2 kΩ to GND, C<sub>LOAD</sub> = 200 pF to GND, digital inputs at V<sub>IO</sub> or GND, T<sub>A</sub> = –40°C to 125°C (unless otherwise noted).

| PARAMETER                               | TEST CONDITIONS                                                                               | MIN | TYP    | MAX   | UNIT          |
|-----------------------------------------|-----------------------------------------------------------------------------------------------|-----|--------|-------|---------------|
| <b>STATIC PERFORMANCE<sup>(1)</sup></b> |                                                                                               |     |        |       |               |
| Resolution                              | DAC80508                                                                                      | 16  |        |       | Bits          |
|                                         | DAC70508                                                                                      | 14  |        |       |               |
|                                         | DAC60508                                                                                      | 12  |        |       |               |
| INL Integral nonlinearity               | DAC80508                                                                                      |     | ±0.5   | ±1    | LSB           |
|                                         | DAC70508                                                                                      |     | ±0.5   | ±1    |               |
|                                         | DAC60508                                                                                      |     | ±0.5   | ±1    |               |
| DNL Differential nonlinearity           | DAC80508. Specified 16-bit monotonic                                                          |     | ±0.5   | ±1    | LSB           |
|                                         | DAC70508. Specified 14-bit monotonic                                                          |     | ±0.5   | ±1    |               |
|                                         | DAC60508. Specified 12-bit monotonic                                                          |     | ±0.5   | ±1    |               |
| TUE Total unadjusted error              | DAC80508. All Gains                                                                           |     | ±0.05  | ±0.1  | %FSR          |
|                                         | DAC70508 and DAC60508. Gain = 1 and Gain = 2                                                  |     | ±0.06  | ±0.14 |               |
|                                         | DAC70508 and DAC60508. Gain = ½                                                               |     | ±0.1   | ±0.2  |               |
| Offset error                            | DAC80508. WQFN and BGA packages. All gains.                                                   |     | ±0.75  | ±1.5  | mV            |
|                                         | DAC70508 and DAC60508. WQFN package: Gain = 1, Gain = 2 and Gain = ½. DSBGA package: Gain = 2 |     | ±0.75  | ±1.5  |               |
|                                         | DAC70508 and DAC60508. DSBGA package: Gain = 1 and Gain = ½                                   |     | ±0.75  | ±2.5  |               |
| Zero-code error                         | DAC code = zero scale                                                                         |     | 0.5    | 1.5   | mV            |
| Full-scale error                        | DAC80508. All gains                                                                           |     | ±0.05  | ±0.1  | % FSR         |
|                                         | DAC70508 and DAC60508. Gain = 1 and Gain = 2                                                  |     | ±0.075 | ±0.14 |               |
|                                         | DAC70508 and DAC60508. Gain = ½                                                               |     | ±0.1   | ±0.22 |               |
| Gain error                              | DAC80508                                                                                      |     | ±0.05  | ±0.1  | % FSR         |
|                                         | DAC70508 and DAC60508                                                                         |     | ±0.05  | ±0.14 |               |
| Offset error drift                      |                                                                                               |     | ±1     |       | μV/°C         |
| Zero-code error drift                   |                                                                                               |     | ±2     |       | μV/°C         |
| Full-scale error drift                  |                                                                                               |     | ±2     |       | ppm of FSR/°C |
| Gain error drift                        |                                                                                               |     | ±1     |       | ppm of FSR/°C |
| Output voltage drift over time          | T <sub>A</sub> = 25°C, DAC code = midscale, 1600 hours                                        |     | 20     |       | ppm of FSR    |

- (1) Static performance specified with DAC outputs unloaded for all gain options, unless otherwise noted. End point fit between codes. 16-bit: Code 256 to 65280, 14-bit: Code 128 to 16127, 12-bit: Code 16 to 4031

## Electrical Characteristics (continued)

All minimum and maximum specifications at  $V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IO} = 1.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REFIN} = 1.25\text{ V}$  to  $5.5\text{ V}$ ,  $R_{LOAD} = 2\text{ k}\Omega$  to GND,  $C_{LOAD} = 200\text{ pF}$  to GND, digital inputs at  $V_{IO}$  or GND,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted).

| PARAMETER                              | TEST CONDITIONS                                                                                                                     | MIN   | TYP                          | MAX | UNIT   |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------|-----|--------|
| OUTPUT CHARACTERISTICS                 |                                                                                                                                     |       |                              |     |        |
| Voltage range                          | Gain = 2 (BUFF-GAIN = 1, REF-DIV = 0)                                                                                               | 0     | $2 \times V_{REF}$           |     | V      |
|                                        | Gain = 1 (BUFF-GAIN = 1, REF-DIV = 1)                                                                                               | 0     | $V_{REF}$                    |     |        |
|                                        | Gain = ½ (BUFF-GAIN = 0, REF-DIV = 1)                                                                                               | 0     | $\frac{1}{2} \times V_{REF}$ |     |        |
| Output voltage headroom                | to GND or $V_{DD}$ (unloaded)                                                                                                       | 0.004 |                              |     | V      |
|                                        | to GND or $V_{DD}$ ( $-5\text{ mA} \leq I_{OUT} \leq 5\text{ mA}$ )                                                                 | 0.15  |                              |     |        |
|                                        | to GND or $V_{DD}$ ( $-10\text{ mA} \leq I_{OUT} \leq 10\text{ mA}$ )                                                               | 0.3   |                              |     |        |
|                                        | to GND or $V_{DD}$ ( $-20\text{ mA} \leq I_{OUT} \leq 20\text{ mA}$ )                                                               | 0.5   |                              |     |        |
| Short circuit current <sup>(2)</sup>   | DAC code = full scale. Output shorted to GND                                                                                        | 30    |                              |     | mA     |
|                                        | DAC code = zero scale. Output shorted to $V_{DD}$                                                                                   | 35    |                              |     |        |
| Load regulation                        | DAC code = midscale, $-10\text{ mA} \leq I_{OUT} \leq 10\text{ mA}$                                                                 | 85    |                              |     | µV/mA  |
| Maximum capacitive load <sup>(3)</sup> | $R_{LOAD} = \infty$                                                                                                                 | 0     | 2                            |     | nF     |
|                                        | $R_{LOAD} = 2\text{ k}\Omega$                                                                                                       | 0     | 10                           |     |        |
| DC output impedance                    | DAC code = midscale                                                                                                                 | 0.085 |                              |     | Ω      |
|                                        | DAC output at GND or $V_{DD}$                                                                                                       | 15    |                              |     |        |
| DYNAMIC PERFORMANCE                    |                                                                                                                                     |       |                              |     |        |
| Output voltage settling time           | ¼ to ¾ scale and ¾ to ¼ scale settling time to ±2 LSB, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2              | 5     |                              |     | µs     |
| Slew rate                              | $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2                                                                     | 1.8   |                              |     | V/µs   |
| Power-up time                          | DACx-PWDWN 1 to 0 transition. DAC code = full scale. $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2 <sup>(4)</sup> | 12    |                              |     | µs     |
| Power-up glitch magnitude              | DAC code = zero scale. $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2. $C_{LOAD} = 50\text{ pF}$                   | 25    |                              |     | mV     |
| Output noise                           | 0.1 Hz to 10 Hz, DAC code = midscale, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2                               | 14    |                              |     | µVpp   |
| Output noise density                   | 1 kHz, DAC code = midscale, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2                                         | 78    |                              |     | nV/√Hz |
|                                        | 10 kHz, DAC code = midscale, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 2                                        | 74    |                              |     |        |
|                                        | 1 kHz, DAC code = full scale, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 1                                       | 55    |                              |     |        |
|                                        | 10 kHz, DAC code = full scale, $V_{DD} = 5.5\text{ V}$ , $V_{REFIN} = 2.5\text{ V}$ , Gain = 1                                      | 50    |                              |     |        |
| AC PSRR                                | DAC code = midscale, frequency = 60 Hz, amplitude = 200 mV <sub>PP</sub> superimposed on $V_{DD}$                                   | 85    |                              |     | dB     |
| DC PSRR                                | DAC code = midscale, $V_{DD} = 5\text{ V} \pm 10\%$                                                                                 | 10    |                              |     | µV/V   |
| Code change glitch impulse             | 1 LSB change around major carrier                                                                                                   | 4     |                              |     | nV-s   |
| Channel to Channel AC crosstalk        | DAC code = midscale. Code 32 to full-scale swing on adjacent channel                                                                | 0.2   |                              |     | nV-s   |
| Channel to Channel DC crosstalk        | DAC80508. Measured channel at midscale. Adjacent channel at full scale                                                              | 5     |                              |     | µV     |
|                                        | DAC70508 and DAC60508. Measured channel at midscale. Adjacent channel at full scale                                                 | 10    |                              |     |        |
|                                        | DAC80508. Measured channel at midscale. All other channels at full scale                                                            | 10    |                              |     |        |
|                                        | DAC70508 and DAC60508. Measured channel at midscale. All other channels at full scale                                               | 80    |                              |     |        |
| Digital feedthrough                    | DAC code = midscale. $f_{SCLK} = 1\text{ MHz}$ , SDO disabled                                                                       | 0.1   |                              |     | nV-s   |
| EXTERNAL REFERENCE INPUT               |                                                                                                                                     |       |                              |     |        |
| Reference input current                | $V_{REFIN} = 2.5\text{ V}$                                                                                                          | 25    |                              |     | µA     |
| Reference input impedance              |                                                                                                                                     | 100   |                              |     | kΩ     |
| Reference input capacitance            |                                                                                                                                     | 5     |                              |     | pF     |

- (2) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
- (3) Specified by design and characterization. Not tested during production.
- (4) Time to exit DAC power-down mode. Measured from CS rising edge to 90% of DAC final value.



## Electrical Characteristics (continued)

All minimum and maximum specifications at  $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{IO} = 1.7\text{ V to }5.5\text{ V}$ ,  $V_{REFIN} = 1.25\text{ V to }5.5\text{ V}$ ,  $R_{LOAD} = 2\text{ k}\Omega$  to GND,  $C_{LOAD} = 200\text{ pF to GND}$ , digital inputs at  $V_{IO}$  or GND,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted).

| PARAMETER                                     |                                | TEST CONDITIONS                                                                                         | MIN                   | TYP | MAX   | UNIT   |
|-----------------------------------------------|--------------------------------|---------------------------------------------------------------------------------------------------------|-----------------------|-----|-------|--------|
| INTERNAL REFERENCE                            |                                |                                                                                                         |                       |     |       |        |
| Reference output voltage, V <sub>REFOUT</sub> |                                | T <sub>A</sub> = 25°C                                                                                   | 2.495                 | 2.5 | 2.505 | V      |
| Reference output drift                        |                                | DAC80508                                                                                                |                       | 2   | 5     | ppm/°C |
|                                               |                                | DAC70508 and DAC60508                                                                                   |                       | 5   | 8     |        |
| Reference output impedance                    |                                |                                                                                                         |                       | 0.1 |       | Ω      |
| Reference output noise                        |                                | 0.1 Hz to 10 Hz                                                                                         |                       | 15  |       | μVpp   |
| Reference output noise density                |                                | 10 kHz, REF <sub>LOAD</sub> = 10 nF                                                                     |                       | 130 |       | nV/√Hz |
| Reference load current                        |                                |                                                                                                         |                       | ±5  |       | mA     |
| Reference load regulation                     |                                | Source and sink                                                                                         |                       | 100 |       | μV/mA  |
| Reference line regulation                     |                                |                                                                                                         |                       | 20  |       | μV/V   |
| Reference output drift over time              |                                | T <sub>A</sub> = 25°C, 1600 hours                                                                       |                       | 4.8 |       | ppm    |
| Reference thermal hysteresis                  |                                | DAC80508. First cycle                                                                                   |                       | 50  |       | ppm    |
|                                               |                                | DAC70508 and DAC60508. First cycle                                                                      |                       | 190 |       |        |
|                                               |                                | Additional cycle                                                                                        |                       | 18  |       |        |
| DIGITAL INPUTS                                |                                |                                                                                                         |                       |     |       |        |
| V <sub>IH</sub>                               | High-level input voltage       |                                                                                                         | 0.7 × V <sub>IO</sub> |     |       | V      |
| V <sub>IL</sub>                               | Low-level input voltage        |                                                                                                         | 0.3 × V <sub>IO</sub> |     |       | V      |
|                                               | Input current                  |                                                                                                         |                       | ±2  |       | μA     |
|                                               | Input pin capacitance          |                                                                                                         |                       | 2   |       | pF     |
| DIGITAL OUTPUTS: SDO/ALARM                    |                                |                                                                                                         |                       |     |       |        |
| V <sub>OH</sub>                               | High-level output voltage      | I <sub>LOAD</sub> = 0.2 mA                                                                              | V <sub>IO</sub> – 0.4 |     |       | V      |
| V <sub>OL</sub>                               | Low-level output voltage       | I <sub>LOAD</sub> = -0.2 mA                                                                             | 0.4                   |     |       | V      |
|                                               | Output pin capacitance         |                                                                                                         |                       | 4   |       | pF     |
| POWER SUPPLY REQUIREMENTS                     |                                |                                                                                                         |                       |     |       |        |
| I <sub>DD</sub>                               | V <sub>DD</sub> supply current | Active mode. Internal reference enabled. Gain = 1. DAC code = full scale. Outputs unloaded. SPI static  |                       | 5   | 6     | mA     |
|                                               |                                | Active mode. Internal reference disabled. Gain = 1. DAC code = full scale. Outputs unloaded. SPI static |                       | 4.5 | 5.5   |        |
|                                               |                                |                                                                                                         | Power-down            |     | 15    |        |
| I <sub>IO</sub>                               | V <sub>IO</sub> supply current |                                                                                                         |                       | 2   | 3     | μA     |

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.

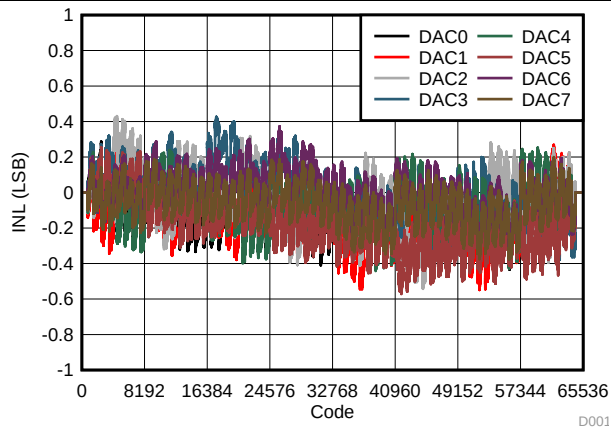


Figure 1. Integral Linearity Error vs Digital Input Code

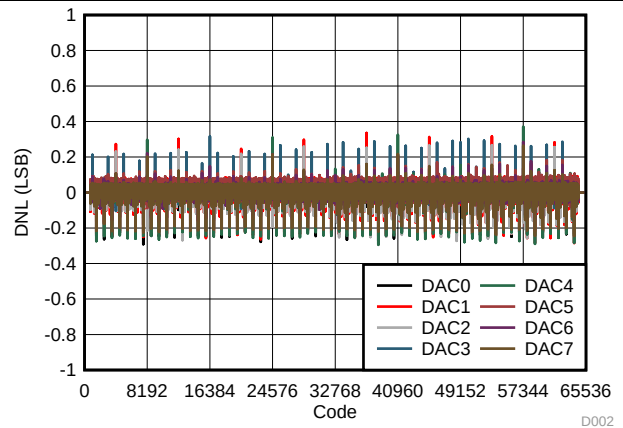


Figure 2. Differential Linearity Error vs Digital Input Code

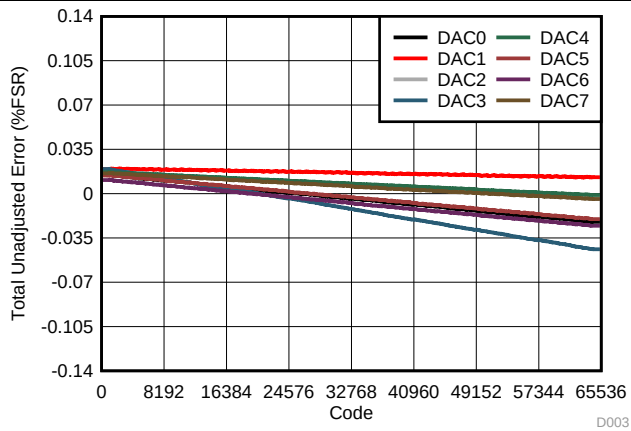


Figure 3. Total Unadjusted Error vs Digital Input Code

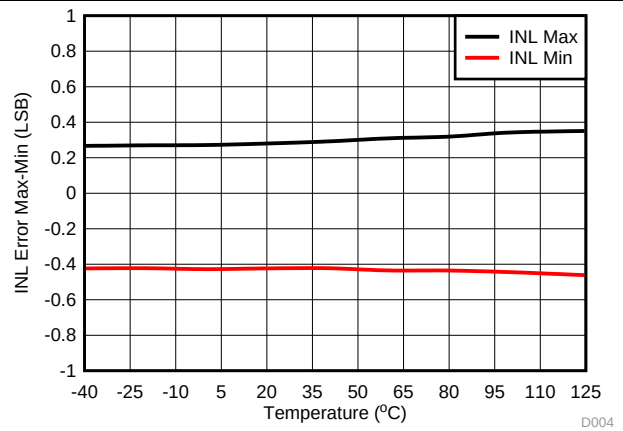


Figure 4. Integral Linearity Error vs Temperature

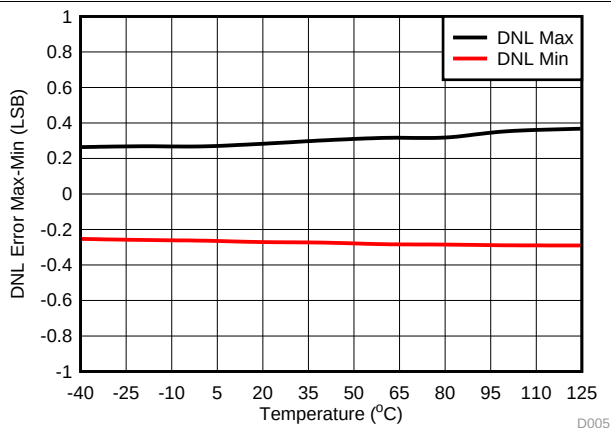


Figure 5. Differential Linearity Error vs Temperature

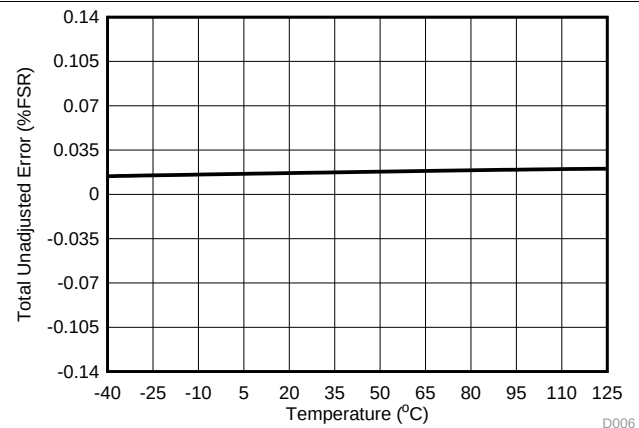
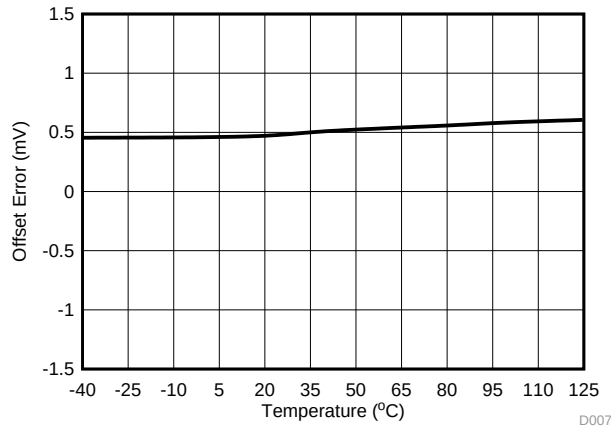


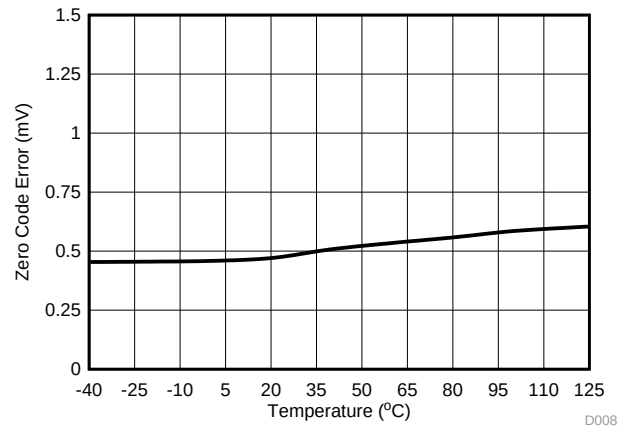
Figure 6. Total Unadjusted Error vs Temperature

## Typical Characteristics (continued)

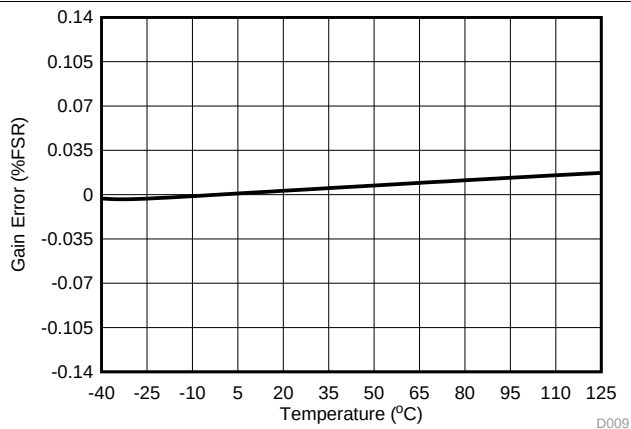
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.



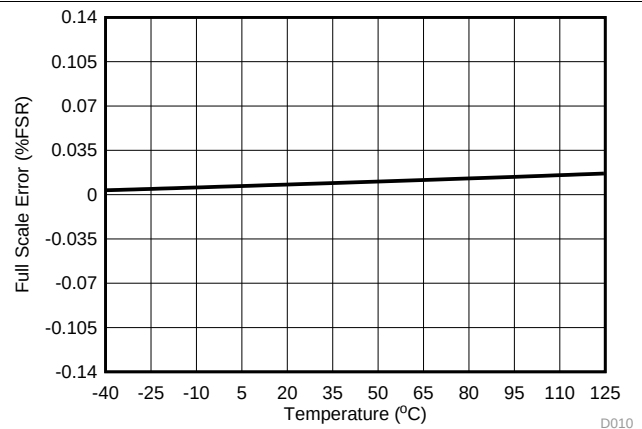
**Figure 7. Offset Error vs Temperature**



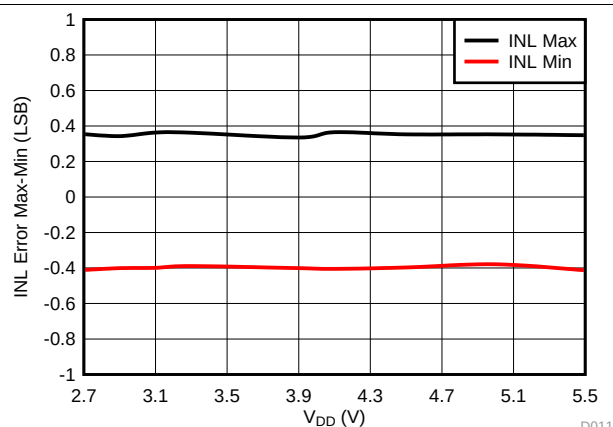
**Figure 8. Zero Code Error vs Temperature**



**Figure 9. Gain Error vs Temperature**

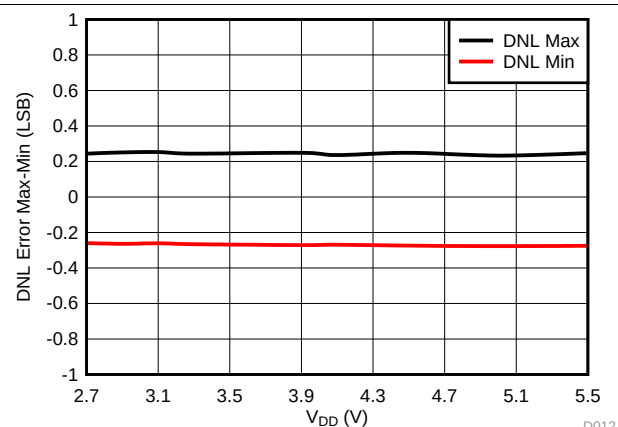


**Figure 10. Full Scale Error vs Temperature**



Gain = 1

**Figure 11. Integral Linearity Error vs Supply Voltage**



Gain = 1

**Figure 12. Differential Linearity Error vs Supply Voltage**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.

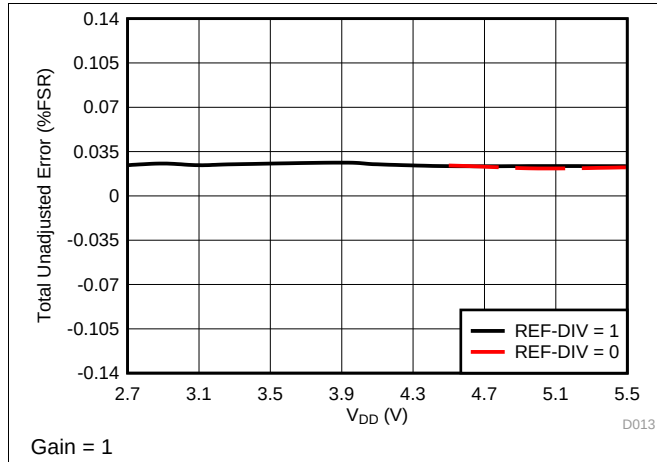


Figure 13. Total Unadjusted Error vs Supply Voltage

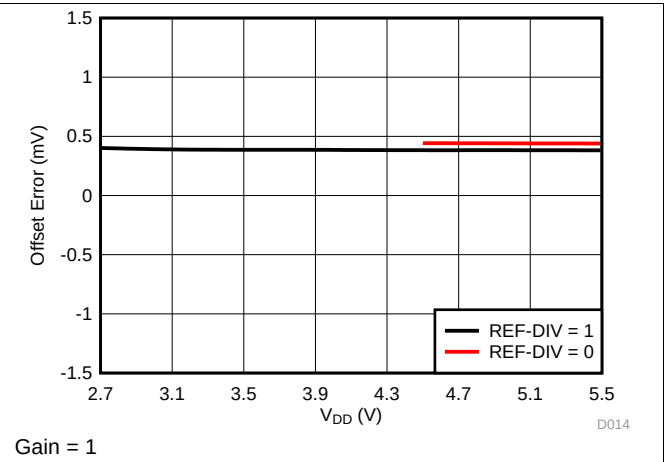


Figure 14. Offset Error vs Supply Voltage

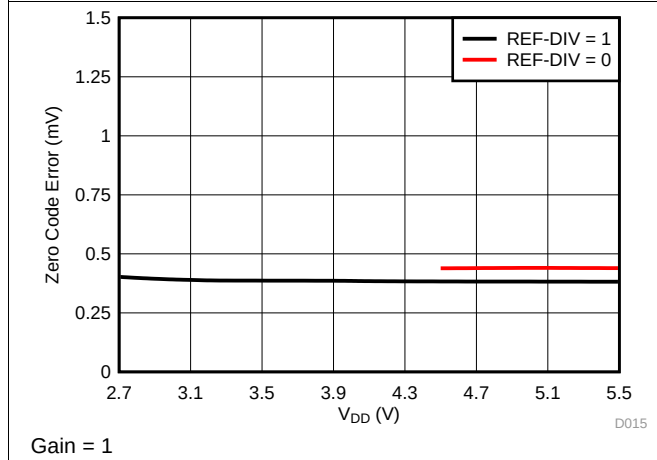


Figure 15. Zero Code Error vs Supply Voltage

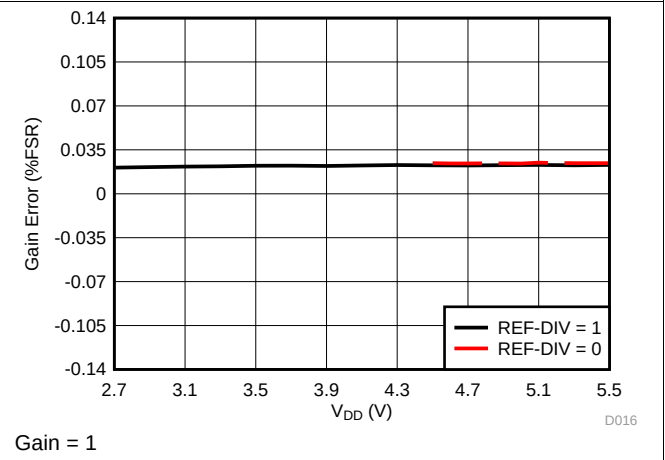


Figure 16. Gain Error vs Supply Voltage

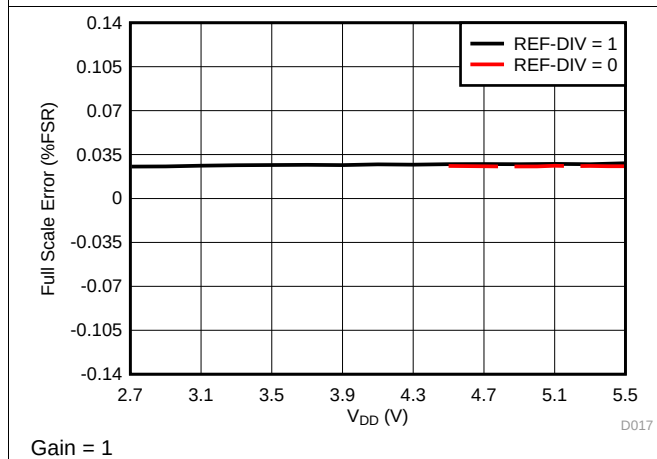


Figure 17. Full Scale Error vs Supply Voltage

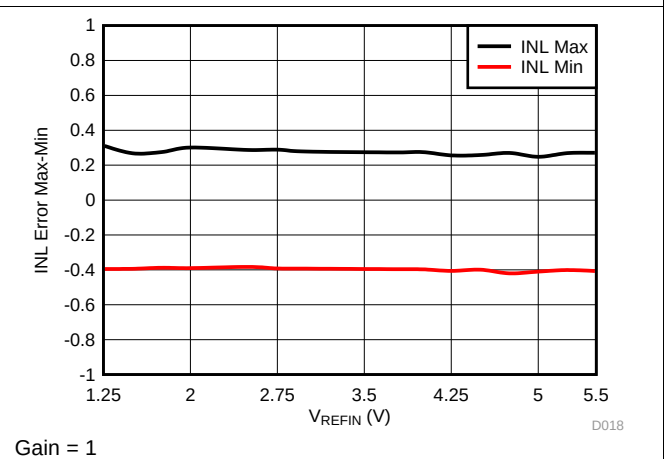
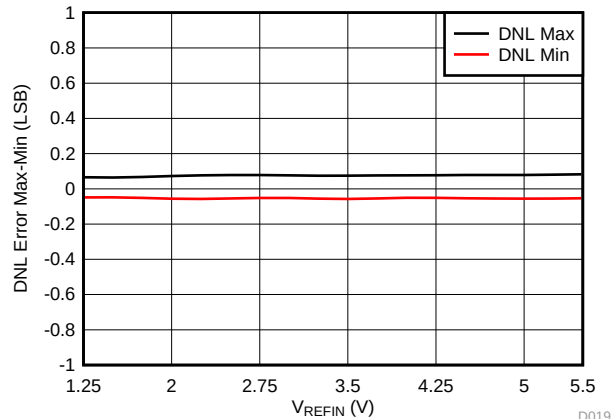


Figure 18. Integral Linearity Error vs Reference Voltage

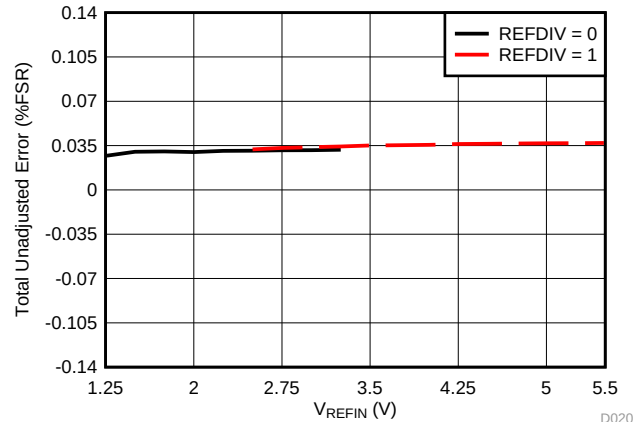
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.



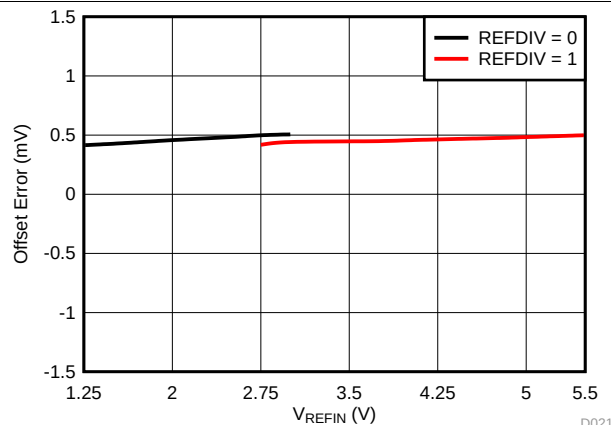
Gain = 1

**Figure 19. Differential Linearity Error vs Reference Voltage**



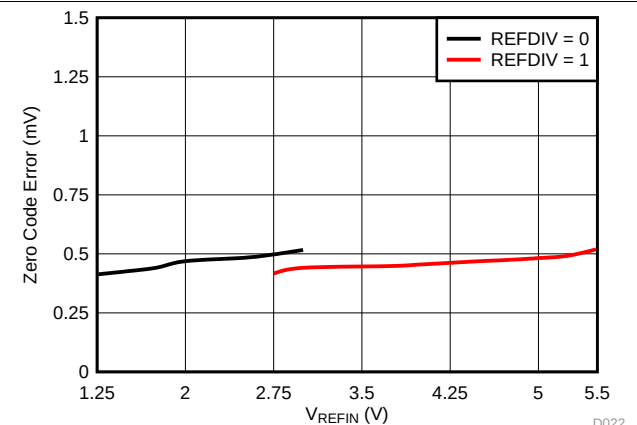
Gain = 1

**Figure 20. Total Unadjusted Error vs Reference Voltage**



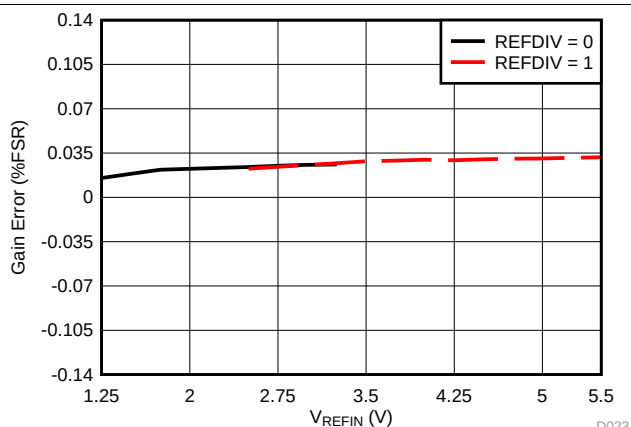
Gain = 1

**Figure 21. Offset Error vs Reference Voltage**



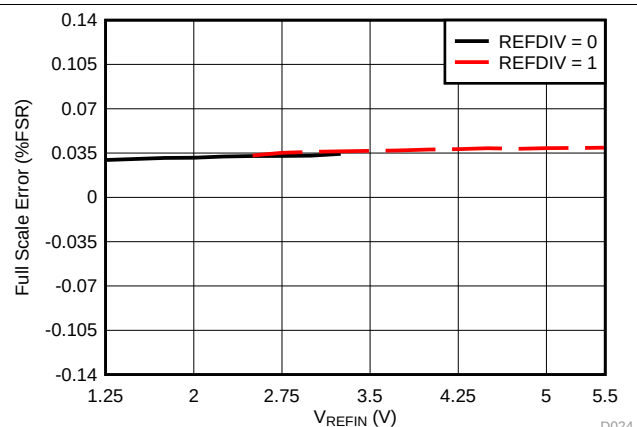
Gain = 1

**Figure 22. Zero Code Error vs Reference Voltage**



Gain = 1

**Figure 23. Gain Error vs Reference Voltage**

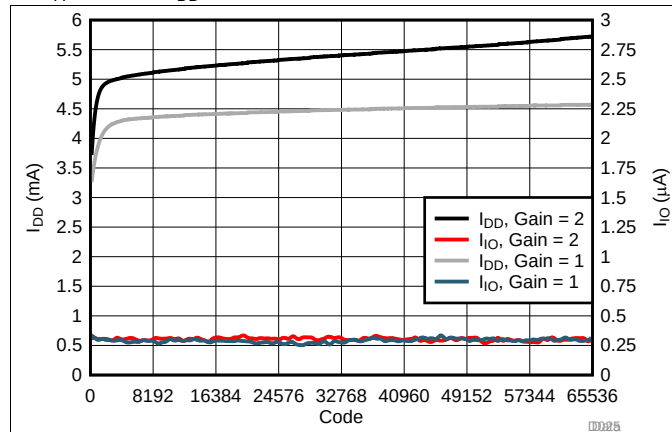


Gain = 1

**Figure 24. Full Scale Error vs Reference Voltage**

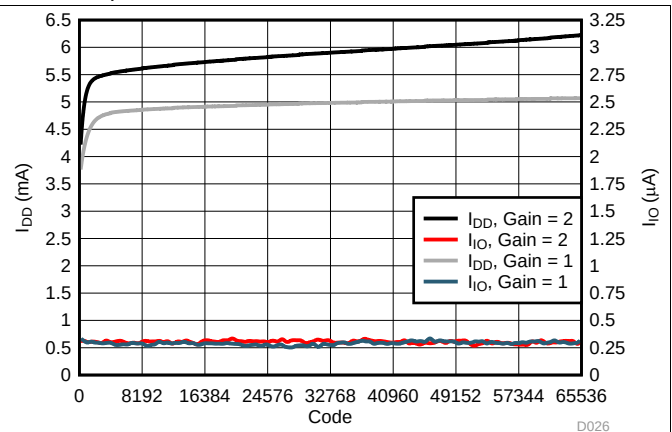
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.



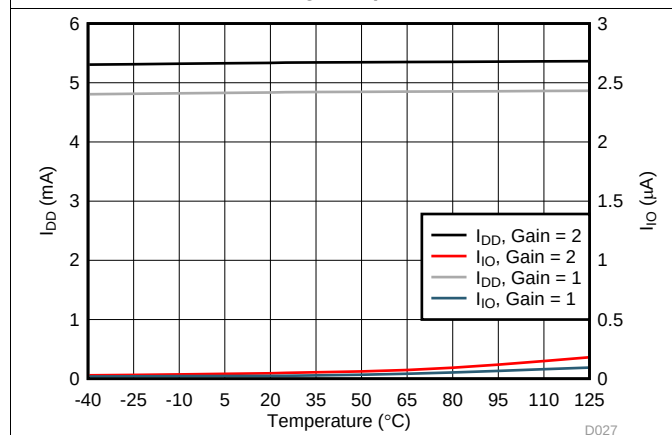
Gain = 1. External Reference =  $2.5\text{ V}$

Figure 25. Supply Current with External Reference vs Digital Input Code



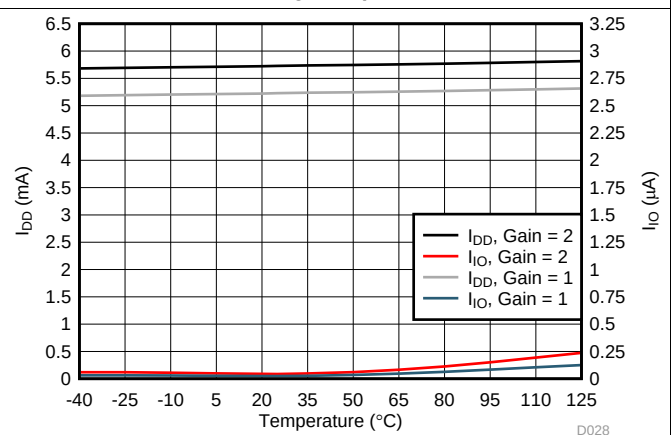
Gain = 1

Figure 26. Supply Current with Internal Reference vs Digital Input Code



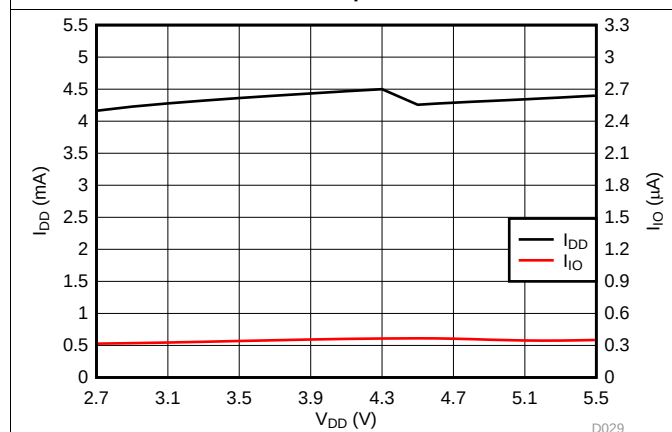
Gain = 1. External Reference =  $2.5\text{ V}$

Figure 27. Supply Current with External Reference vs Temperature



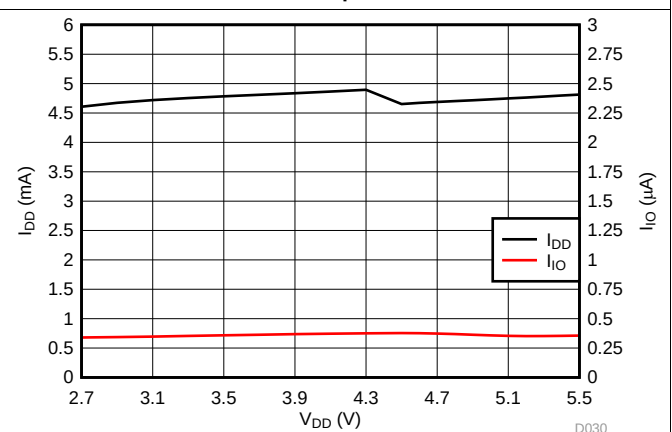
Gain = 1

Figure 28. Supply Current with Internal Reference vs Temperature



Gain = 1. External Reference =  $2.5\text{ V}$

Figure 29. Supply Current with External Reference vs Supply Voltage



Gain = 1

Figure 30. Supply Current with Internal Reference vs Supply Voltage

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.

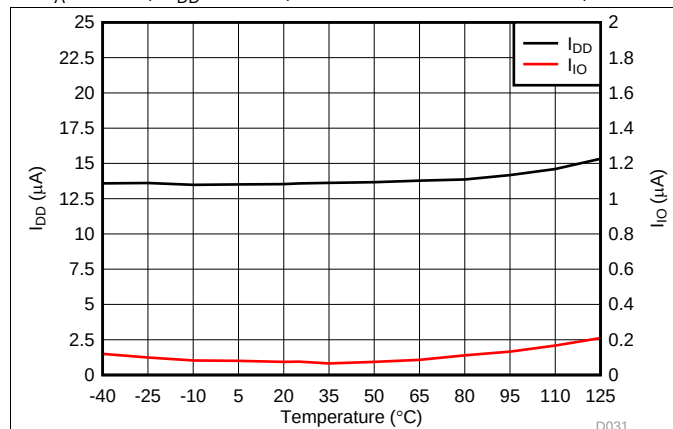


Figure 31. Power Down Current vs Temperature

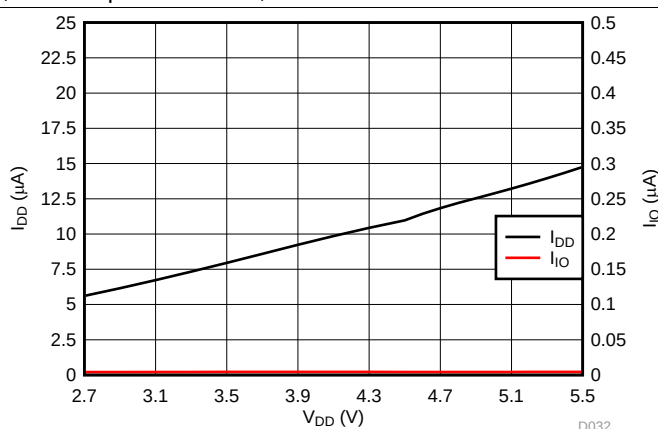


Figure 32. Power Down Current vs Supply Voltage

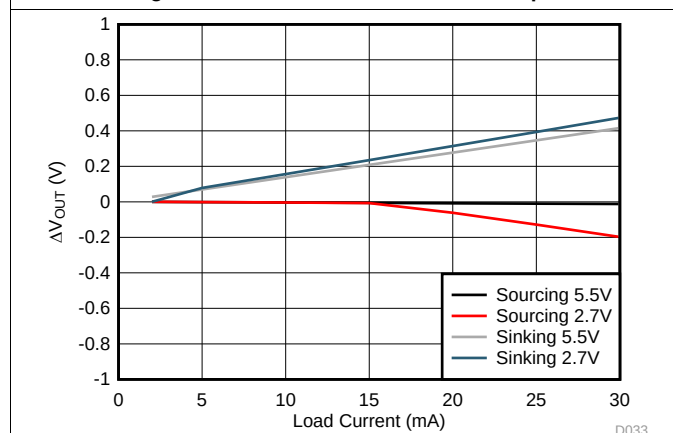


Figure 33. Headroom/Footroom vs Load Current

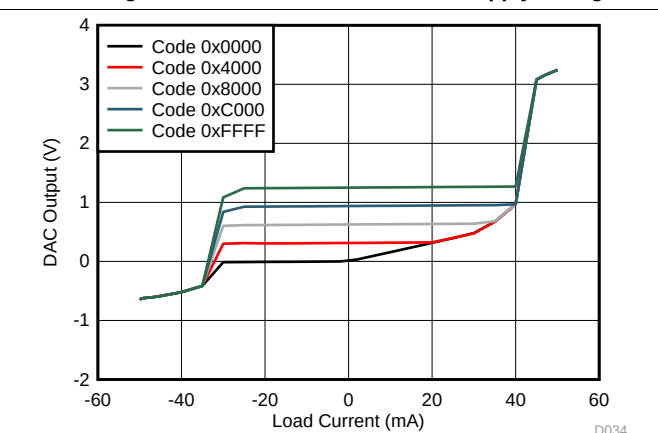


Figure 34. Source and Sink Capability with Gain =  $\frac{1}{2}$

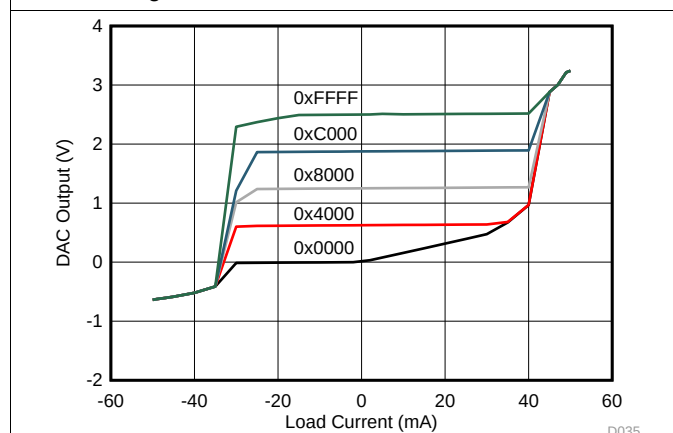


Figure 35. Source and Sink Capability with Gain = 1

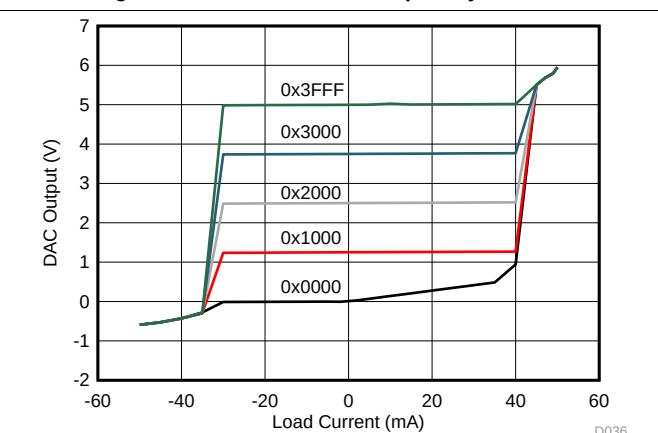
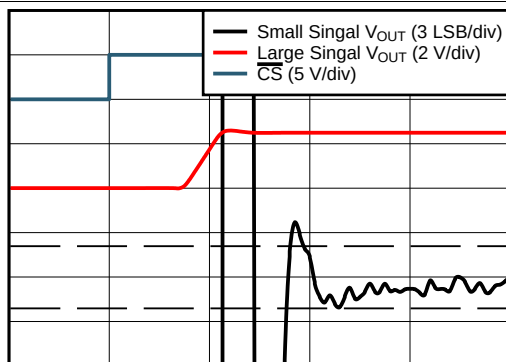


Figure 36. Source and Sink Capability with Gain = 2

## Typical Characteristics (continued)

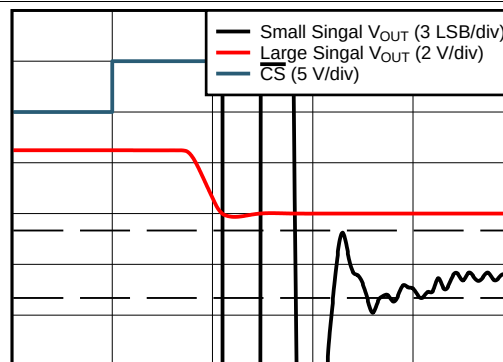
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.



Time (2 μsec/div)

D037

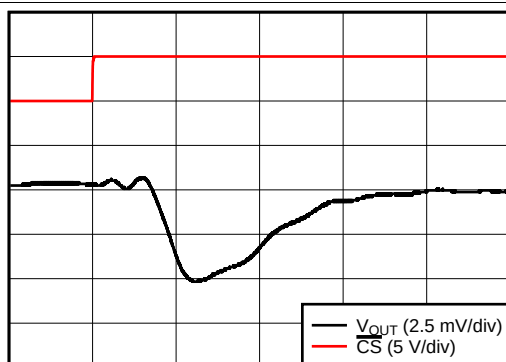
Gain = 1

**Figure 37. Full-Scale Settling Time, Rising Edge**


Time (2 μsec/div)

D038

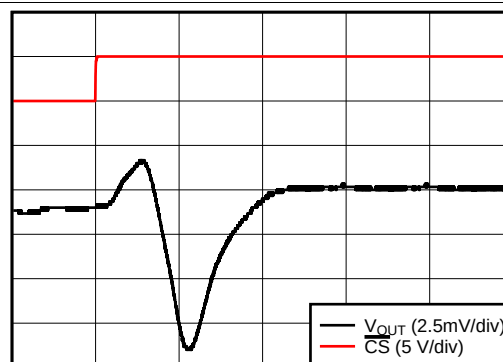
Gain = 1

**Figure 38. Full-Scale Settling Time, Falling Edge**


Time (0.5 μs/div)

D039

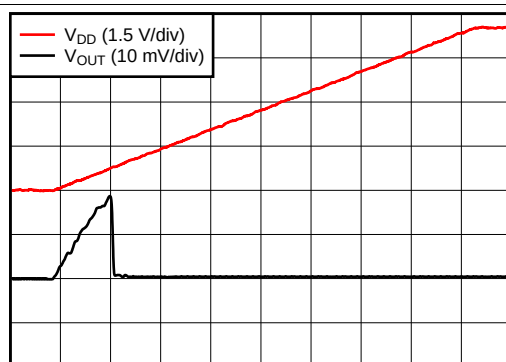
Gain = 1

**Figure 39. Glitch Impulse, Falling Edge, 1 LSB Step**


Time (0.5 μs/div)

D040

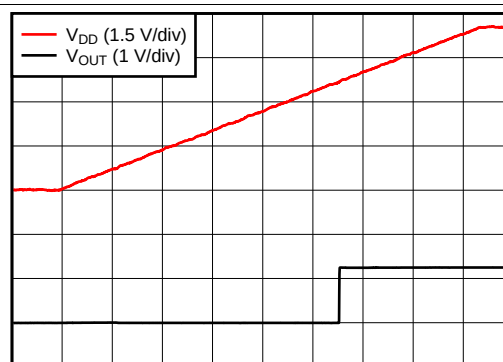
Gain = 1

**Figure 40. Glitch Impulse, Rising Edge, 1 LSB Step**


Time (600 μs/div)

D041

Gain = 1

**Figure 41. Power-On, Reset to Zero Scale**


Time (600 μs/div)

D042

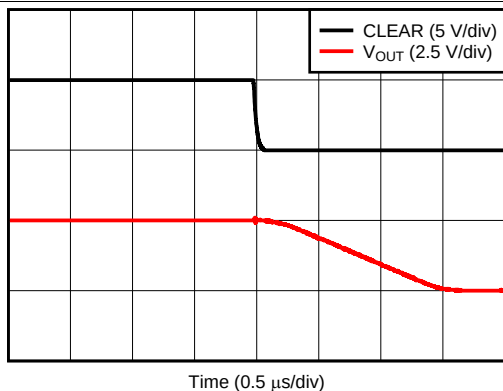
Gain = 1

**Figure 42. Power-On, Reset to Midscale**



## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference =  $2.5\text{ V}$ , Gain = 2, DAC outputs unloaded, unless otherwise noted.

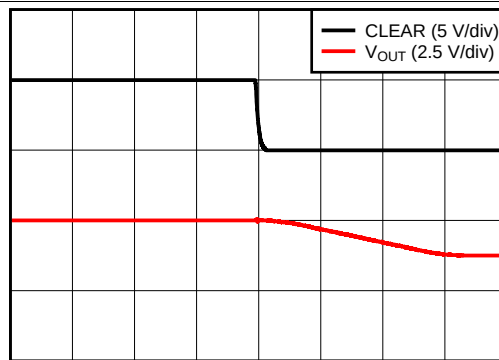


Time (0.5  $\mu\text{s}/\text{div}$ )

D059

Gain = 1

**Figure 43. DACx0508C, Clear to Zero Scale**

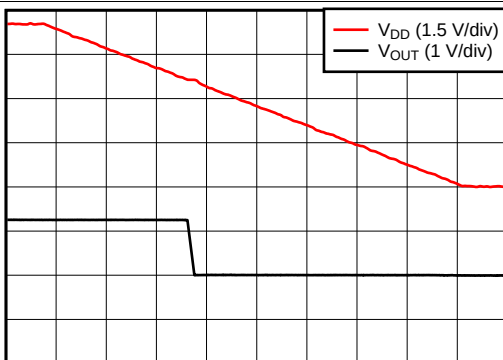


Time (0.5  $\mu\text{s}/\text{div}$ )

D060

Gain = 1

**Figure 44. DACx0508C, Clear to Midscale**

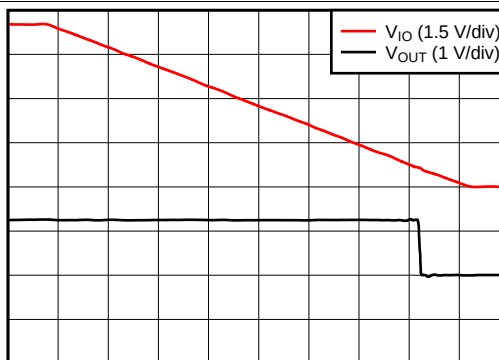


Time (600  $\mu\text{s}/\text{div}$ )

D044

Gain = 1. DAC code at midscale

**Figure 45.  $V_{DD}$  Power-Down**

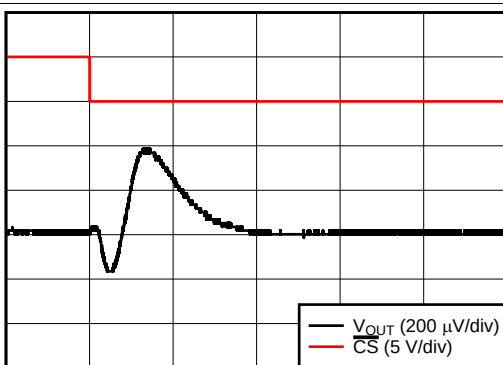


Time (600  $\mu\text{s}/\text{div}$ )

D060

Gain = 1. DAC code at midscale

**Figure 46.  $V_{IO}$  Power-Down**

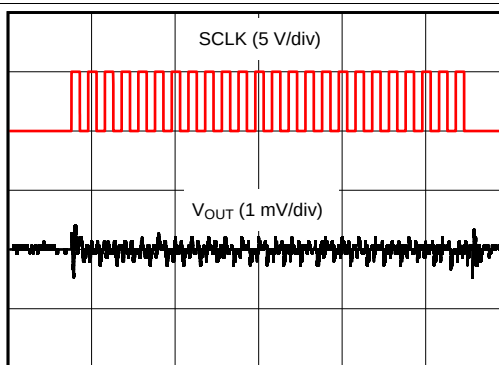


Time (2  $\mu\text{s}/\text{div}$ )

D045

Gain = 1. Measured DAC at midscale. All other DACs switch from code 32 to full scale

**Figure 47. Channel to Channel Crosstalk**



Time (5  $\mu\text{s}/\text{div}$ )

D046

Gain = 1. DAC code at midscale

**Figure 48. Clock Feedthrough with SCLK = 1 MHz**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.

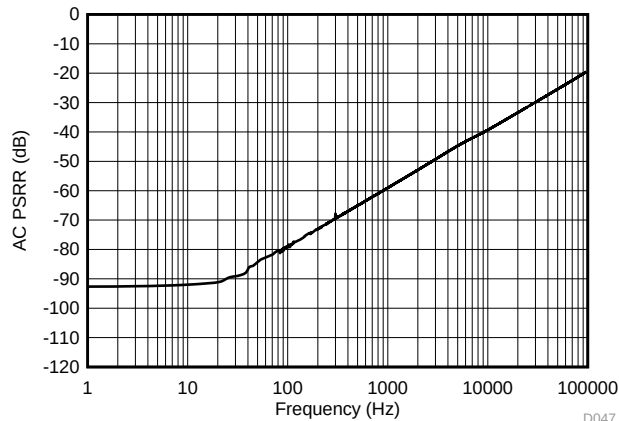


Figure 49. DAC Output AC PSRR vs Frequency

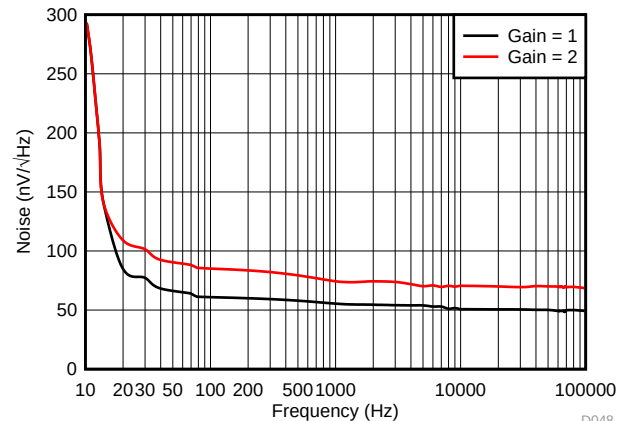


Figure 50. DAC Output Noise Density vs Frequency

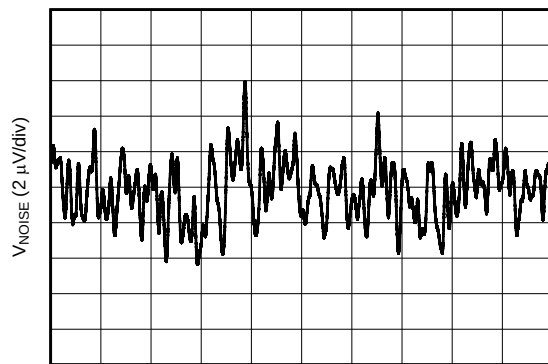


Figure 51. DAC Output Noise with External Reference  
0.1 Hz to 10 Hz

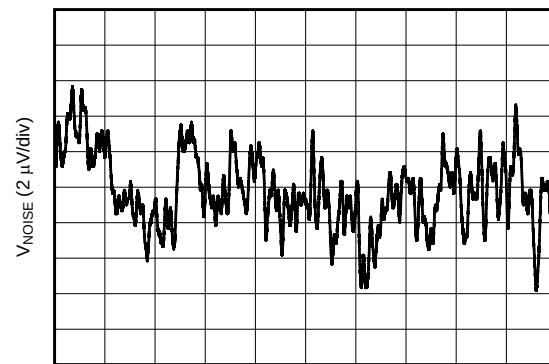


Figure 52. DAC Output Noise with Internal Reference  
0.1 Hz to 10 Hz

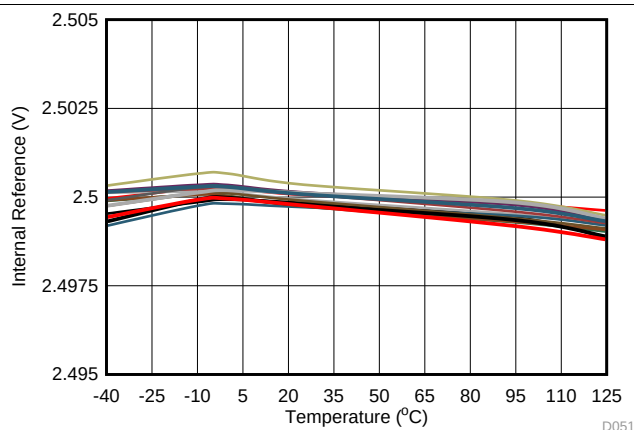


Figure 53. Internal Reference Voltage vs Temperature

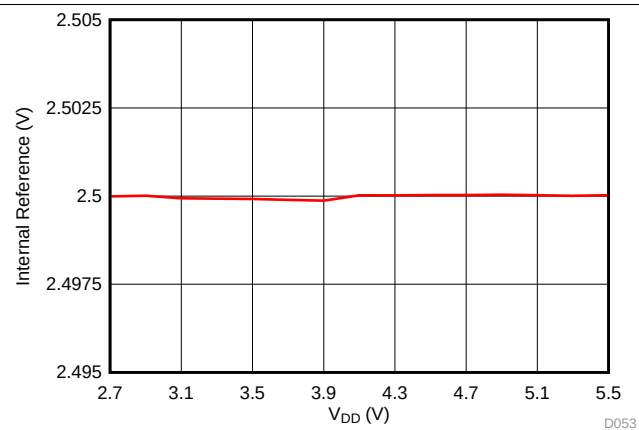
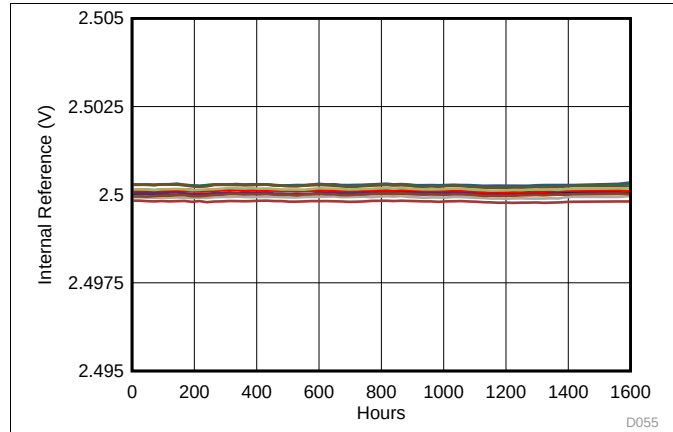


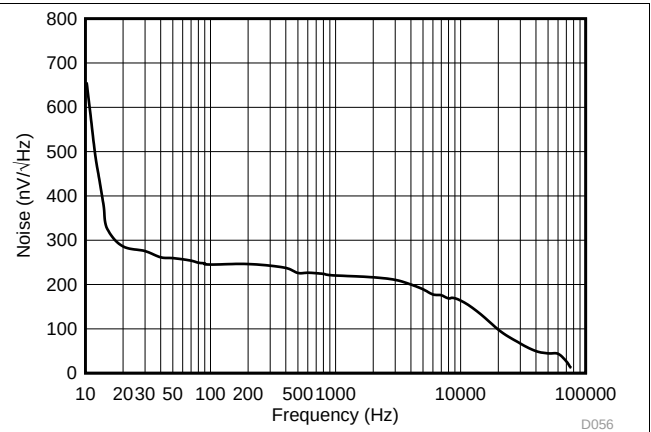
Figure 54. Internal Reference Voltage vs Supply Voltage

## Typical Characteristics (continued)

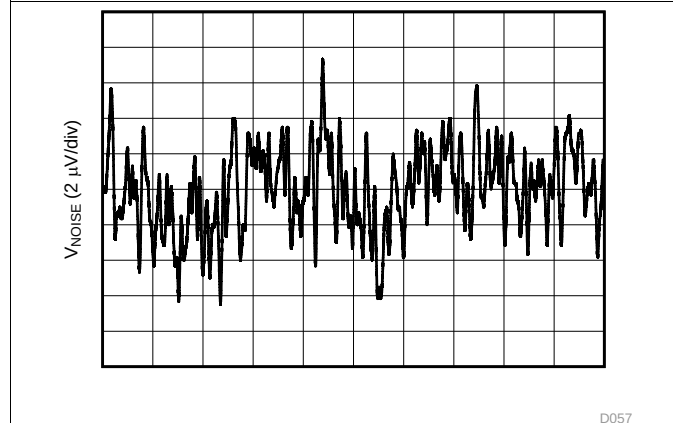
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.



**Figure 55. Internal Reference Voltage vs Time**

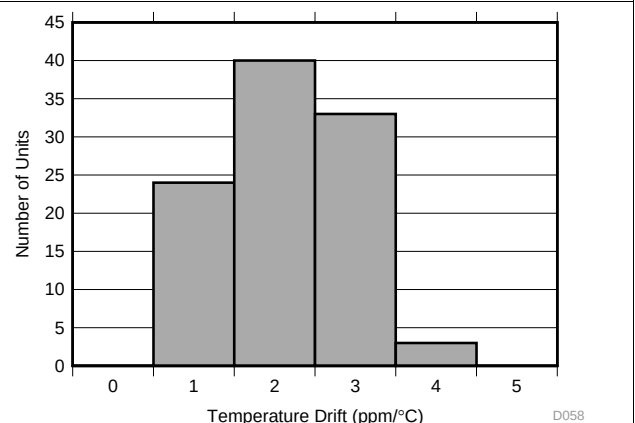


**Figure 56. Internal Reference Noise Density vs Frequency**



0.1 Hz to 10 Hz

**Figure 57. Internal Reference Noise**



**Figure 58. Internal Reference Temperature Drift Histogram**

## 8 Detailed Description

### 8.1 Overview

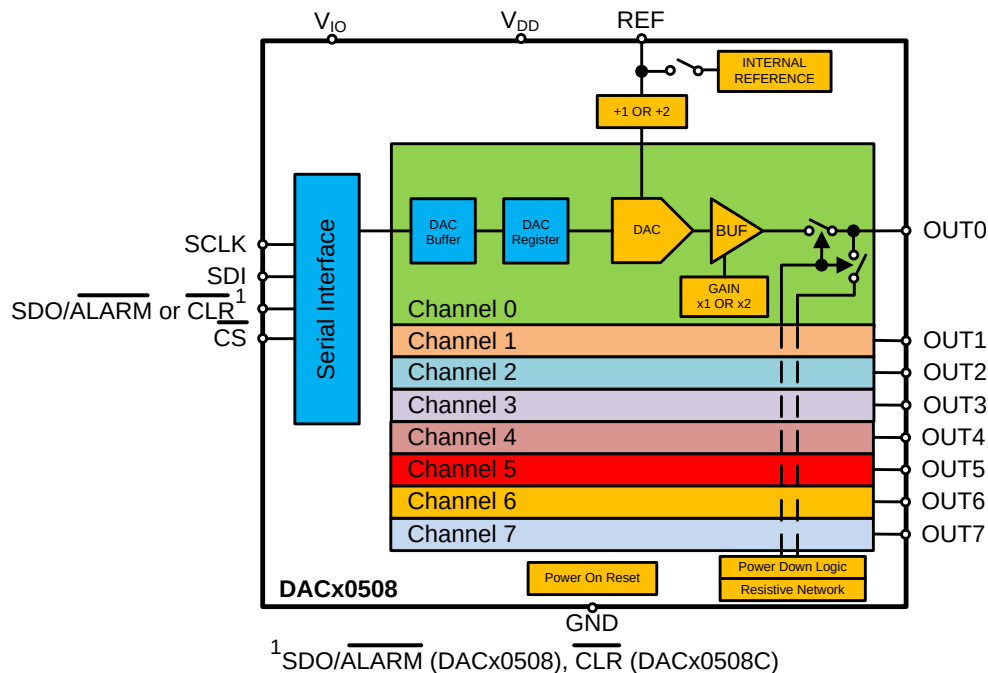
The DACx0508 is a pin-compatible family of low-power, eight-channel, buffered voltage-output digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx0508 includes a 2.5 V internal reference and user selectable gain configuration providing full scale output voltages of 1.25 V (gain =  $\frac{1}{2}$ ), 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7 V to 5.5 V supply, is specified monotonic, and provides high linearity of  $\pm 1$  LSB INL.

Communication to the DACx0508 is performed through a serial interface that supports stand-alone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx0508 serial interface.

The DACx0508 incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device.

A dedicated clear pin (DACx0508C) enables a simultaneous update of multiple DAC channels to their power-on-reset value.

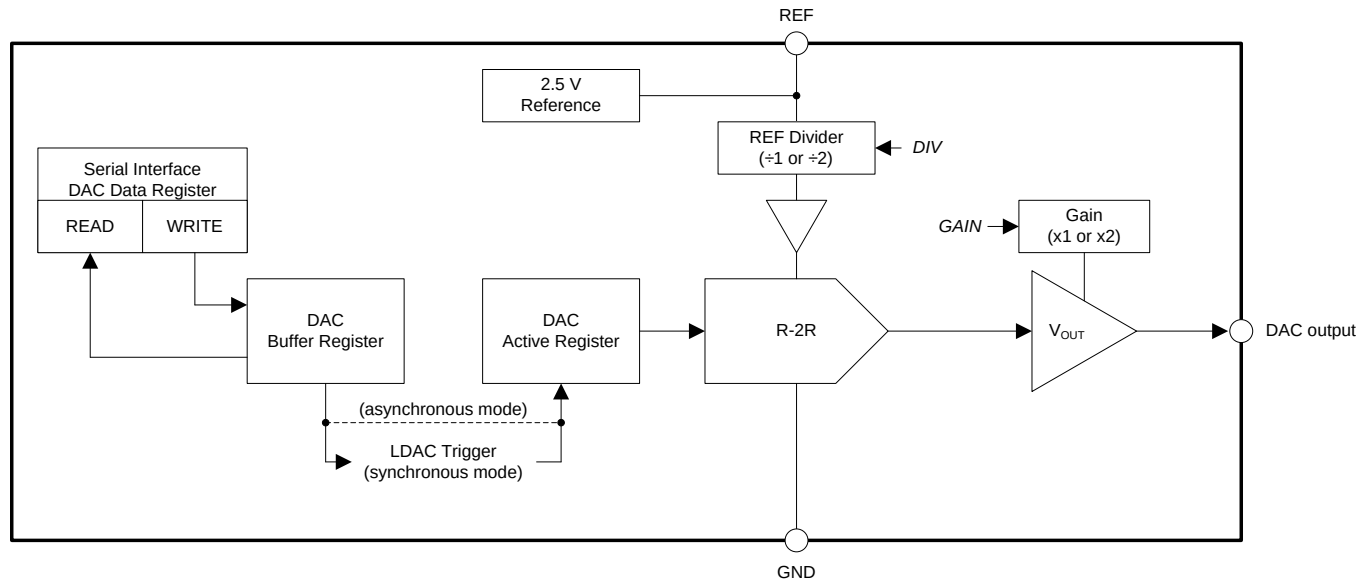
### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx0508 consists of an R-2R ladder architecture followed by an output buffer amplifier. Figure 59 shows a block diagram of the DAC architecture.



Copyright © 2016, Texas Instruments Incorporated

Figure 59. DACx0508 DAC Block Diagram

#### 8.3.1.1 DAC Transfer Function

The input data are written to the individual DAC Data registers in straight binary format. After a power-on or a reset event, all DAC registers are set to either zero code (DACx0508Z) or midscale code (DACx0508M). The DAC transfer function is given by Equation 1.

$$V_{OUT} = \frac{CODE}{2^n} \times \frac{V_{REF}}{DIV} \times GAIN \quad (1)$$

where:

CODE = decimal equivalent of the binary code that is loaded to the DAC register. CODE ranges from 0 to  $2^n - 1$ .

$V_{REF}$  = DAC reference voltage. Either  $V_{REFOUT}$  from the internal 2.5 V reference or  $V_{REFIN}$  if using an external one.

n = resolution in bits. Either 12 (DAC60508), 14 (DAC70508) or 16 (DAC80508).

DIV = 1 or 2 as set by the REF-DIV bit in the GAIN register. Set to 1 by default.

GAIN = 1 or 2 as set by the BUFF-GAIN bit for that DAC channel in the GAIN register. Set to 1 by default in DACx0508Z and to 2 in DACx0508M.

## Feature Description (continued)

### 8.3.1.2 Output Amplifiers

The DACx0508 output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0 V to  $V_{DD}$ . Each buffer amplifier is capable of driving a load of 2 k $\Omega$  in parallel with 10 nF to GND.

The full-scale output voltage for each channel is determined by the reference voltage ( $V_{REF}$ ), the reference divider setting (DIV), and the output buffer gain for that channel (GAIN), as shown in Table 1. During normal operation the DIV and GAIN settings can be reconfigured through the REF-DIV and BUFF-GAIN bit (See Equation 1). The GAIN setting for each output channel can be individually configured thus enabling independent output voltage ranges for each DAC output.

**Table 1. DAC Output Range Configuration**

| DIV Setting | GAIN Setting | DAC OUTPUT RANGE                    |
|-------------|--------------|-------------------------------------|
| $\div 2$    | $\times 1$   | 0 V to $\frac{1}{2} \times V_{REF}$ |
| $\div 1$    | $\times 1$   | Not recommended                     |
| $\div 2$    | $\times 2$   | 0 V to $V_{REF}$                    |
| $\div 1$    | $\times 2$   | 0 V to $2 \times V_{REF}$           |

### 8.3.1.3 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by an LDAC trigger (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to their new values. When the host reads from a DAC Data register, the value held in the DAC buffer register is returned (not the value held in the DAC active register).

#### 8.3.1.3.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of its corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on  $\overline{CS}$  rising edge. In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after an LDAC trigger event. An LDAC trigger is generated through the LDAC bit in the TRIGGER register. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 1  $\mu$ s is required between DAC output updates.

#### 8.3.1.3.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BROADCAST-EN bit in the SYNC register. A register write to the BROADCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their outputs. The DAC outputs update to the broadcast value on  $\overline{CS}$  rising edge independently of their synchronous mode configuration.

#### 8.3.1.3.3 CLEAR Operation (DACx0508C only)

The  $\overline{CLR}$  pin enables a simultaneous update of multiple DAC channels to the clear value: zero code (DACx0508ZC) or midscale code (DACx0508MC). DAC channels 0 through 3 and channels 4 through 7 can be independently configured to update or remain unaffected by the  $\overline{CLR}$  pin by setting the corresponding CLR-MSK bit. A  $\overline{CLR}$  pin logic low forces those DAC channels that have been configured for clear operation to clear the contents of their buffer and active registers to the clear value and sets the analog outputs accordingly, regardless of their synchronization setting. Those channels not configured for clear operation retain their buffer and active register contents as well as the corresponding analog outputs even if a clear command is issued. While the  $\overline{CLR}$  pin is kept low, register writes to the DAC data registers of those channels set for clear operation are ignored. A logic high on the  $\overline{CLR}$  pin causes the device to exit clear mode.

### 8.3.2 Internal Reference

The DACx0508 includes a 2.5 V precision bandgap reference enabled by default. Operation from an external reference is supported by disabling the internal reference in the CONFIG register. The internal reference is externally available at the REF pin.

A minimum 150 nF capacitor is recommended between the reference output and GND for noise filtering.

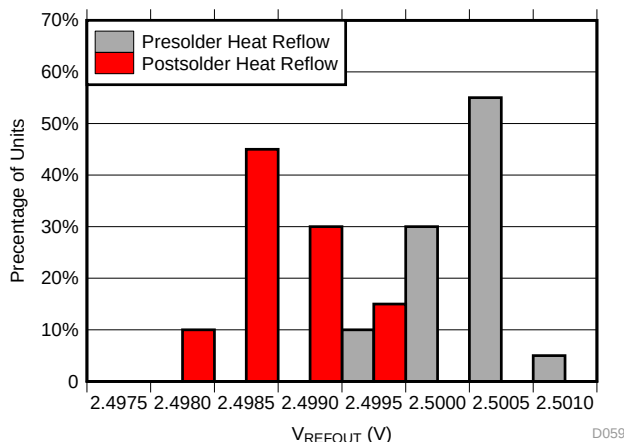
#### 8.3.2.1 Reference Divider

The reference voltage to the device, either from the internal reference or an external one can be divided by a factor of two by setting the REF-DIV bit in the GAIN register to 1 during normal operation. The reference voltage divider provides additional flexibility in setting the full-scale output voltage for each DAC output and must be configured so that there is sufficient headroom from  $V_{DD}$  to the DAC operating reference voltage ( $V_{REF}/DIV$ ). See the [Recommended Operating Conditions](#) table for more information.

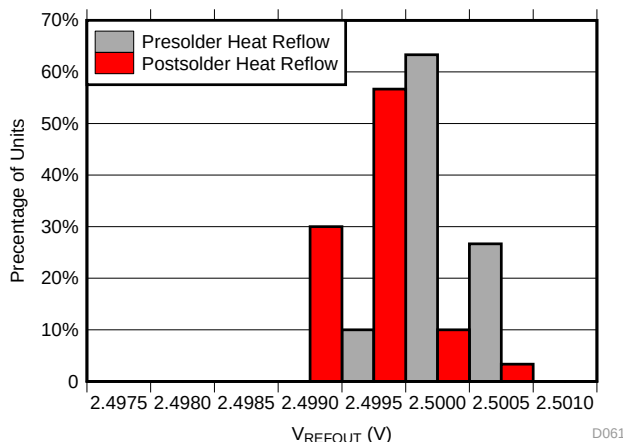
Improper configuration of the reference divider issues a reference alarm condition. In this case, the reference buffer is shut down, and all the DAC outputs go to 0 V. The DAC data registers are unaffected by the alarm condition thus enabling the DAC output to return to normal operation once the reference divider is configured correctly. The reference alarm status can be read from the REF-ALM bit in the STATUS register. Additionally by setting ALM-EN = 1 and ALM-SEL = 1 in the CONFIG register, the SDO/ALARM pin is configured as a reference alarm pin.

#### 8.3.2.2 Solder Heat Reflow

A known behavior of IC reference voltage circuits is the shift induced by the soldering process. [Figure 60](#) and [Figure 61](#) show the effect of solder heat reflow for the DACx0508 internal reference.



**Figure 60. DAC70508 and DAC60508 Solder Heat Reflow Reference Voltage Shift**



**Figure 61. DAC80508 Solder Heat Reflow Reference Voltage Shift**

### 8.3.3 Device Reset Options

#### 8.3.3.1 Power-on-Reset (POR)

The DACx0508 includes a power-on reset function that controls the output voltage at power up. After the  $V_{DD}$  and  $V_{IO}$  supplies have been established a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 250  $\mu$ s power-on-reset delay. The default value for all DACs in the DACx0508Z devices is zero-code and midscale-code for the DACx0508M ones. Each DAC channel remains at the power-up voltage until a valid command is written to it.

The POR circuit requires specific supply levels to discharge the internal capacitors and to reset the device on power up, as indicated in Figure 62 and Figure 63. In order to ensure a POR event,  $V_{DD}$  or  $V_{IO}$  must be below their corresponding low thresholds for at least 100  $\mu$ s. If  $V_{DD}$  and  $V_{IO}$  remain above their specified high threshold a POR event will not occur. When the supplies drop below their high threshold but remain over the lower one (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions.

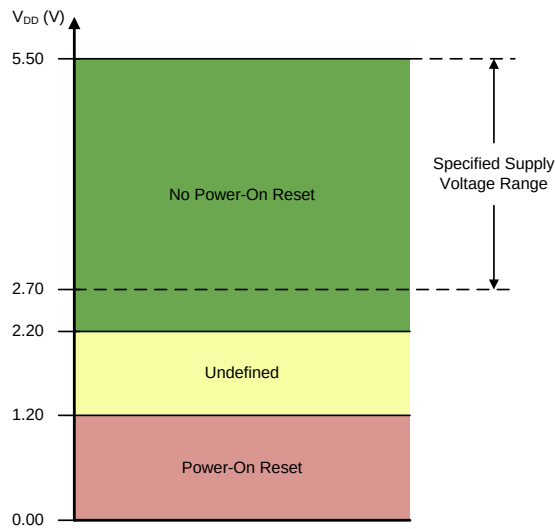


Figure 62. Threshold Levels for  $V_{DD}$  POR Circuit

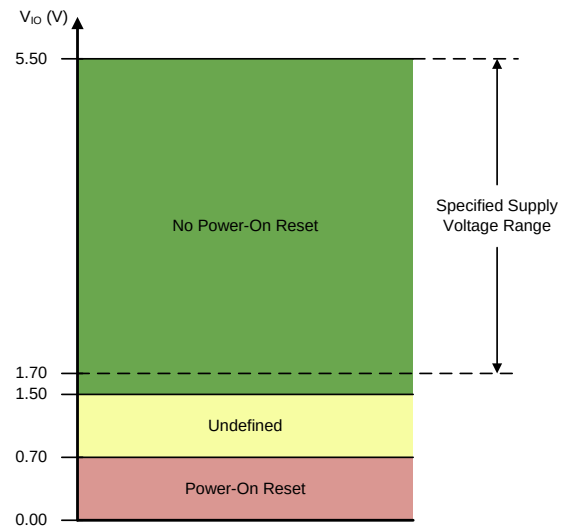


Figure 63. Threshold Levels for  $V_{IO}$  POR Circuit

#### 8.3.3.2 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the  $\overline{CS}$  rising edge of the instruction. A software reset initiates a POR event.



## 8.4 Device Functional Modes

### 8.4.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the  $\overline{CS}$  pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the  $\overline{CS}$  pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the  $\overline{CS}$  pin is de-asserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the last 24 or 32 bits are used by the device. When  $\overline{CS}$  is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

In an error checking disabled access cycle (24-bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 4-bit address to be accessed. The following bits in the cycle form the data cycle, as shown in [Table 2](#).

**Table 2. Serial Interface Access Cycle**

| BIT   | FIELD    | DESCRIPTION                                                                                                                                                                              |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | RW       | Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.                                        |
| 22:20 | Reserved | Reserved bits. Must be filled with zeros.                                                                                                                                                |
| 19:16 | A[3:0]   | Register address. Specifies the register to be accessed during the read or write operation.                                                                                              |
| 15:0  | DI[15:0] | Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[3:0]. If a read command, the data cycle bits are don't care values. |

A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data, as shown in [Table 3](#). Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit in the CONFIG register.

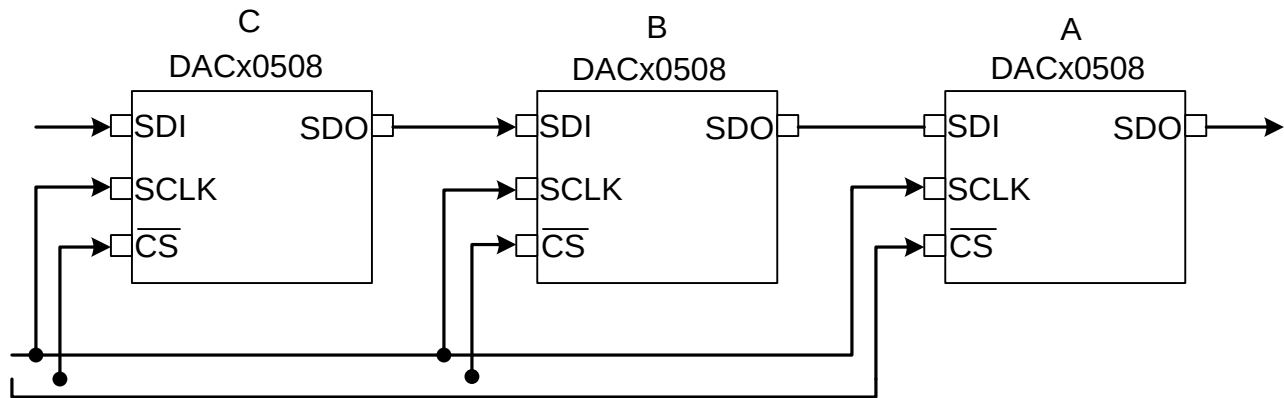
**Table 3. SDO Output Access Cycle**

| BIT   | FIELD    | DESCRIPTION                                             |
|-------|----------|---------------------------------------------------------|
| 23    | RW       | Echo RW from previous access cycle.                     |
| 22:20 | Reserved | Echo bits 22:20 from previous access cycle (all zeros). |
| 19:16 | A[3:0]   | Echo address from previous access cycle.                |
| 15:0  | DO[15:0] | Readback data requested on previous access cycle.       |

### 8.4.2 Daisy-Chain Operation

For systems that contain more than one DACx0508 devices, the SDO pin can be used to daisy-chain them together. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the  $\overline{CS}$  pin starts the operation cycle. If more than 24 SCLK pulses are applied while the  $\overline{CS}$  pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to  $24 \times N$ , where N is the total number of DACx0508 devices in the daisy chain. When the serial transfer to all devices is complete the  $\overline{CS}$  signal is taken high. This action transfers the data from the serial peripheral interface (SPI) shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register.



Copyright © 2017, Texas Instruments Incorporated

**Figure 64. Daisy-Chain Layout**

### 8.4.3 Frame Error Checking

If the DACx0508 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CRC-EN bit in the CONFIG register.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial  $x^8 + x^2 + x + 1$  (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data is appended with an 8-bit CRC polynomial by the host processor before feeding it to the device, as shown in Table 4. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

**Table 4. Error Checking Serial Interface Access Cycle**

| BIT   | FIELD     | DESCRIPTION                                                                                                                                                                              |
|-------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RW        | Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.                                        |
| 30    | CRC-ERROR | Reserved bit. Set to zero.                                                                                                                                                               |
| 29:28 | Reserved  | Reserved bits. Must be filled with zeros.                                                                                                                                                |
| 27:24 | A[3:0]    | Register address. Specifies the register to be accessed during the read or write operation.                                                                                              |
| 23:8  | DI[15:0]  | Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[3:0]. If a read command, the data cycle bits are don't care values. |
| 7:0   | CRC       | 8-bit CRC polynomial.                                                                                                                                                                    |

The DACx0508 decodes the 32-bit access cycle to compute the CRC remainder on  $\overline{CS}$  rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking result (CRC-ERROR bit) on the SDO pin, as shown in Table 5. Additionally, by setting ALM-EN = 1 and ALM-SEL = 0 in the CONFIG register, the SDO/ALARM pin is configured as a CRC alarm pin.

**Table 5. Write Operation Error Checking Cycle**

| BIT   | FIELD     | DESCRIPTION                                             |
|-------|-----------|---------------------------------------------------------|
| 31    | RW        | Echo RW from previous access cycle (RW = 0).            |
| 30    | CRC-ERROR | Returns a 1 when a CRC error is detected, 0 otherwise.  |
| 29:28 | Reserved  | Echo bits 29:28 from previous access cycle (all zeros). |
| 27:24 | A[3:0]    | Echo address from previous access cycle.                |
| 23:8  | DO[15:0]  | Echo data from previous access cycle.                   |
| 7:0   | CRC       | Calculated CRC value of bits 31:8.                      |

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin, as shown in [Table 6](#). As in the case of a write operation failing the CRC check, the SDO/ALARM pin if configured as a CRC alarm pin can be used to indicate a read command CRC failure.

**Table 6. Read Operation Error Checking Cycle**

| BIT   | FIELD     | DESCRIPTION                                             |
|-------|-----------|---------------------------------------------------------|
| 31    | RW        | Echo RW from previous access cycle (RW = 1).            |
| 30    | CRC-ERROR | Returns a 1 when a CRC error is detected, 0 otherwise.  |
| 29:28 | Reserved  | Echo bits 29:28 from previous access cycle (all zeros). |
| 27:24 | A[3:0]    | Echo address from previous access cycle.                |
| 23:8  | DO[15:0]  | Readback data requested on previous access cycle.       |
| 7:0   | CRC       | Calculated CRC value of bits 31:8.                      |

#### 8.4.4 Power-Down Mode

The DACx0508 DAC output amplifiers and internal reference can be independently powered down through the CONFIG register. At power-up all output channels and the device internal reference are active by default. A DAC output channel in power-down mode is connected internally to GND through a 1 kΩ resistor.

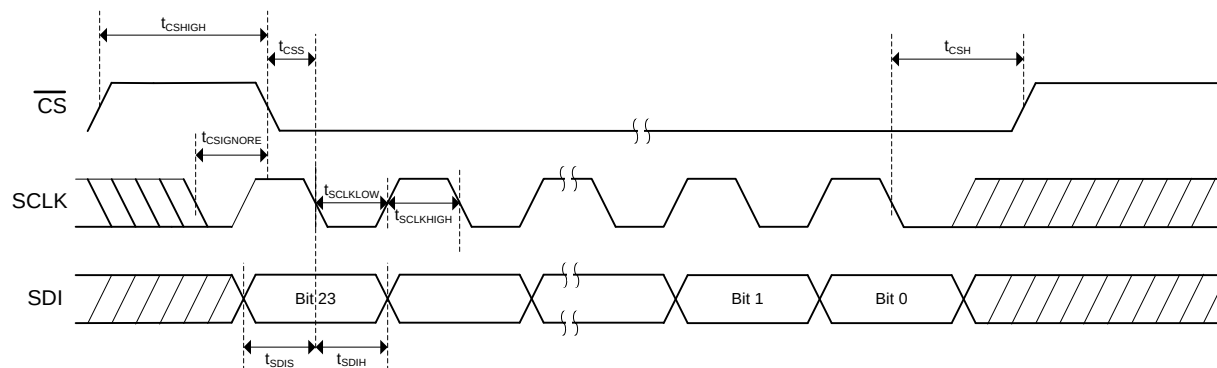
## 8.5 Programming

The DACx0508 is controlled through a flexible serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. [Table 7](#) shows the SPI timing requirements. [Figure 65](#) and [Figure 66](#) show the SPI write and read timing diagrams, respectively.

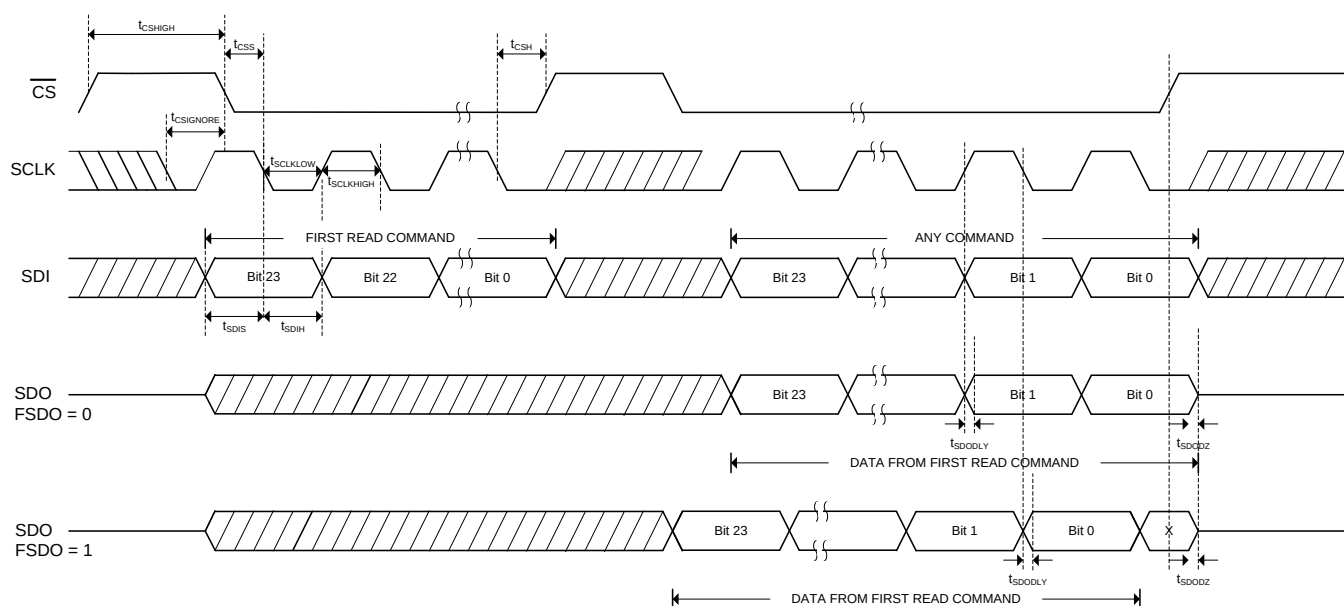
**Table 7. Programming Timing Requirements<sup>(1)</sup>**

|                                                             |                                                         | V <sub>IO</sub> = 1.7 V to 2.7 V  |     |     | V <sub>IO</sub> = 2.7 V to 5.5 V  |     |     | UNIT |
|-------------------------------------------------------------|---------------------------------------------------------|-----------------------------------|-----|-----|-----------------------------------|-----|-----|------|
|                                                             |                                                         | MIN                               | NOM | MAX | MIN                               | NOM | MAX |      |
| SERIAL INTERFACE – WRITE OPERATION                          |                                                         |                                   |     |     |                                   |     |     |      |
| f <sub>SCLK</sub>                                           | SCLK frequency                                          | 50                                |     |     | 50                                |     |     | MHz  |
| t <sub>SCLKHIGH</sub>                                       | SCLK high time                                          | 9                                 |     |     | 9                                 |     |     | ns   |
| t <sub>SCLKLOW</sub>                                        | SCLK low time                                           | 9                                 |     |     | 9                                 |     |     | ns   |
| t <sub>SDIS</sub>                                           | SDI setup                                               | 5                                 |     |     | 5                                 |     |     | ns   |
| t <sub>SDIH</sub>                                           | SDI hold                                                | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSS</sub>                                            | $\overline{\text{CS}}$ to SCLK falling edge setup       | 13                                |     |     | 13                                |     |     | ns   |
| t <sub>CSH</sub>                                            | SCLK falling edge to $\overline{\text{CS}}$ rising edge | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSHIGH</sub>                                         | $\overline{\text{CS}}$ high time                        | 15                                |     |     | 15                                |     |     | ns   |
| t <sub>CSIGNORE</sub>                                       | SCLK falling edge to $\overline{\text{CS}}$ ignore      | 7                                 |     |     | 7                                 |     |     | ns   |
| SERIAL INTERFACE – READ AND DAISY CHAIN OPERATION, FSDO = 0 |                                                         |                                   |     |     |                                   |     |     |      |
| f <sub>SCLK</sub>                                           | SCLK frequency                                          | 12                                |     |     | 18                                |     |     | MHz  |
| t <sub>SCLKHIGH</sub>                                       | SCLK high time                                          | 35                                |     |     | 25                                |     |     | ns   |
| t <sub>SCLKLOW</sub>                                        | SCLK low time                                           | 35                                |     |     | 25                                |     |     | ns   |
| t <sub>SDIS</sub>                                           | SDI setup                                               | 5                                 |     |     | 5                                 |     |     | ns   |
| t <sub>SDIH</sub>                                           | SDI hold                                                | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSS</sub>                                            | $\overline{\text{CS}}$ to SCLK falling edge setup       | 32                                |     |     | 20                                |     |     | ns   |
| t <sub>CSH</sub>                                            | SCLK falling edge to $\overline{\text{CS}}$ rising edge | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSHIGH</sub>                                         | $\overline{\text{CS}}$ high time                        | 15                                |     |     | 15                                |     |     | ns   |
| t <sub>SDODLY</sub>                                         | SDO output delay from SCLK rising edge                  | 3.5                      33.5     |     |     | 3.5                      23       |     |     | ns   |
| t <sub>SDODZ</sub>                                          | SDO driven to tri-state                                 | 0                              30 |     |     | 0                              25 |     |     | ns   |
| t <sub>CSIGNORE</sub>                                       | SCLK falling edge to $\overline{\text{CS}}$ ignore      | 7                                 |     |     | 7                                 |     |     | ns   |
| SERIAL INTERFACE – READ AND DAISY CHAIN OPERATION, FSDO = 1 |                                                         |                                   |     |     |                                   |     |     |      |
| f <sub>SCLK</sub>                                           | SCLK frequency                                          | 20                                |     |     | 25                                |     |     | MHz  |
| t <sub>SCLKHIGH</sub>                                       | SCLK high time                                          | 22                                |     |     | 18                                |     |     | ns   |
| t <sub>SCLKLOW</sub>                                        | SCLK low time                                           | 22                                |     |     | 18                                |     |     | ns   |
| t <sub>SDIS</sub>                                           | SDI setup                                               | 5                                 |     |     | 5                                 |     |     | ns   |
| t <sub>SDIH</sub>                                           | SDI hold                                                | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSS</sub>                                            | $\overline{\text{CS}}$ to SCLK falling edge setup       | 32                                |     |     | 20                                |     |     | ns   |
| t <sub>CSH</sub>                                            | SCLK falling edge to $\overline{\text{CS}}$ rising edge | 10                                |     |     | 10                                |     |     | ns   |
| t <sub>CSHIGH</sub>                                         | $\overline{\text{CS}}$ high time                        | 15                                |     |     | 15                                |     |     | ns   |
| t <sub>SDODLY</sub>                                         | SDO output delay from SCLK falling edge                 | 3.5                      45       |     |     | 3.5                      32       |     |     | ns   |
| t <sub>SDODZ</sub>                                          | SDO driven to tri-state                                 | 0                              30 |     |     | 0                              25 |     |     | ns   |
| t <sub>CSIGNORE</sub>                                       | SCLK falling edge to $\overline{\text{CS}}$ ignore      | 7                                 |     |     | 7                                 |     |     | ns   |
| DIGITAL LOGIC                                               |                                                         |                                   |     |     |                                   |     |     |      |
| t <sub>RSTDLYPOR</sub>                                      | POR reset delay                                         | 170              250              |     |     | 170              250              |     |     | μs   |
| t <sub>DACWAIT</sub>                                        | Sequential DAC output updates                           | 1                                 |     |     | 1                                 |     |     | μs   |
| t <sub>CLR</sub>                                            | $\overline{\text{CLR}}$ pulse                           | 20                                |     |     | 20                                |     |     | ns   |
| t <sub>CLRD</sub>                                           | $\overline{\text{CLR}}$ delay <sup>(2)</sup>            | 100                               |     |     | 100                               |     |     | ns   |

- (1) All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90% of  $V_{IO}$ ), timed from a voltage level of  $(V_{IL} + V_{IH})/2$ ,  $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$ ,  $V_{IO} = 1.7 \text{ V to } 5.5 \text{ V}$ ,  $V_{REFIN} = 1.25 \text{ V to } 5.5 \text{ V}$ , SDO loaded with 20 pF,  $T_A = -40^\circ\text{C to } +125^\circ\text{C}$
- (2) Specified from a logic-low on  $\overline{CLR}$  pin to when the DAC output starts to change. In the special case when the DAC output is at GND or  $V_{DD}$ , the  $\overline{CLR}$  delay may be as long as 1  $\mu$ s



**Figure 65. Serial Interface Write Timing Diagram**



**Figure 66. Serial Interface Read Timing Diagram**

## 8.6 Register Map

**Table 8. Register Map**

| REGISTER   | TYPE | RESET | ADDRESS BITS |    |    |    | DATA BITS          |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
|------------|------|-------|--------------|----|----|----|--------------------|---------|--------|--------|--------------------|--------------------|--------------|------------|----|----|----|-------|-----------------|----|-----------|----|
|            |      |       | A3           | A2 | A1 | A0 | D15                | D14     | D13    | D12    | D11                | D10                | D9           | D8         | D7 | D6 | D5 | D4    | D3              | D2 | D1        | D0 |
| NOP        | W    | 0000  | 0            | 0  | 0  | 0  | NOP                |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DEVICE ID  | R    | —     | 0            | 0  | 0  | 1  | DEVICEID           |         |        |        |                    |                    |              |            |    |    |    |       |                 |    | VERSIONID |    |
| SYNC       | R/W  | FF00  | 0            | 0  | 1  | 0  | DACx-BRDCAST-EN    |         |        |        |                    |                    | DACx-SYNC-EN |            |    |    |    |       |                 |    |           |    |
| CONFIG     | R/W  | 0000  | 0            | 0  | 1  | 1  | RESERVED           | ALM SEL | ALM EN | CRC EN | F SDO              | D SDO              | REF PW DWN   | DACx-PWDWN |    |    |    |       |                 |    |           |    |
| GAIN       | R/W  | 0000  | 0            | 1  | 0  | 0  | RESERVED           |         |        |        | CLR-4TO 7 -MSK (1) | CLR-0TO 3 -MSK (1) | REF DIV-EN   | BUFFx-GAIN |    |    |    |       |                 |    |           |    |
| TRIGGER    | W    | 0000  | 0            | 1  | 0  | 1  | RESERVED           |         |        |        |                    |                    |              |            |    |    |    | L DAC | SOFT-RESET[3:0] |    |           |    |
| BRDCAST    | R/W  | 0000  | 0            | 1  | 1  | 0  | BRDCAST-DATA[15:0] |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| STATUS     | R/W  | 0000  | 0            | 1  | 1  | 1  | RESERVED           |         |        |        |                    |                    |              |            |    |    |    |       |                 |    | REF ALM   |    |
| DAC0       | R/W  | 0000  | 1            | 0  | 0  | 0  | DAC0-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC1       | R/W  | 0000  | 1            | 0  | 0  | 1  | DAC1-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC2       | R/W  | 0000  | 1            | 0  | 1  | 0  | DAC2-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC3       | R/W  | 0000  | 1            | 0  | 1  | 1  | DAC3-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC4       | R/W  | 0000  | 1            | 1  | 0  | 0  | DAC4-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC5       | R/W  | 0000  | 1            | 1  | 0  | 1  | DAC5-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC6       | R/W  | 0000  | 1            | 1  | 1  | 0  | DAC6-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| DAC7       | R/W  | 0000  | 1            | 1  | 1  | 1  | DAC7-DATA[15:0]    |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |
| All Others | —    | —     | —            | —  | —  | —  | RESERVED           |         |        |        |                    |                    |              |            |    |    |    |       |                 |    |           |    |

(1) DACx0508C only. Reserved bits in DACx0508.

### 8.6.1 NOP Register (address = 0x00) [reset = 0x0000]

**Figure 67. NOP Register**

|     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NOP |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9. NOP Register Field Descriptions**

| Bit  | Field | Type | Reset  | Description                                               |
|------|-------|------|--------|-----------------------------------------------------------|
| 15:0 | NOP   | W    | 0x0000 | No operation. Write 0000h for proper no-operation command |

### 8.6.2 DEVICE ID Register (address = 0x01) [reset = 0x---]

**Figure 68. DEVICE ID Register**

|          |    |    |    |    |    |   |   |   |   |   |   |   |   |           |   |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|-----------|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0 |
| DEVICEID |    |    |    |    |    |   |   |   |   |   |   |   |   | VERSIONID |   |
| R        |    |    |    |    |    |   |   |   |   |   |   |   |   | R         |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. DEVICE ID Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | DEVICEID  | R    | ----  | Device ID:<br>D15 Reserved - 0<br>D14:12 Resolution - 000 (16-bit); 001 (14-bit); 010 (12-bit)<br>D11:8 Channels - 1000 (8 channels)<br>D7 Reset - 0 (DACx0508Z: reset to zero); 1 (DACx0508M: reset-to-midscale)<br>D6:2 Reserved - 00101 |
| 1:0  | VERSIONID | R    | 10    | Version ID. Subject to change                                                                                                                                                                                                              |

### 8.6.3 SYNC Register (address = 0x2) [reset = 0xFF00]

**Figure 69. SYNC Register**

| 15              | 14              | 13              | 12              | 11              | 10              | 9               | 8               |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| DAC7-BRDCAST-EN | DAC6-BRDCAST-EN | DAC5-BRDCAST-EN | DAC4-BRDCAST-EN | DAC3-BRDCAST-EN | DAC2-BRDCAST-EN | DAC1-BRDCAST-EN | DAC0-BRDCAST-EN |
| R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             |
| 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| DAC7-SYNC-EN    | DAC6-SYNC-EN    | DAC5-SYNC-EN    | DAC4-SYNC-EN    | DAC3-SYNC-EN    | DAC2-SYNC-EN    | DAC1-SYNC-EN    | DAC0-SYNC-EN    |
| R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. SYNC Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                       |
|-----|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | DAC7-BRDCAST-EN | R/W  | 1     | When set to 1 the corresponding DAC is set to update its output after a serial interface write to the BRDCAST register. When cleared to 0 the corresponding DAC output remains unaffected after a serial interface write to the BRDCAST register. |
| 14  | DAC6-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 13  | DAC5-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 12  | DAC4-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 11  | DAC3-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 10  | DAC2-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 9   | DAC1-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 8   | DAC0-BRDCAST-EN | R/W  | 1     |                                                                                                                                                                                                                                                   |
| 7   | DAC7-SYNC-EN    | R/W  | 0     | When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0 the corresponding DAC output is set to update immediately on a CS rising edge (asynchronous mode).               |
| 6   | DAC6-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 5   | DAC5-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 4   | DAC4-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 3   | DAC3-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 2   | DAC2-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 1   | DAC1-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |
| 0   | DAC0-SYNC-EN    | R/W  | 0     |                                                                                                                                                                                                                                                   |



### 8.6.4 CONFIG Register (address = 0x3) [reset = 0x0000]

**Figure 70. CONFIG Register**

| 15         | 14         | 13         | 12         | 11         | 10         | 9          | 8          |
|------------|------------|------------|------------|------------|------------|------------|------------|
| Reserved   |            | ALM-SEL    | ALM-EN     | CRC-EN     | FSDO       | DSDO       | REF-PWDWN  |
| —          |            | R/W        | R/W        | R/W        | R/W        | R/W        | R/W        |
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| DAC7-PWDWN | DAC6-PWDWN | DAC5-PWDWN | DAC4-PWDWN | DAC3-PWDWN | DAC2-PWDWN | DAC1-PWDWN | DAC0-PWDWN |
| R/W        | R/W        | R/W        | R/W        | R/W        | R/W        | R/W        | R/W        |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. CONFIG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | Reserved   | —    | 00    | Reserved for factory use                                                                                                                                                                                                                                                                                                  |
| 13    | ALM-SEL    | R/W  | 0     | ALARM select.<br>0: $\overline{\text{ALARM}}$ pin is CRC-ERROR<br>1: $\overline{\text{ALARM}}$ pin is REF-ALARM                                                                                                                                                                                                           |
| 12    | ALM-EN     | R/W  | 0     | Configure SDO/ $\overline{\text{ALARM}}$ pin. When 1: SDO/ $\overline{\text{ALARM}}$ pin is an active-low, open-drain, alarm pin. An external 10 k $\Omega$ pullup resistor to $V_{IO}$ is required. FSDO and DSDO bits are ignored. When 0: SDO/ $\overline{\text{ALARM}}$ pin is a serial interface, push-pull, SDO pin |
| 11    | CRC-EN     | R/W  | 0     | CRC enable bit. Set to 1 to enable CRC. Set to 0 to disable                                                                                                                                                                                                                                                               |
| 10    | FSDO       | R/W  | 0     | Fast SDO bit (half-cycle speedup). When 0, SDO updates on an SCLK rising edge. When 1, SDO updates a half-cycle earlier, during an SCLK falling edge.                                                                                                                                                                     |
| 9     | DSDO       | R/W  | 0     | Disable SDO bit. When 1, SDO is always tri-stated. When 0, SDO is driven while $\overline{\text{CS}}$ is low, and tri-stated while $\overline{\text{CS}}$ is high                                                                                                                                                         |
| 8     | REF-PWDWN  | R/W  | 0     | When set to 1 disables the device internal reference                                                                                                                                                                                                                                                                      |
| 7     | DAC7-PWDWN | R/W  | 0     | When set to 1 the corresponding DAC is set in power-down mode and its output is connected to GND through a 1 k $\Omega$ internal resistor.                                                                                                                                                                                |
| 6     | DAC6-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 5     | DAC5-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 4     | DAC4-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 3     | DAC3-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 2     | DAC2-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 1     | DAC1-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |
| 0     | DAC0-PWDWN | R/W  | 0     |                                                                                                                                                                                                                                                                                                                           |

### 8.6.5 GAIN Register (address = 0x04) [reset = 0x---]

**Figure 71. GAIN Register**

| 15         | 14         | 13         | 12         | 11         | 10                                           | 9                                            | 8          |
|------------|------------|------------|------------|------------|----------------------------------------------|----------------------------------------------|------------|
| Reserved   |            |            |            |            | Reserved/<br>CLR-4TO7-<br>MSK <sup>(1)</sup> | Reserved/<br>CLR-0TO3-<br>MSK <sup>(1)</sup> | REFDIV-EN  |
| —          |            |            |            |            | R/W                                          | R/W                                          | R/W        |
| 7          | 6          | 5          | 4          | 3          | 2                                            | 1                                            | 0          |
| BUFF7-GAIN | BUFF6-GAIN | BUFF5-GAIN | BUFF4-GAIN | BUFF3-GAIN | BUFF2-GAIN                                   | BUFF1-GAIN                                   | BUFF0-GAIN |
| R/W        | R/W        | R/W        | R/W        | R/W        | R/W                                          | R/W                                          | R/W        |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) DACx0508C only. Reserved bits in DACx0508.

**Table 13. GAIN Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                                                                                                  |
|-------|-------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Reserved                | —    | 0     | Reserved for factory use.                                                                                                                                                                                                                    |
| 10    | Reserved / CLR-4TO7-MSK | R/W  | 0     | DACx0508. Reserved for factory use.                                                                                                                                                                                                          |
| 9     | Reserved / CLR-0TO3-MSK | R/W  | 0     | DACx0508C. When cleared to 0 the corresponding DAC group is set to clear in response to a logic-low value on the CLR pin. When set to 1 the corresponding DAC group remains unaffected by the CLR pin.                                       |
| 8     | REFDIV-EN               | R/W  | 0/1   | When set to 1 the reference voltage is internally divided by a factor of 2.<br>When cleared to 0 the reference voltage is unaffected.                                                                                                        |
| 7     | BUFF7-GAIN              | R/W  | 0/1   | When set to 1 the buffer amplifier for corresponding DAC has a gain of 2. Default value for the DACx0508M devices.<br>When cleared to 0 the buffer amplifier for corresponding DAC has a gain of 1. Default value for the DACx0508Z devices. |
| 6     | BUFF6-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 5     | BUFF5-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 4     | BUFF4-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 3     | BUFF3-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 2     | BUFF2-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 1     | BUFF1-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |
| 0     | BUFF0-GAIN              | R/W  | 0/1   |                                                                                                                                                                                                                                              |

### 8.6.6 TRIGGER Register (address = 0x05) [reset = 0x0000]

**Figure 72. TRIGGER Register**

| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4    | 3               | 2 | 1 | 0 |
|----------|----|----|----|----|----|---|---|---|---|---|------|-----------------|---|---|---|
| Reserved |    |    |    |    |    |   |   |   |   |   | LDAC | SOFT-RESET[3:0] |   |   |   |
| —        |    |    |    |    |    |   |   |   |   |   | W    | W               |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. TRIGGER Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 15:5 | Reserved        | —    | 0     | Reserved for factory use.                                                                                       |
| 4    | LDAC            | W    | 0     | Set this bit to 1 to synchronously load those DACs that have been set in synchronous mode in the SYNC register. |
| 3:0  | SOFT-RESET[3:0] | W    | 0x0   | When set to the reserved code 1010 resets the device to its default state.                                      |

### 8.6.7 BRDCAST Register (address = 0x6) [reset = 0x0000]

**Figure 73. BRDCAST Register**

| 15                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| BRDCAST-DATA[15:0] |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R/W                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. BRDCAST Register Field Descriptions**

| Bit  | Field              | Type | Reset  | Description                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------------------|------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | BRDCAST-DATA[15:0] | R/W  | 0x0000 | Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the SYNC register to update their active data register with the BRDCAST-DATA value. Data are MSB aligned in straight binary format and follows the format below:<br>DAC80508: { DATA[15:0] }<br>DAC70508: { DATA[13:0], x, x }<br>DAC60508: { DATA[11:0], x, x, x, x }<br>x – Don't care bits |

### 8.6.8 STATUS Register (address = 0x7) [reset = 0x0000]

**Figure 74. STATUS Register**

| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0 |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---------|---|
| Reserved |    |    |    |    |    |   |   |   |   |   |   |   |   | REF-ALM |   |
| —        |    |    |    |    |    |   |   |   |   |   |   |   |   | R/W     |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 16. STATUS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                            |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | Reserved | —    | 0     | Reserved for factory use.                                                                                                                              |
| 0    | REF-ALM  | R    | 0     | Reference alarm bit. Reads 1 when the difference between $V_{REF}/DIV$ and $V_{DD}$ is below the required minimum analog threshold. Reads 0 otherwise. |

### 8.6.9 DACx Register (address = 0x8 to 0xF) [reset = 0x0000 or 0x8000]

**Figure 75. DACx Register**

| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| DACx-DATA[15:0] |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R/W             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 17. DACx Register Field Descriptions**

| Bit  | Field           | Type | Reset            | Description                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DACx-DATA[15:0] | R/W  | 0x0000 or 0x8000 | Stores the 16-, 14- or 12-bit data to be loaded to DACx in MSB aligned straight binary format. The default value is zero-code for the DACx0508Z devices and midscale-code for the DACx0508M ones.<br>Data follows the format below:<br>DAC80508: { DATA[15:0] }<br>DAC70508: { DATA[13:0], x, x }<br>DAC60508: { DATA[11:0], x, x, x, x }<br>x – Don't care bits |

## 9 Application and Implementation

### NOTE

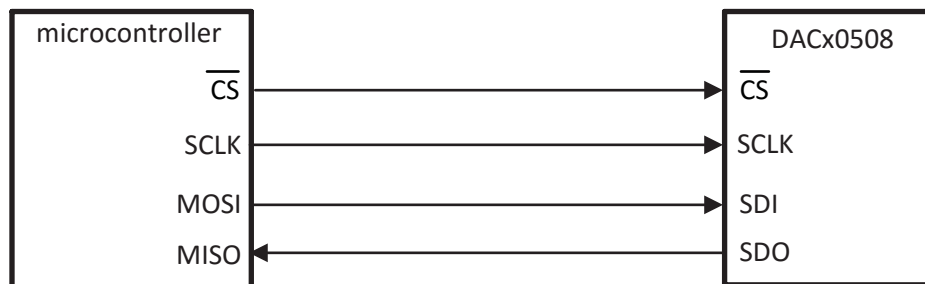
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The high linearity, small package size and wide temperature range make the DACx0508 suitable in applications such as optical networking, wireless infrastructure, industrial automation and data acquisition systems. The device incorporates a 2.5 V internal reference with an internal reference divider circuit that enables full-scale DAC output voltages of 1.25 V, 2.5 V, or 5 V.

#### 9.1.1 Interfacing to Microcontroller

Figure 76 displays a typical serial interface that may be observed when connecting the DACx0508 SPI serial interface to a (master) microcontroller type platform. The setup for the interface is as follows: The microcontroller output SPI CLK drives the SCLK pin of the DACx0508, while the DACx0508 SDI pin is driven by the MOSI pin of the microcontroller. The  $\overline{\text{CS}}$  pin of the DACx0508 can be asserted from a general program input/output pin of the microcontroller. When data are to be transmitted to the DACx0508, the  $\overline{\text{CS}}$  pin is taken low. The data from the microcontroller is then transmitted to the DACx0508, totaling 24 bits latched into the DACx0508 device through the falling edge of SCLK.  $\overline{\text{CS}}$  is then brought high after the completed write. The DACx0508 requires data with the MSB as the first bit received.



Copyright © 2017, Texas Instruments Incorporated

**Figure 76. Typical Serial Interface**

## Application Information (continued)

### 9.1.2 Programmable Current Source Circuit

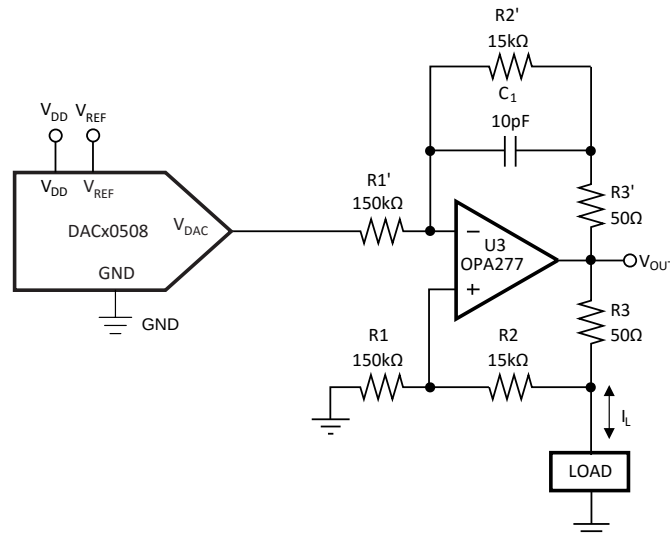
The DACx0508 can be integrated into the circuit in [Figure 77](#) to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by [Equation 2](#).

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times \frac{CODE}{2^n} \quad (2)$$

The value of R3 in [Equation 2](#) can be reduced to increase the output current drive of U3. U3 can drive  $\pm 20$  mV in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested as a result of the change in the output impedance  $Z_O$ , according to [Equation 3](#).

$$Z_O = \frac{(R1')(R3)(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (3)$$

As shown in [Equation 3](#), with matched resistors,  $Z_O$  is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used,  $Z_O$  is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

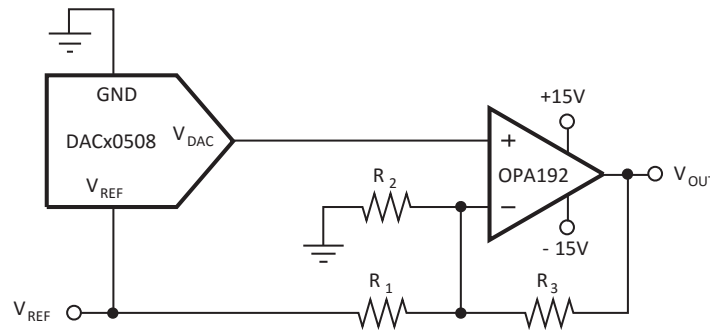


Copyright © 2017, Texas Instruments Incorporated

**Figure 77. Programmable Bidirectional Current Source Circuit**

## 9.2 Typical Application

The DACx0508 is designed for single-supply operation; however, a bipolar output is also possible using the circuit shown in [Figure 78](#).



NOTE: Some pins omitted for clarity.

Copyright © 2017, Texas Instruments Incorporated

**Figure 78. Bipolar Operation Using the DACx0508**

### 9.2.1 Design Requirements

The circuit shown in [Figure 78](#) gives a bipolar output voltage at  $V_{OUT}$ . When  $GAIN = 1$ ,  $V_{OUT}$  can be calculated using [Equation 4](#):

$$V_{OUT}(\text{CODE}) = \left[ \left( V_{REF} \times \frac{\text{CODE}}{2^n} \right) \left( 1 + \frac{R_3}{R_2} + \frac{R_3}{R_1} \right) - \left( V_{REF} \times \frac{R_3}{R_1} \right) \right] \quad (4)$$

Where:

- $V_{OUT}(\text{CODE})$  = output voltage versus code
- CODE = 0 to  $2^n - 1$ . This is the digital code loaded to the DAC
- $V_{REF}$  = reference voltage applied to the DACx0508
- $n$  = resolution in bits. Either 12 (DAC60508), 14 (DAC70508) or 16 (DAC80508)

**Table 18. Design Parameters**

| PARAMETER | VALUE      |
|-----------|------------|
| $V_{OUT}$ | $\pm 10$ V |
| $V_{REF}$ | 2.5 V      |
| $n$       | 12         |

### 9.2.2 Detailed Design Procedure

The bipolar output span can be calculated through [Equation 4](#) by defining a few parameters, the first being the value for the reference voltage. Once a reference voltage is chosen, the gain resistors can be set accordingly by determining the desired  $V_{OUT}$  at code 0 and code  $2^n$ . For a  $V_{REF}$  of 2.5 V and a desired output voltage range of  $\pm 10$  V the calculation is as follows.

CODE = 0:

$$V_{OUT}(0) = - \left( V_{REF} \times \frac{R_3}{R_1} \right) = - \left( 2.5\text{V} \times \frac{R_3}{R_1} \right) \quad (5)$$

Setting the equation to minimum output span,  $V_{OUT}(0) = -10$  V, will reduce the equation to:  $R_3/R_1 = 4$ :

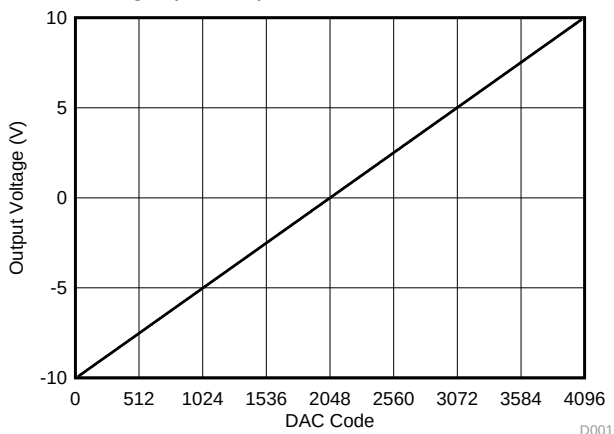
CODE = 4096:

Setting the equation to maximum output scan,  $V_{OUT}(4096) = 10$  V, and  $R_3/R_1 = 4$  will reduce the equation to:  $R_3/R_2 = 3$

It is important to note that the maximum code of a 12-bit DAC is 4095; code 4096 was used to simplify the equation above. For practical use, the true output span will encompass a range of  $-10\text{ V}$  to  $(10\text{ V} - 1\text{ LSB})$ , which in this case is  $-10\text{ V}$  to  $9.995\text{ V}$ .

### 9.2.3 Application Curve

The  $\pm 10\text{ V}$  output span with a reference voltage of  $2.5\text{ V}$  can be achieved by using values of  $30\text{ k}\Omega$ ,  $10\text{ k}\Omega$ , and  $7.5\text{ k}\Omega$  for  $R_3$ ,  $R_2$ , and  $R_1$  respectively. A curve to illustrate this output span is shown in [Figure 79](#). Note: 1% tolerance resistors were used in evaluating bipolar operation.



**Figure 79. Bipolar Operation**

## 10 Power Supply Recommendations

The DACx0508 operates within the specified  $V_{DD}$  supply range of 2.7 V to 5.5 V and  $V_{IO}$  supply range of 1.7 V to 5.5 V. The DACx0508 does not require specific supply sequencing.

The  $V_{DD}$  supply must be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. In order to further minimize noise from the power supply, include a 1- $\mu$ F to 10- $\mu$ F capacitor and 0.1- $\mu$ F bypass capacitor. The current consumption on the  $V_{DD}$  pin, the short-circuit current limit, and the load current for the device is listed in the [Electrical Characteristics](#). The power supply must meet the aforementioned current requirements.



## 11 Layout

### 11.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- Bypass all power supply pins to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1- to 0.22- $\mu$ F ceramic with a X7R or NP0 dielectric.
- Place power supplies and REF bypass capacitors close to the pins to minimize inductance and optimize performance.
- Use a high-quality ceramic type NP0 or X7R for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections must have proper placement with respect to the digital pins and analog pins of the DACx0508 device. The separation of analog and digital blocks minimizes coupling into neighboring blocks, as well as interaction between analog and digital return currents.

### 11.2 Layout Examples

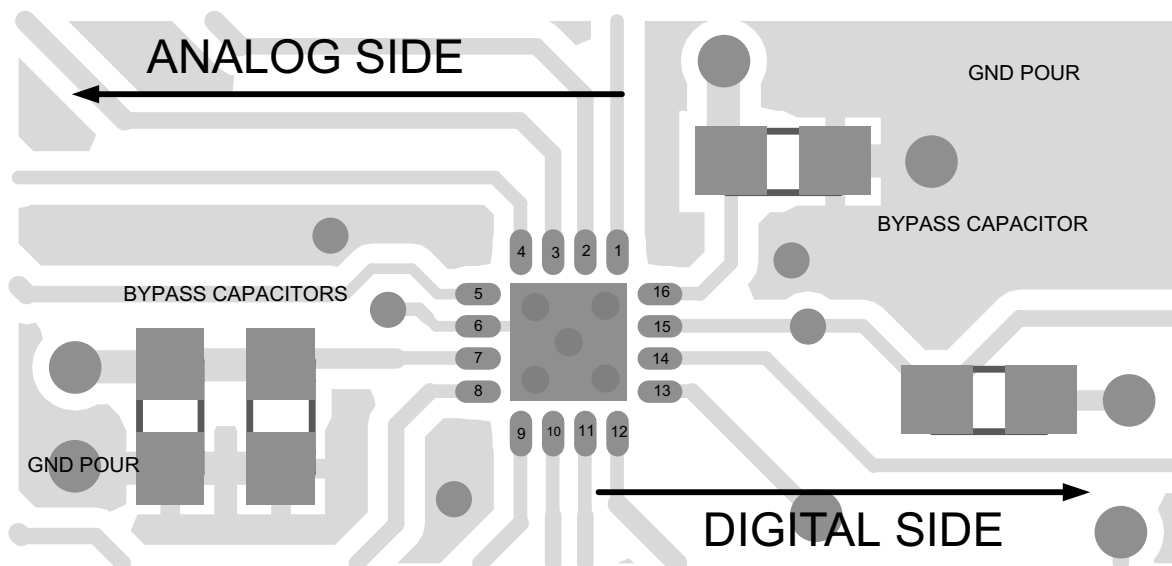
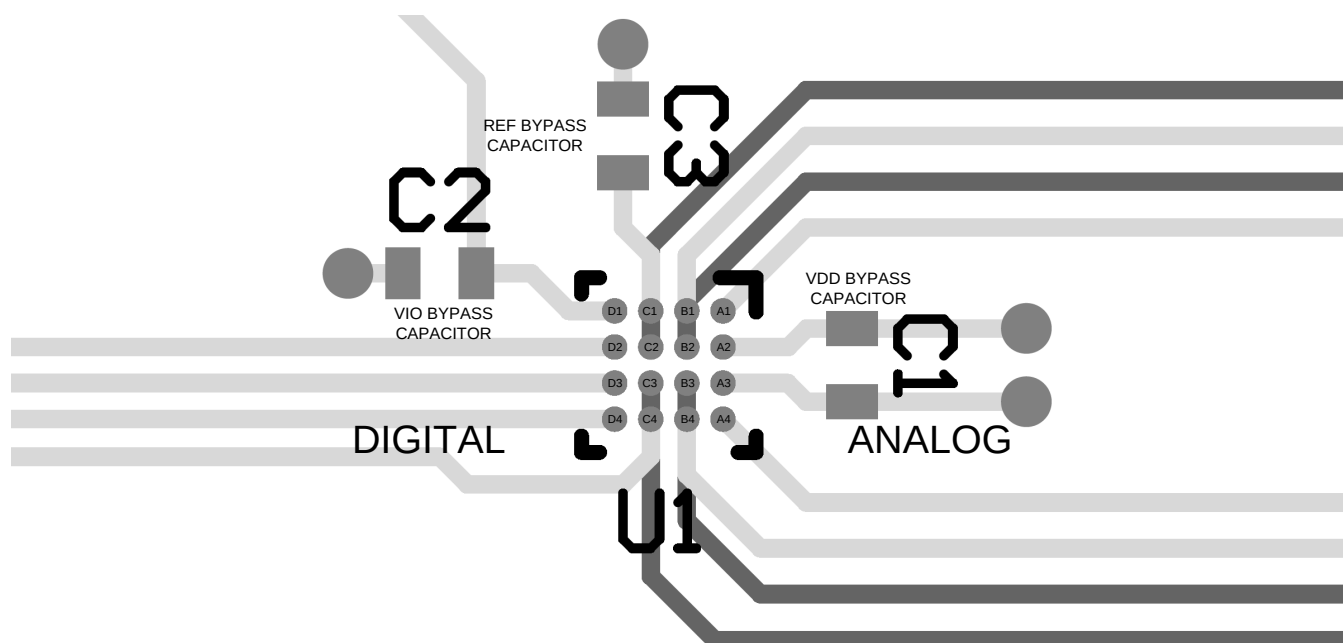


Figure 80. DACx0508 QFN Layout Example

## Layout Examples (continued)



**Figure 81. DACx0508 DSBGA Layout Example**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 19. Related Links**

| PARTS    | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DAC80508 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DAC70508 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DAC60508 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DAC60508MCRTER   | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658MC                   | <a href="#">Samples</a> |
| DAC60508MCRTET   | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658MC                   | <a href="#">Samples</a> |
| DAC60508MCYZFR   | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65MC                    | <a href="#">Samples</a> |
| DAC60508MCYZFT   | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65MC                    | <a href="#">Samples</a> |
| DAC60508MRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658M                    | <a href="#">Samples</a> |
| DAC60508MRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658M                    | <a href="#">Samples</a> |
| DAC60508MYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65M                     | <a href="#">Samples</a> |
| DAC60508MYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65M                     | <a href="#">Samples</a> |
| DAC60508ZCATER   | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658ZC                   | <a href="#">Samples</a> |
| DAC60508ZCATER   | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658ZC                   | <a href="#">Samples</a> |
| DAC60508ZCYZFR   | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65ZC                    | <a href="#">Samples</a> |
| DAC60508ZCYZFT   | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65ZC                    | <a href="#">Samples</a> |
| DAC60508ZRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658Z                    | <a href="#">Samples</a> |
| DAC60508ZRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 658Z                    | <a href="#">Samples</a> |
| DAC60508ZYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65Z                     | <a href="#">Samples</a> |
| DAC60508ZYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 65Z                     | <a href="#">Samples</a> |
| DAC70508MRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 758M                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DAC70508MRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 758M                    | <a href="#">Samples</a> |
| DAC70508MYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 75M                     | <a href="#">Samples</a> |
| DAC70508MYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 75M                     | <a href="#">Samples</a> |
| DAC70508ZRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 758Z                    | <a href="#">Samples</a> |
| DAC70508ZRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 758Z                    | <a href="#">Samples</a> |
| DAC70508ZYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 75Z                     | <a href="#">Samples</a> |
| DAC70508ZYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 75Z                     | <a href="#">Samples</a> |
| DAC80508MCRTER   | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858MC                   | <a href="#">Samples</a> |
| DAC80508MCRTET   | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858MC                   | <a href="#">Samples</a> |
| DAC80508MCYZFR   | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85MC                    | <a href="#">Samples</a> |
| DAC80508MCYZFT   | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85MC                    | <a href="#">Samples</a> |
| DAC80508MRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858M                    | <a href="#">Samples</a> |
| DAC80508MRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858M                    | <a href="#">Samples</a> |
| DAC80508MYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85M                     | <a href="#">Samples</a> |
| DAC80508MYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85M                     | <a href="#">Samples</a> |
| DAC80508ZCRTER   | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858ZC                   | <a href="#">Samples</a> |
| DAC80508ZCRTET   | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858ZC                   | <a href="#">Samples</a> |
| DAC80508ZCYZFR   | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85ZC                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DAC80508ZCYZFT   | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85ZC                    | <a href="#">Samples</a> |
| DAC80508ZRTER    | ACTIVE        | WQFN         | RTE                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858Z                    | <a href="#">Samples</a> |
| DAC80508ZRTET    | ACTIVE        | WQFN         | RTE                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 125   | 858Z                    | <a href="#">Samples</a> |
| DAC80508ZYZFR    | ACTIVE        | DSBGA        | YZF                | 16   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85Z                     | <a href="#">Samples</a> |
| DAC80508ZYZFT    | ACTIVE        | DSBGA        | YZF                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 85Z                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

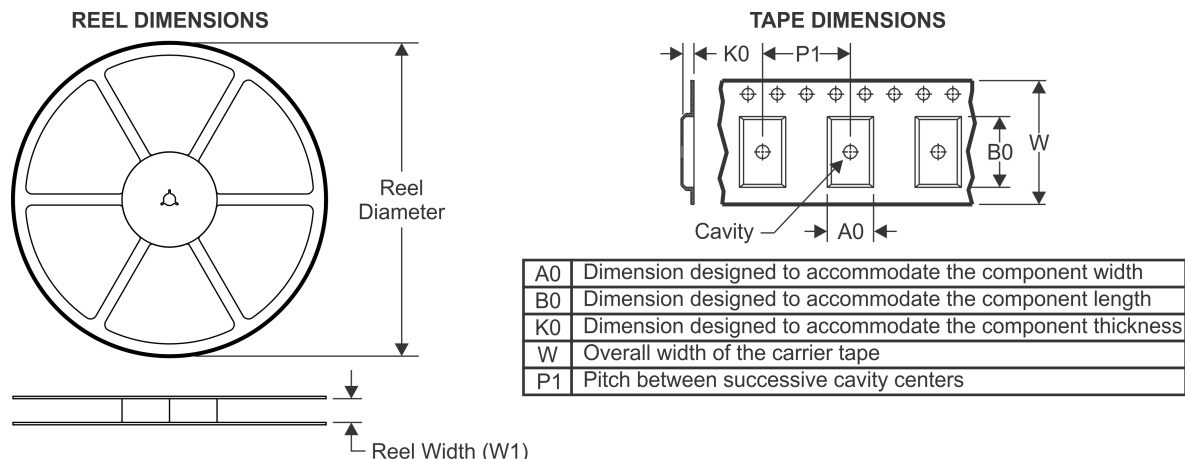
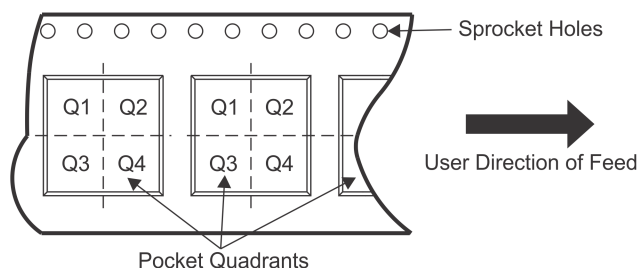
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


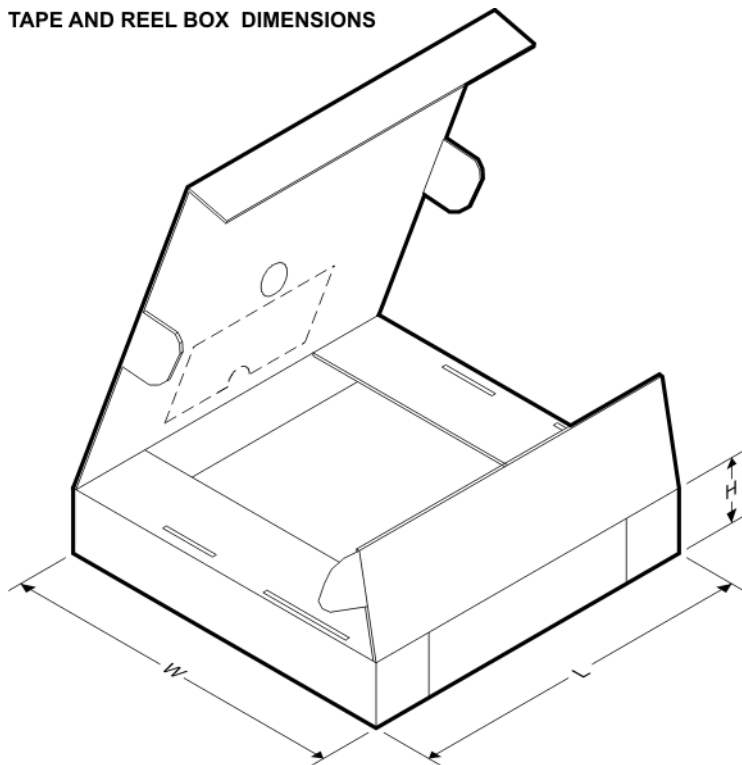
\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC60508MCRTER | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508MCRTER | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508MCYZFR | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508MCYZFT | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508MRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508MRTER  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508MYZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508ZCRTER | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508ZCRTER | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508ZCYZFR | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508ZCYZFT | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508ZRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508ZRTER  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC60508YZZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC60508YZZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC70508MRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC70508MRTER  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |



| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC70508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC70508MYZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC70508ZRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC70508ZRTET  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC70508ZYZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC70508ZYZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508MCRTER | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508MCRTET | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508MCYZFR | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508MCYZFT | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508MRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508MRTET  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508MYZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508ZCRTER | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508ZCRTET | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508ZCYZFR | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508ZCYZFT | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508ZRTER  | WQFN         | RTE             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508ZRTET  | WQFN         | RTE             | 16   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| DAC80508ZYZFR  | DSBGA        | YZF             | 16   | 3000 | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |
| DAC80508ZYZFT  | DSBGA        | YZF             | 16   | 250  | 180.0              | 8.4                | 2.54    | 2.54    | 0.76    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

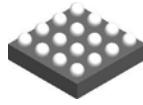


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC60508MCRTER | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC60508MCRTET | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC60508MCYZFR | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC60508MCYZFT | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC60508MRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC60508MRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC60508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC60508MYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC60508ZCRTER | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC60508ZCRTET | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC60508ZCYZFR | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC60508ZCYZFT | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC60508ZRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC60508ZRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC60508ZYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC60508ZYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC70508MRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC70508MRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC70508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC70508MYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC70508ZRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC70508ZRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC70508ZYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC70508ZYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC80508MCRTER | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC80508MCRTET | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC80508MCYZFR | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC80508MCYZFT | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC80508MRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC80508MRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC80508MYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC80508MYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC80508ZCRTER | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC80508ZCRTET | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC80508ZCYZFR | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC80508ZCYZFT | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| DAC80508ZRTER  | WQFN         | RTE             | 16   | 3000 | 370.0       | 355.0      | 55.0        |
| DAC80508ZRTET  | WQFN         | RTE             | 16   | 250  | 195.0       | 200.0      | 45.0        |
| DAC80508ZYZFR  | DSBGA        | YZF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| DAC80508ZYZFT  | DSBGA        | YZF             | 16   | 250  | 182.0       | 182.0      | 20.0        |

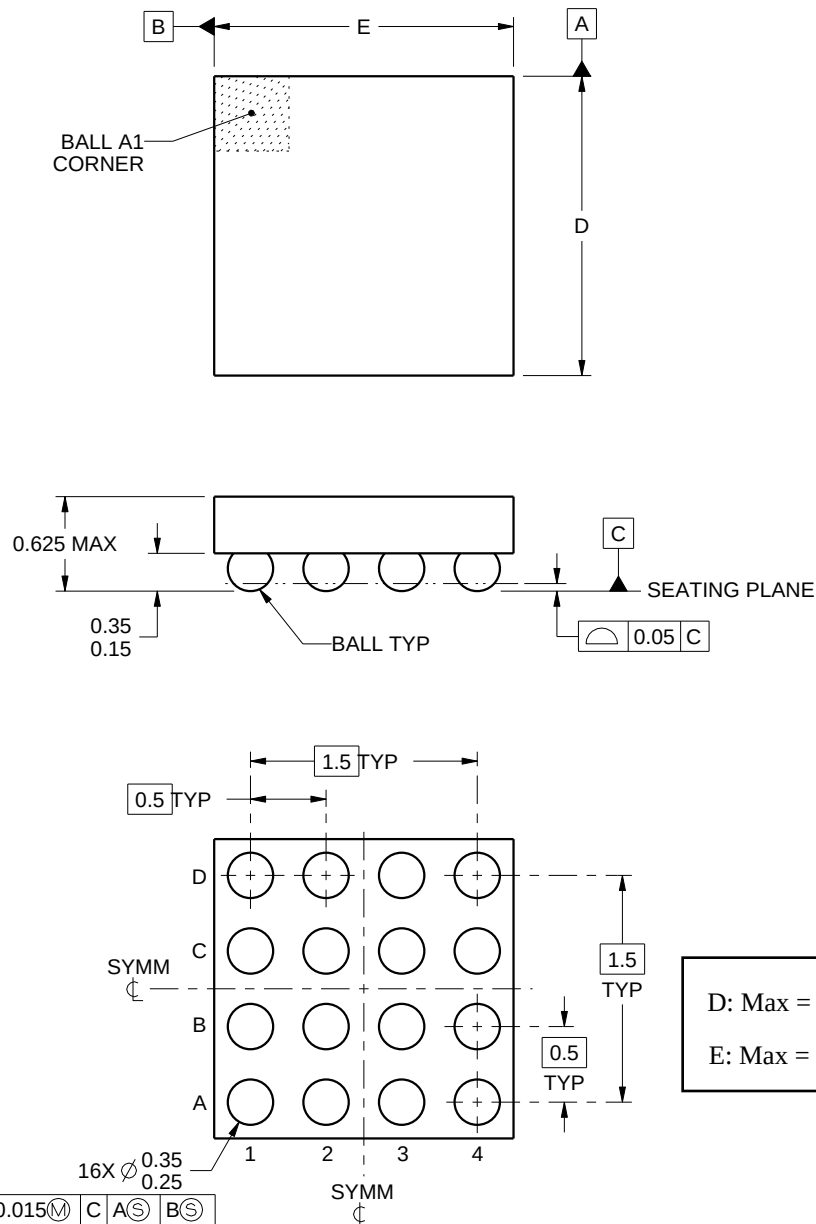
YZF0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4222182/A 08/2015

## NOTES:

NanoFree is a trademark of Texas Instruments.

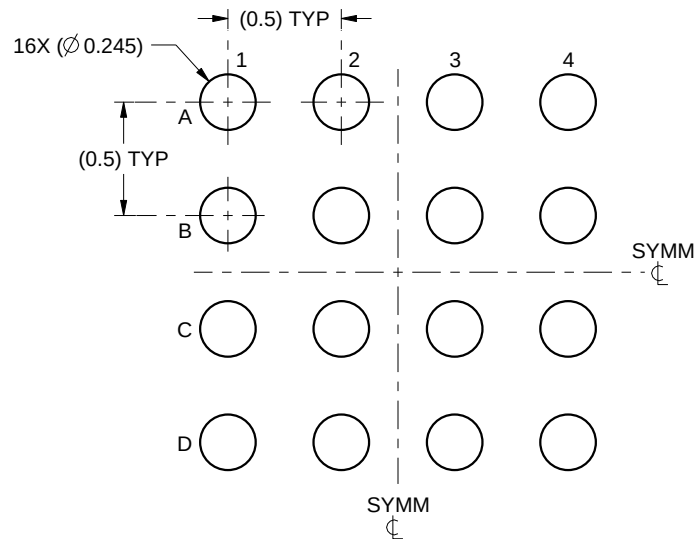
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

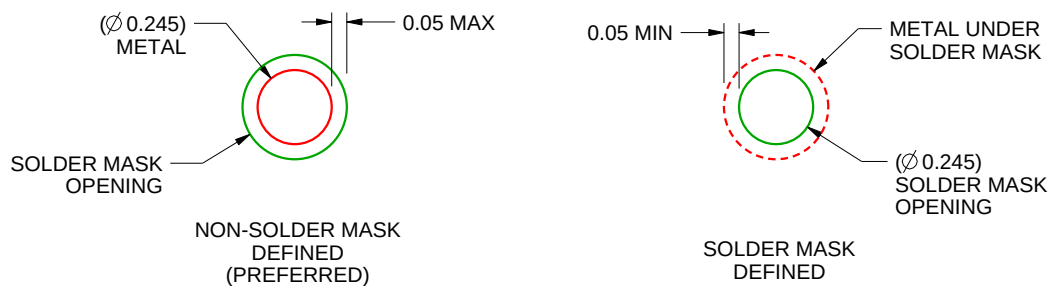
YZF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4222182/A 08/2015

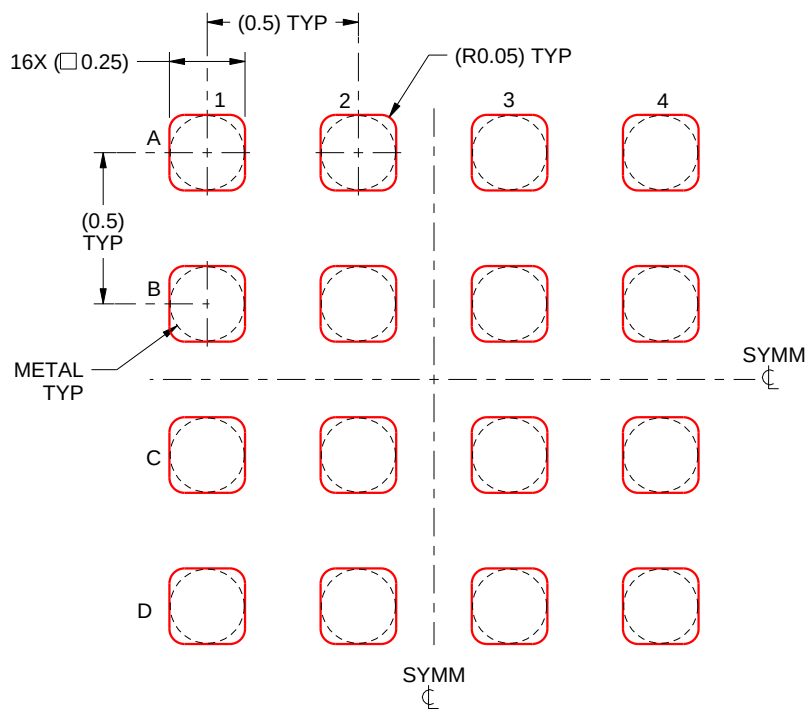
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

**YZF0016**

**DSBGA - 0.625 mm max height**

## DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

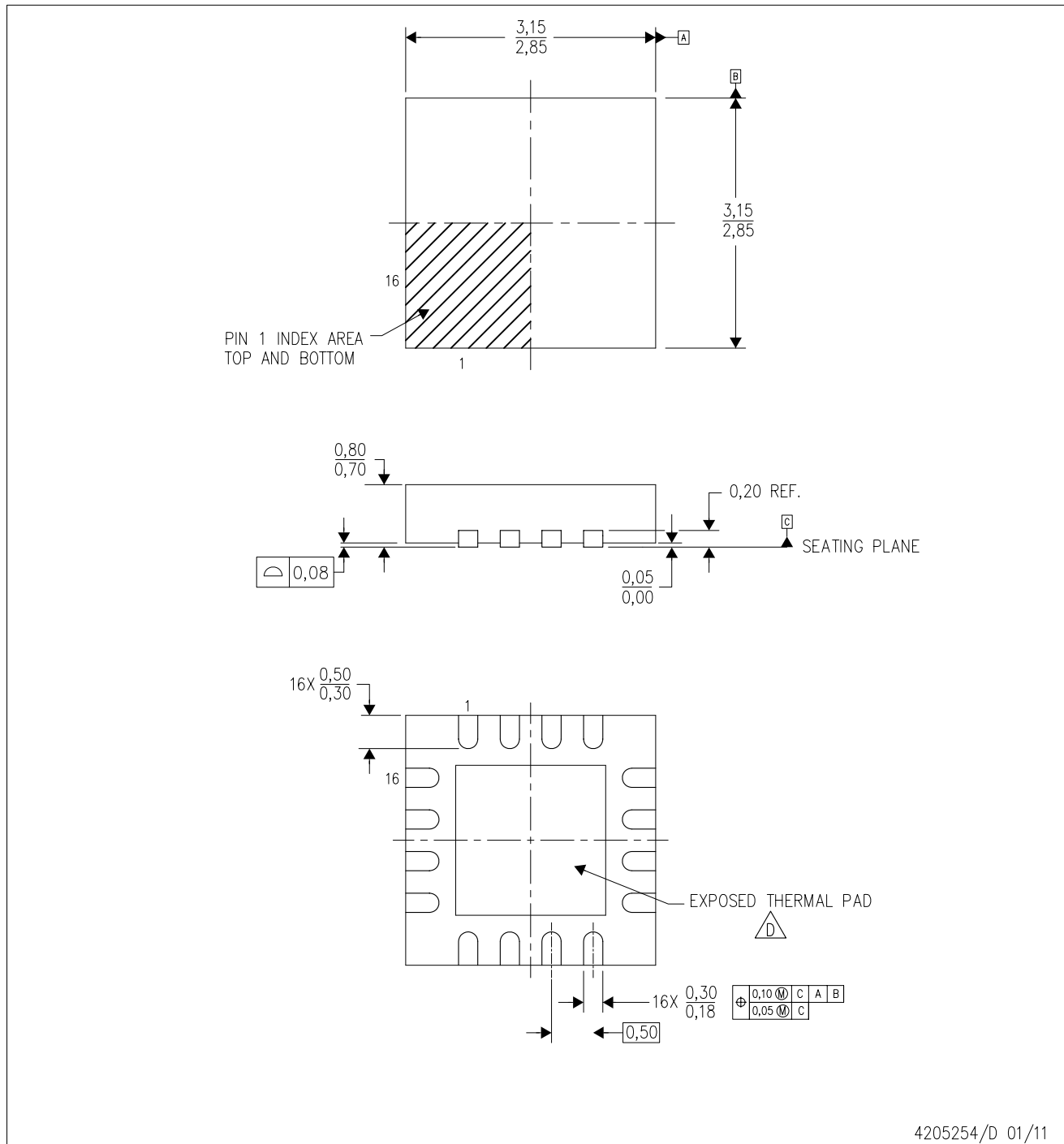
4222182/A 08/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

RTE (S-PWQFN-N16)

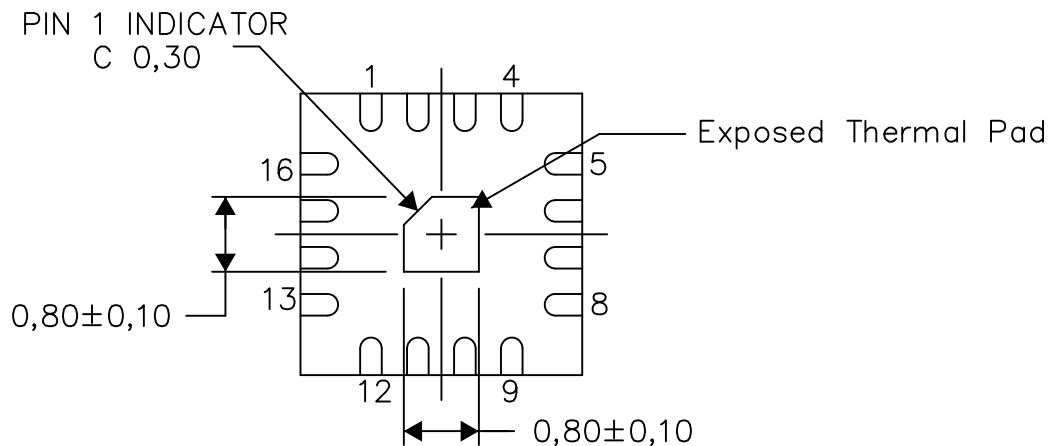
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

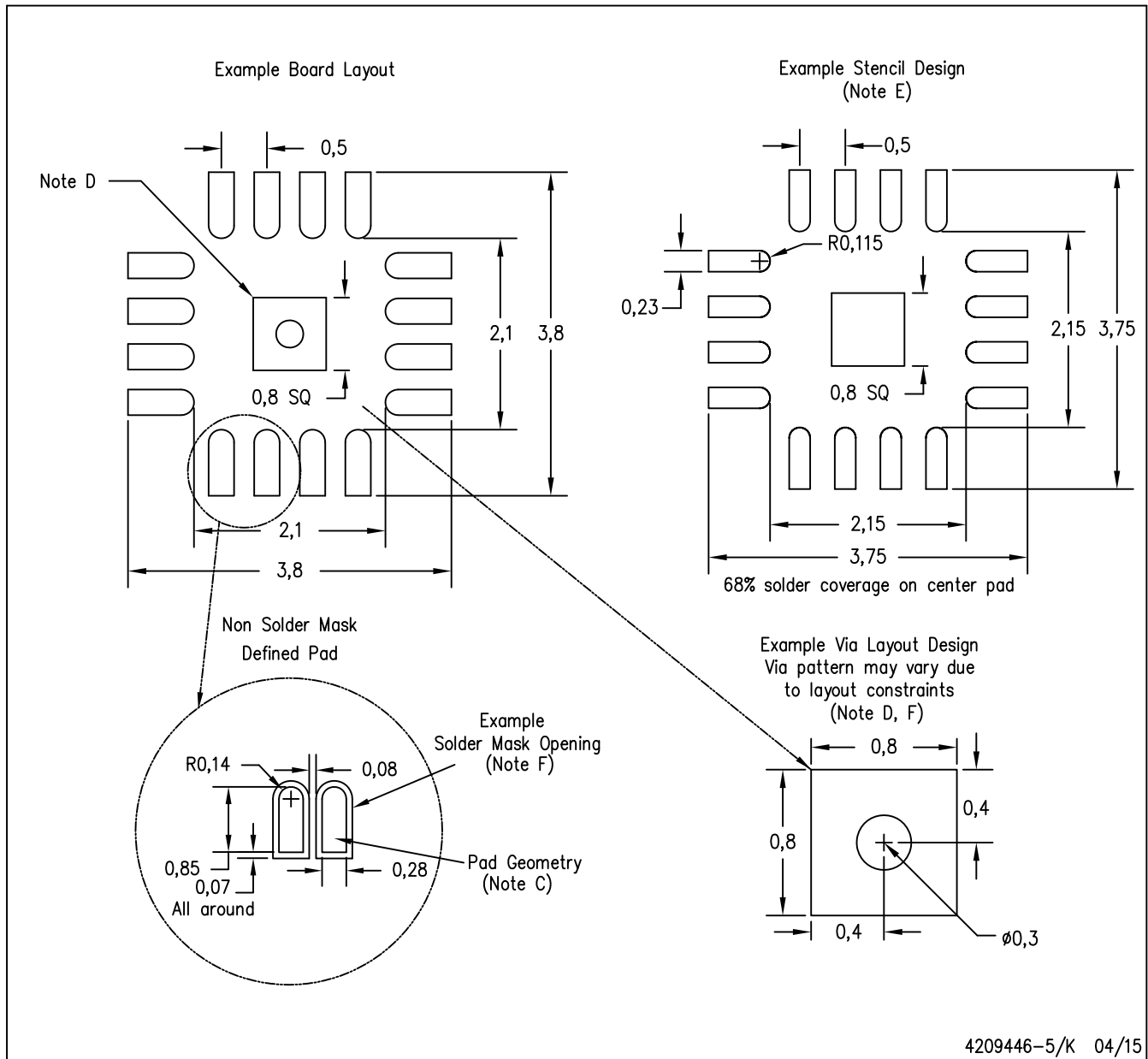
4206446-5/U 08/15

NOTE: A. All linear dimensions are in millimeters



RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated