# DAC-10

## 10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

### FEATURES

- **Fast Settling ..... 85ns**
- **Low Full-Scale Drift ..... 10ppm/°C**
- **Nonlinearity to 0.05% Max Over Temp Range**
- **Complementary Current Outputs ..... 0 to 4mA**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Wide Power Supply Range .. +5, −7.5 Min to ±18V Max**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**
- **Available in Die Form**

### ORDERING INFORMATION †

| | PACKAGE: 18-PIN CERDIP |
|---|---|
| NL LSB | COMMERCIAL TEMPERATURE 0°C to +70°C |
| ±1/2 | DAC10FX |
| ±1 | DAC10GX |
| ±1 | DAC10GS |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

### GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying digital-to-analog converters provide high-speed performance and full-scale accuracy.

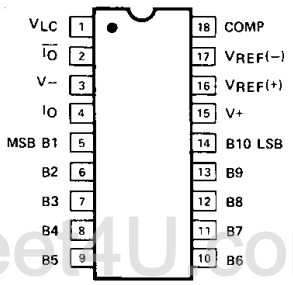
Advanced circuit design achieves 85ns settling times with very low 'glitch' energy and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable-threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as ±0.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±18V power supply range, with 85mW power consumption attainable at lower supplies.

A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

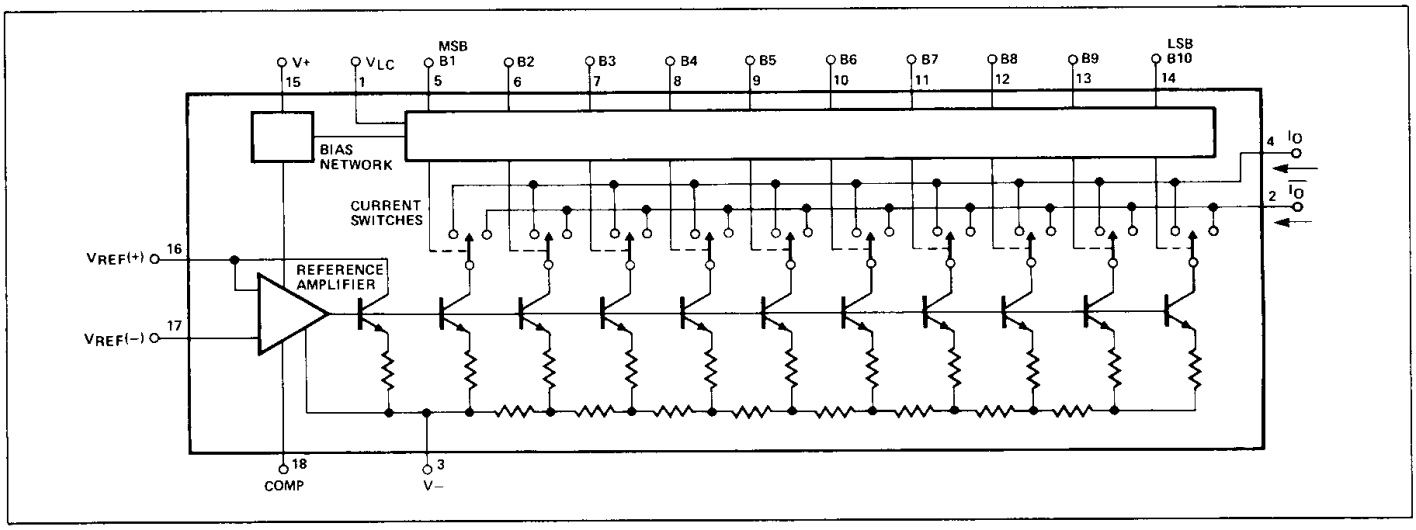
### PIN CONNECTIONS




**18-PIN HERMETIC DIP (X-Suffix)**



### SIMPLIFIED SCHEMATIC




Manufactured under one or more of the following patents. 4,055,770, 4,056,740, 4,092,639.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature
DAC-10FX, GX, GS ..... 0°C to +70°C
Junction Temperatre ($T_j$) ..... –65°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply ..... 36V
Logic Inputs ..... V– to V– plus 36V
$V_{LC}$ ..... V– to V+
Analog Current Outputs ..... +18V to –18V
Reference Inputs ($V_{16}$ to $V_{17}$) ..... V– to V+
Reference Input Differential Voltage
($V_{16}$ to $V_{17}$) ..... ±18V
Reference Input Current ($I_{16}$) ..... 2.5mA

| PACKAGE TYPE | $\Theta_{JA}$ (NOTE 2) | $\Theta_{JC}$ | UNITS |
|---|---|---|---|
| 18-Pin Hermetic DIP (X) | 84 | 15 | °C/W |

**NOTES:**
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. $\Theta_{JA}$ is specified for worst case mounting conditions, i.e., $\Theta_{JA}$ is specified for device in socket for CerDIP packages.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$; $I_{REF} = 2mA$; $0°C \le T_A \le 70°C$ FOR DAC-10F and G, unless otherwise noted.

Output characteristics apply to both $I_{OUT}$ and $\overline{I_{OUT}}$.

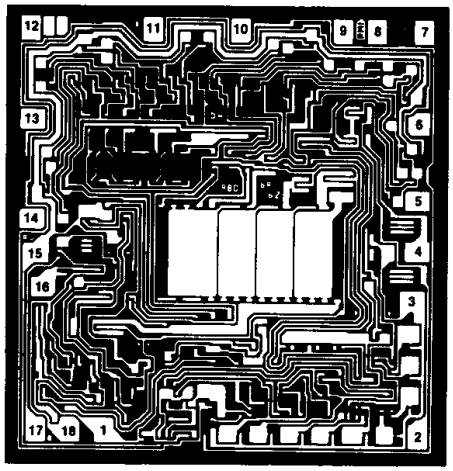
| PARAMETER | SYMBOL | CONDITIONS | DAC-10F MIN | DAC-10F TYP | DAC-10F MAX | DAC-10G MIN | DAC-10G TYP | DAC-10G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Monotonicity | | | 10 | — | — | 10 | — | — | Bits |
| Nonlinearity | NL | | — | 0.3 | 0.5 | — | 0.6 | 1 | LSB |
| Differential Nonlinearity | DNL | | — | 0.3 | 1 | — | 0.7 | — | LSB |
| Settling Time | $t_S$ | All Bits Switched ON or OFF<br>Settle to 0.05% of FS (See Note) | — | 85 | 135 | — | 85 | 150 | ns |
| Output Capacitance | $C_O$ | | — | 18 | — | — | 18 | — | pF |
| Propagation Delay | $t_{PLH}$<br>$t_{PHL}$ | All Bits Switched $R_L = 5k\Omega$<br>$R_L = 0$ | —<br>— | 50<br>50 | —<br>— | —<br>— | 50<br>50 | —<br>— | ns |
| Output Voltage Compliance | $V_{OC}$ | Full-Scale Current Change <1 LSB | —<br>— | −5.5<br>+10 | —<br>— | —<br>— | −5.5<br>+10 | —<br>— | V |
| Gain Tempco | $TCI_{FS}$ | (See Note) | — | ±10 | ±25 | — | ±10 | ±50 | ppm/°C |
| Full-Scale Symmetry | $I_{FSS}$ | $I_{FR} - \overline{I_{FR}}$ | — | 0.1 | 4 | — | 0.1 | 4 | µA |
| Zero-Scale Current | $I_{ZS}$ | | — | 0.01 | 0.5 | — | 0.01 | 0.5 | µA |
| Full-Scale Current | $I_{FR}$ | (See Note) | 3.960 | 3.996 | 4.032 | 3.920 | 3.996 | 4.072 | mA |
| Reference Input Slew Rate | DI/dt | | — | 6 | — | — | 6 | — | mA/µs |
| Reference Bias Current | $I_B$ | | — | −1 | −3 | — | −1 | −3 | µA |
| Power Supply Sensitivity | $PSSI_{FS}+$<br>$PSSI_{FS}-$ | $4.5V \le V+ \le 18V$<br>$-18V \le V- \le -10V$ | —<br>— | 0.001<br>0.0012 | 0.01<br>0.01 | —<br>— | 0.001<br>0.0012 | 0.01<br>0.01 | $\%\Delta I_{FS}/\%\Delta V$ |
| Power Supply Current | I+<br>I–<br>I+<br>I– | $V_S = \pm15V$; $I_{REF} = 2mA$<br>$V_S = +5V, -7.5V$; $I_{REF} = 1mA$ | —<br>—<br>—<br>— | 2.3<br>−9<br>1.8<br>−5.9 | 4<br>−15<br>4<br>−9 | —<br>—<br>—<br>— | 2.3<br>−9<br>1.8<br>−5.9 | 4<br>−15<br>4<br>−9 | mA |
| Power Dissipation | $P_d$ | $V_S = \pm15V$; $I_{REF} = 2mA$<br>$V_S = +5V, -7.5V$; $I_{REF} = 1mA$ | —<br>— | 231<br>85 | 285<br>88 | —<br>— | 231<br>85 | 285<br>88 | mW |
| Logic Input Levels | $V_{IL}$<br>$V_{IH}$ | $V_{LC} = 0$ | —<br>2 | —<br>— | 0.8<br>— | —<br>2 | —<br>— | 0.8<br>— | V |
| Logic Input Currents | $I_{IL}$<br>$I_{iH}$ | $V_{LC} = 0$; $V_{IN} = 0.8V$<br>$V_{IN} = 2.0V$ | −10<br>— | −5<br>0.001 | —<br>10 | −10<br>— | −5<br>0.001 | —<br>10 | µA |

## ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$; $I_{REF} = 2mA$; $T_A = 25°C$, unless otherwise noted. Output characteristics apply to both $I_{OUT}$ and $\overline{I_{OUT}}$.

| PARAMETER | SYMBOL | CONDITIONS | DAC-10F MIN | DAC-10F TYP | DAC-10F MAX | DAC-10G MIN | DAC-10G TYP | DAC-10G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Monotonicity | | | 10 | — | — | 10 | — | — | Bits |
| Nonlinearity | NL | | — | 0.3 | 0.5 | — | 0.6 | 1 | LSB |
| Differential Nonlinearity | DNL | | — | 0.3 | 1 | — | 0.7 | — | LSB |
| Output Voltage Compliance | $V_{OC}$ | Full-Scale Current Change <1 LSB | −5 | −6/+18 | +10 | −5 | −6/+15 | +10 | V |
| Full-Scale Current | $I_{FS}$ | $V_{REF} = 10.000V$,<br>$R_{14} = R_{15} = 5.000k\Omega$ | 3.978 | 3.996 | 4.014 | 3.956 | 3.996 | 4.036 | mA |
| Full-Scale Symmetry | $I_{FSS}$ | $I_{FR} - \overline{I_{FR}}$ | — | 0.1 | 4 | — | 0.1 | 4 | µA |
| Zero-Scale Current | $I_{ZS}$ | | — | 0.01 | 0.5 | — | 0.01 | 0.5 | µA |

**NOTE:** Guaranteed by design.

## DICE CHARACTERISTICS




DIE SIZE 0.091 × 0.087 inch, 7917 sq. mils
(2.311 × 2.210 mm, 5.107 sq. mm)

1. $V_{LC}$ (LOGIC) THRESHOLD CONTROL
2. $\overline{I_O}$
3. V−
4. $I_O$
5. B1 (MSB)
6. B2
7. B3
8. B4
9. B5
10. B6
11. B7
12. B8
13. B9
14. B10 (LSB)
15. V+
16. $V_{REF}$ (+)
17. $V_{REF}$ (−)
18. COMPENSATION

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

**WAFER TEST LIMITS** at $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both $I_{OUT}$ and $\overline{I_{OUT}}$.

| PARAMETER | SYMBOL | CONDITIONS | DAC-10N LIMIT | DAC-10G LIMIT | UNITS |
|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | Bits MIN |
| Monotonicity | | | 10 | 10 | Bits MIN |
| Nonlinearity | NL | | ±0.5 | ±1 | LSB MAX |
| Output Voltage Compliance | $V_{OC}$ | True 1 LSB | +10<br>−5 | +10<br>−5 | V MAX<br>V MIN |
| Output Current Range | | $I_{FS}$ ±3.996 MA | ±18 | ±40 | μA MAX |
| Zero-Scale Current | $I_{ZS}$ | All Bits OFF | 0.5 | 0.5 | μA MAX |
| Logic Input "1" | $V_{IH}$ | $I_{IN}$ = 100nA | 2 | 2 | V MIN |
| Logic Input "0" | $V_{IL}$ | $V_{LC}$ @ Ground<br>$I_{IN} = -100\mu A$ | 0.8 | 0.8 | V MAX |
| Positive Supply Current | I+ | V+ = 15V | 4 | 4 | mA MAX |
| Negative Supply Current | I− | V− = −15V | −15 | −15 | mA MAX |

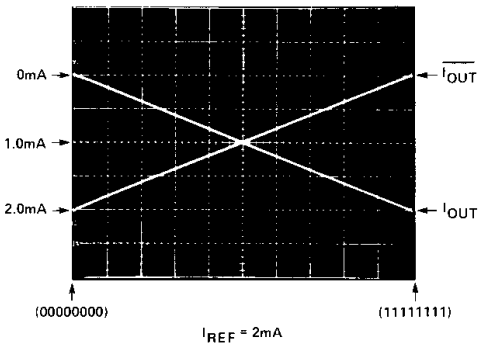
**NOTE:**
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, and $I_{REF} = 2mA$, unless otherwise noted. Output characteristics refer to both $I_{OUT}$ and $\overline{I_{OUT}}$.

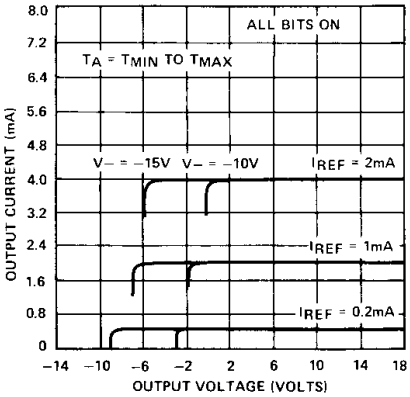
| PARAMETER | SYMBOL | CONDITIONS | DAC-10N TYPICAL | DAC-10G TYPICAL | UNITS |
|---|---|---|---|---|---|
| Settling Time | $t_S$ | To ±1/2 LSB When Output is Switched from 0 to FS | 85 | 85 | ns |
| Gain Temperature Coefficient (TC) | | $V_{REF}$ Tempco Excluded | ±10 | ±10 | ppm FS/°C |
| Output Capacitance | | | 18 | 18 | pF |
| Output Resistance | | | 10 | 10 | MΩ |

## TYPICAL PERFORMANCE CHARACTERISTICS

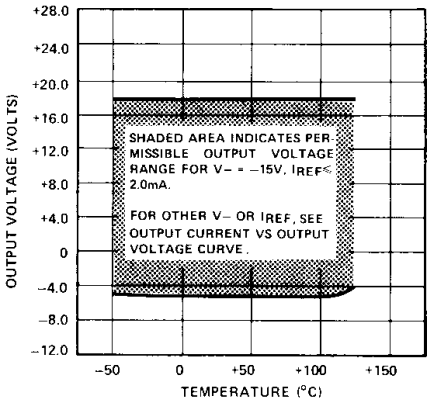
### TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



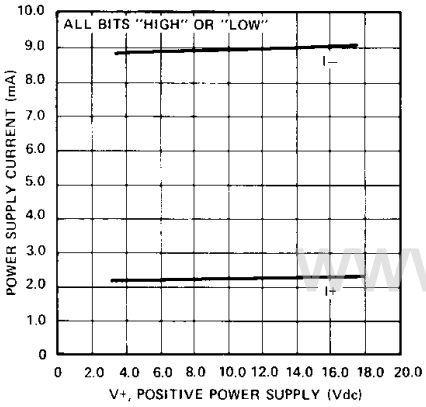

### OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



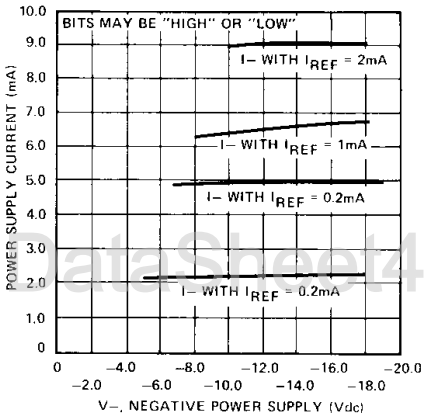

### OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



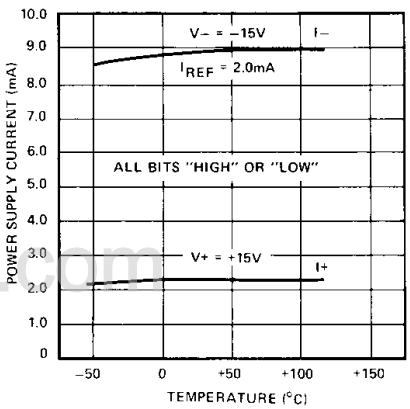

### POWER SUPPLY CURRENT vs V+




### POWER SUPPLY CURRENT vs V–

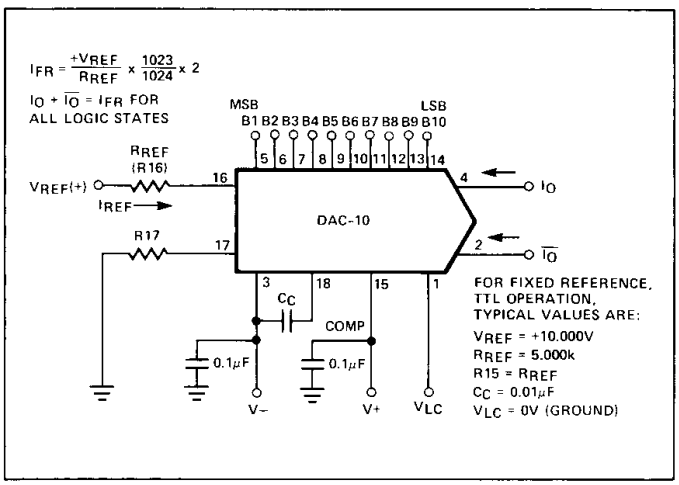



### POWER SUPPLY CURRENT vs TEMPERATURE

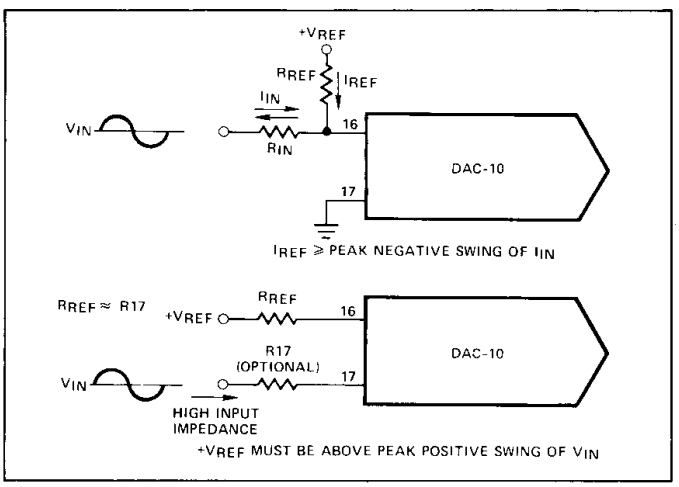



## BASIC CONNECTIONS

### BASIC POSITIVE REFERENCE OPERATION




### ACCOMMODATING BIPOLAR REFERENCES

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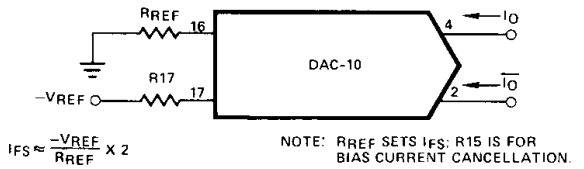
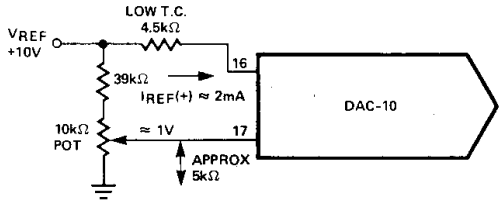
DIGITAL-TO-ANALOG CONVERTERS

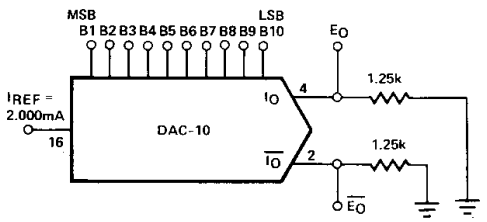
## BASIC NEGATIVE REFERENCE OPERATION




## RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT

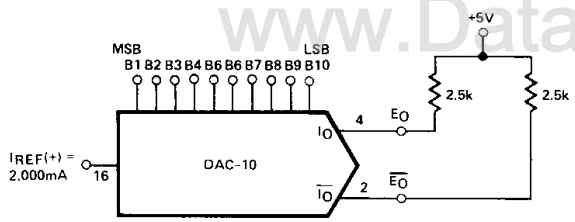



## BASIC UNIPOLAR NEGATIVE OPERATION



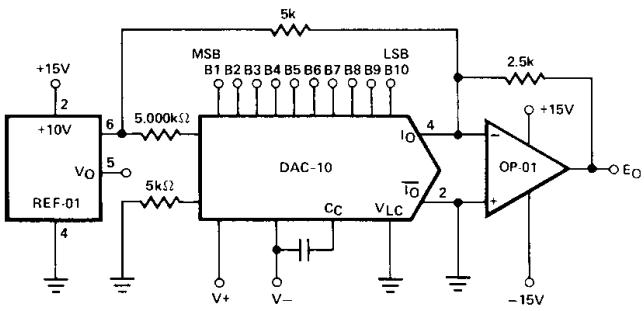

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | $I_O$mA | $\overline{I_O}$mA | $E_O$ | $\overline{E_O}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FULL RANGE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3.996 | 0.000 | −4.995 | −0.000 |
| HALF-SCALE +LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2.004 | 1.992 | −2.505 | −2.490 |
| HALF-SCALE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2.000 | 1.996 | −2.500 | −2.495 |
| HALF-SCALE −LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1.996 | 2.000 | −2.495 | 2.500 |
| ZERO-SCALE +LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.004 | 3.992 | −0.005 | −4.990 |
| ZERO-SCALE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | 3.996 | −0.000 | −4.995 |

## BASIC BIPOLAR OUTPUT OPERATION



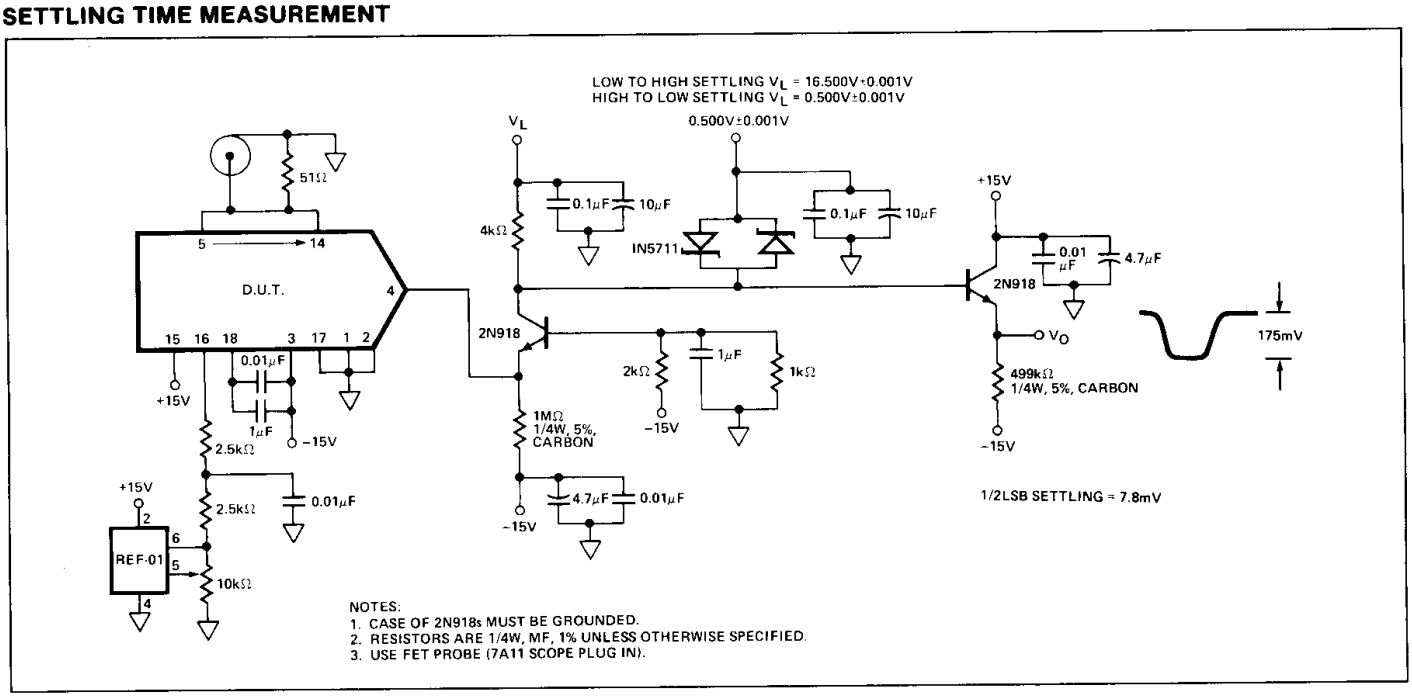

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | $E_O$ | $\overline{E_O}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| POS FULL RANGE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −4.990 | +5.000 |
| POS FULL RANGE −LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | −4.980 | +4.990 |
| ZERO-SCALE +LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −0.010 | +0.020 |
| ZERO-SCALE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.010 |
| ZERO-SCALE −LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +0.010 | 0.000 |
| NEG FULL-SCALE +LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +4.990 | −4.980 |
| NEG FULL-SCALE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +5.000 | −4.990 |

## OFFSET BINARY OPERATION

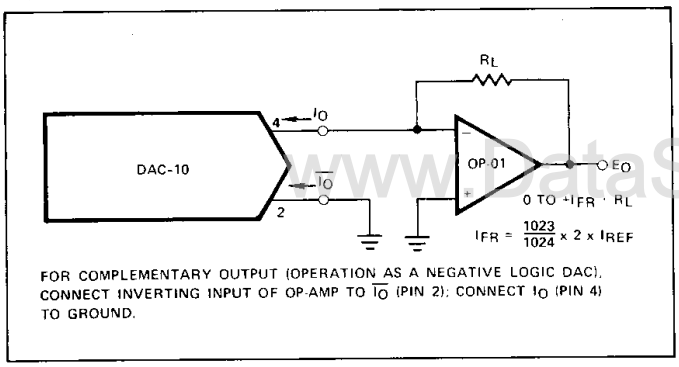



| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | $E_O$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| POS FULL RANGE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +4.990 |
| ZERO-SCALE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.00 |
| NEG FULL-SCALE +LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −4.990 |
| NEG FULL-SCALE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −5.000 |

## SETTLING TIME MEASUREMENT

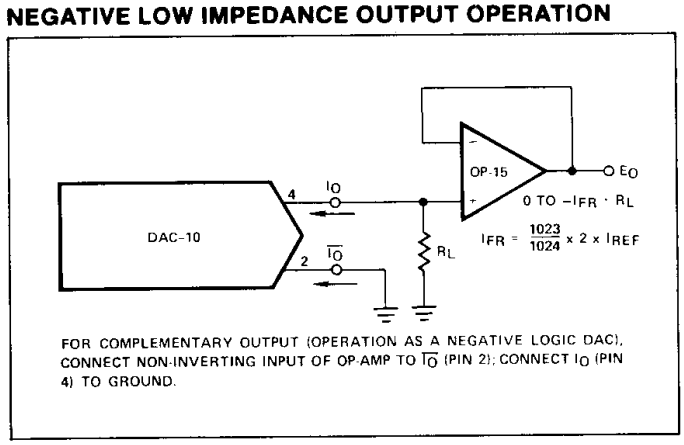



## POSITIVE LOW IMPEDANCE OUTPUT OPERATION



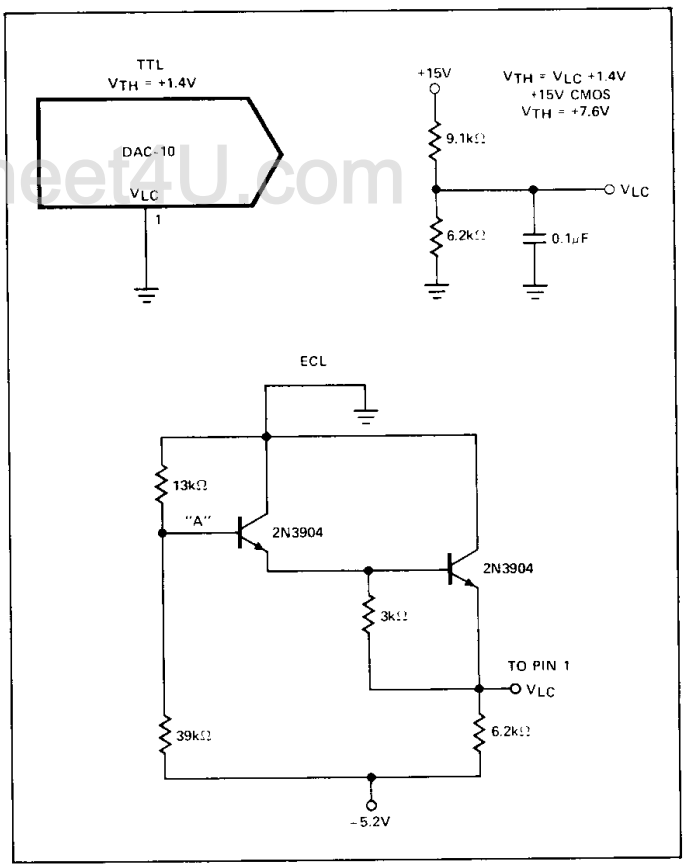

FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT $I_O$ (PIN 4) TO GROUND.

## NEGATIVE LOW IMPEDANCE OUTPUT OPERATION




FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT $I_O$ (PIN 4) TO GROUND.

## INTERFACING WITH VARIOUS LOGIC FAMILIES

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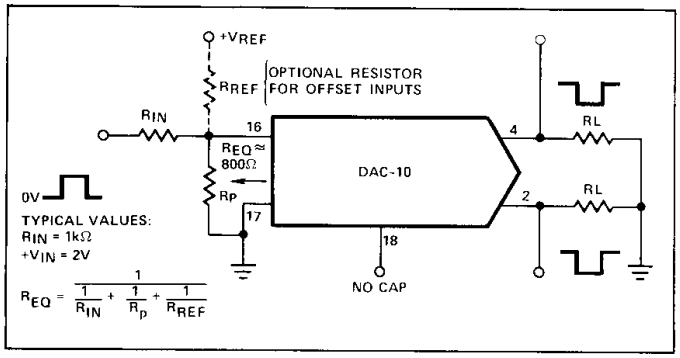
DIGITAL-TO-ANALOG CONVERTERS

### PULSED REFERENCE OPERATION




## APPLICATIONS INFORMATION

### REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the $V_{REF(+)}$ terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 17; reference current flows from ground through R16 into $V_{(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. The voltage at pin 18 is equal to and tracks the voltage at pin 17 due to the high gain of the internal reference amplifier. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting $V_{REF}$ or pin 17. The negative common-mode range of the reference amplifier is given by: $V_{CM}-$ = V− plus ($I_{REF} \times 2k\Omega$) plus 2V. The positive common-mode range is V+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between $I_{REF}$ and $I_{FS}$ will eliminate the need for trimming $I_{REF}$. If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

### MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between $I_{FS}$ and $I_{REF}$ over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of $I_{REF}$ from 100μA to 2mA.

### REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V−. The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0kΩ, minimum values of $C_C$ are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of $C_C$ for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small $C_C$ values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1kΩ and $C_C$ = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF}$ = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF}$ = 0) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200Ω and $C_C$ = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of $R_{IN}$ and $V_{IN}$ values.

### LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 2k\Omega$) plus 3V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, $V_{LC}$). The appropriate graph shows the relationship between $V_{LC}$ and $V_{TH}$ over the temperature range, with $V_{TH}$ nominally 1.4V above $V_{LC}$. For TTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF}$ = 1mA is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1.1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

## ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing $I_{FS}$; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

## POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1$mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −9V with $I_{REF}$ = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain within acceptable limits.

## TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-10 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

## SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at $I_{REF}$ = 2mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 130ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for $I_{REF}$ values down to 1mA, with gradual increases for lower $I_{REF}$ values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 4kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a 4kΩ load with less than 5pF of parasitic capacitance at the measurement node. At $I_{REF}$ values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 0111111111 to 1000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of $I_{REF}$.

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and $V_{LC}$ terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.