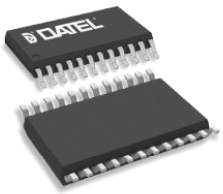
DAC-1025

10-Bit, 250MSPS, Low-Power D/A Converters



FEATURES

- 10-Bit resolution
- 250MSPS conversion rate
- 2mA -20mA output current
- Operates from single +2.7 to +3.6 Volt supply
- Low power, 120mW
- Internal +1.24 Volt reference - optional external reference
- Outstanding dynamic performance
- Guaranteed monotonicity
- Humidity and stress resistant ceramic LCC package for -QL and /883 models
- -40°C to +105°C and -55°C to +125°C operating temperature ranges
- 100% testing over temperature
- High-Rel process flow, burn-in, environmental, lot and ATE traceability
- 28 pin TSSOP package (SE, SM)
- Pb-free RoHS compliant

PRODUCT OVERVIEW

The 10-Bit DAC-1025 is one in a series of high speed pin to pin compatible 10 to 10 bit D/A's from DATEL. This D/A converter offers up to 250MSPS conversion rate from a segmented current source topology that is built on an advanced CMOS process and delivers a low glitch energy output of 2mA to 20mA.

This series is offered in either a small 28-pin TSSOP or a fully hermetic sealed ceramic LCC package. The hermetic package, offered for the –QL and /883 versions, protects the IC from the effects of moisture making the precision DC characteristics of the DAC more stable in environments where humidity is a concern. In addition, the LCC package isolates the IC from the stresses that may occur on the printed circuit board caused by variations in temperature.

The DAC-1025 operates from a single +3 Volt supply and contains a precision internal 1.24 Volt reference with ±40PPM/°C drift coefficient with the option to use an external reference. Excellent dynamic performance, a power saving "sleep-mode" feature as well as edge-triggered LVCMOS input latches makes the TSSOP version of this family pin-to-pin compatible with several industry DACs.

DATEL offers these converters fully tested over temperature with ATE results recorded and stored for the operating temperature ranges of -40°C to +105°C (Enhanced) or –55°C to +125°C (military). Burn-in and environmental screening are also available.

Products are offered in military temperature grades as well as fully screened High-Reliability -QL and /883 models.

APPLICATIONS

- MIL-STD/883 systems
- Defense/ aerospace applications
- Signal reconstruction
- High resolution imaging
- Cellular base stations
- Scientific test instruments

INPUT/ OUTPUT DESCRIPTIONS / BLOCK DIAGRAM

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	CLK
2	BIT 2	27	DVDD
3	BIT 3	26	DGND
4	BIT 4	25	NC
5	BIT 5	24	AVDD
6	BIT 6	23	COMP
7	BIT 7	22	IOUTA
8	BIT 8	21	IOUTB
9	BIT 9	20	AGND
10	BIT 10 (LSB)	19	NC
11	DGND	18	GAINADJ
12	DGND	17	REFI/O
13	DGND	16	REFSEL
14	DGND	15	SHTDWN

*Pinout applies to TSSOP package

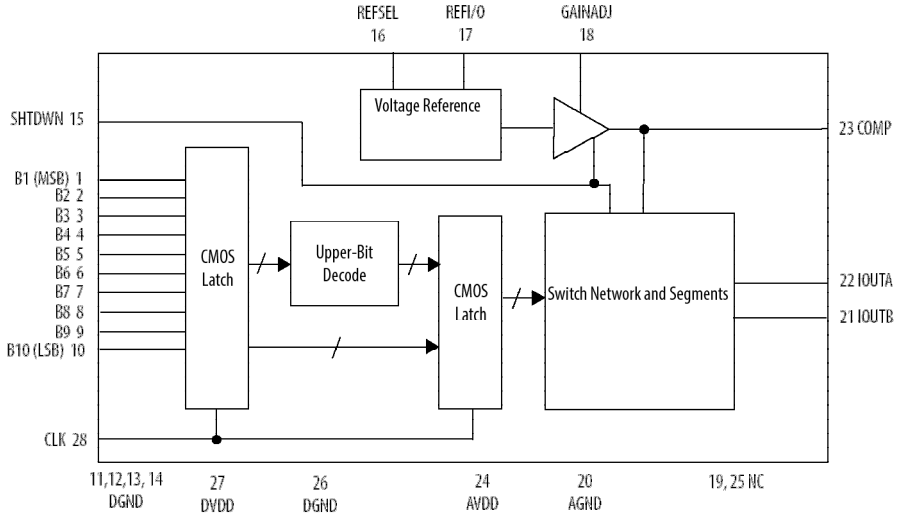


Figure 1. DAC-1025 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
DV_{DD} to DGND (Pins 27/26)	3.6	Volts
AV_{DD} to AGND (Pins 24/20)	3.6	Volts
AGND to DGND (Pins 20/26)	-0.3 to +0.3	Volts
Digital Inputs (Pins 1-14, 15, 28)	DV_{DD} to DV_{DD}+0.3	Volts
Reference Input Voltage Range (Pin 17)	AV_{DD} + 0.3	Volts
Analog Output Current (21,22)	24	mA

Note:
1. Exceeding specifications listed in Absolute Maximum Ratings may cause permanent damage to the device.
2. θja is measured with device soldered to a PCB in still air.

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temperature Range, Case				
E - suffix	–40	—	+85	°C
M, -QL, /883 - suffix	–55	—	+125	°C
Thermal Impedance				
θja - TSSOP package	—	110	—	°C/Watt
θja - CLCC package	—		—	°C/Watt
Maximum Junction Temperature			+150	°C
Storage Temperature Range	–65	—	+150	°C
Maximum Lead Temperature 10s (SOIC lead tips only)			+300	°C

FUNCTIONAL SPECIFICATIONS [1]

(Typical at +25°C, AV_{DD} = DV_{DD} = 3.3V , V_{REF} = Internal, I_{OUT} = 20mA unless otherwise specified.)

DIGITAL INPUT	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Resolution		10			
Logic Levels					
Logic "1"	DV_{DD} = +3.3V	2.3	3.3		Volts
Logic "0"	DV_{DD} = +3.3V		0	1	Volts
Input Current HI		-20		20	µA
Input Current LO		-20		20	µA
SHTDWN Input Current		-27		27	µA
Digital Input Capacitance			6		pf
STATIC PERFORMANCE					
Full Scale Output Current		2		20	mA
Differential Linearity		-0.5	±0.25	+0.5	LSB
Integral Nonlinearity	Best Fit Method	-0.5	±0.25	+0.5	LSB
Offset Error		-0.0075	±0.005	+ 0.0075	% FSR
Offset Tempco			0.1		ppm FSR/°C
Gain Error[2]	Internal Reference	-3	±0.75	+3	% FSR
Gain Error[2]	External Reference	-3	±0.75	+3	% FSR
Gain Tempco	Internal Reference		±95		ppm FSR/°C
Gain Tempco	External Reference		±45		ppm FSR/°C
Output Compliance Voltage		-1.00		1.25	Volts
Output Capacitance			10		pf
DYNAMIC PERFORMANCE					
Conversion Rate		250	290		MHz
Output Rise Time	Full Scale Step		1.5		ns
Output Fall Time	Full Scale Step		1.5		ns
Output Noise	Iout = 2mA		28		pA/√Hz
Output Noise	Iout = 20mA		50		pA/√Hz
Spurious Free Dynamic Range[3] (within a window, AV_{DD} = +3.3V DV_{DD} = +3.3V)					
Fout = 20.1MHz, Fclk = 125MHz	20MHz Span		85		dBc
Fout = 40.1MHz, Fclk = 250MHz	30MHz Span		82		dBc
Fout = 80.1MHz, Fclk = 250MHz	30MHz Span		72		dBc
Spurious Free Dynamic Range[3] (up to Nyquist, AV_{DD} = +3.3V, DV_{DD} = +3.3V)					
Fout = 10.1MHz, Fclk = 62.5MHz	Up to Nyquist		74		dBc
Fout = 20.1MHz, Fclk = 62.5MHz	Up to Nyquist		69		dBc
Fout = 30.1MHz, Fclk = 62.5MHz	Up to Nyquist		67		dBc
Fout = 10.1MHz, Fclk = 125MHz	Up to Nyquist		76		dBc
Fout = 20.1MHz, Fclk = 125MHz	Up to Nyquist		70		dBc
Fout = 30.1MHz, Fclk = 125MHz,	Up to Nyquist		67		dBc
Fout = 40.1MHz, Fclk = 125MHz,	Up to Nyquist		64		dBc
Fout = 50.1MHz, Fclk = 125MHz,	Up to Nyquist		60		dBc
Fout = 10.1MHz, Fclk = 250MHz,	Up to Nyquist		72		dBc
Fout = 20.1MHz, Fclk = 250MHz,	Up to Nyquist		64		dBc
Fout = 40.1MHz, Fclk = 250MHz,	Up to Nyquist		62		dBc
Fout = 80.1MHz, Fclk = 250MHz,	Up to Nyquist		50		dBc

DYNAMIC PERFORMANCE (CONT.)					
Multi-Tone Power Ratio (8 Tones, AV_{DD} = +3.3V, DV_{DD} = +3.3V)					
Fout=18.1MHz to 29.1MHz, Fclk = 125 MHz	Tones shifted 1.1MHz		71		dBc
Fout=29.1MHz to 46.1MHz, Fclk=250 MHz	Tones shifted 2.1MHz		65		dBc
Total Harmonic Distortion (AV_{DD} = +3.3V, DV_{DD} = +3.3V)					
Fout = 10.1MHz, Fclk = 250MHz	Up to Nyquist		-70		dBc
Fout = 10.1MHz, Fclk = 125MHz	Up to Nyquist		-72		dBc
Fout = 10.1MHz, Fclk = 62.5MHz	Up to Nyquist		-75		dBc
TIMING CHARACTERISTICS					
Data Setup Time (tsu)			1.5		ns
Data Hold Time (thld)			1.3		ns
Propagation Delay Time (tpd)			2.3		ns
Clock (CLK) Pulse Width HI (t_{PH})		2			ns
Clock (CLK) Pulse Width LO (t_{PL})		2			ns
CLK to Iout Delay (t_{OUT})		1/Fclk			
POWER REQUIREMENTS					
Power Supply Ranges[4]					
AV_{DD}		2.7	3	3.6	Volts
DV_{DD}		2.7	3	3.6	Volts
Power Supply Currents					
AV_{DD} (2.7V to 3.6V)	I_{OUT} = 20mA		26	30	mA
AV_{DD} (2.7V to 3.6V)	I_{OUT} = 2mA		9	15	mA
DV_{DD}	3.3V		5	10	mA
AV_{DD} Shut-Down Mode	3.3V		2		mA
Power Dissipation	3.3V, I_{OUT} = 2mA		50	60	mW
Power Dissipation	3.3V, I_{OUT} = 20mA		100	125	mW
Power Supply Rejection Ratio		-0.125		+0.125	% FSR/V
REFERENCE					
Internal Reference Voltage		1.2	1.24	1.28	Volts
Reference Voltage Drift				±40	ppm/°C
Reference Current Sink/Source			50		µA
Reference Input Impedance			1		MΩ
Reference Input Mutiplying Bandwidth			1.2		MHz

NOTES

1. See Glossary of Specifications
2. Gain Error specified as ratio of output current to current through Rset (pin 18). Ideal ratio = 31.969.
3. Spectrum Analysis using differential coupled transformer; no external filter.
4. Reduced dynamic performance may result from operating with supply voltage < 3.0V. In such cases 2mA output current is recommended.

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TECHNICAL NOTES

Theory of Operation

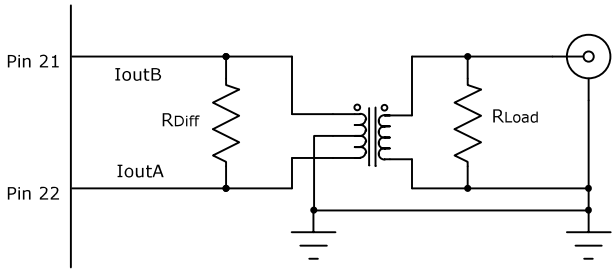
The DAC-1025 is a 10-Bit, 20mA current output, CMOS, digital to analog converter with a maximum conversion rate of 250MSPS and a recommended power supply range of +3.0 to +3.6 Volts . The design topology incorporates segmented current source circuitry with the five upper bits being comprised of 31 major current sources of equivalent current and the remaining lower bits comprised of binary weighted current sources. In earlier D/A design approaches the converter had substantially larger amounts of current turning on and off at major code transitions such as ¼, ½, and ¾ of the full scale range. The reduction of current switching at these major transitions significantly reduces the overall transient glitch of the converter thereby improving output settling times and transient spikes that directly affect spurious free dynamic range and signal to noise ratio.

Output Current

IOUTA and IOUTB of the DAC-1025 provide complementary output current. The sum of IOUTA and IOUTB is always equal to the full scale output current minus one LSB. For single-ended applications, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be terminated with an equivalent value resistance or connected to AGND. The voltage developed at the output must not exceed the output voltage compliance range (see specifications). The termination resistor is chosen to produce the desired output voltage:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were attained using a 1:1 transformer on the output of the DAC (see Figure 2). With the center tap grounded, the output swing of pins 21 and 22 will be biased at zero volts. It is important to note here that the output compliance specification of the device not be violated with this configuration. The loading as shown in Figure 2 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA.



Vout = 2 x Iout x Requivalent.

Figure 2

Voltage Reference

The internal +1.24V voltage reference of the device has a drift specification of ±40 ppm/°C over the operating temperature range. It is recommended that a bypass capacitor be placed as close as possible to the REFI/O pin and bypassed to AGND. The REFSEL (pin 16) selects whether an internal or external reference is used.. The internal reference can be selected if pin 16 is tied to AGND. If an external reference is desired, then pin 16 should be tied to A_{VDD}, with the external reference being driven into REFI/O, pin 17.

The full scale output current of the converter is a function of both the reference voltage and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range. Signal to noise as well as SFDR performance may degrade slightly when operating with a low full scale output of 2mA. If the internal reference is used, the voltage at GAINADJ ($V_{GAINADJ}$), pin 18, will equal approximately 1.2 Volts. If an external reference is used, the voltage at GAINADJ will equal the external reference.

I_{OUT} Full Scale can be calculated as:

$$I_{OUT}\ FS = (V_{GAINADJ}/R_{SET}) \times 32$$

If the full scale output current is set to 20mA, by using the internal voltage reference (1.2V) and a 1.91kΩ R_{SET} resistor, then the input to output transfer function will be according to the following table.

INPUT CODE / IOUT		
INPUT CODE (B1 - B14)	IOUTA (mA)	IOUTB (mA)
11 1111 1111	20	0
00 0000 0000	10	10
00 0000 0000	0	20

Digital Inputs / Propogation Delay

The DAC-1025 digital inputs are specified to 3V LVMOS logic levels. Proper termination should be implemented to minimize line reflection. A 50Ω resistor located close to the device and terminated at the DGND ground plane should be used if driving the digital inputs from a length of more than several inches.

The DAC requires two rising edge CLK commands to produce the analog output. The rising edge of the N^{th} CLK signal stores the 10 bit input word in the LVCMOS input registers. The subsequent N+1 rising edge CLK command completes the conversion process bringing out the N^{th} output for IOUTA and IOUTB.

Power Supplies

To maintain optimal SFDR and SNR performance it is recommended that separate supplies ranging between +3.0V to +3.6V are used for A_{VDD} and D_{VDD}. The DAC-1025 is capable of operating with supplies as low as +2.7V but the SFDR performance may be degraded. Reducing the full scale output current to 2mA could improve this parameter. To minimize power supply noise, 0.1uF capacitors should be placed as close as possible to the converter's power supply pins, AVDD and DVDD. Be assured that capacitors are bypassed to their proper AGND or DGND planes.

Ground Planes

It is recommended that separate AGND and DGND ground planes be used. These two planes should may be connected at the DAC, however, the optimal connection location of the two planes may be system dependent. If separate DGND and AGND planes are used, all of the digital components and switching signals should be located over the DGND and all critical analog components and signals located over the AGND plane. In addition, a signal ground can be employed for all low current signal path grounding.

TECHNICAL NOTES

Humidity Susceptibility

Plastic mold compounds that are used to house ICs can absorb moisture. When these devices are exposed to humidity the plastic package can undergo slight changes that can apply pressure to the internal die. Stresses placed on a precision data converters can cause changes in its performance in the order of 100ppm. The fully hermetic package offered for the –QL and /883 versions are not affected by humidity, and are therefore more stable in environments where humidity is a concern.

Board Mounting Considerations

For applications requiring the highest accuracy, attention should be paid to the board mounting location of SE and SM devices. These models use a plastic TSSOP package that could subject the die to mild stresses when the printed circuit board is cooled or heated. Placing the device in areas subject to slight twisting may cause die stresses and consequently degradation in the accuracy of the converter. It is preferred that the device be placed in the center of the PCB or near the edge of the shortest side where stresses due to flexing are reduced. Mounting the device in a cutout also minimizes flex. Mounting the device on an extremely thin PCB or flexprint will increase the potential for loss of accuracy due to stress. The CLCC package offered for -QL and /883 devices eliminates the potential for die stress.

Board Assembly Considerations

Precision converters provide high accuracy over temperature extremes, but some PC board assembly precautions are necessary. Changes in DC parameters can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

PIN DESCRIPTIONS

PIN	PIN NAME	DESCRIPTION
1 -10	BIT 1 (MSB) through B10 (LSB)	Digital Data input bits. B1 (MSB), B10 (LSB).
11, 12, 13,14	DGND	Digital Ground
19,25	NC	No Connection. For noise rejection may be tied to AGND.
15	SHTDWN	Control pin to power-down the DAC. Sleep = HI, On = LO. Internal 20µA active pull-down current.
16	REFSEL	Connect to AGND to enable internal 1.24V reference. Connect to AVDD to disable internal reference.
17	REFI/O	Reference voltage output when using internal 1.24V reference Input pin when supplying external reference.
18	GAINADJ	Full Scale current adjustment (gain). Use resistor to AGND to set current (see technical notes).
23	COMP	External capacitor to AGND helps to reduce bandwidth.
20	AGND	Analog Ground
21	IOUTB	Complimentary output current. Full scale is attained when digital inputs are at all 0's.
22	IOUTA	True output current. Full scale is attained when digital inputs are at all 1's.
24	AVDD	Supply for analog circuitry+2.7V to +3.6V (+3.0V to +3.6V recommended).
26	DGND	Digital Ground
27	DVDD	Supply for digital circuitry +2.7V to +3.6V
28	CLK	Rising edge of clock latches data into input registers

GLOSSARY OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTERNAL REFERENCE VOLTAGE DRIFT: The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

OUTPUT COMPLIANCE RANGE: The allowable Maximum Voltage at the output of a D/A.

OFFSET ERROR: The deviation from the ideal at analog zero output

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

POWER SUPPLY REJECTION RATIO (PSRR): The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

REFERENCE INPUT MULTIPLYING BANDWIDTH: The -3dB reduction in the output when applying a sinusoidal voltage to the external reference (digital inputs are set to all 1s). The frequency is increased until the amplitude of the output waveform is -3dB of its original value.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and D/A converters.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the first 5 harmonics to the rms of the fundamental signal, usually expressed in dB

GLITCH AREA: The transient appearing at the output when the input switches from one code to another. Typically the worst case is found at the MSB code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification.

SPURIOUS FREE DYNAMIC RANGE (SFDR): The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

Typical Connection Diagram / Input Output Connections

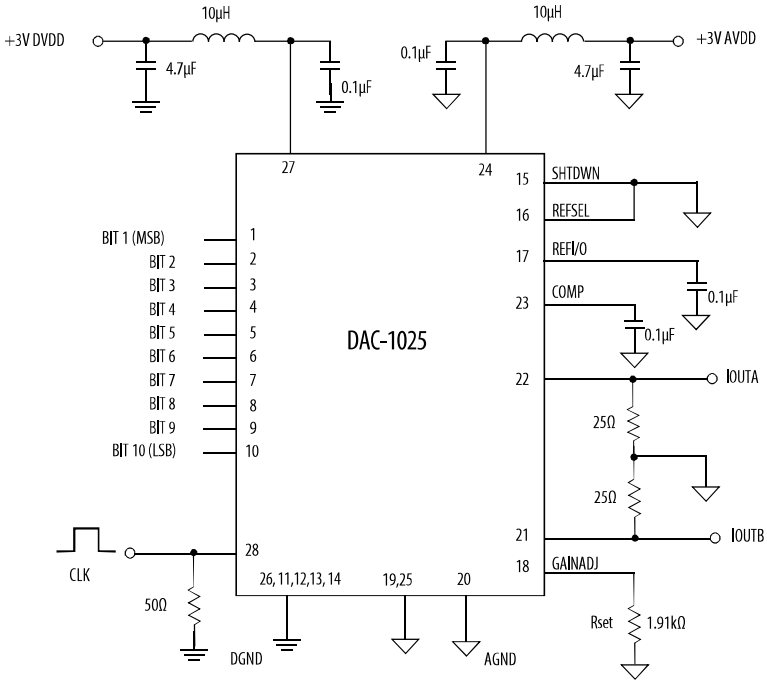


Figure 3. Typical Connection Diagram

Timing Diagram

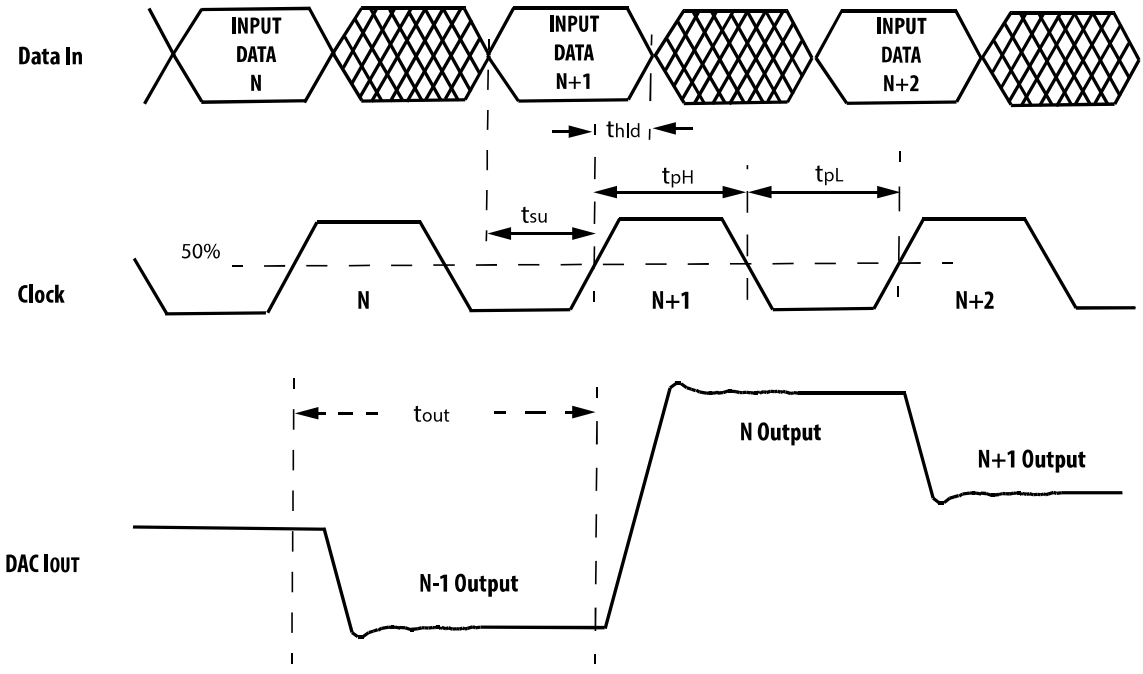
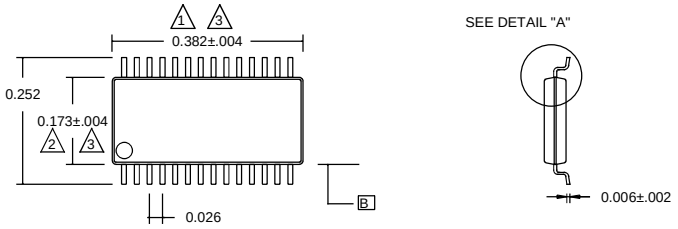
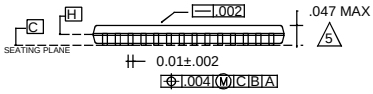
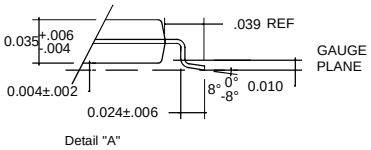


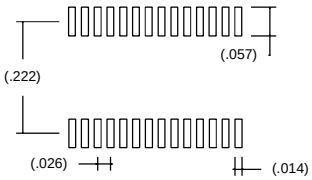
Figure 4. Timing / Settling Diagram

MECHANICAL DIMENSIONS - INCHES (mm)









1. Dimension does not include mold flash, protrusions or gate burrs
   Mold flash, protrusions or gate burrs shall not exceed 0.006 per side
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.010 per side
3. Dimension are measured at datum plane H

   Dimension and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.003in total in excess of dimension at maximun material condition. Minimum space between protrusion and adjacent lead is 0.003in.

   Dimensions in ( ) are for reference only

   Conforms to JEDEC MO-153

ORDERING INFORMATION

ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE (°C)	PACKAGE	SHIPPING
DAC-1025SE	-40 to +105	28 Pin TSSOP	Tube
DAC-1025SM	-55 to +125	28 Pin TSSOP	Tube
DAC-1025-QL	-55 to +125	Ceramic LCC	Tray
DAC-1025/883	-55 to +125	Ceramic LCC	Tray