

FEATURES

- 10-bit resolution
- 125MSPS conversion rate
- 34 ns settling time to 1/2 LSB
- Operates from single +3V to +5V supply
- Humidity and stress resistant ceramic LCC package for -QL and /883 models
- -40°C to +105°C and -55°C to +125°C operating temperature ranges
- 100% testing over temperature
- High-Rel process flow, burn-in, environmental, lot and ATE traceability
- Low power, 165mW (5V supply) 75mW (+3V supply)
- Internal +1.2V temperature compensated bandgap reference with an external reference option
- Outstanding dynamic performance
- Guaranteed monotonicity over temperature
- ± 0.5 LSB Differential Non-Linearity (Max) over temperature
- ± 1 LSB Integral Non-Linearity (Max) over temperature
- TSSOP package (SE, SM models), Pb-free RoHS compliant

PRODUCT OVERVIEW

The 10-bit DAC-1012 is one in a series of high speed pin to pin compatible 8 to 14 bit D/A's from DATEL. This D/A converter offers up to 125MSPS conversion rate from a segmented current source topology that is built on an advanced CMOS process and delivers a low glitch energy output of 2mA to 20mA.

This series is offered in either a small 28-pin TSSOP or a fully hermetic sealed ceramic LCC package. The hermetic package, offered for the -QL and /883 versions, protects the IC from the effects of moisture making the precision DC characteristics of the DAC more stable in environments where humidity is a concern. In addition, the LCC package isolates the IC from the stresses that may occur on the printed circuit board caused by variations in temperature.

The DAC-1012 operates from a single +3V to +5V supply and

contains a precision internal 1.2V temperature compensated bandgap voltage reference, external reference option, edge-triggered CMOS input latches and a power-down "sleep" mode. This converter provides excellent dynamic performance making it ideal for applications such as signal reconstruction, high-resolution imaging, cellular base-stations, and medical/test instruments.

DATEL offers these converters fully tested over temperature with ATE results recorded and stored for the operating temperature ranges of -40°C to +105°C (Enhanced) or -55°C to +125°C (military). Burn-in and environmental screening are also available.

Products are offered in military temperature grades as well as fully screened High-Reliability -QL and /883 models.

APPLICATIONS

- MIL-STD/883 systems
- Defense/ aerospace applications
- Signal reconstruction
- High resolution imaging
- Cellular base stations
- Scientific test instruments

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	CLK
2	BIT 2	27	DVDD
3	BIT 3	26	DGND
4	BIT 4	25	NC
5	BIT 5	24	AVDD
6	BIT 6	23	NC
7	BIT 7	22	IOUTA
8	BIT 8	21	IOUTB
9	BIT 9	20	AGND
10	BIT 10 (LSB)	19	COMP
11	NC	18	GAINADJ
12	NC	17	REFI/O
13	NC	16	REFSEL
14	NC	15	SHTDWN

*Pinout TSSOP package

BLOCK DIAGRAM

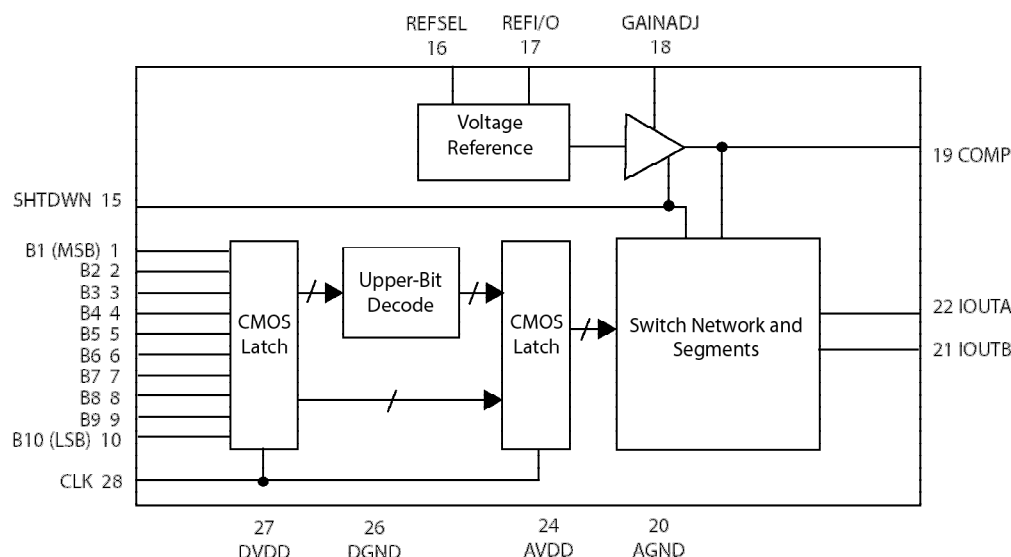


Figure 1. DAC-1012 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
DVDD to DGND (Pins 27/26)	+5.5	Volts
AVDD to AGND (Pins 24/20)	+5.5	Volts
AGND to DGND (Pins 20/26)	-0.3 to +0.3	Volts
Digital Inputs (Pins 1-10, 15,28)	DVDD to DVDD+0.3	Volts
Reference Output Current (Pin 17)	±50μA	Volts
Analog Output Current (21,22)	24mA	°C

Note:

- Exceeding specifications listed in Absolute Maximum Ratings may cause permanent damage to the device.
- θja is measured with device soldered to a PCB in still air.

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
C - suffix	0	—	+70	°C
E - suffix	-40	—	+85	°C
M, QL, 883 - suffix	-55	—	+125	°C
Thermal Impedance				
θja - SOIC package	—	75	—	°C/Watt
θja - TSSOP package	—	135	—	°C/Watt
Maximum Junction Temperature			+150	°C
Storage Temperature Range	-65	—	+150	°C
Maximum Lead Temperature 10s (SOIC lead tips only)			+300	°C

FUNCTIONAL SPECIFICATIONS ¹

(Typical at +25°C, AVDD = DVDD = +5V, VREF = Internal, IOUT full scale = 20mA unless otherwise specified.)

DIGITAL INPUT	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Resolution		10			
Logic Levels					
Logic "1"	DVDD = +5V	3.5	5		Volts
Logic "1"	DVDD = +3V	2.1	3		Volts
Logic "0"	DVDD = +5V		0	1.3	Volts
Logic "0"	DVDD = +3V		0	0.9	Volts
Input Current HI		-10		+10	μA
Input Current LO		-10		+10	μA
SHTDWN Input Current		-27		+27	μA
Digital Input Capacitance			3		pf
STATIC PERFORMANCE					
Full Scale Output Current		2		20	mA
Differential Nonlinearity		-0.5	±0.25	+0.5	LSB
Integral Nonlinearity	Best Fit Method	-1	±0.5	+1	LSB
Offset Error		-0.025		+0.025	% FSR
Offset Tempco			0.1		ppm FSR/°C
Gain Error ²	Internal Reference	-10	±0.8	+10	% FSR
Gain Error ²	External Reference	-10	±1.5	+10	% FSR
Gain Tempco	Internal Reference		±95		ppm FSR/°C
Gain Tempco	External Reference		±45		ppm FSR/°C
Output Compliance Voltage		-0.3		1.25	Volts
DYNAMIC PERFORMANCE					
Conversion Rate		125			MHz
Output Settling Time	0.1% FSR (±1/2 LSB)		34		ns
Output Settling Time	0.2% FSR (±1 LSB)		22		ns
Glitch Area	RL = 25Ω		5		pV/s
Output Rise Time	Full Scale Step		1.1		ns
Output Fall Time	Full Scale Step		1.6		ns
Output Noise	Iout = 2mA		30		pA/√Hz
Output Noise	Iout = 20mA		50		pA/√Hz
Total Harmonic Distortion ⁵					
Fout = 2.0MHz, Fclk = 100MHz	Up to Nyquist		-71		dBc
Fout = 2.0MHz, Fclk = 50MHz	Up to Nyquist		-72		dBc
Fout = 1.0MHz, Fclk = 50MHz	Up to Nyquist		-76		dBc
Spurious Free Dynamic Range ⁶ (within a window)					
Fout = 33.1MHz, Fclk = 125MHz	10MHz Span		76		dBc
Fout = 5.02MHz, Fclk = 100MHz	4MHz Span		76		dBc
Fout = 10.1MHz, Fclk = 60MHz	10MHz Span		75		dBc
Fout = 5.01MHz, Fclk = 50MHz	2MHz Span		76		dBc
Fout = 1.0MHz, Fclk = 50MHz	2MHz Span		78		dBc
Spurious Free Dynamic Range ⁶ (up to Nyquist)					
Fout = 33.1MHz, Fclk = 125MHz			55		dBc
Fout = 10.1MHz, Fclk = 125MHz			65		dBc
Fout = 40.2MHz, Fclk = 100MHz			53		dBc
Fout = 20.1MHz, Fclk = 100MHz			60		dBc

DYNAMIC PERFORMANCE (Cont.)	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Spurious Free Dynamic Range ⁶ (up to Nyquist) (cont.)					
Fout = 2.51MHz, Fclk = 100MHz			74		dBc
Fout = 20.2MHz, Fclk = 60MHz			57		dBc
Fout = 10.1MHz, Fclk = 60MHz			63		dBc
Fout = 20.1MHz, Fclk = 50MHz			56		dBc
Fout = 2.52MHz, Fclk = 50MHz			73		dBc
Fout = 1.00MHz, Fclk = 50MHz			74		dBc
Fout = 5.01MHz, Fclk = 50MHz			67		dBc
Fout = 5.01MHz, Fclk = 25MHz			71		dBc
REFERENCE					
Internal Reference Voltage		1.04	1.16	1.28	Volts
Reference Voltage Drift			±58		ppm/°C
Reference Current Sink/Source			0.1		μA
Reference Input Impedance			1		MΩ
Reference Input Multiplying Bandwidth			1.4		MHz
TIMING CHARACTERISTICS					
Data Setup Time ⁷ (tsu)		3			ns
Data Hold Time ⁷ (thd)		3			ns
Propagation Delay Time ⁷ (tpd)			1		ns
Clock (CLK) Pulse Width HI ⁷		4			ns
Clock (CLK) Pulse Width LO ⁷		4			ns
POWER REQUIREMENTS					
Power Supply Ranges					
AVDD ³		2.7	5.0	5.5	Volts
DVDD ³		2.7	5.0	5.5	Volts
Power Supply Currents					
AVDD ⁴ (3V to 5V)	IOUT = 20mA		22	30	mA
AVDD ⁴ (3V to 5V)	IOUT = 2mA		5		mA
DVDD ⁴	5V		3	5	mA
DVDD ⁴	3V		1.5		mA
AVDD Shut-Down Mode	3V or 5V		1.6	3	mA
Power Dissipation	5V, IOUT = 2mA ⁴		70		mW
	5V, IOUT = 20mA ⁴		164		mW
	3V, IOUT = 2mA ⁴		28		mW
	3V, IOUT = 20mA ⁴		86		mW
Power Supply Rejection Ratio		-0.2		+0.2	% FSR/V

- See Glossary of Specifications
- Gain Error specified as ratio of output current to current through Rset (pin 18). Ideal ratio = 31.969.
- For optimal performance, when operating with supply voltages below 3V IOUT should be less than 12mA.
- fclock = 100MHz, fout = 39MHz.
- Spectrum Analysis using differential coupled transformer.
- fclk = 50MHz, fout = 2MHz
- See Figure 4

TECHNICAL NOTES

Theory of Operation

The DAC-1012 is a 10-bit, 20mA current output, CMOS, digital to analog converter. The maximum conversion rate is 125MSPS with an operating power supply range of +3V to +5V. The design topology incorporates segmented current source circuitry that reduces transient glitches. The five upper bits are comprised of 31 major current sources of equivalent current. The remaining lower bits are comprised of binary weighted current sources. In the situation where an input waveform to the converter is ramped through all the codes from 0 to 1023, the five lower bit current sources would begin to count up. When they reached the transition of code 31 to code 32, the lower bits would all turn off and the first major current source would turn on. As the input continues to ramp up, the 5 lower bits will count up another 31 codes until the next major current source turns on and the five lower bits turn off. In earlier D/A architectures the converter had a substantially larger amount of current turning on and off at major code transitions such as $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{3}{4}$ scale of the full scale range. The reduction of current switching at these major transitions significantly reduces the overall glitch of the converter thereby improving output settling times and transient spikes.

Digital Inputs / Termination

The DAC-1012 digital inputs are specified to CMOS logic levels. However, lowering the supply voltage to 3V will reduce the logic threshold level and thereby provide TTL compatible inputs. The internal CMOS register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the inputs are driven from 50Ω drivers then 50Ω termination resistors should be located as close to the inputs and DGND as possible.

Voltage Reference

The internal +1.2V voltage reference of the device has a drift specification of ± 60 ppm/°C over the full temperature range. It is recommended that a bypass capacitor be placed as close as possible to the REF1/O pin, connected to AGND. The REFSEL (pin 16) selects whether an internal or external reference is used. The internal reference can be selected if pin 16 is tied low (AGND). If an external reference is desired, then pin 16 should be tied high (AVDD) and the external reference driven into REF1/O, pin 17. The full scale output current of the converter is a function of both the reference voltage and the value of RSET. IOUT should be within the 2mA to 20mA range. Performance may degrade at 2mA FS Iout.

If the internal reference is used, the voltage at GAINADJ (VGAINADJ) will equal approximately 1.16V (pin 18). If an external reference is used, the voltage at GAINADJ will equal the external reference. IOUT Full Scale can be calculated as:

$$IOUT\ FS = (VGAINADJ / RSET) \times 32$$

If the full scale output current is set to 20mA by using the internal voltage reference (1.16V) and a 1.86kΩ RSET resistor, then the input coding to output current vs input coding will be as follows:

INPUT CODE / IOUT		
INPUT CODE (B1 - B10)	IOUTA (mA)	IOUTB (mA)
11 1111 1111	20	0
10 0000 0000	10	10
00 0000 0000	0	20

Output Current

IOUTA and IOUTB provide complementary output current. The sum of IOUTA and IOUTB is always equal to the full scale output current minus one LSB. For single-ended applications, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be terminated with an equivalent value resistance or connected to AGND. The voltage developed at the output must not exceed the output voltage compliance range (see specifications). The termination resistor is chosen to produce the desired output voltage:

$$VOUT = IOUT \times RLOAD$$

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were attained using a 1:1 transformer on the output of the DAC (see Figure 2). With the center tap grounded, the output swing of pins 21 and 22 will be biased at zero volts. It is important to note here that the negative voltage output compliance range limit is -300mV, imposing a maximum of 600mVp-p amplitude with this configuration. The loading as shown in Figure 2 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA.

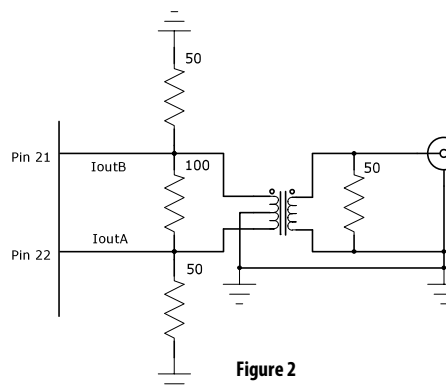


Figure 2

$$Vout = 2 \times Iout \times \text{Equivalent. (Equivalent. } \sim 12.5\Omega)$$

Ground Planes

If separate DGND and AGND planes are used, then all of the digital functions of the device and the corresponding components should be located over the DGND plane and terminated to the DGND plane. The same is true for the analog components and the AGND. If proper grounding practices are implemented the converter will function properly with a single common ground plane.

Supply Bypassing

To minimize power supply noise, 0.1μF capacitors should be placed as close as possible to the converter's power supply pins, AVDD and DVDD. Be assured that capacitors are bypassed to their proper AGND or DGND planes.

TECHNICAL NOTES

Humidity Susceptibility

Plastic mold compounds that are used to house ICs can absorb moisture. When these devices are exposed to humidity the plastic package can undergo slight changes that can apply pressure to the internal die. Stresses placed on a precision data converters can cause changes in its performance in the order of 100ppm. The fully hermetic package offered for the -QL and /883 versions are not affected by humidity, and are therefore more stable in environments where humidity is a concern.

Board Mounting Considerations

For applications requiring the highest accuracy, attention should be paid to the board mounting location of SE and SM devices. These models use a plastic TSSOP package that could subject the die to mild stresses when the printed circuit board is cooled or heated. Placing the device in areas subject to slight twisting may cause die stresses and consequently degradation in the accuracy of the converter. It is preferred that the device be placed in the center of the PCB or near the edge of the shortest side where stresses due to flexing are reduced. Mounting the device in a cutout also minimizes flex. Mounting the device on an extremely thin PCB or flexprint will increase the potential for loss of accuracy due to stress. The CLCC package offered for -QL and /883 devices eliminates the potential for die stress.

Board Assembly Considerations

Precision converters provide high accuracy over temperature extremes, but some PC board assembly precautions are necessary. Changes in DC parameters can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

Typical Connection Diagram

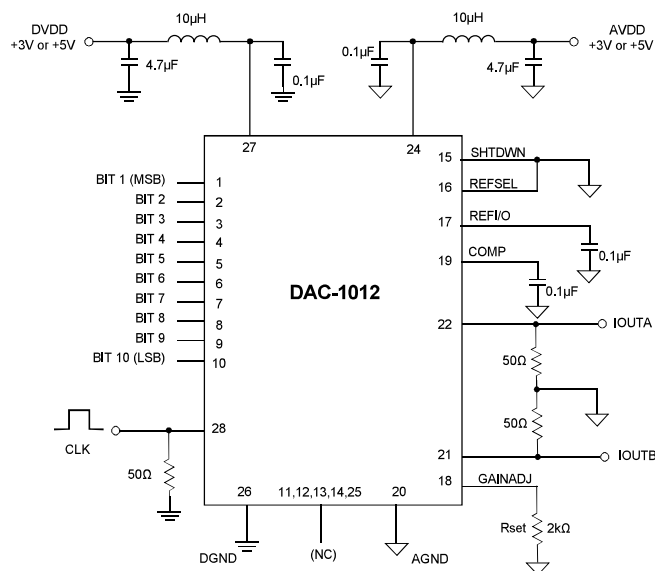


Figure 3. Typical Connection Diagram

Timing Diagram

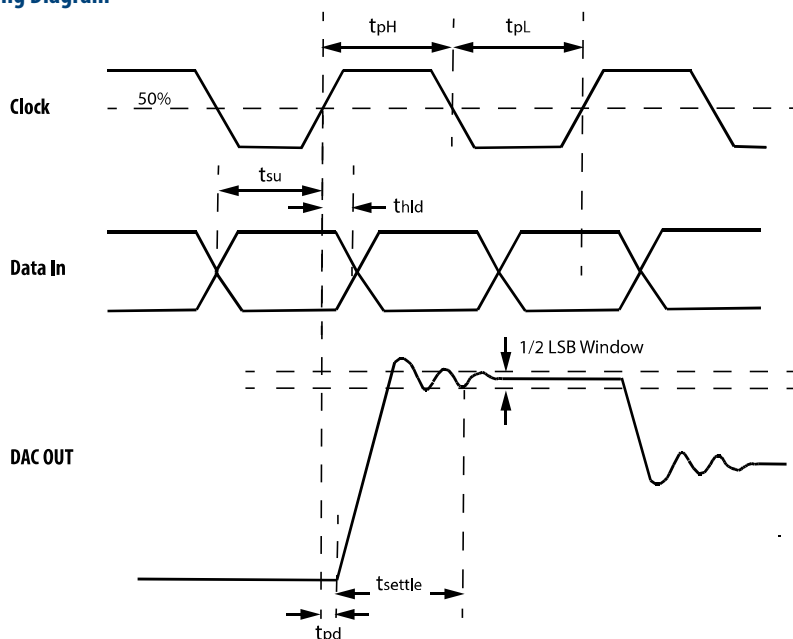


Figure 4. Timing / Settling Diagram

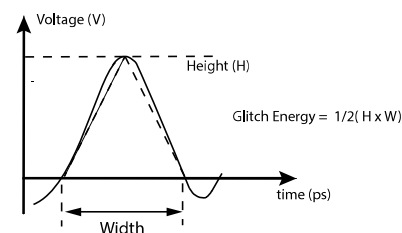


Figure 5. Peak Glitch Area

Typical Performance Curves: 5 Volt Supplies

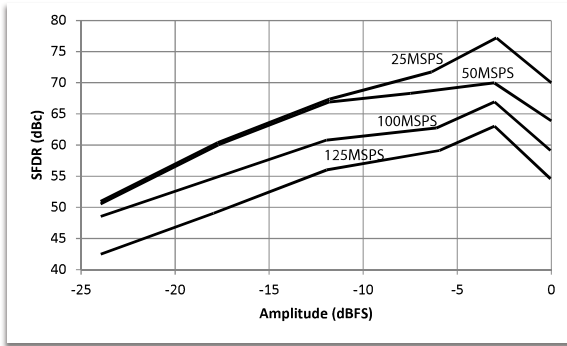


Figure 6b. SFDR vs Amplitude, $f_{clk} = 5 \times f_{out}$

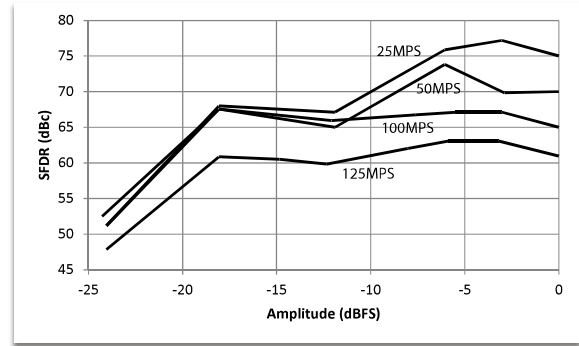


Figure 6a. SFDR vs Amplitude, $f_{clk} = 10 \times f_{out}$

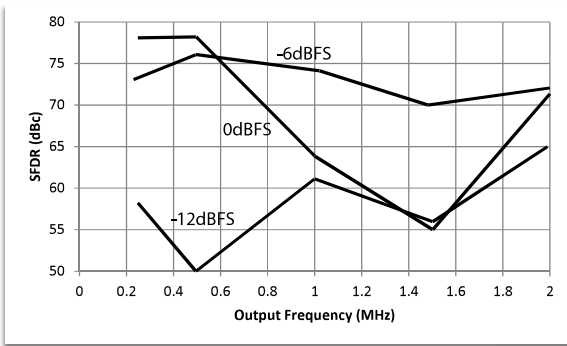


Figure 7a. SFDR vs f_{out} , $f_{clk} = 5\text{MHz}$

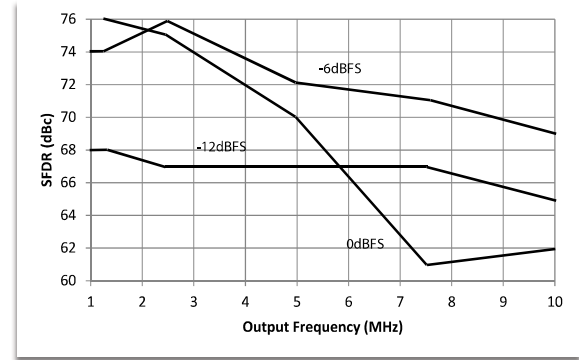


Figure 7b. SFDR vs f_{out} , $f_{clk} = 25\text{MHz}$

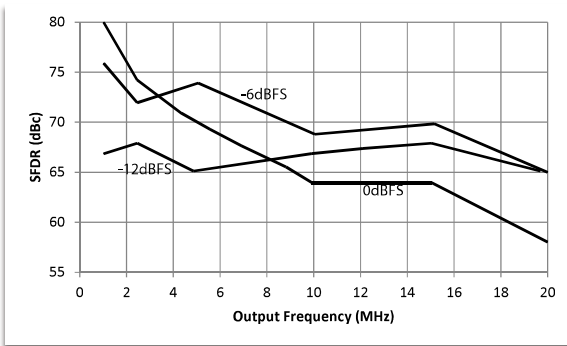


Figure 7c. SFDR vs f_{out} , $f_{clk} = 50\text{MHz}$

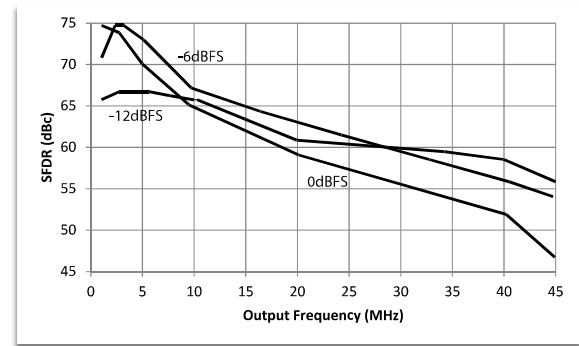


Figure 7d. SFDR vs f_{out} , $f_{clk} = 100\text{MHz}$

TECHNICAL NOTES

Typical Performance Curves: 5 Volt Supplies

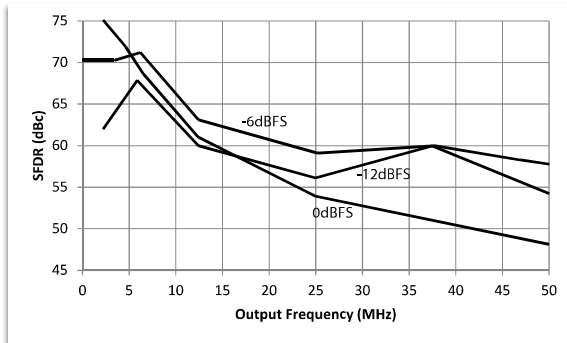


Figure 7e. SFDR vs f_{out} , $f_{clk}=125\text{MHz}$

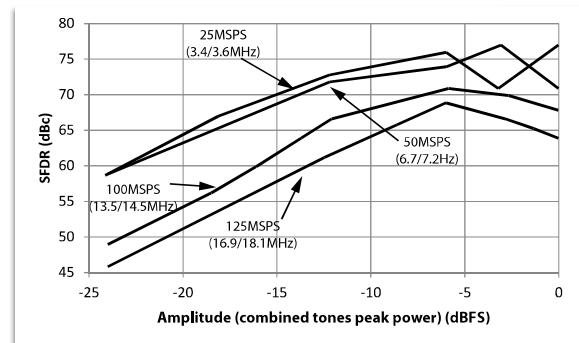


Figure 8. SFDR vs Amplitude of Two Tones, $f_{clk} = 7 \times f_{out}$

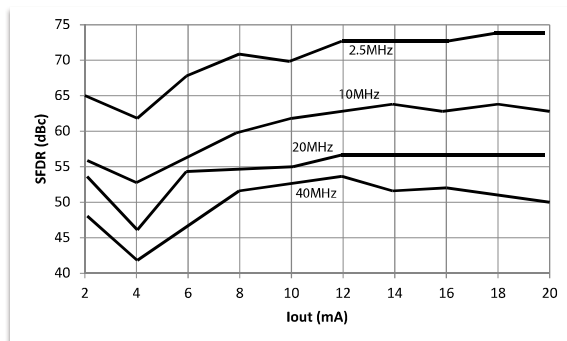


Figure 9. SFDR vs I_{out} , $f_{clk} = 100\text{MHz}$

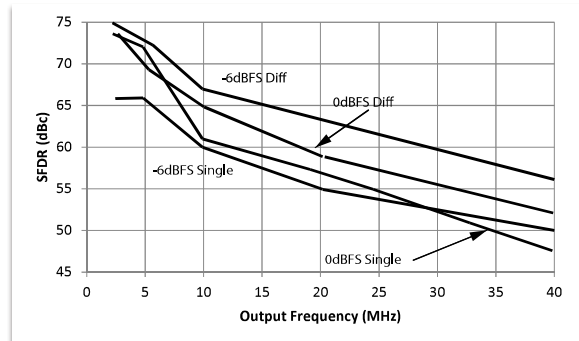


Figure 10. Differential vs Single-ended, $f_{clk} = 100\text{MHz}$

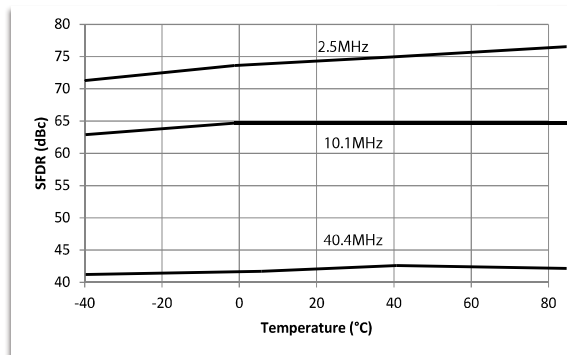


Figure 11. SFDR vs Temperature, $f_{clk} = 100\text{MHz}$

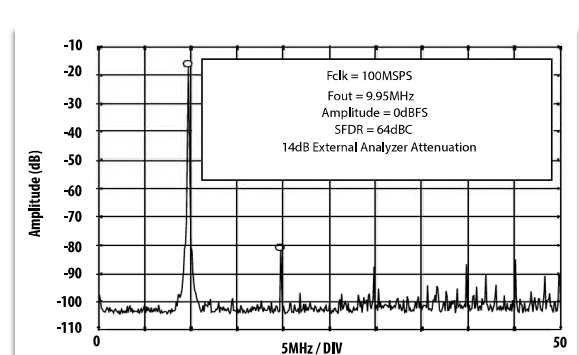


Figure 12. SFDR Single Tone, $f_{clk} = 100\text{MHz}$

Typical Performance Curves: 5 Volt Supplies

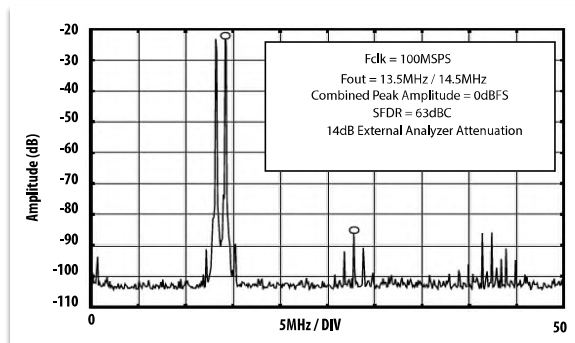


Figure 13. SFDR Two Tones, fclk=100MHz

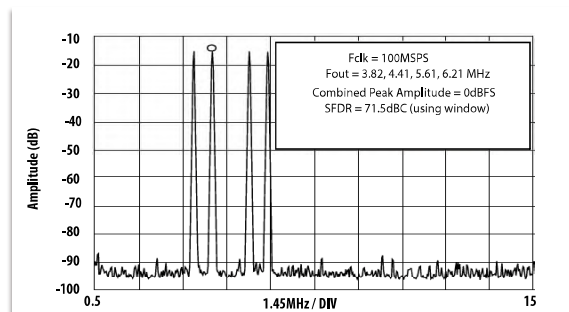


Figure 14. SFDR Four Tones, fclk = 100MHz

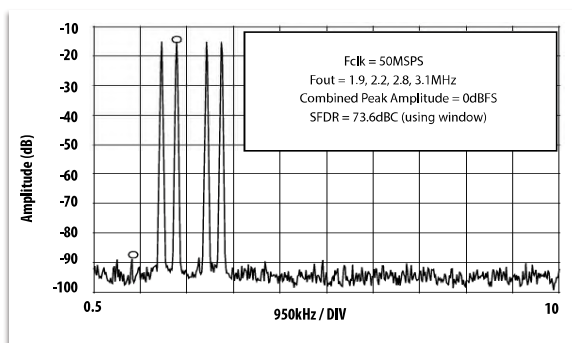


Figure 15. SFDR Four Tones, fclk = 50MHz

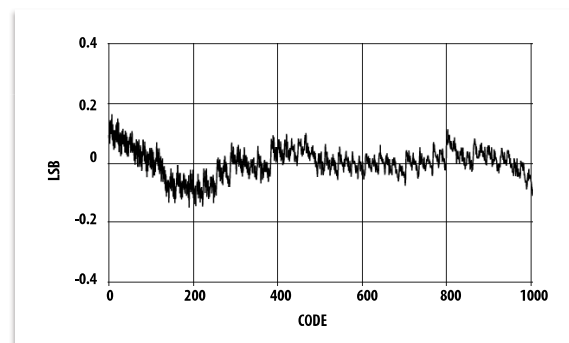


Figure 16. Integral Nonlinearity

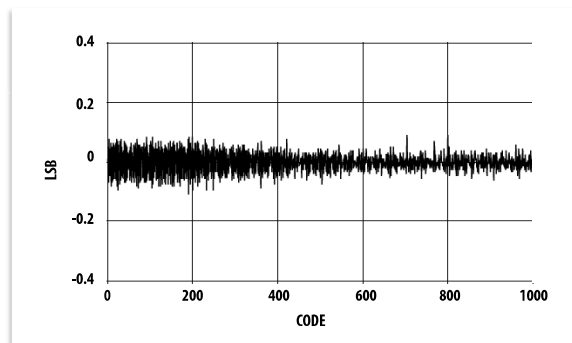


Figure 17. Differential Nonlinearity

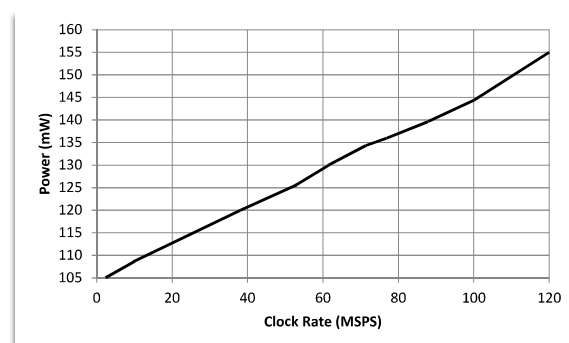


Figure 18. Power vs Clock rate, Iout = 20mA, fclk = 10 x fout

Typical Performance Curves: 3 Volt Supplies

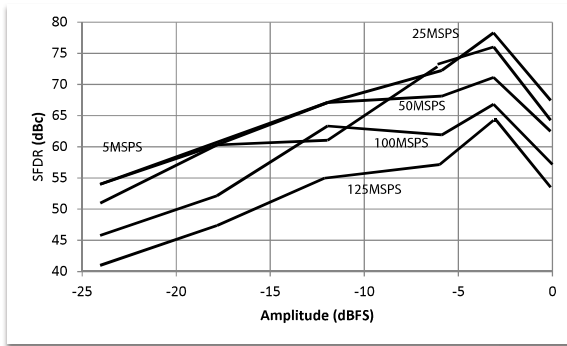


Figure 19a. SFDR vs Amplitude, $f_{clk} = 5 \times f_{out}$

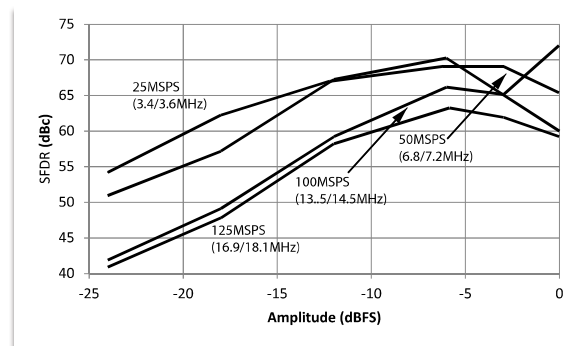


Figure 19b. SFDR vs Amplitude, $f_{clk} = 10 \times f_{out}$

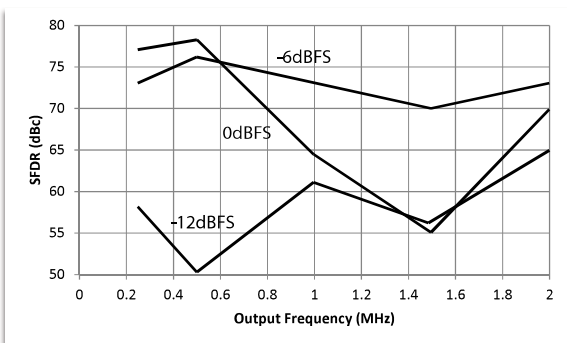


Figure 20a. SFDR vs f_{out} , $f_{clk} = 5\text{MHz}$

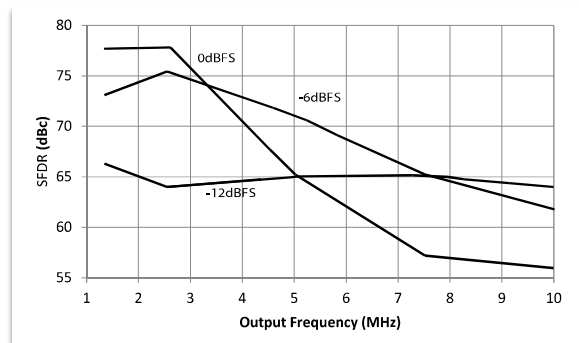


Figure 20b. SFDR vs f_{out} , $f_{clk} = 25\text{MHz}$

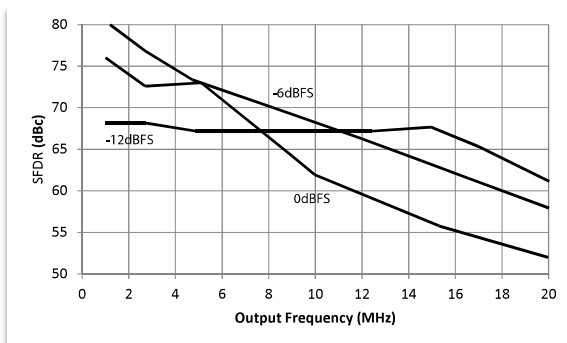


Figure 20c. SFDR vs f_{out} , $f_{clk} = 50\text{MHz}$

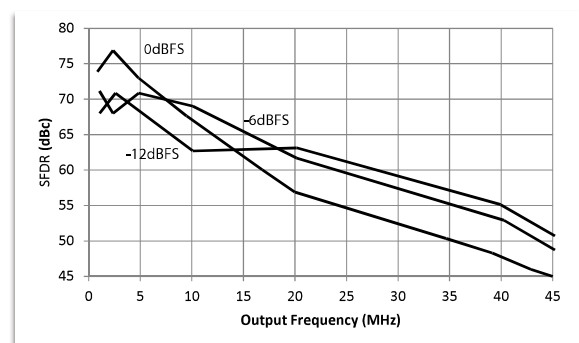


Figure 20d. SFDR vs f_{out} , $f_{clk} = 100\text{MHz}$

Typical Performance Curves: 3 Volt Supplies

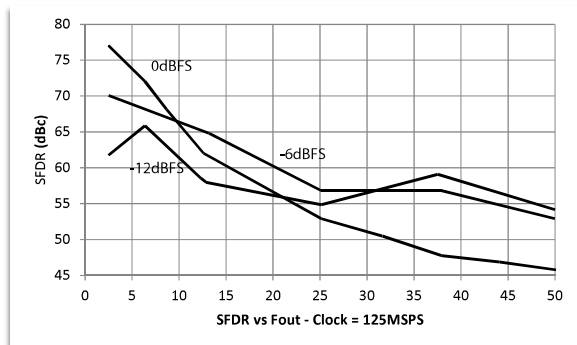


Figure 20e. SFDR vs fout, fclk = 125MSPS

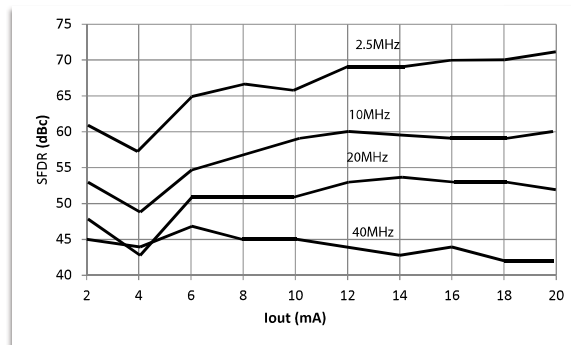


Figure 21. SFDR vs Iout, fclk = 100MHz

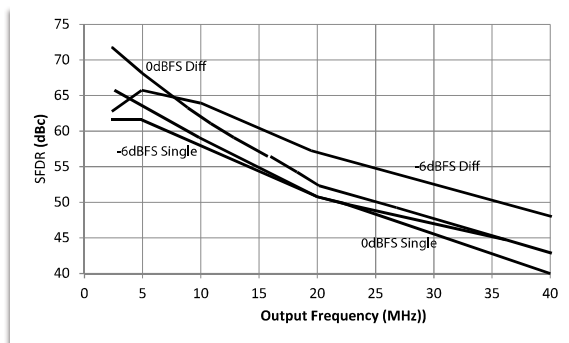


Figure 22. Differential vs Single-ended, fclk = 100MHz

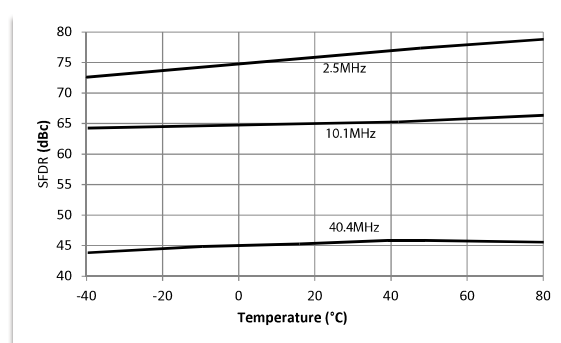


Figure 23. SFDR vs Temperature, fclk = 100MHz

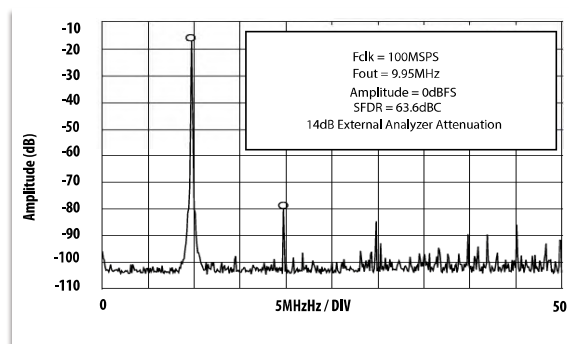


Figure 24. SFDR Single Tone, fclk = 100MHz

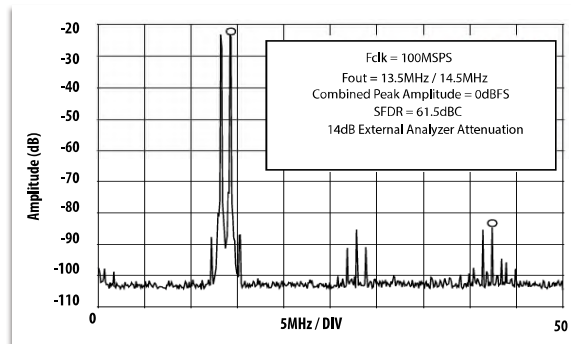


Figure 25. SFDR Two Tone, fclk = 100MHz

Typical Performance Curves: 3 Volt Supplies

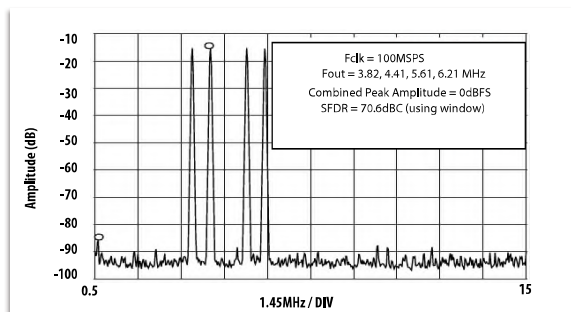


Figure 26. SFDR Four Tone, fclk = 100MHz

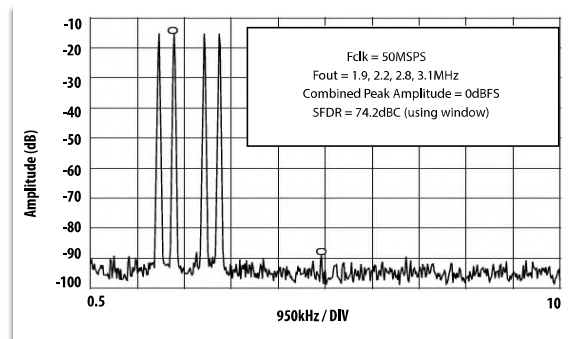


Figure 27. SFDR Four Tones, fclk = 50MHz

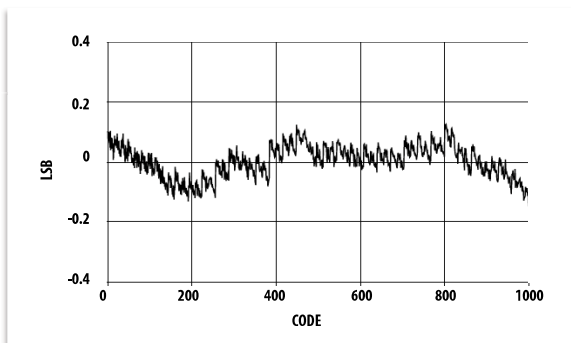


Figure 28. Integral Nonlinearity

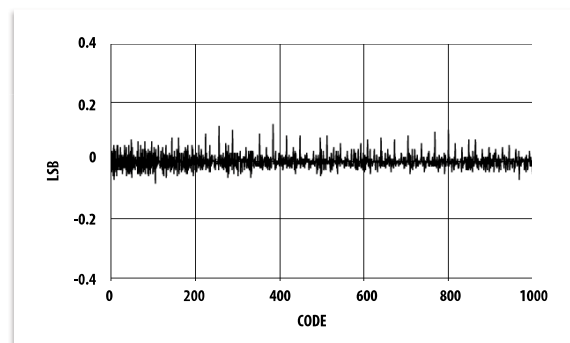


Figure 29. Differential Nonlinearity

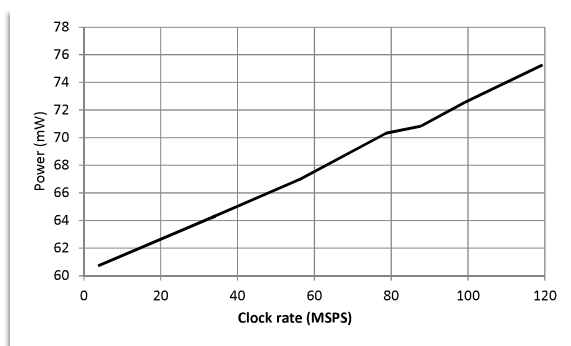


Figure 30. Power vs Clock rate, Iout = 20mA, fclk = 10 x fout

GLOSSARY OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the first 5 harmonics to the rms of the fundamental signal, usually expressed in dB

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTERNAL REFERENCE VOLTAGE DRIFT: The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

OUTPUT COMPLIANCE RANGE: The allowable Maximum Voltage at the output of a D/A.

OFFSET ERROR: The deviation from the ideal at analog zero output

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

POWER SUPPLY REJECTION RATIO (PSRR): The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

REFERENCE INPUT MULTIPLYING BANDWIDTH: The -3dB reduction in the output when applying a sinusoidal voltage to the external reference (digital inputs are set to all 1s). The frequency is increased until the amplitude of the output waveform is -3dB of its original value.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and D/A converters.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the first 5 harmonics to the rms of the fundamental signal, usually expressed in dB

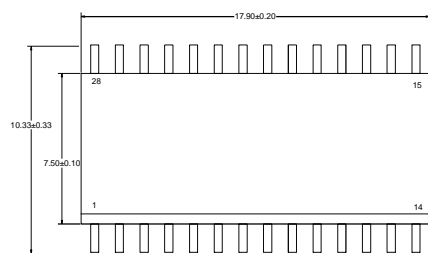
GLITCH AREA: The transient appearing at the output when the input switches from one code to another. Typically the worst case is found at the MSB code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification.

SPURIOUS FREE DYNAMIC RANGE (SFDR): The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

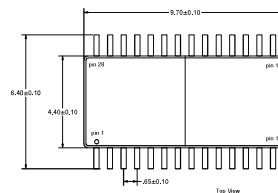
INPUT / OUTPUT DESCRIPTIONS

PIN DESCRIPTIONS		
PIN	PIN NAME	DESCRIPTION
1-10	BIT 1 (MSB) through B10 (LSB)	Digital Data input bits. B1 (MSB), B10 (LSB).
11-14	NC	No Connection. For noise rejection may be tied to AGND.
15	SHTDWN	Control pin to power-down the DAC. Sleep = HI, On = LO. Internal 20µA active pull-down current.
16	REFSEL	Connect to AGND to enable internal 1.2V reference. Connect to AVDD to disable internal reference.
17	REFI/O	Reference voltage output when using internal 1.2V reference. Input pin when supplying external reference.
18	GAINADJ	Full Scale current adjustment (gain). Use resistor to AGND to set current (see technical notes).
19	COMP	External capacitor to AGND helps to reduce bandwidth.
20	AGND	Analog Ground
21	IOUTB	Complimentary output current. Full scale is attained when digital inputs are at all 0's.
22	IOUTA	True output current. Full scale is attained when digital inputs are at all 1's.
23	NC	Do not connect. Internal resistive connection to AGND.
24	AVDD	Supply for analog circuitry (typically +3V to +5V).
25	NC	No Connection. (12 and 14 bit devices in this series require pin 25 tied to AGND)
26	DGND	Digital Ground
27	DVDD	Supply for digital circuitry (typically +3V to +5V).
28	CLK	Rising edge of clock latches data into input registers thereby updating converter.

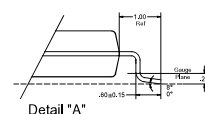
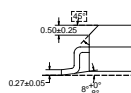
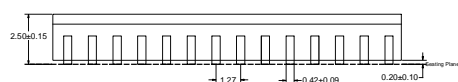
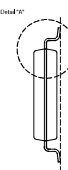
MECHANICAL DIMENSIONS - INCHES (mm)



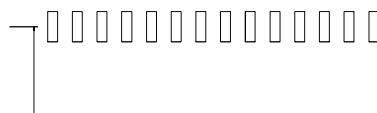
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



See Detail "A"



TYPICAL RECOMMENDED LAND PATTERN



ORDERING INFORMATION

ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE (°C)	PACKAGE	SHIPPING
DAC-1012SE	-40 to +105	28 Pin TSSOP	Tube
DAC-1012SM	-55 to +125	28 Pin TSSOP	Tube
DAC-1012-QL	-55 to +125	Ceramic LCC	Tray
DAC-1012/883	-55 to +125	Ceramic LCC	Tray