NEC

MOS INTEGRATED CIRCUIT

μPD78052(A), 78053(A), 78054(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

A stricter quality assurance program (called special grade in NEC's grade classification) is applied to the μPD78052(A), 78053(A), and 78054(A), compared to the μPD78052, 78053, and 78054, which are classified as standard grade.

The μPD78052(A), 78053(A), and 78054(A) belong to the μPD78054 Subseries products of the 78K/0 Series.

These microcontrollers include the rich peripheral hardware, such as 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port, and interrupt functions.

Various development tools are also available.

Details of the function description, etc., are described in the following User's Manuals. Be sure to read the documents when designing.

μPD78054, 78054Y Subseries User's Manual : U11747E
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Large on-chip ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	Buffer RAM	
μPD78052(A)	16 Kbytes	512 bytes	32 bytes	• 80-pin plastic QFP (14 × 14 mm)
μPD78053(A)	24 Kbytes	1024 bytes		
μPD78054(A)	32 Kbytes			

- External memory expansion space: 64 Kbytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 69 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
- Timer: 5 channels
- Power supply voltage : V_{DD} = 2.0 to 6.0 V

APPLICATIONS

Control devices of transport system, gas detector circuit-breakers, safety devices, etc.

The information in this document is subject to change without notice.

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ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD78052GC(A)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	Special
μPD78053GC(A)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	Special
μPD78054GC(A)-×××-3B9	80-pin plastic QFP (14 × 14 mm)	Special

Remark ××× indicates ROM code suffix.

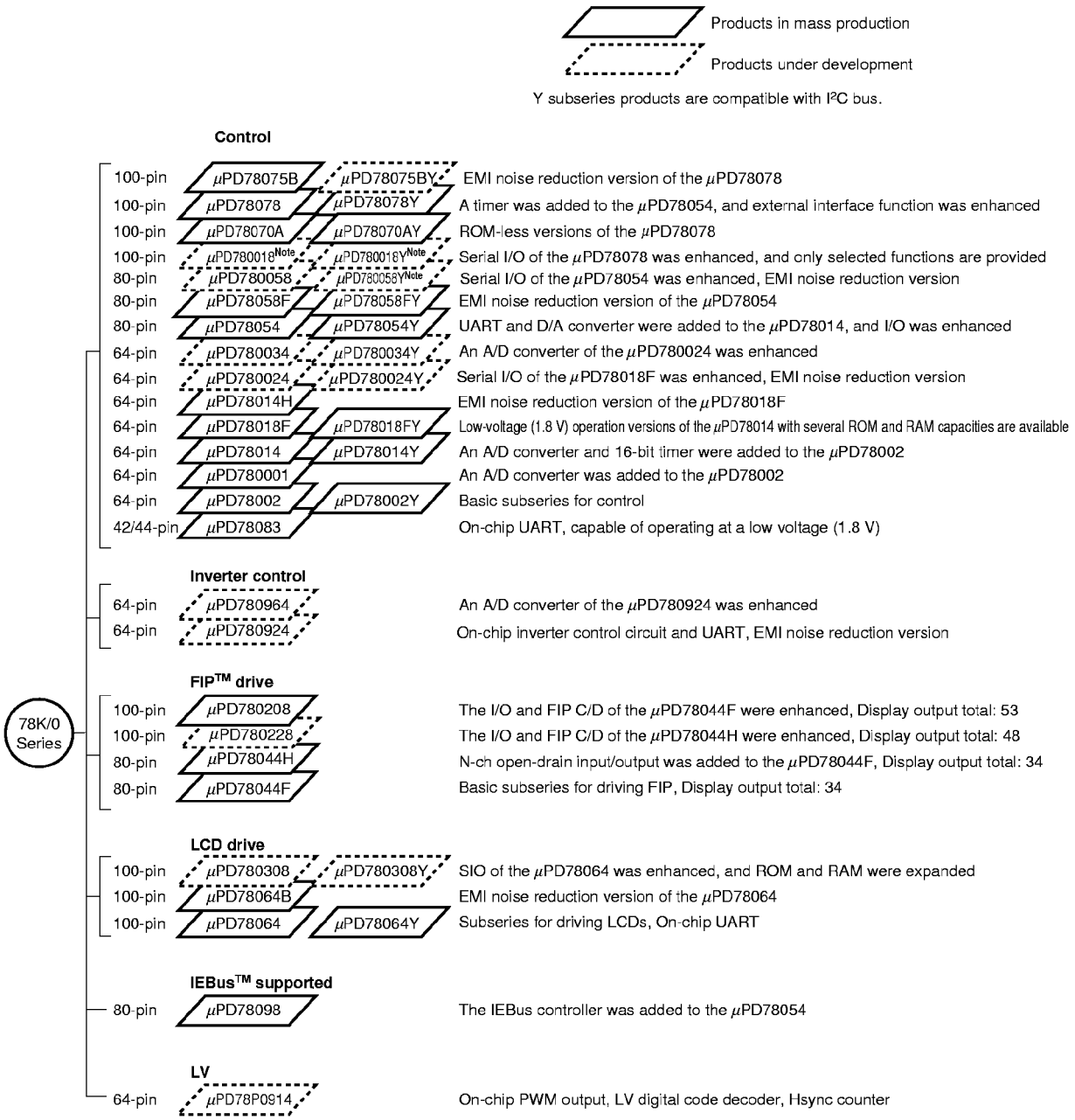
Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCES BETWEEN μPD78052(A), 78053(A), 78054(A) AND STANDARD PRODUCTS (μPD78052, 78053, 78054)

Item \ Part Number	μPD78052(A), 78053(A), 78054(A)	μPD78052, 78053, 78054
Package	• 80-pin plastic QFP (14 × 14 mm)	• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch (12 × 12 mm))
Quality grade	Special	Standard

78K/0 SERIES PRODUCT DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under planning

The major functional differences among the subseries are shown below.

Subseries Name / Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K-40 K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78078	48 K-60 K											
	μPD78070A	–									61	2.7 V	
	μPD780018	48 K-60 K							–	2ch (time-division 3-wire:1ch)	88		
	μPD780058	24 K-60 K	2ch						2ch	3ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780034	8 K-32 K					–	8ch	–	3ch (UART: 1ch, time-division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K-60 K											
	μPD78014	8 K-32 K										2.7 V	
	μPD780001	8 K		–	–					1ch	39		–
	μPD78002	8 K-16 K			1ch		–				53		Available
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780964	8 K-32 K	3ch	**Note**	–	1ch	–	8ch	–	2ch (UART: 2ch)	47	2.7 V	Available
	μPD780924						8ch	–					
FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48 K-60 K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32 K-48 K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16 K-40 K								2ch			
LCD drive	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time-division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2ch (UART: 1ch)		2.0 V	
	μPD78064	16 K-32 K											
IEBus supported	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	Available
LV	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	Available

Note 10-bit timer: 1 channel

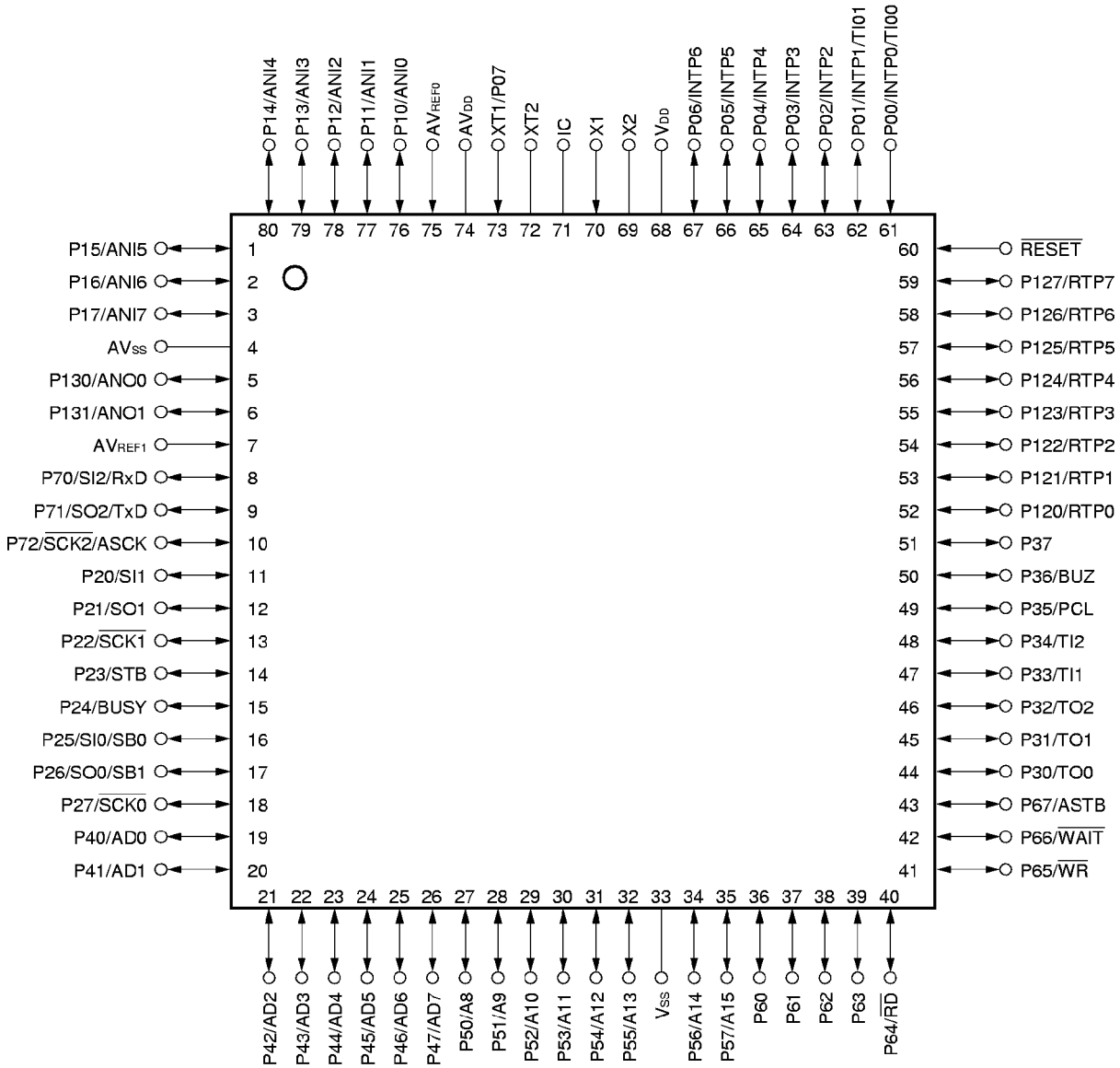
FUNCTION OVERVIEW

Item \ Part Number		μPD78052(A)	μPD78053(A)	μPD78054(A)
Internal memory	ROM	16 Kbytes	24 Kbytes	32 Kbytes
	High-speed RAM	512 bytes	1024 bytes	
	Buffer RAM	32 bytes		
Memory space		64 Kbytes		
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Instruction cycle		On-chip instruction execution time cycle modification function		
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0-MHz operation)		
	When subsystem clock selected	122 μs (at 32.768-kHz operation)		
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc.		
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4		
A/D converter		8-bit resolution × 8 channels		
D/A converter		8-bit resolution × 2 channels		
Serial interface		• 3-wire serial I/O, SBI, or 2-wire serial I/O mode selectable: 1 channel • 3-wire serial I/O mode (on-chip max. 32 bytes automatic transmit/receive function): 1 channel • 3-wire serial I/O or UART mode selectable: 1 channel		
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel		
Timer output		3 (14-bit PWM output × 1)		
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0-MHz operation) 32.768 kHz (at subsystem clock 32.768-kHz operation)		
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0-MHz operation)		
Vectored interrupt source	Maskable	Internal : 13, external : 7		
	Non-maskable	Internal : 1		
	Software	1		
Test input		Internal : 1, external : 1		
Power supply voltage		V_{DD} = 2.0 to 6.0 V		
Operating ambient temperature		T_A = −40 to +85 °C		
Package		• 80-pin plastic QFP (14 × 14 mm)		

CONTENTS

1. PIN CONFIGURATION (Top View)

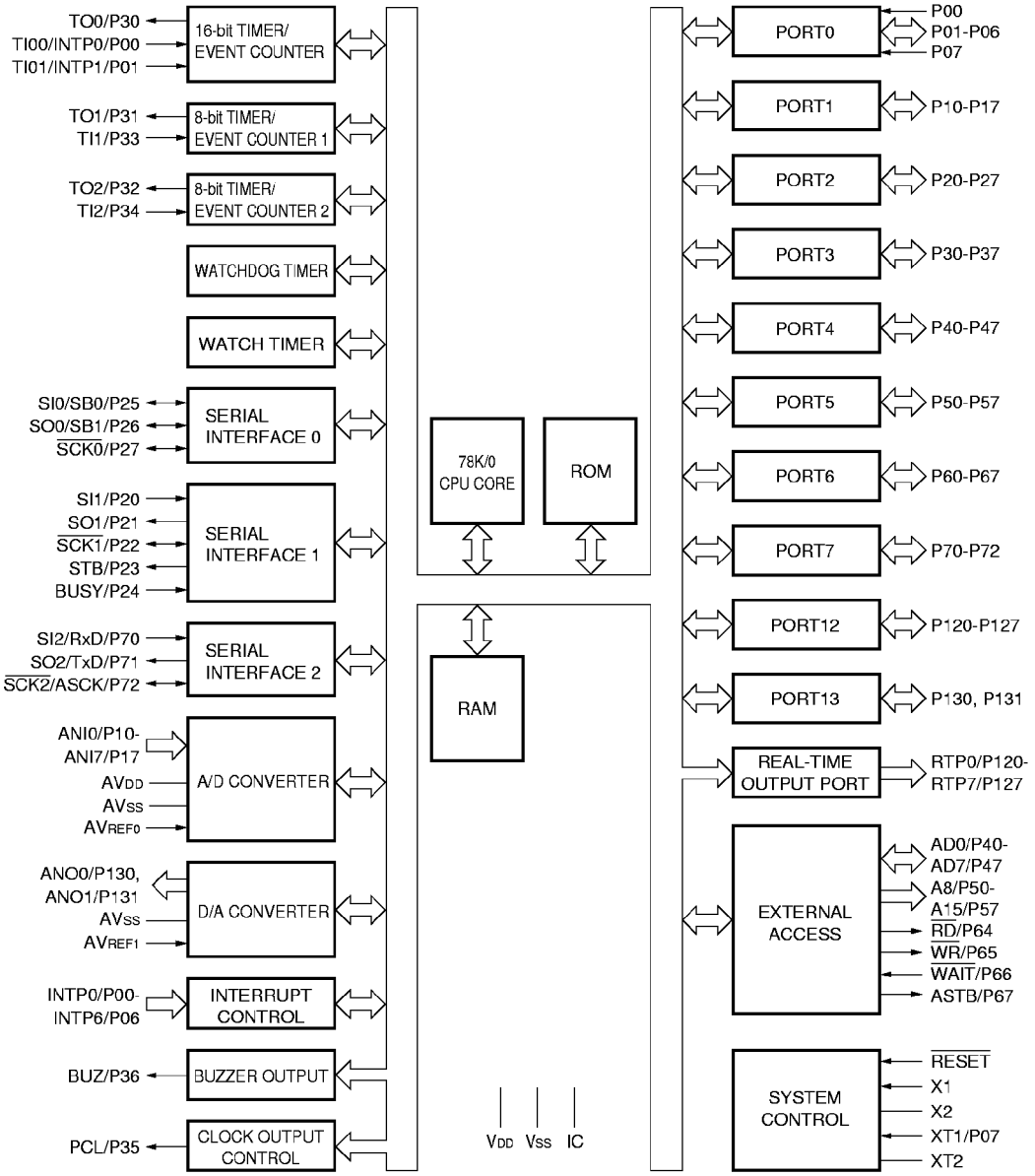
- **80-pin plastic QFP (14 × 14 mm)**
  μPD78052GC(A)-×××-3B9
  μPD78053GC(A)-×××-3B9
  μPD78054GC(A)-×××-3B9



Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS}.
2. Connect the AV_{DD} pin to V_{DD}.
3. Connect the AV_{SS} pin to V_{SS}.

A8-A15 : Address Bus
AD0-AD7 : Address/Data Bus
ANI0-ANI7 : Analog Input
ANO0, ANO1 : Analog Output
ASCK : Asynchronous Serial Clock
ASTB : Address Strobe
AV_{DD} : Analog Power Supply
AV_{REF0}, AV_{REF1} : Analog Reference Voltage
AV_{SS} : Analog Ground
BUSY : Busy
BUZ : Buzzer Clock
IC : Internally Connected
INTP0-INTP6 : Interrupt from Peripherals
P00-P07 : Port0
P10-P17 : Port1
P20-P27 : Port2
P30-P37 : Port3
P40-P47 : Port4
P50-P57 : Port5
P60-P67 : Port6
P70-P72 : Port7
P120-P127 : Port12
P130, P131 : Port13
PCL : Programmable Clock
$\overline{RD}$: Read Strobe
$\overline{RESET}$: Reset
RTP0-RTP7 : Real-Time Output Port
RxD : Receive Data
SB0, SB1 : Serial Bus
$\overline{SCK0}$-$\overline{SCK2}$: Serial Clock
SI0-SI2 : Serial Input
SO0-SO2 : Serial Output
STB : Strobe
TI00, TI01 : Timer Input
TI1, TI2 : Timer Input
TO0-TO2 : Timer Output
TxD : Transmit Data
V_{DD} : Power Supply
V_{SS} : Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write Strobe
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 Note 1	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.Note 2		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pin as an input port, set 1 in the bit 6 (FRC) of the processor clock control register (PCC). On-chip feedback resistor of the subsystem clock oscillator should not be used.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, use of the pull-up resistor is cancelled automatically.

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/outport port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, on-chip pull-up resistor can be used by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	Input/output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	ANO0, ANO1

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (dual-function as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input/output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connect to V_{DD}.	—	—
AV_{SS}	—	A/D and D/A converter ground potential. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect to V_{SS} directly.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Connect to V_{SS} via a resistor individually.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	Input/output	Connect to V_{DD} or V_{SS} via a resistor individually.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Connect to V_{DD} via a resistor individually.
P50/A8 to P57/A15	5-A		Connect to V_{DD} or V_{SS} via a resistor individually.
P60 to P63	13-B		Connect to V_{DD} via a resistor individually.
P64/$\overline{RD}$	5-A		Connect to V_{DD} or V_{SS} via a resistor individually.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P70/SI2/RxD	8-A	Input/ output	Connect to V_{DD} or V_{SS} via a resistor individually.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A		Connect to V_{SS} via a resistor individually.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
IC			Connect to V_{SS} directly.

Figure 3-1. Pin Input/Output Circuits (1/2)

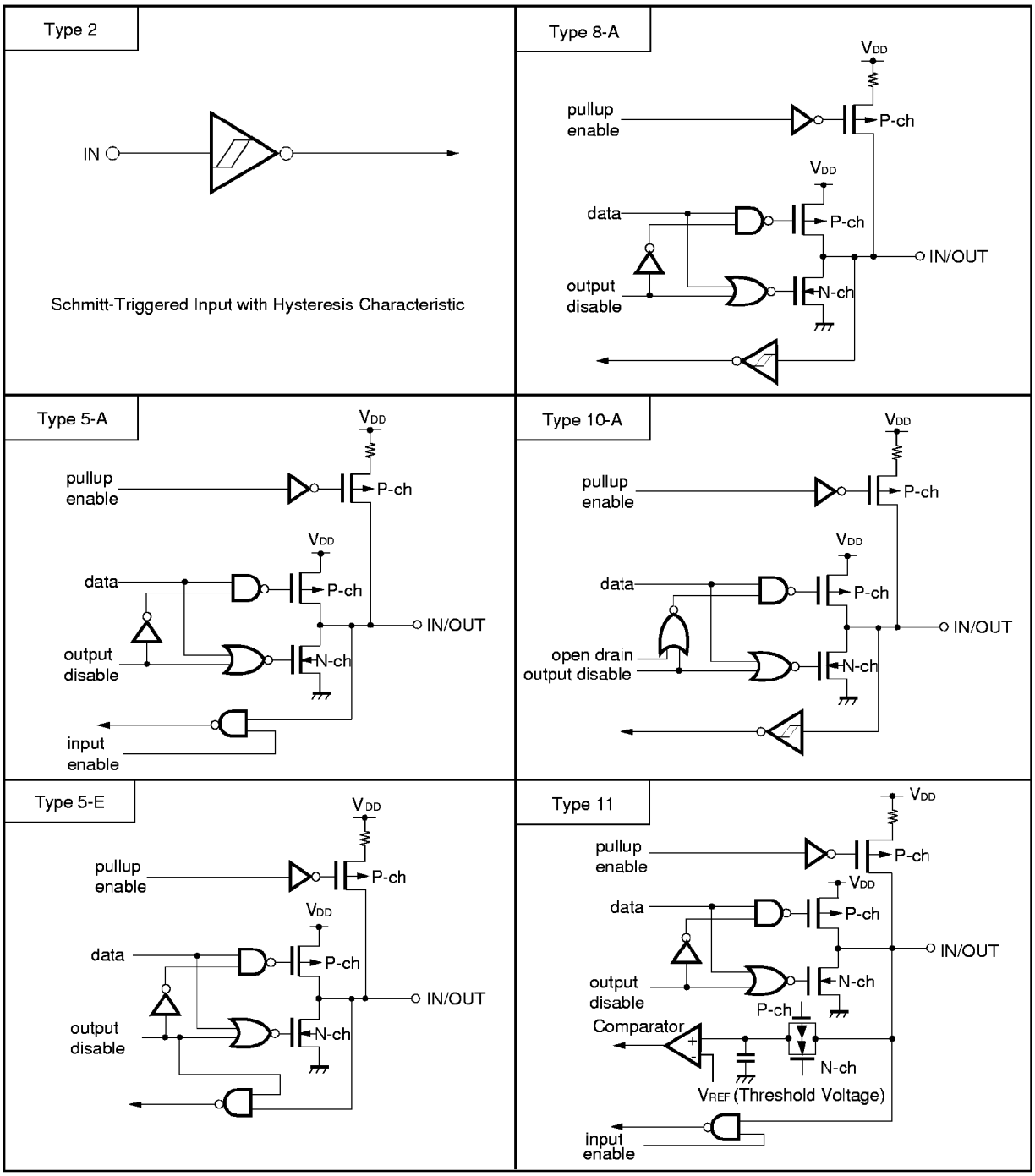
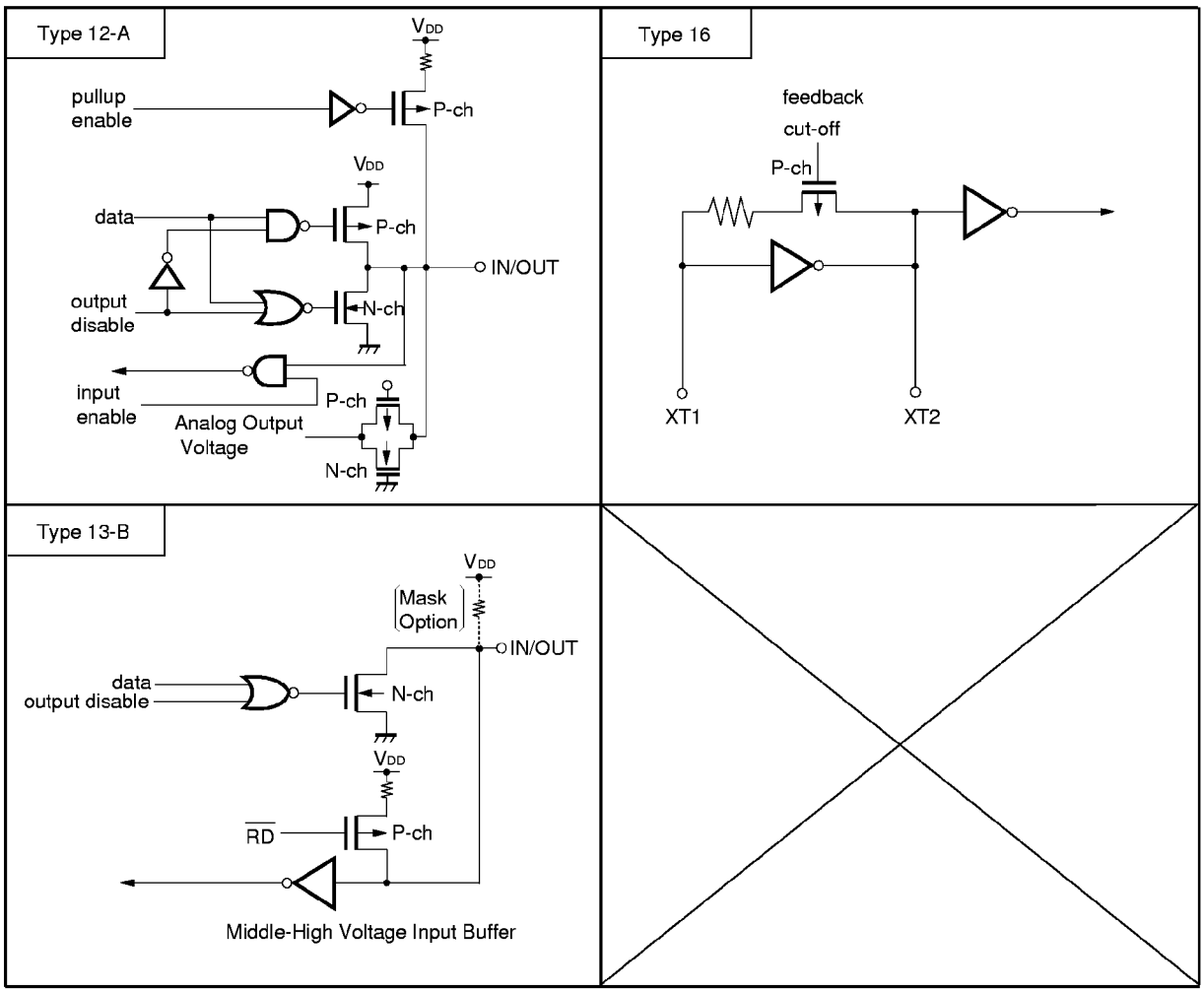


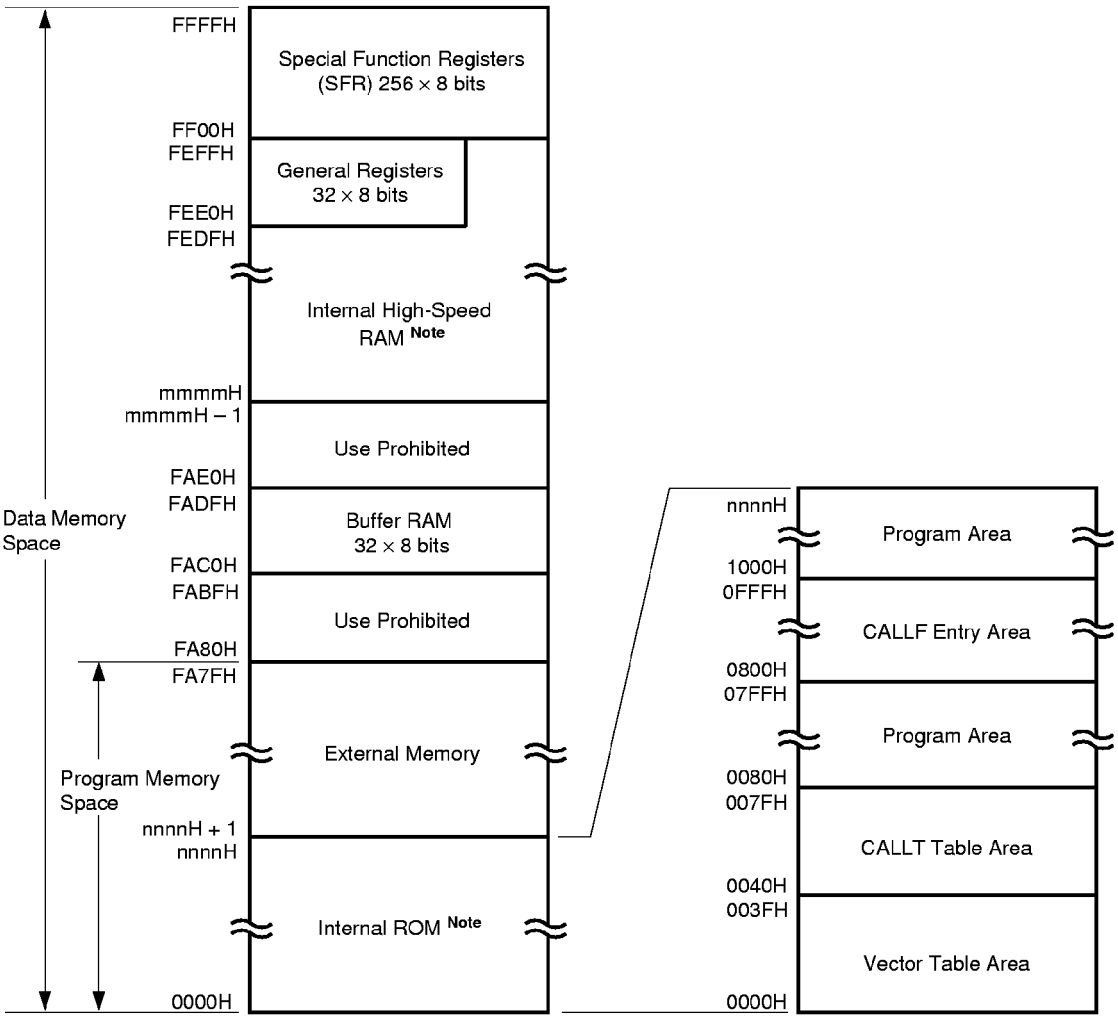
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD78052(A), 78053(A), 78054(A) memory map.

Figure 4-1. Memory Map



Note The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the following table).

Relevant Product Name	Internal ROM Last Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78052(A)	3FFFH	FD00H
μPD78053(A)	5FFFH	FB00H
μPD78054(A)	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13) : 63
- N-channel open-drain input/output (P60 to P63) : 4

Total : 69

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED direct drive capability.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 12	P120 to P127	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 13	P130, P131	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.

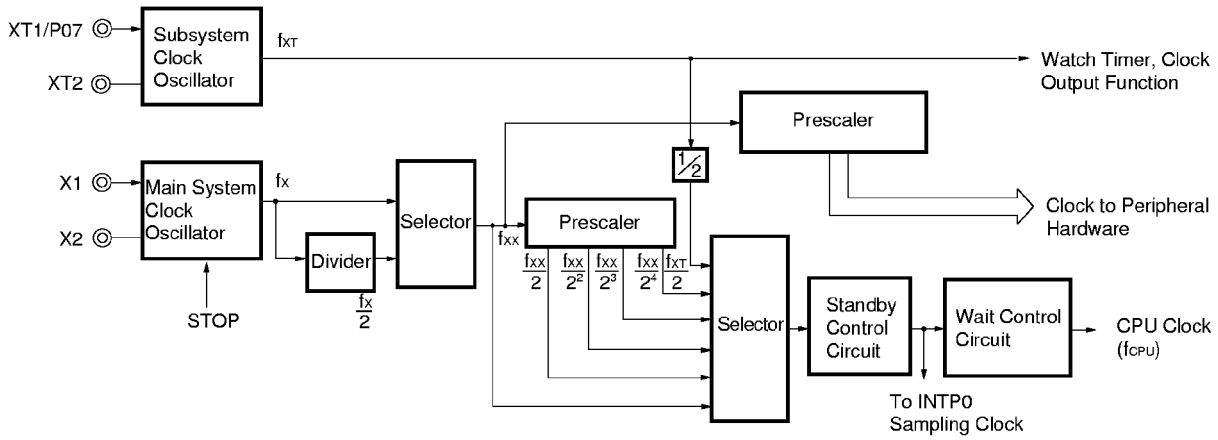
5.2 Clock Generator

Two types of generators, a main system clock generator and a subsystem clock generator, are available.

The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0-MHz operation)
- 122 μs (subsystem clock: at 32.768-kHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

The μPD78052(A), 78053(A), and 78054(A) incorporate 5 channels of the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

	16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type				
Interval timer	1 channel	2 channels	1 channel	1 channel
External event counter	1 channel	2 channels	——	——
Function				
Timer output	1 output	2 outputs	——	——
PWM output	1 output	——	——	——
Pulse width measurement	2 inputs	——	——	——
Square wave output	1 output	2 outputs	——	——
One-shot pulse output	1 output	——	——	——
Interrupt source	2	2	1	1
Test input	——	——	1 input	——

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

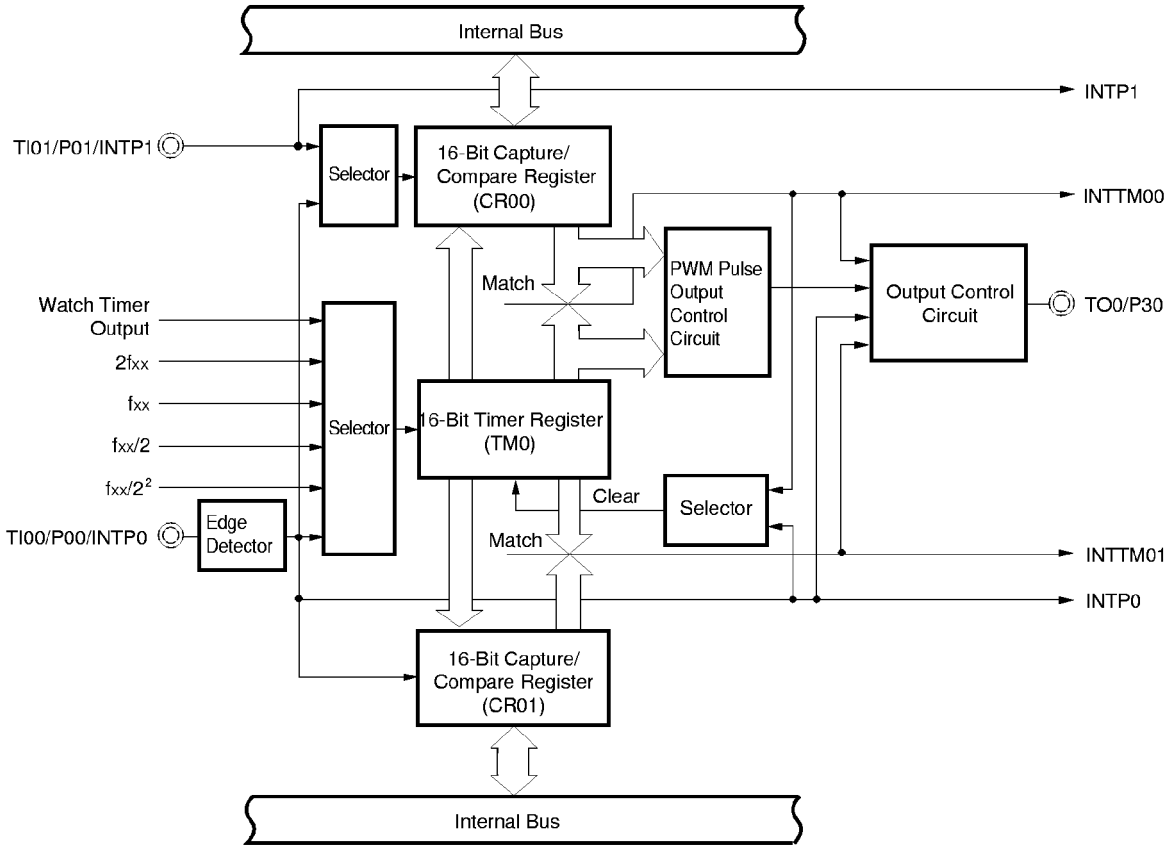


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

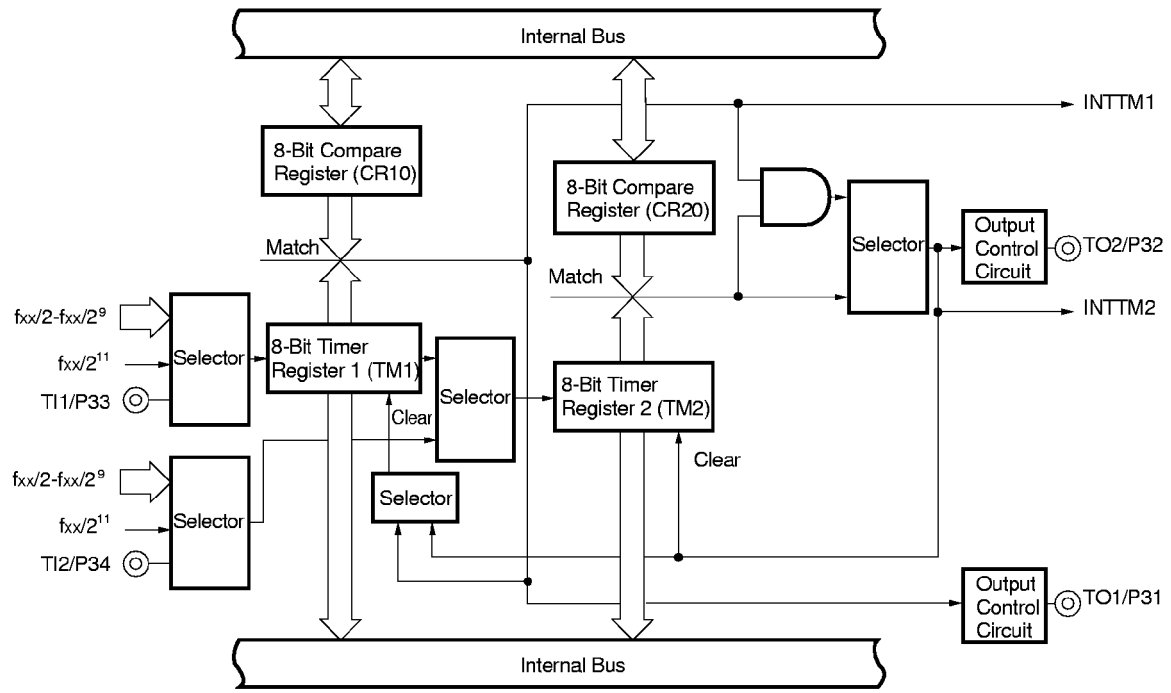


Figure 5-4. Watch Timer Block Diagram

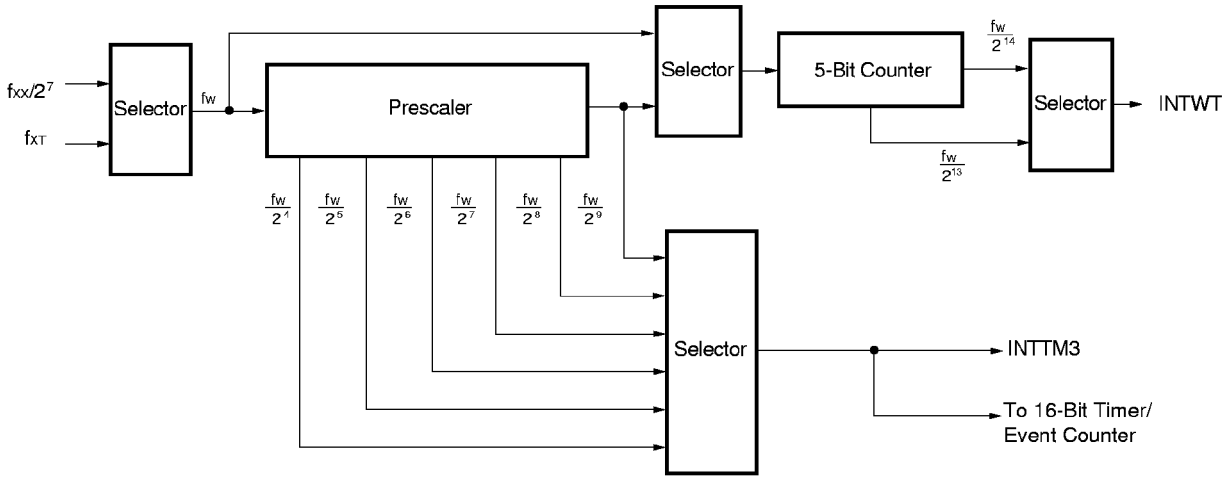
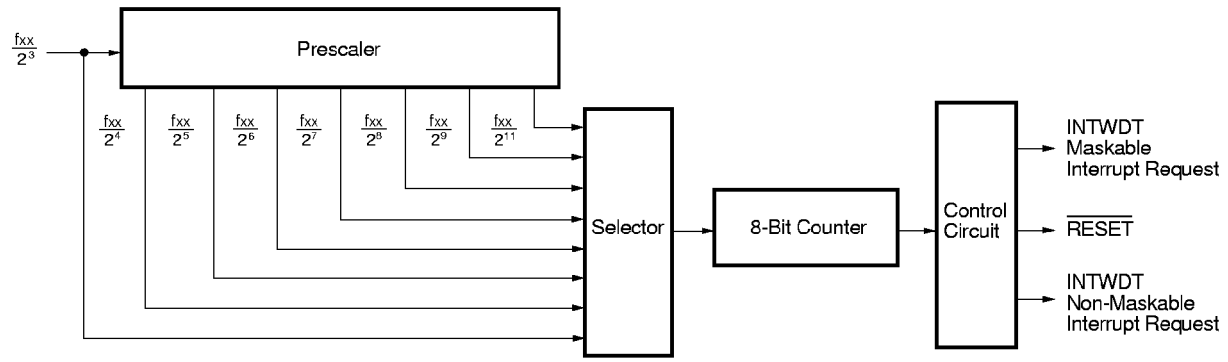


Figure 5-5. Watchdog Timer Block Diagram

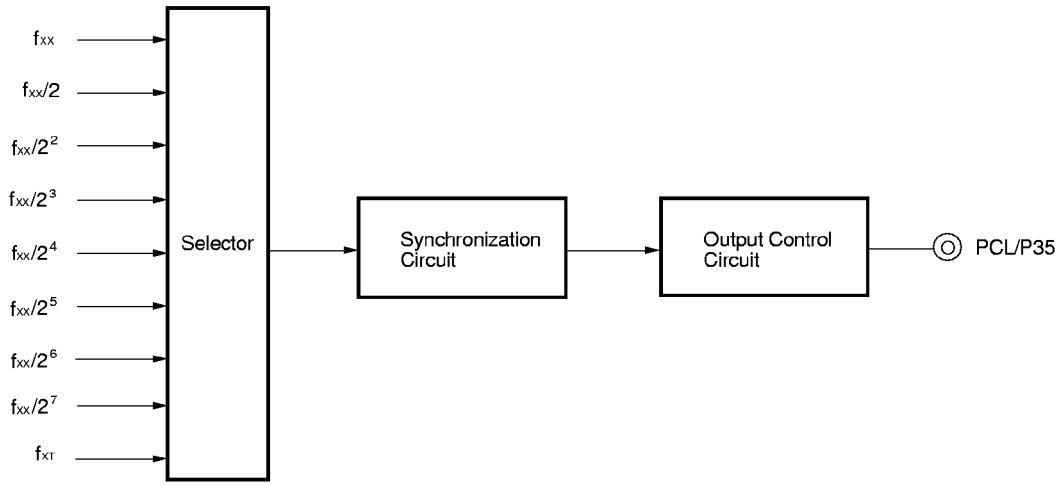


5.4 Clock Output Control Circuit

The clock with the following frequency can be output as a clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0-MHz operation)
- 32.768 kHz (subsystem clock: at 32.768-kHz operation)

Figure 5-6. Clock Output Control Circuit Block Diagram

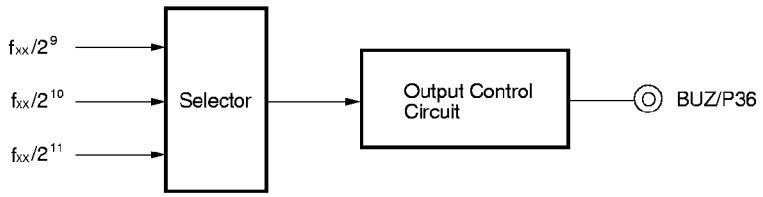


5.5 Buzzer Output Control Circuit

The clock with the following frequency can be output as a buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock: at 5.0-MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



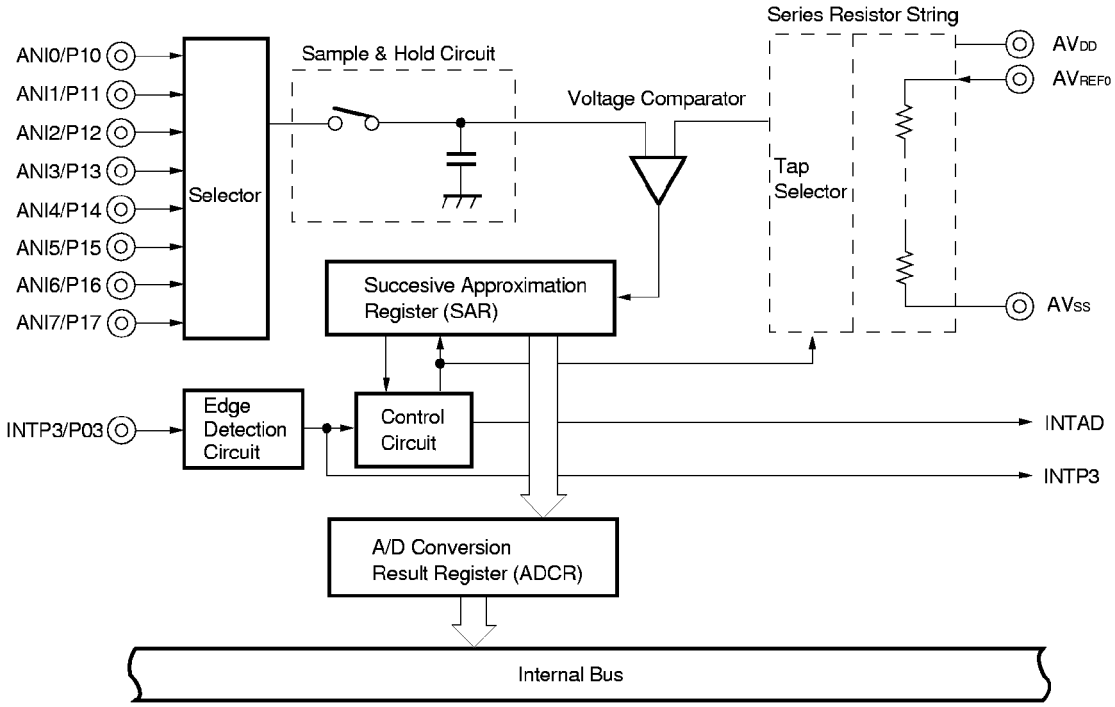
5.6 A/D Converter

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram

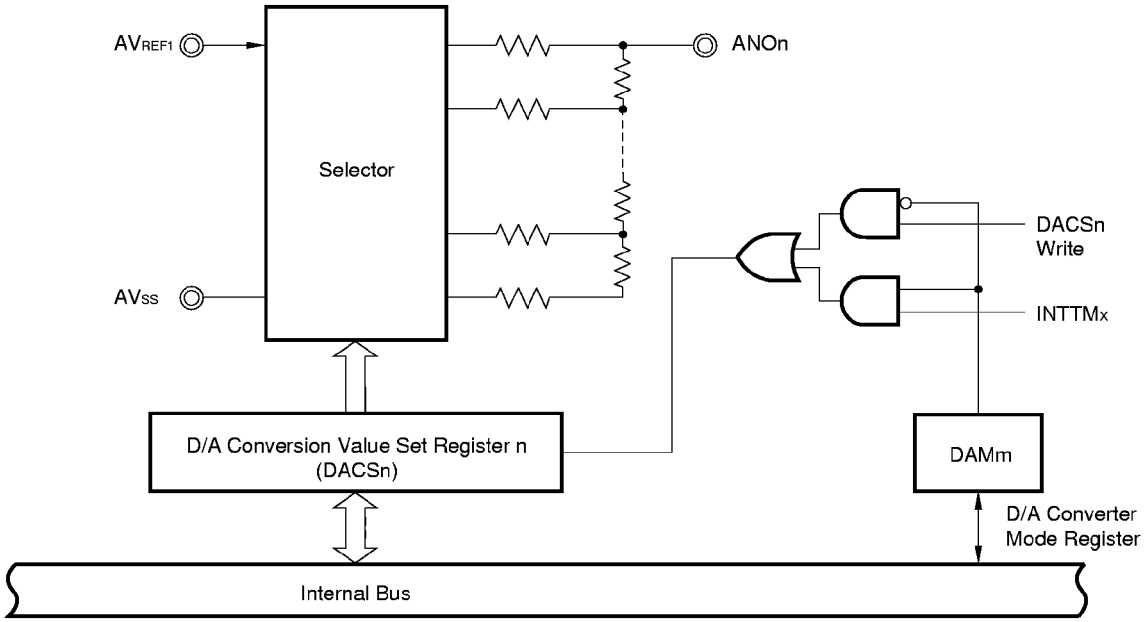


5.7 D/A Converter

A D/A converter of 8-bit resolution × 2 channels is incorporated.

Conversion method is R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1

m = 4, 5

x = 1, 2

5.8 Serial Interfaces

3 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	√ (MSB/LSB first switchable)	√ (MSB/LSB first switchable)	√ (MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmit/ receive function	—	√ (MSB/LSB first switchable)	—
SBI (serial bus interface) mode	√ (MSB first)	—	—
2-wire serial I/O mode	√ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	√ (Dedicated baud rate generator incorporated)

Figure 5-10. Serial Interface Channel 0 Block Diagram

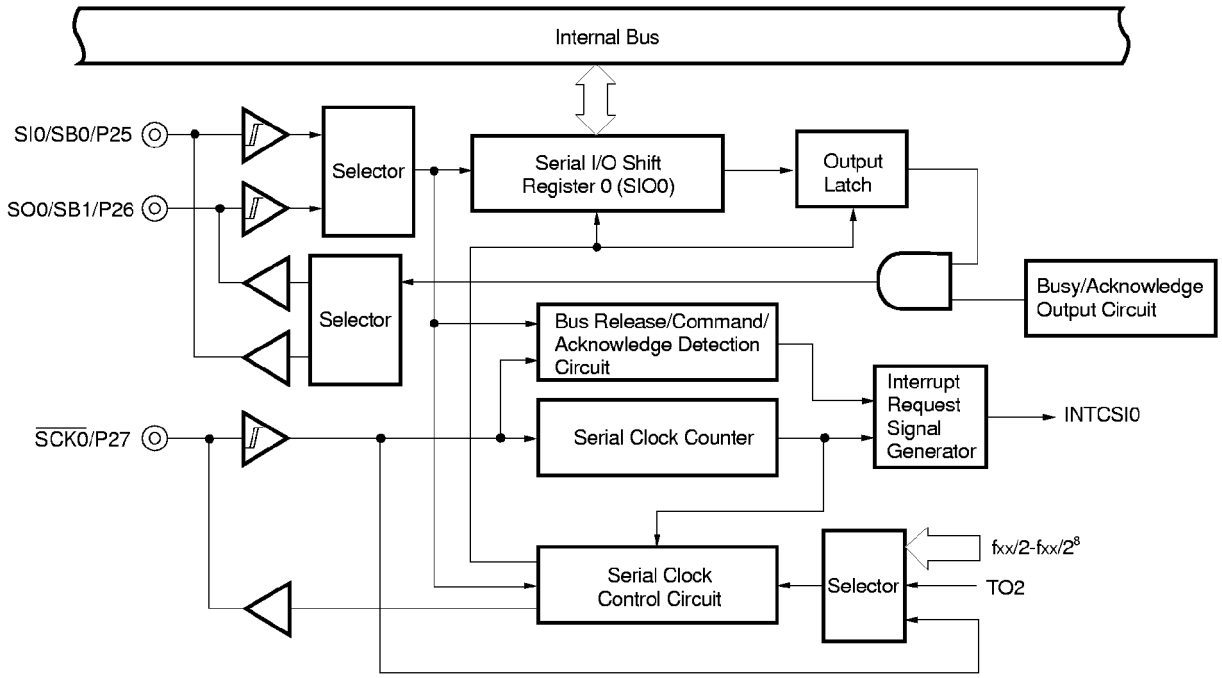


Figure 5-11. Serial Interface Channel 1 Block Diagram

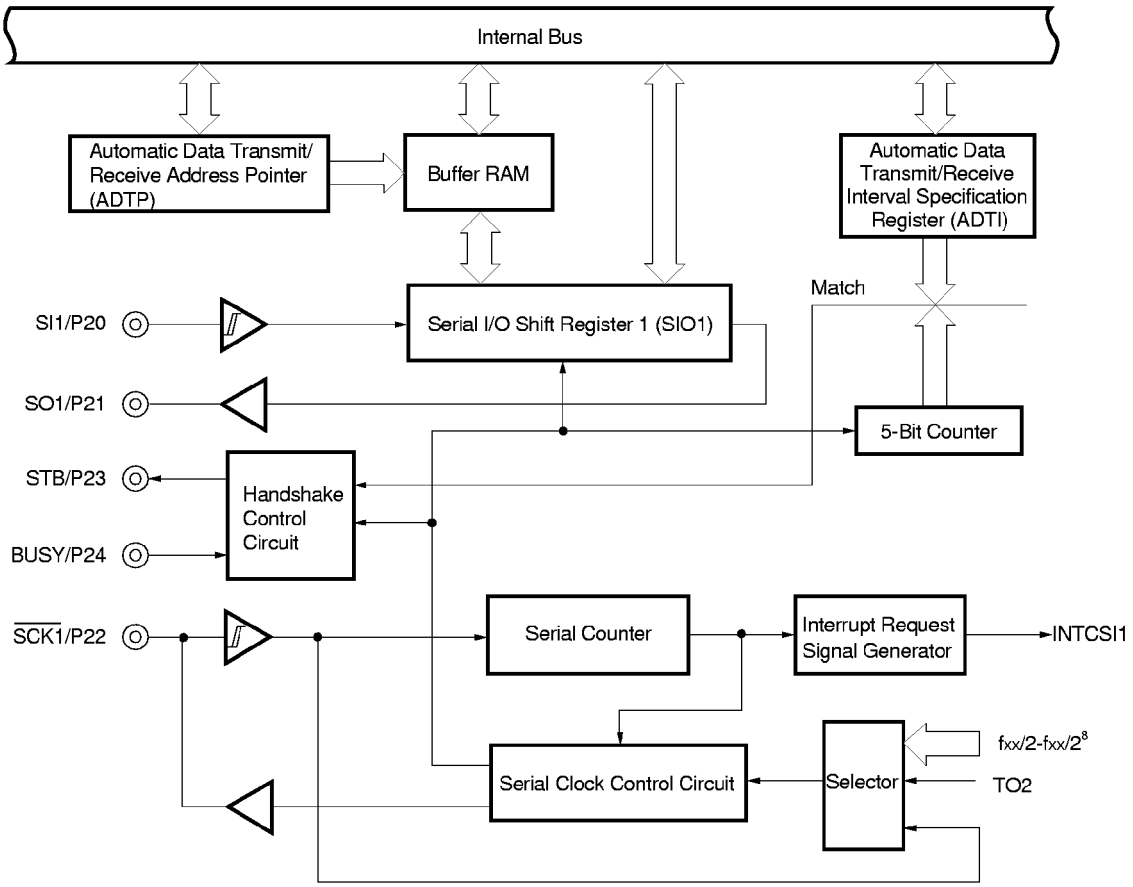
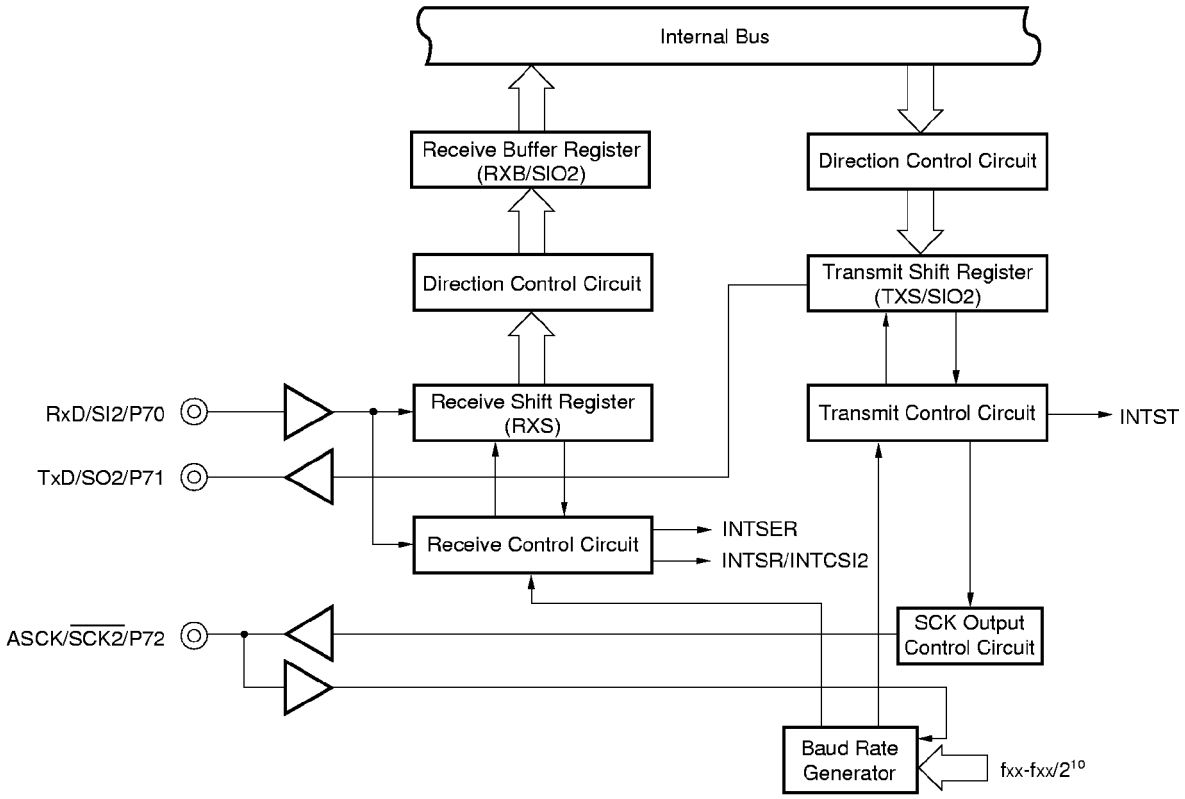


Figure 5-12. Serial Interface Channel 2 Block Diagram

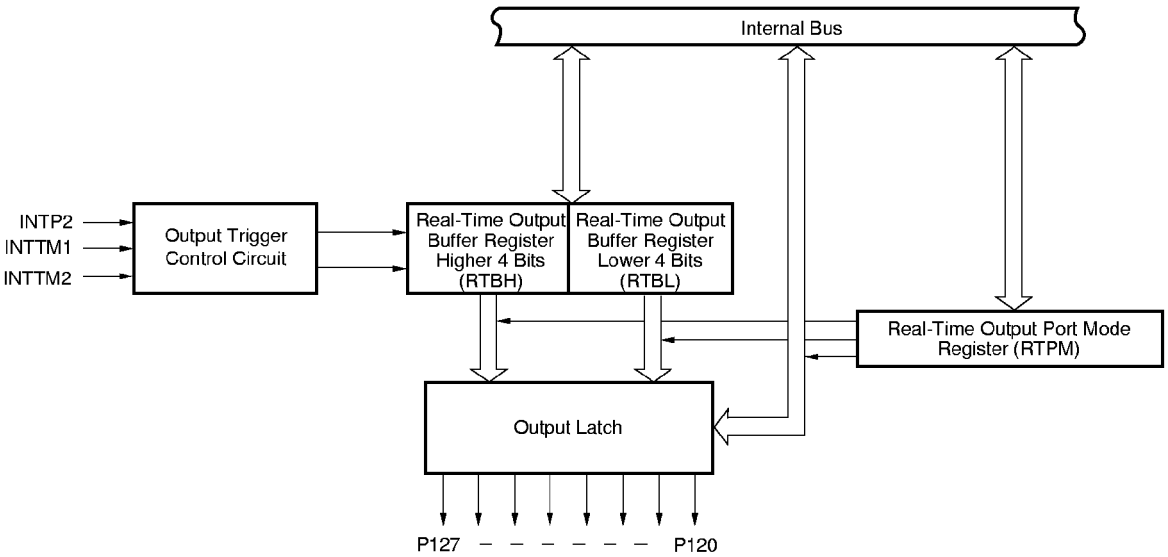


5.9 Real-Time Output Port

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is real-time output function. And pins to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

Figure 5-13. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

There are 22 interrupt functions of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 20
- Software : 1

Table 6-1. Interrupt Source List (1/2)

Kind of Interrupt	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	——	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	End of serial interface channel 1 transfer		0016H	
	10	INTSER	Generation of serial interface channel 2 UART receive error		0018H	
	11	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	12	INTST	End of serial interface channel 2 UART transmission		001CH	

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Table 6-1. Interrupt Source List (2/2)

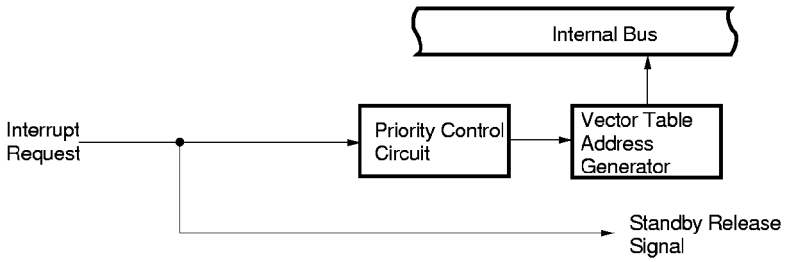
Kind of Interrupt	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Maskable	13	INTTM3	Reference time interval signal from watch timer	Internal	001EH	(B)
	14	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of match signal of 8-bit timer/ event counter 2		0026H	
	18	INTAD	End of conversion by A/D converter		0028H	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

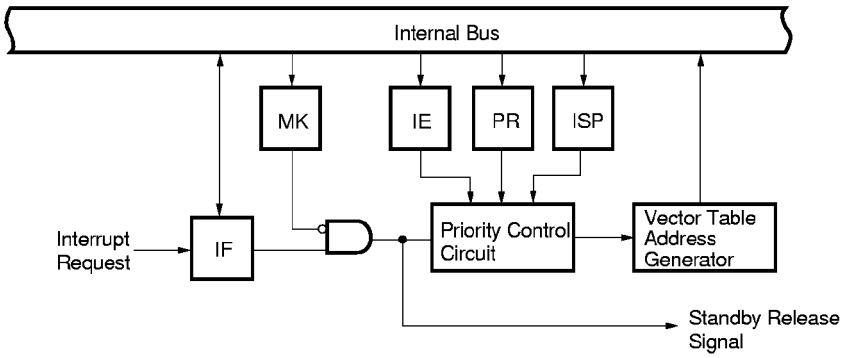
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

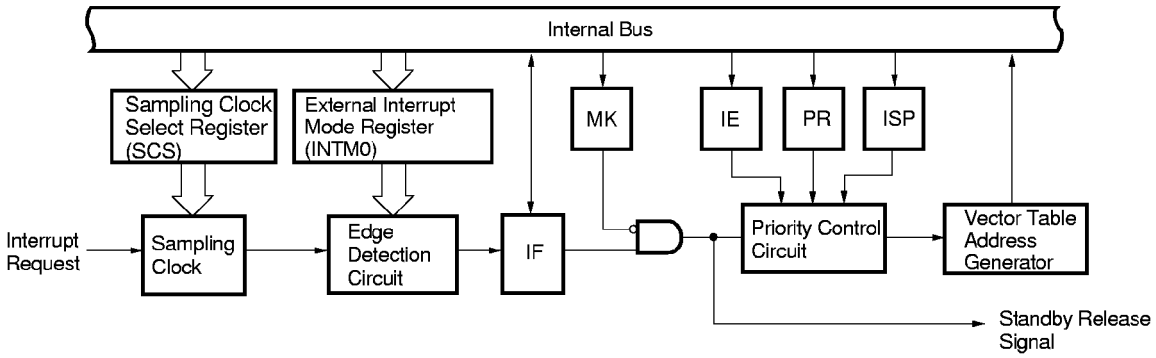
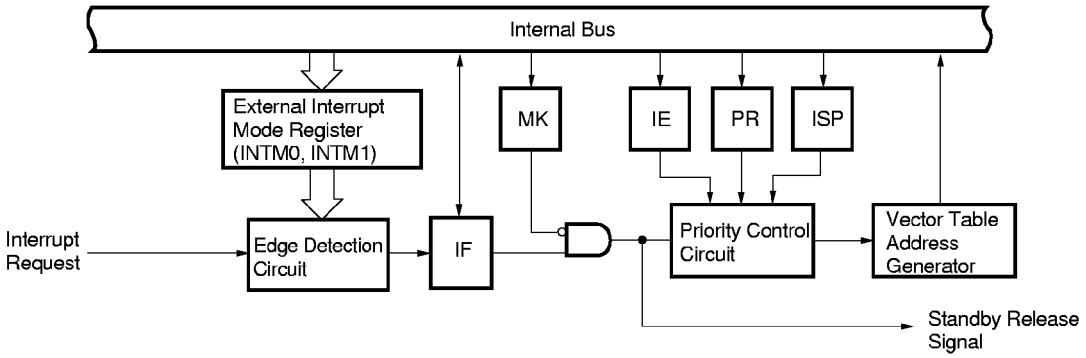
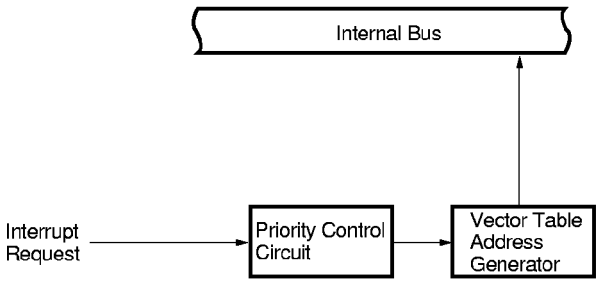


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

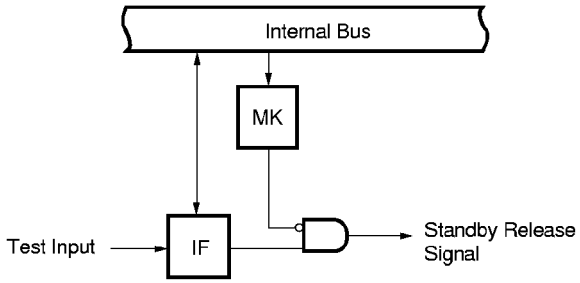
6.2 Test Functions

There are two test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

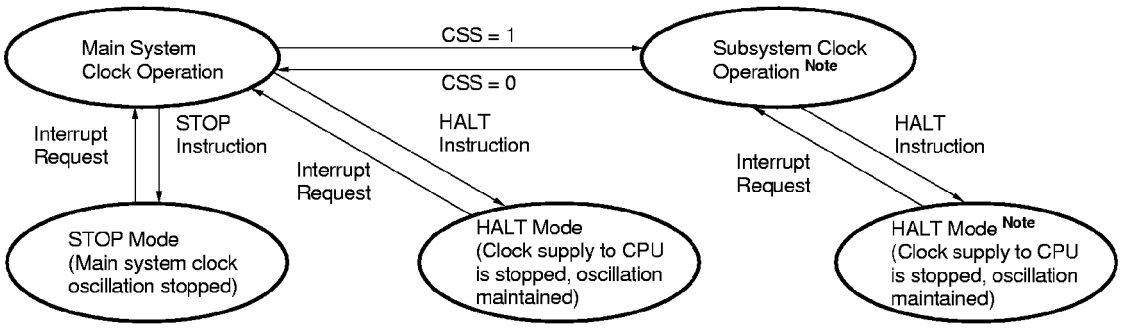
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the consumption current.

- HALT mode : The CPU operating clock is stopped.
  The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Function



Note The consumption current can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) in the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Remark CSS : bit 4 in the PCC

9. RESET FUNCTION

There are the following two reset methods.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First operand \ Second operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

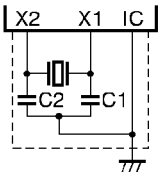
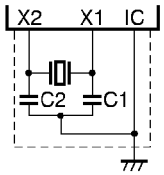
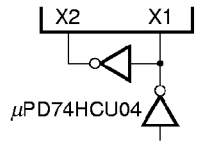
Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD}+0.3	V
	AV_{REF0}			–0.3 to V_{DD}+0.3	V
	AV_{REF1}			–0.3 to V_{DD}+0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 toP37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{RESET}$		–0.3 to V_{DD}+0.3	V
	V_{I2}	P60 to P63	N-ch open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD}+0.3	V
Analog intput voltage	V_O	P10 to P17	Analog input pin	AV_{SS}–0.3 to AV_{REF0}+0.3	V
High level output current	I_{OH}	1 pin		–10	mA
		P01 to P06, P30-P37, P56, P57, P60 to P67, P120 to P127 total		–15	mA
		P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 total		–15	mA
Low level output current	I_{OL} Note	1 pin	Peak value	30	mA
			Effective value	15	mA
		P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P56, P57, P60 to P63 total	Peak value	100	mA
			Effective value	70	mA
		P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 total	Peak value	50	mA
			Effective value	20	mA
		P01 to P06, P30 to P37, P64 to P67, P120 to P127 total	Peak value	50	mA
			Effective value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note Effective value should be calculated as follows: [Effective value] = [Peak value] × $\sqrt{duty}$

Caution **Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to 85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (fx) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (fx) Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

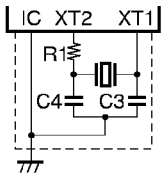
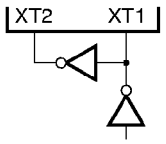
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figure should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	0	2.0	6.0	
	CST5.00MGW	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on-chip
Kyocera Corp.	KBR-5.0MSA	5.00	33	33	0	2.0	6.0	Lead type
	KBR-5.0MKS	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on-chip, lead type
	KBR-5.0MWS	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on-chip, chip type
	PBRC 5.00A	5.00	33	33	0	2.0	6.0	Chip type
TDK Corp.	CCR4.0MC3	4.00	On-chip	On-chip	0	2.0	6.0	Capacitor on-chip
	CCR5.0MC3	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on-chip

MAIN SYSTEM CLOCK: CRYSTAL RESONATOR (T_A = –10 to +70 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	SMD-49	3.579545	27	27	1.5	2.0	6.0

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (T_A = –10 to +70 °C)

Manufacturer	Product Name	Frequency (kHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA252E00)	32.768	27	20	330	2.0	6.0

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open-drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V **Note**	0.9V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V **Note**	0		0.1V_{DD}	V
Output voltage high	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, open-drain, pulled-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note For use as P07, use an inverter to input the inverted phase of P07 to the XT2 pin.

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note 1	μA
Output leakage current high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resistor Note 2	R_2	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. When the pull-up resistor is not included in P60 to P63 (specified by a mask option), the –200 μA (MAX.) low-level input leakage current flows only at the 1.5-clock interval (no wait) when the read instruction to the port 6 (P6) and port mode register 6 (PM6) is executed. Other than the 1.5-clock interval, –3 μA (MAX.) current flows.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 6.0 V.

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	5.0-MHz Crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10 % Note 5		4	12	mA
			V_{DD} = 3.0 V ± 10 % Note 6		0.6	1.8	mA
			V_{DD} = 2.2 V ± 10 % Note 6		0.35	1.05	mA
		5.0-MHz Crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10 % Note 5		6.5	19.5	mA
			V_{DD} = 3.0 V ± 10 % Note 6		0.8	2.4	mA
	I_{DD2}	5.0-MHz Crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 %		0.5	1.5	mA
			V_{DD} = 2.2 V ± 10 %		280	840	μA
		5.0-MHz Crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10 %		0.65	1.95	mA
	I_{DD3}	32.768-kHz Crystal oscillation operating mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		32	64	μA
			V_{DD} = 2.2 V ± 10 %		24	48	μA
	I_{DD4}	32.768-kHz Crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	55	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.2 V ± 10 %		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.2 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is unused	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.2 V ± 10 %		0.05	10	μA

Notes 1. The current flowing in the V_{DD} pin. Not including the current flowing in the A/D converter, D/A converter, and on-chip pull-up resistor.

2. f_{XX}=f_X/2 operation (when the oscillation mode selection register (OSMS) is set to 00H)

3. f_{XX} = f_X operation (when the OSMS is set to 01H)

4. When the main system clock is stopped

5. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

6. Low-speed mode operation (when the PCC is set to 04H)

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ Note 1	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			$f_{XX} = f_X$ Note 2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
		Operating on subsystem clock			40	122	125	μs
TI00, TI01, TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V			0		4	MHz
					0		275	kHz
TI00 input high-/low-level width	t_{TIH}, t_{TIL}				8/f_{sam} Note 3			μs
TI01, TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V			100			ns
					1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0			8/f_{sam} Note 3			μs
		INTP1 to INTP6, KR0 to KR7		V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V			10			μs
					20			μs

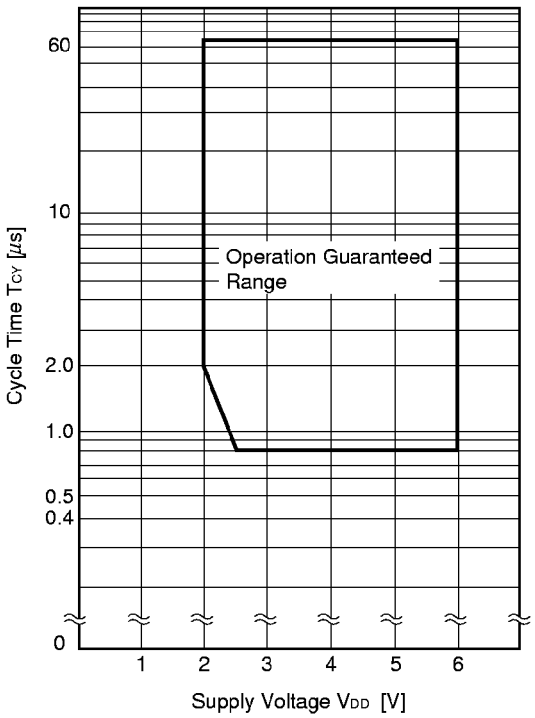
Notes 1. When oscillation mode selection register (OSMS) is set to 00H

2. When OSMS is set to 01H

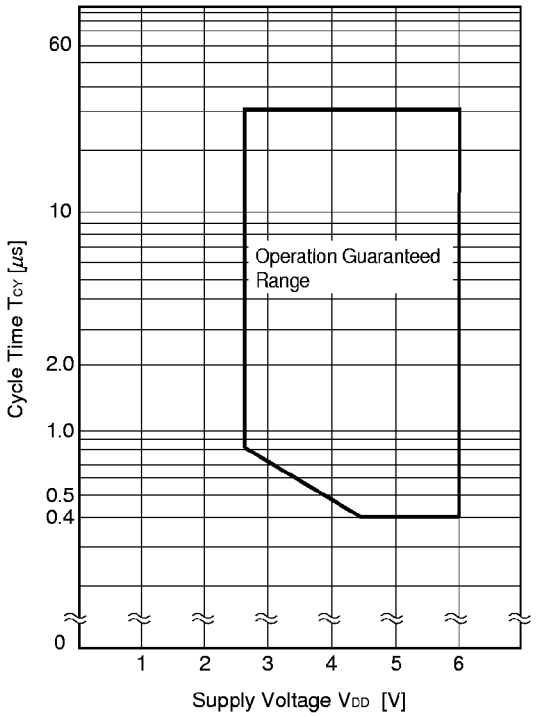
3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock selection register, f_{sam} is selectable between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ (when N = 0 to 4).

Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)
f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) READ/WRITE OPERATION

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}-50$		ns
Address setup time	t_{ADS}		$0.85t_{CY}-50$		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85+2n)t_{CY}-80$	ns
	t_{ADD2}			$(4+2n)t_{CY}-100$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2+2n)t_{CY}-100$	ns
	t_{RDD2}			$(2.85+2n)t_{CY}-100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2+2n)t_{CY}-60$		ns
	t_{RDL2}		$(2.85+2n)t_{CY}-60$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY}-50$	ns
	t_{RDWT2}			$2t_{CY}-60$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY}-60$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15+2n)t_{CY}$	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85+2n)t_{CY}-100$		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85+2n)t_{CY}-60$		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}+20$		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.85t_{CY}-10$	$1.15t_{CY}+20$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.85t_{CY}-50$	$1.15t_{CY}+50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}+40$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY}+40$	$3.15t_{CY}+40$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY}+30$	$3.15t_{CY}+30$	ns

Remarks 1. MCS: Oscillation mode selection register (OSMS) bit 0
2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0 V	t_{CY}–80		ns
			t_{CY}–150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0 V	t_{CY}–80		ns
			t_{CY}–150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY}–10		ns
			0.37t_{CY}–40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0 V		(3+2n)t_{CY}–160	ns
				(3+2n)t_{CY}–320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0 V		(4+2n)t_{CY}–200	ns
				(4+2n)t_{CY}–300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0 V		(1.4+2n)t_{CY}–70	ns
				(1.37+2n)t_{CY}–120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0 V		(2.4+2n)t_{CY}–70	ns
				(2.37+2n)t_{CY}–120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0 V	(1.4+2n)t_{CY}–20		ns
			(1.37+2n)t_{CY}–20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–20		ns
			(2.37+2n)t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0 V		t_{CY}–100	ns
				t_{CY}–200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0 V		2t_{CY}–100	ns
				2t_{CY}–200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0 V		2t_{CY}–100	ns
				2t_{CY}–200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1+2n)t_{CY}	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–60		ns
			(2.37+2n)t_{CY}–100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}	V_{DD} = 2.7 to 6.0 V	(2.4+2n)t_{CY}–20		ns
			(2.37+2n)t_{CY}–20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY}–30		ns
			0.37t_{CY}–50		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0 V	1.4t_{CY}–30		ns
			1.37t_{CY}–50		ns

Remarks **1.** MCS: Oscillation mode selection register (OSMS) bit 0

2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (2/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}–50	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY}–20		ns
			0.37t_{CY}–40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 6.0 V	t_{CY}	t_{CY}+60	ns
			t_{CY}	t_{CY}+120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY}+180	2.6t_{CY}+180	ns
			0.63t_{CY}+350	2.63t_{CY}+350	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY}+120	2.6t_{CY}+120	ns
			0.63t_{CY}+240	2.63t_{CY}+240	ns

Remarks 1. MCS: Oscillation mode selection register (OSMS) bit 0

2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) SERIAL INTERFACE (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 6.0 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2-50$			ns
				$t_{KCY3}/2-150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ,	V_{DD} = 4.5 to 6.0 V	0		250	ns
		C = 100 pF Note		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$ and SB0, SB1 output lines.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0, SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	$t_{KCY5}/2-160$			ns
				$t_{KCY5}/2-190$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	$t_{KCY5}/2-50$			ns
				$t_{KCY5}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$ and SB0, SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0, SB1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 6.0 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF [Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 6.0 V	t_{KCY9}/2–50			ns
			t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF [Note]			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	V_{DD} = 2.7 to 6.0 V	t_{KCY9}–30		t_{KCY9}+30	ns
			t_{KCY9}–60		t_{KCY9}+60	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			200			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF [Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 6.0 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of the SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF [Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

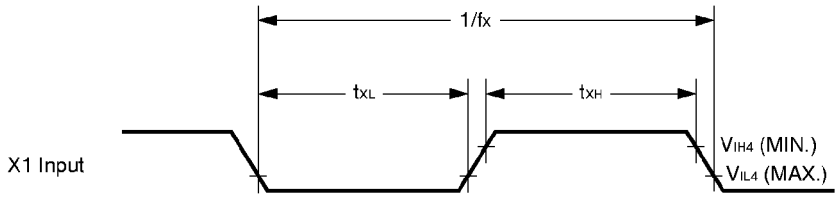
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

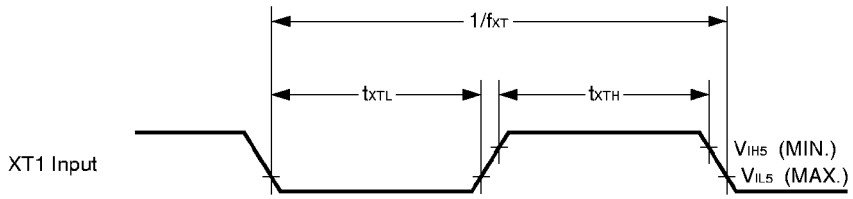
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 6.0 V, when not using external device expansion function			1000	ns
					160	ns

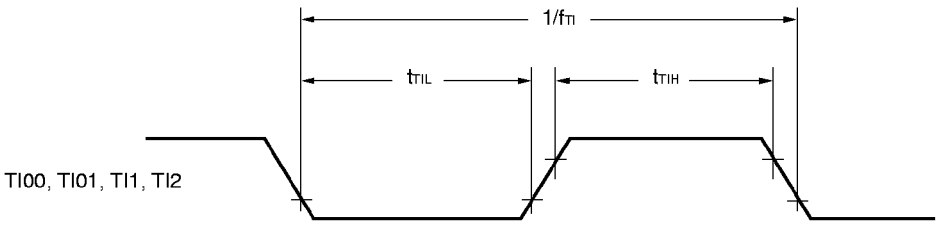
AC Timing Test Point (Excluding X1, XT1 Input)

Clock Timing



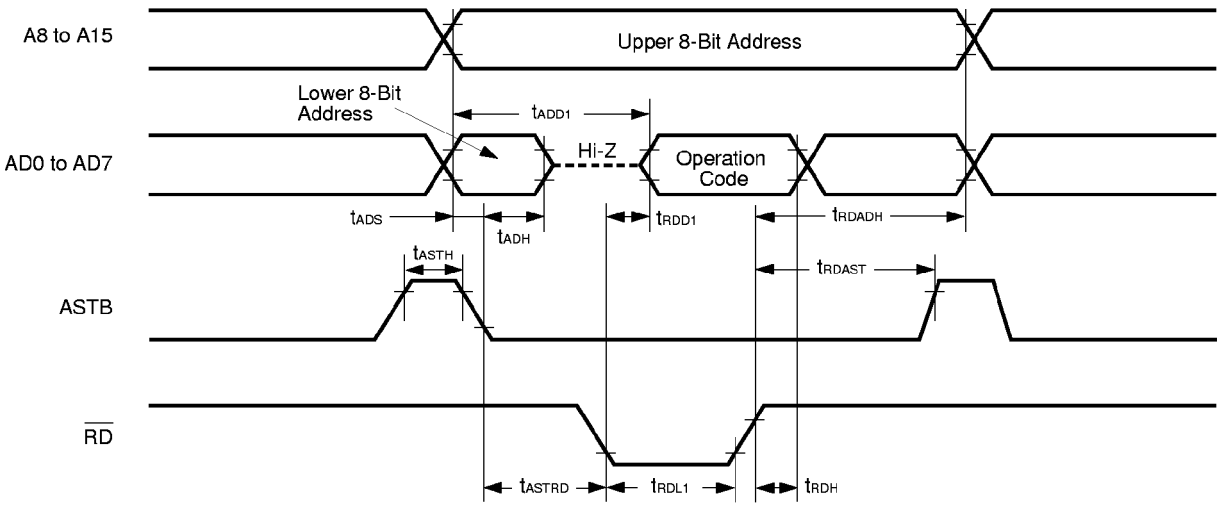


TI Timing

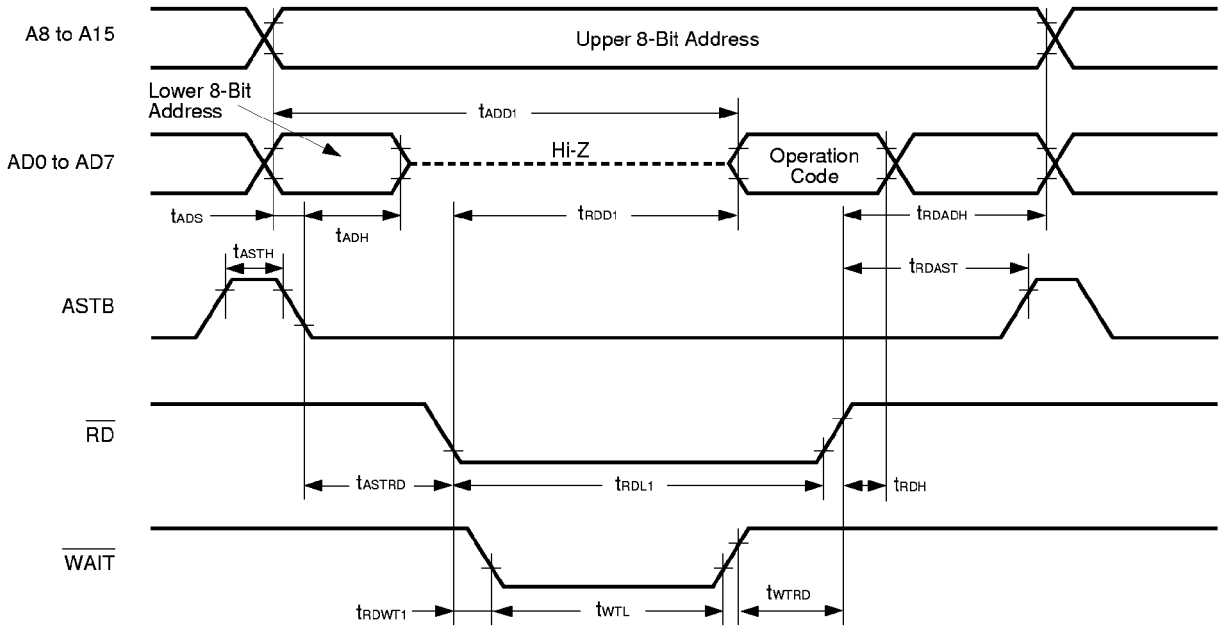


Read/Write Operation

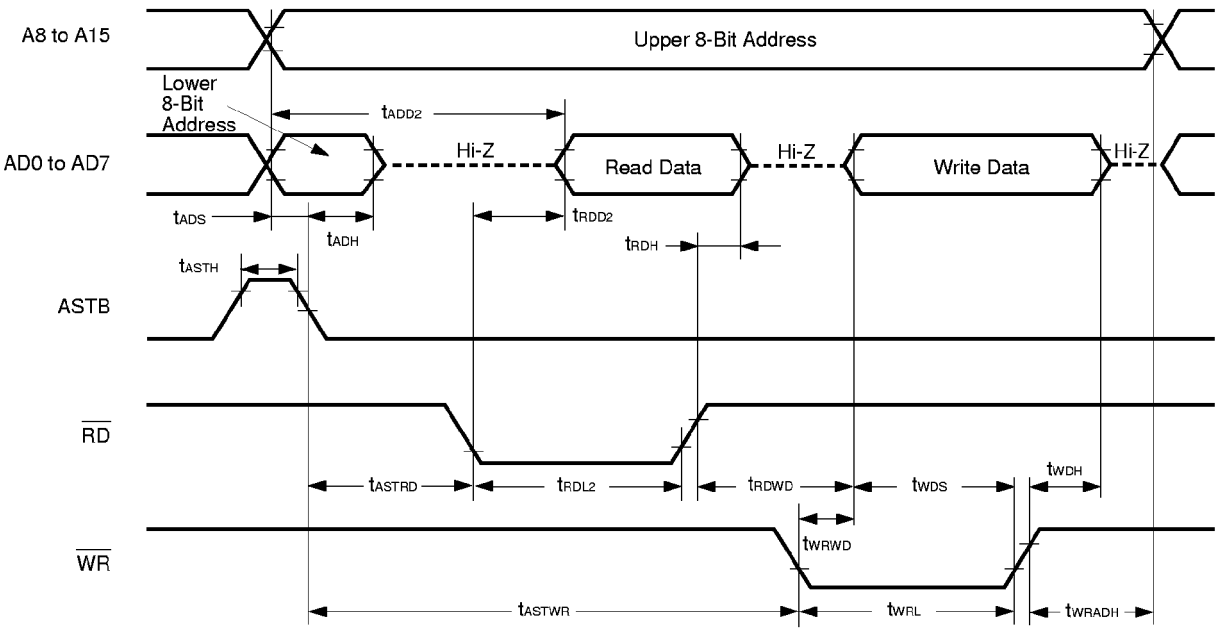
External Fetch (No Wait) :



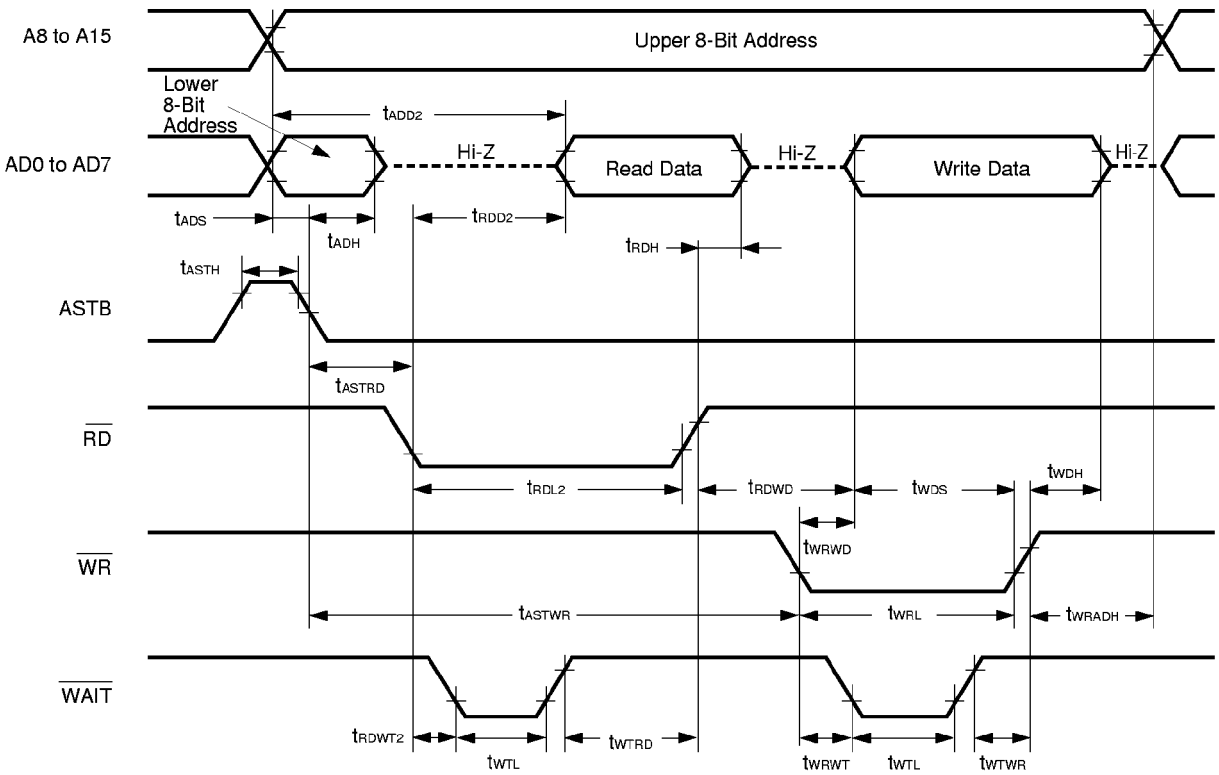
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

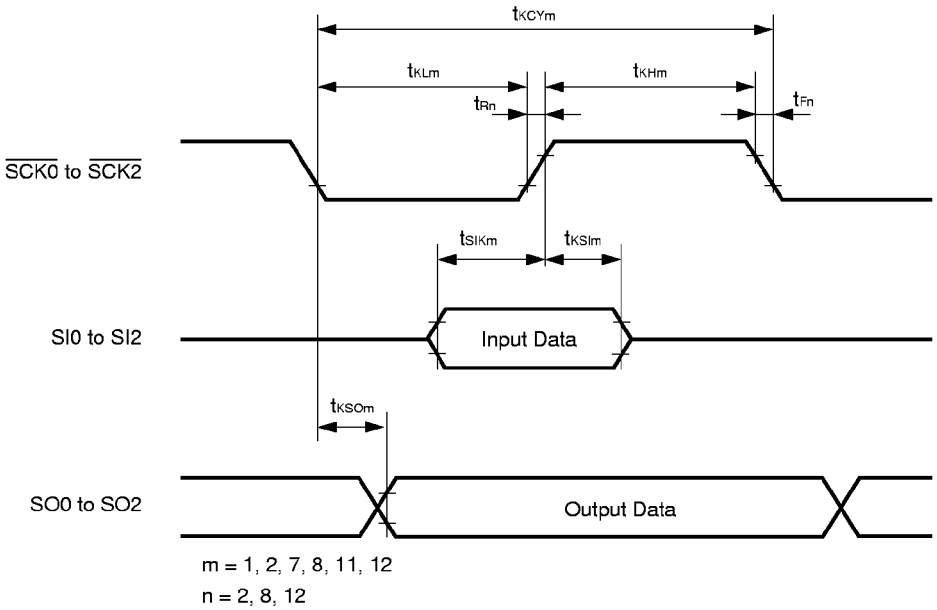


External Data Access (Wait Insertion) :



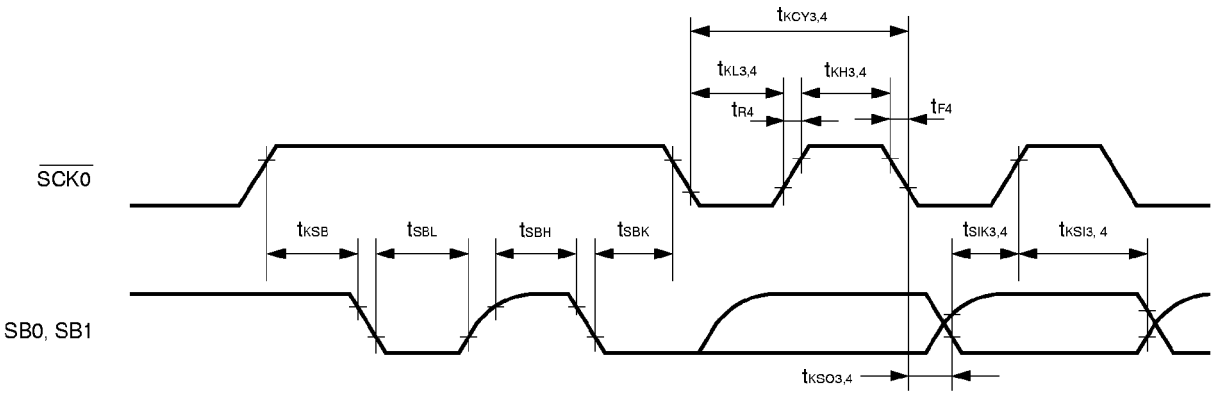
Serial Transfer Timing

3-Wire Serial I/O Mode :

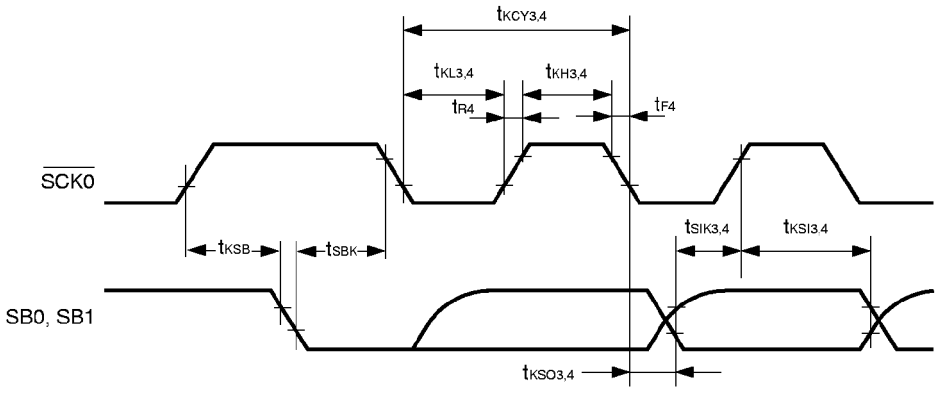


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

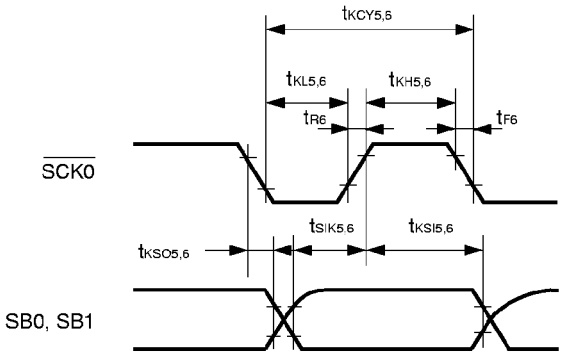
SBI Mode (Bus Release Signal Transfer) :



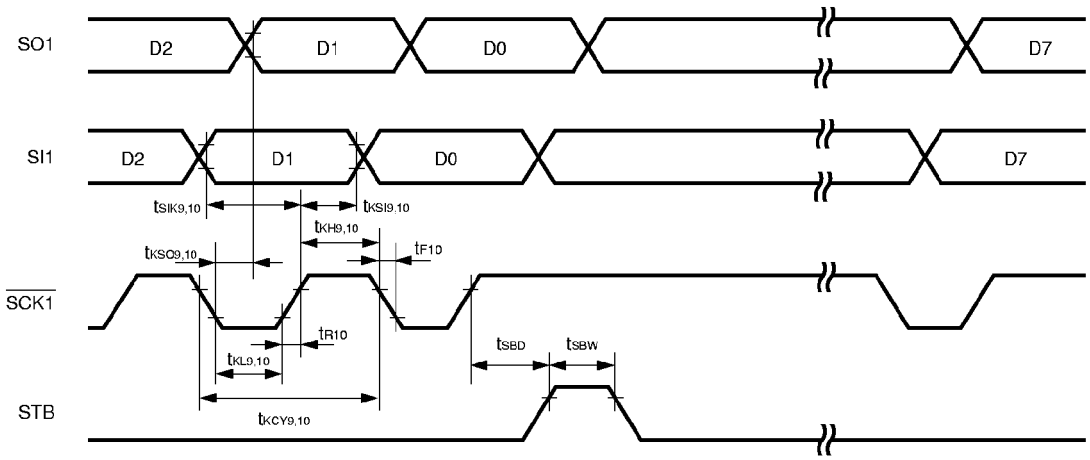
SBI Mode (Command Signal Transfer) :



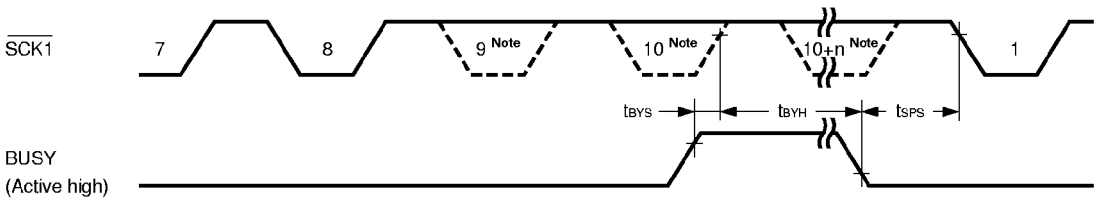
2-Wire Serial I/O Mode :



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function :

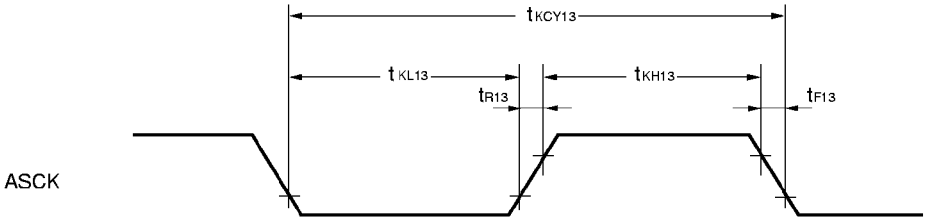


3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART Mode (External Clock Input) :



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			0.6	%
		2.0 V ≤ AV_{REF0} < 2.7 V			1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.0		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AIREF0}		4	14		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Remark fxx : Main system clock frequency (fx or fx/2)
fx : Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2 MΩ Note 1				1.2	%
		R = 4 MΩ Note 1				0.8	%
		R = 10 MΩ Note 1				0.6	%
Settling time		C = 30 pF Note 1	4.5 V ≤ AV_{REF1} ≤ 6.0 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.0 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	DACS0, DACS1 = 55H Note 2			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**				1.5	mA

Notes 1. R and C denote D/A converter output pin load resistance and load capacitance, respectively.
2. Value for one D/A converter channel

Remark DACS0, DACS1: D/A conversion value setting register 0, 1

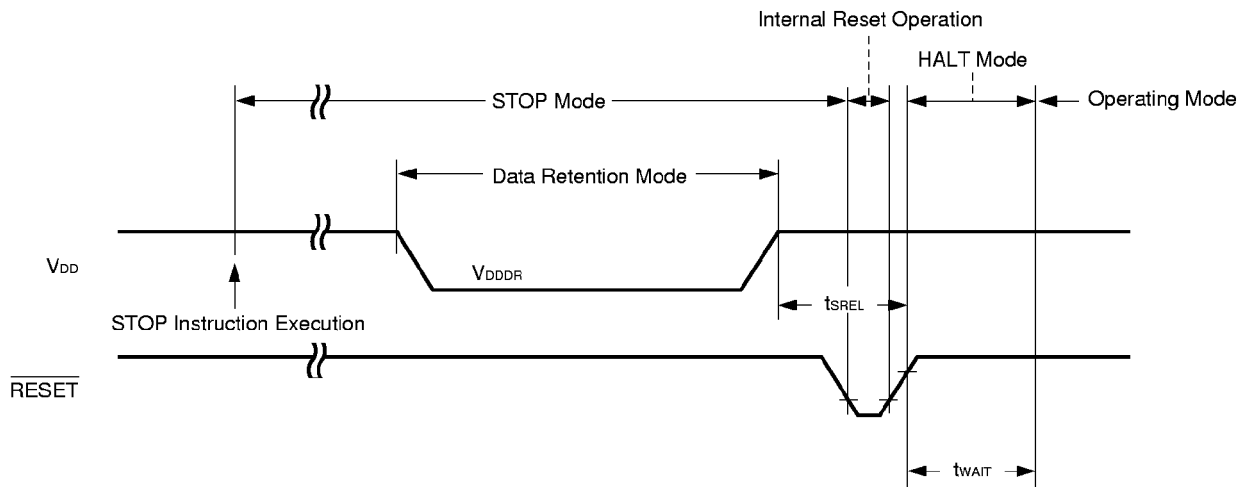
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		6.0	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt		**Note**		ms

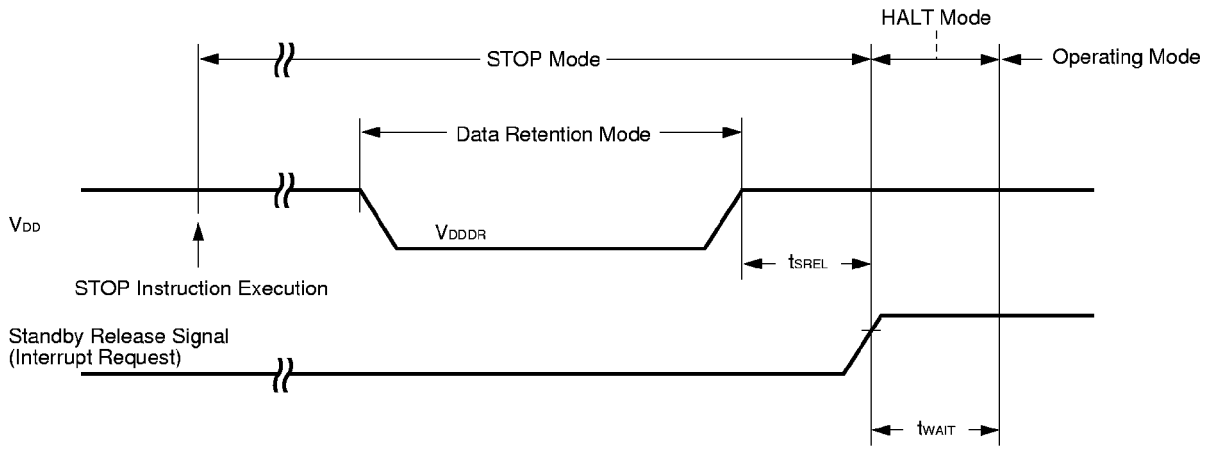
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2^{12}/fxx and 2^{14}/fxx to 2^{17}/fxx is possible.

Remark fxx : Main system clock frequency (fx or fx/2)
fx : Main system clock oscillation frequency

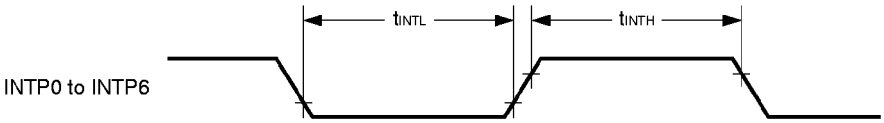
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



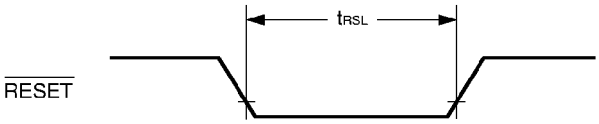
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



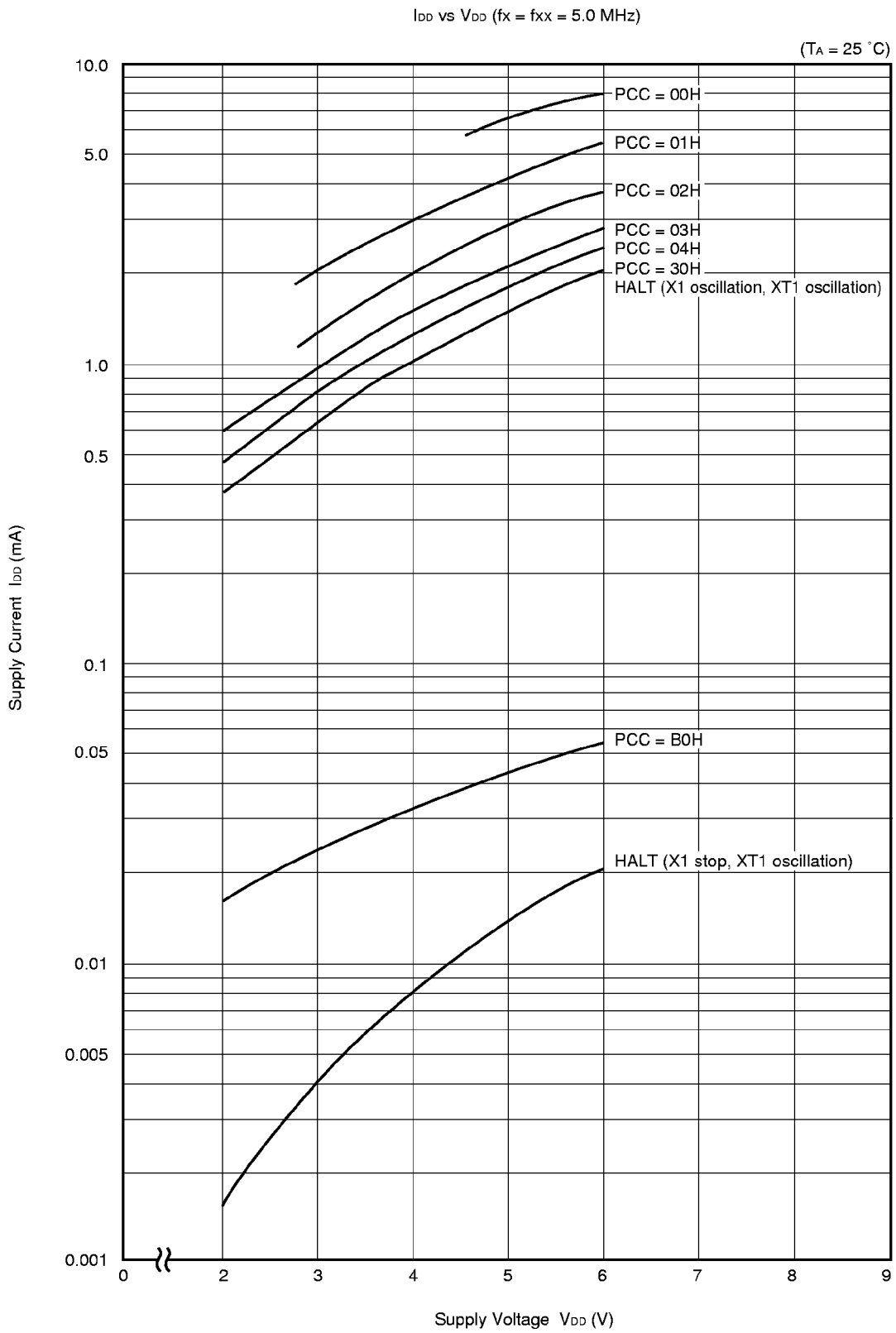
Interrupt Input Timing



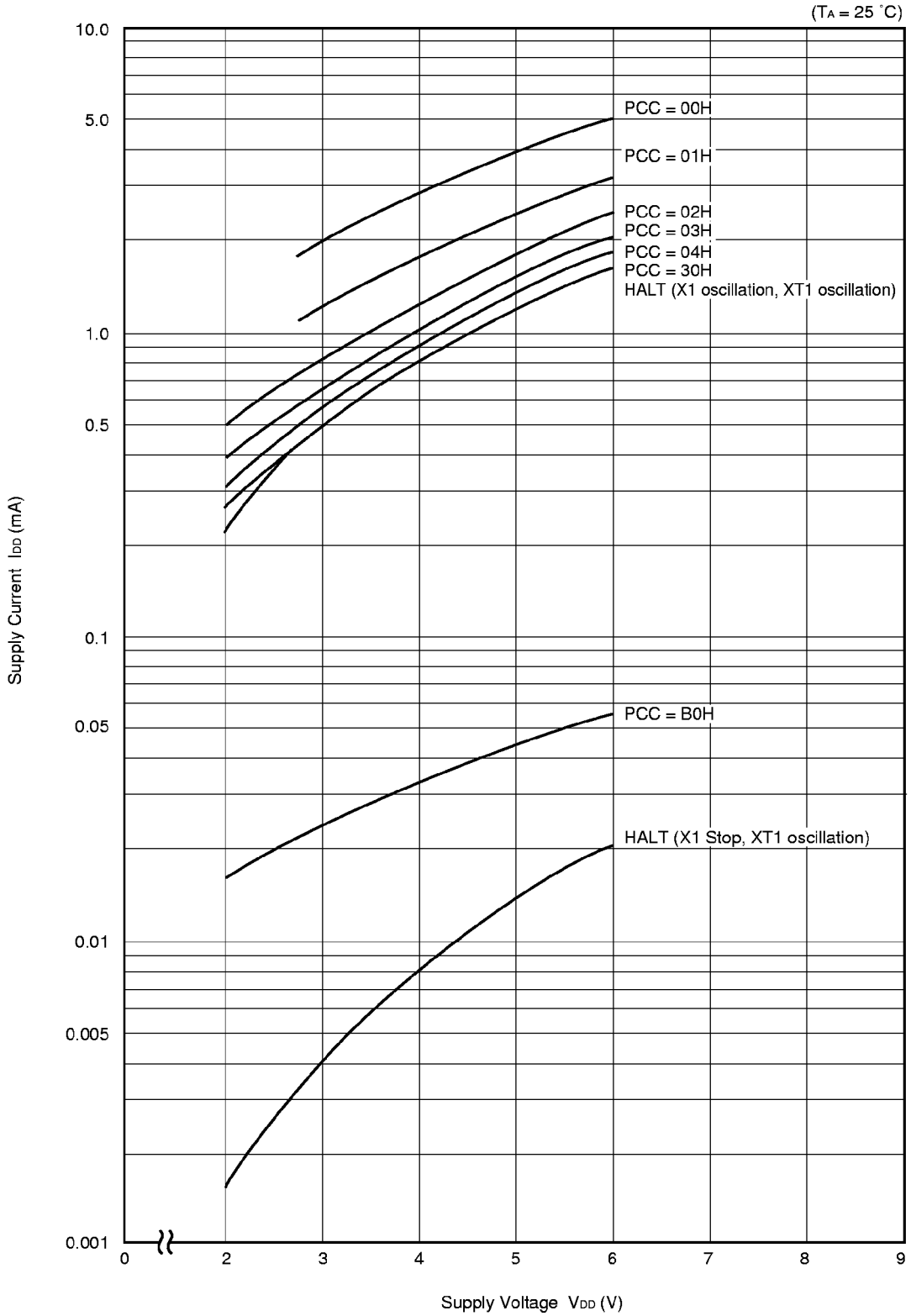
$\overline{\text{RESET}}$ Input Timing



12. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

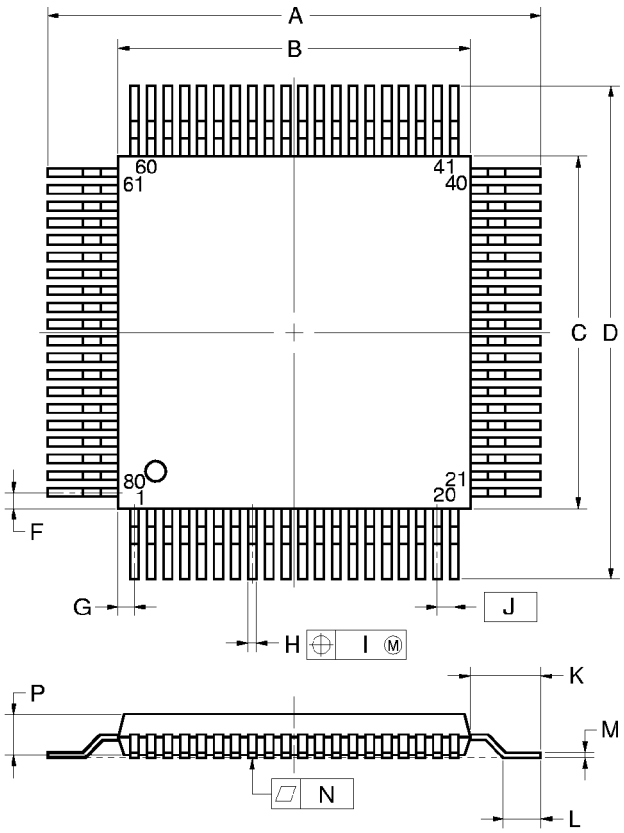


I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)

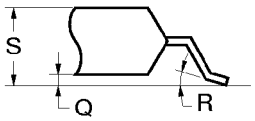


13. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

Remark Dimensions and materials of ES product are the same as those of mass-production products.

14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact our sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD78052GC(A)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)
μPD78053GC(A)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)
μPD78054GC(A)-×××-3B9 : 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or below (at 210 °C or higher), Number of reflow processes: 3 max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or below (at 200 °C or higher), Number of reflow processes: 3 max.	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow processes: once, Preheating temperature: 120 °C or below (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300 °C or below, Time: 3 seconds or below (per device side)	—

Caution Use of more than one soldering method should be avoided (except for the pin partial heating method).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78054 Subseries.

Language Processing Software

RA78K/0 Note 1, 2, 3, 4	Assembler package common to 78K/0 Series
CC78K/0 Note 1, 2, 3, 4	C compiler package common to 78K/0 Series
DF78054 Note 1, 2, 3, 4	Device file common to μPD78054 Subseries
CC78K/0-L Note 1, 2, 3, 4	C compiler library source file common to 78K/0 Series

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 Series
IE-78000-R-A	In-circuit emulator common to 78K/0 Series (for integrated debugger)
IE-78000-R-BK	Break board common to 78K/0 Series
IE-78064-R-EM	Emulation board common to μPD78064 Subseries
EP-78230GC-R	Emulation probe common to μPD78234 Subseries
EV-9200GC-80	Socket to be mounted on the target system board manufactured for 80-pin plastic QFP
SM78K0 Note 5, 6, 7	System simulator common to 78K/0 Series
ID78K0 Note 4, 5, 6, 7	Integrated debugger for IE-78000-R-A
SD78K/0 Note 1, 2	Screen debugger for IE-78000-R
DF78054 Note 1, 2, 4, 5, 6, 7	Device file for μPD78054 Subseries

Notes 1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™ (HP-UX™) based
4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

Remarks 1. For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 are used in combination with DF78054.

Real-Time OS

RX78K/0 Note 1, 2, 3, 4	Real-time OS for 78K/0 Series
MX78K0 Note 1, 2, 3, 4	OS for 78K/0 Series

Fuzzy Inference Development Support System

FE9000 Note 1/FE9200 Note 5	Fuzzy knowledge data input tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Note 1, 2	Fuzzy inference module
FD78K0 Note 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS) based
2. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS) based
3. HP9000 Series 300 (HP-UX) based
4. HP9000 Series 700 (HP-UX) based, SPARCstation (SunOS) based, EWS4800 Series (EWS-UX/V) based
5. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

Remarks 1. For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
2. RX78K/0 is used in combination with DF78054.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (English)	Document No. (Japanese)
μPD78054, 78054Y Subseries User's Manual		U11747E	U11747J
μPD78052(A), 78053(A), 78054(A) Data Sheet		This document	U12171J
78K/0 Series User's Manual Instructions		IEU-1372	IEU-849
78K/0 Series Instruction Set		–	U10904J
78K/0 Series Instruction Table		–	U10903J
μPD78054 Subseries Special Function Register Table		–	U10102J
78K/0 Series Application Note	Fundamental (III)	U10182E	IEA-767
	Floating-Point Arithmetic Programs	IEA-1289	IEA-718

Development Tool Related Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		–	EEU-777
IE-78000-R		U11376E	EEU-810
IE-78000-R-A		U10057E	U10057J
IE-78000-R-BK		EEU-1427	EEU-867
IE-78064-R-EM		EEU-1443	EEU-905
EP-78230		EEU-1515	EEU-985

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

Document Name		Document No. (English)	Document No. (Japanese)
SM78K0 System Simulator, Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0 Integrated Debugger, EWS based	Reference	–	U11151J
ID78K0 Integrated Debugger, PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger, Windows based	Guide	U11649E	U11649J
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) based	Introduction	–	EEU-852
	Reference	–	U10952J
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) based	Introduction	EEU-1414	EEU-5024
	Reference	U11279E	U11279J

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	–	U11537J
	Installation	–	U11536J
	Technical	–	U11538J
78K/0 Series OS MX78K0	Basics	–	EEU-5010
Fuzzy Knowledge Data Input Tools		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Knowledge Debugger		EEU-1458	EEU-921

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	–	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	C11893J
Microcomputer Product Series Guide	–	U11416J

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.