NEC

MOS INTEGRATED CIRCUIT
μPD780232

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780232 is a member of the μPD780232 Subseries in the 78K/0 Series.

The μPD780232 Subseries consists of products that incorporate a VFD controller/driver for panel control.

A flash memory version, the μPD78F0233, that can operate within the same power supply voltage range as the mask ROM version, and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780232 Subseries User's Manual: U13364E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- I/O ports: 40
- Internal ROM and RAM
  - Internal ROM: 16 KB
  - Internal high-speed RAM: 768 bytes
  - Internal buffer RAM: 32 bytes
  - VFD display RAM: 112 bytes
- Minimum instruction execution time can be changed from high speed (0.4 μs) to low speed (6.4 μs)
- VFD controller/driver: 53 display outputs (Universal grid supported)
- 8-bit resolution A/D converter: 4 channels
- Serial interface: 2 channels
- Timer: 4 channels
- Power supply voltage: V_{DD} = 4.5 to 5.5 V

APPLICATIONS

Monolithic mini components, separated mini components, tuners, cassette tape decks, CD/MD players, audio amplifiers, etc.

ORDERING INFORMATION

Part Number	Package
μPD780232GC-×××-8BT	80-pin plastic QFP (14 × 14)

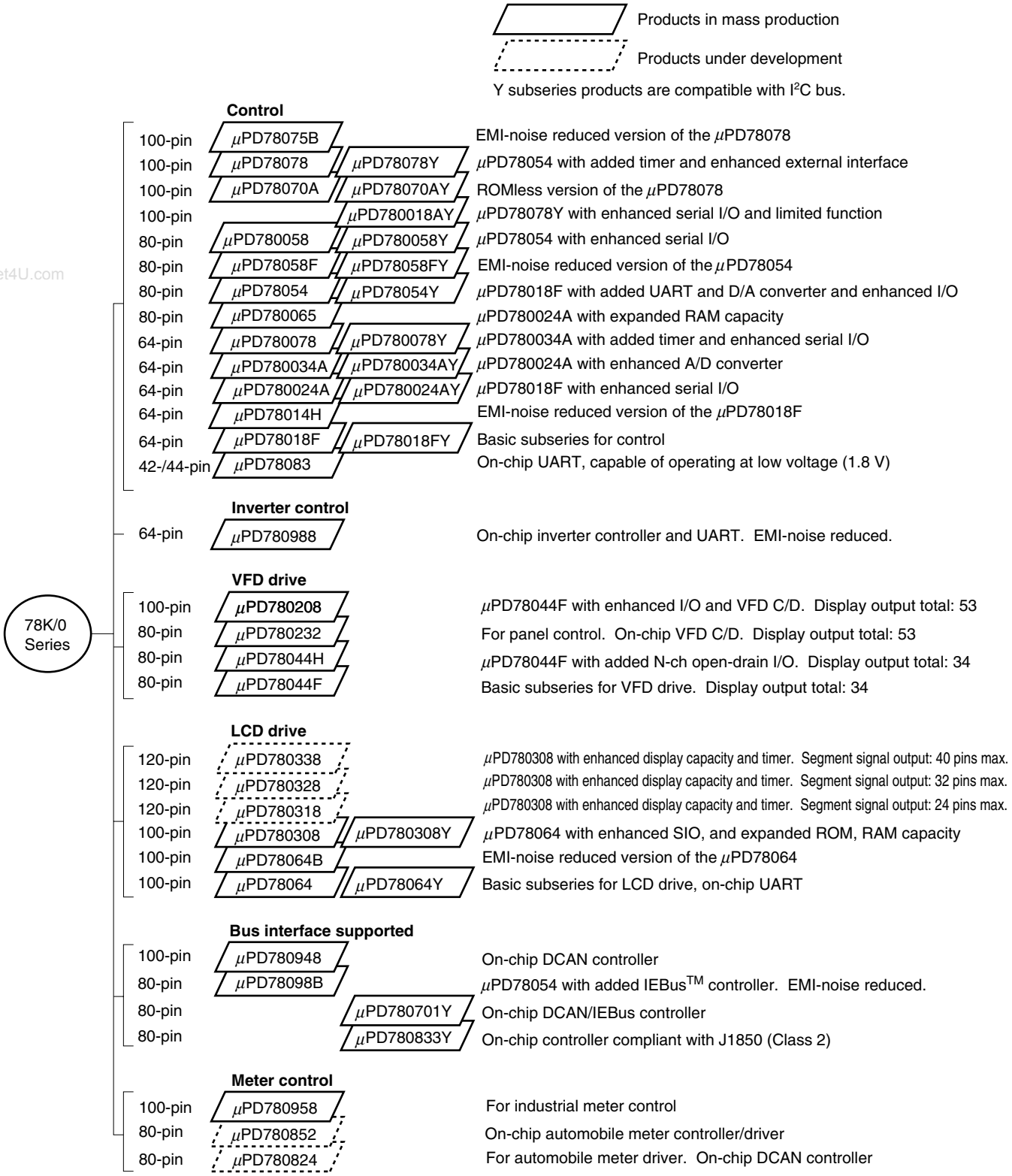
Remark ××× indicates ROM code suffix.

Document No. U13415EJ2V0DS00 (2nd edition)
Date Published May 2001 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

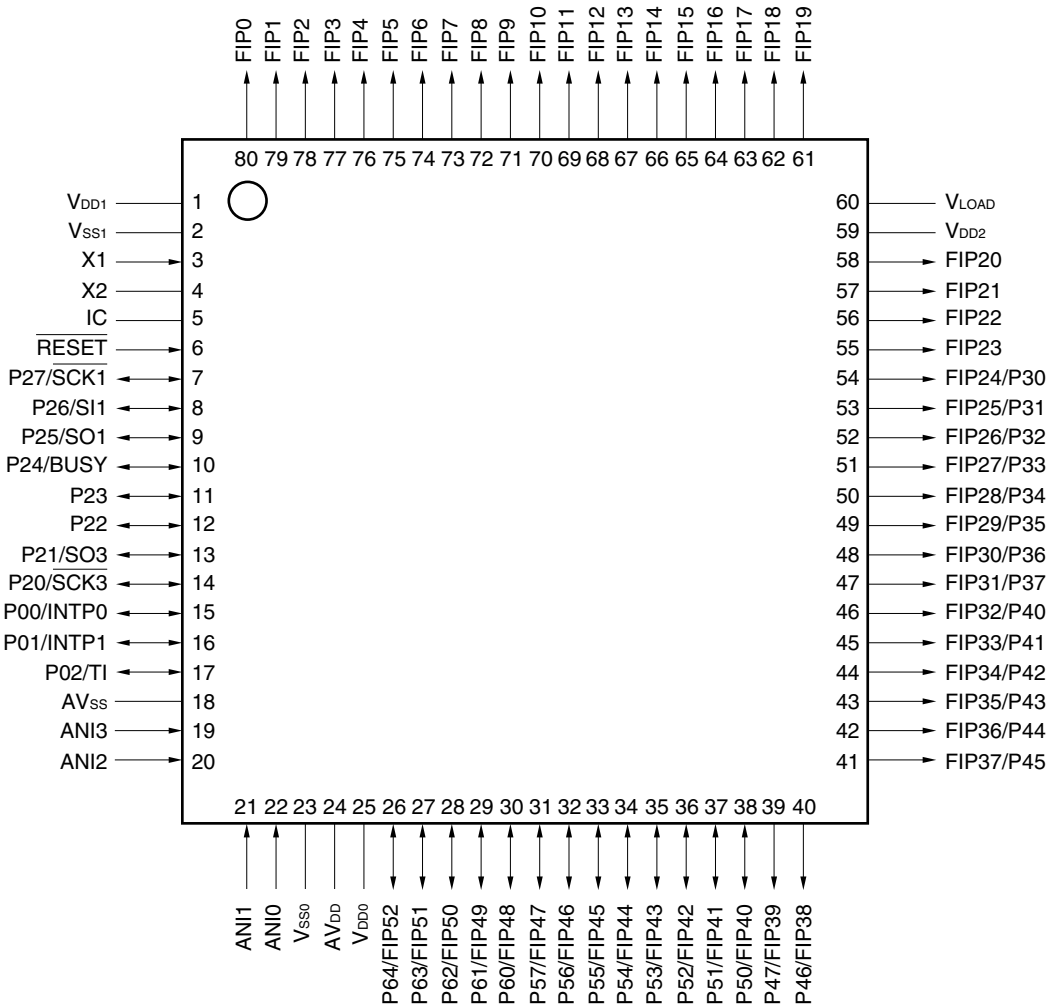
FUNCTION OVERVIEW

Item		Function
Internal memory	ROM	16 KB
	High-speed RAM	768 bytes
	Buffer RAM	32 bytes
	VFD display RAM	112 bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		• On-chip minimum instruction execution time variable function • 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0 MHz operation with system clock)
Instruction set		• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation)
I/O ports (including alternate-function pins for VFD)		Total: 40 • CMOS I/Os: 11 • P-ch open-drain I/Os: 13 • P-ch open-drain outputs: 16
VFD controller/driver		Total of display outputs: 53 • 15 mA display current: 20 • 5 mA display current: 33
A/D converter		• 8-bit resolution × 4 channels • Power supply voltage: AV_{DD} = 4.5 to 5.5 V
Serial interface		• 3-wire serial mode (automatic transmit/receive function): 1 channel • 2-wire serial mode (transmit only): 1 channel
Timer		• 8-bit remote control timer: 1 channel • 8-bit timer: 2 channels • Watchdog timer: 1 channel
Vectored interrupt sources	Maskable	Internal: 10, external: 2
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.5 to 5.5 V
Package		80-pin plastic QFP (14 × 14)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**
  μPD780232GC-×××-8BT



Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS1}.

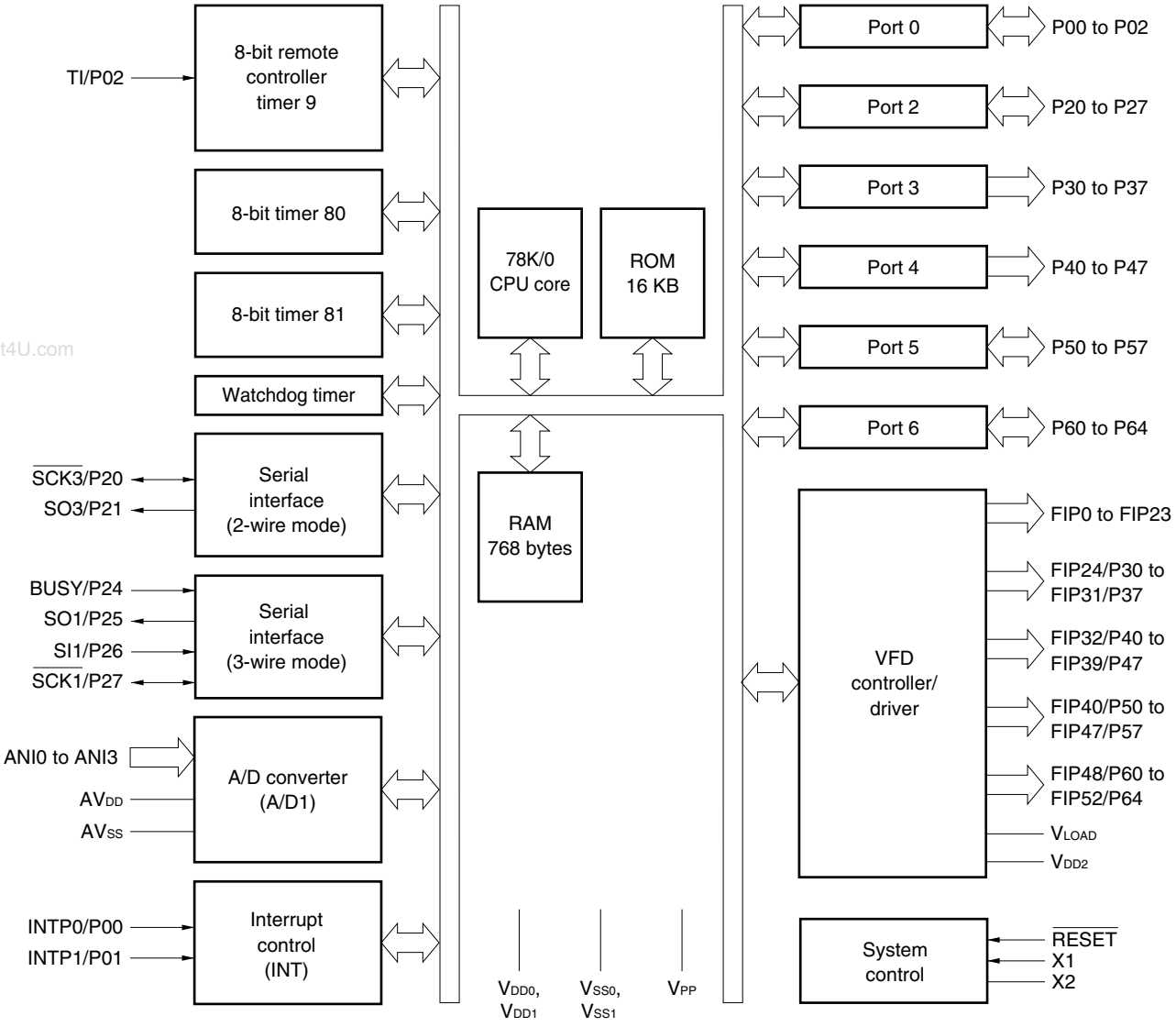
2. Connect the AV_{DD} pin to V_{DD1}.

3. Connect the AV_{SS} pin to V_{SS1}.

Remark When the μPD780232 is used in application fields that require reduction of the noise from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI3:	Analog input	P50 to P57:	Port 5
AV_{DD}:	Analog power supply	P60 to P64:	Port 6
AV_{SS}:	Analog ground	$\overline{RESET}$:	Reset
BUSY:	Busy	$\overline{SCK1}$, $\overline{SCK3}$:	Serial clock
FIP0 to FIP52:	Fluorescent indicator panel	SI1:	Serial input
IC:	Internally connected	SO1, SO3:	Serial output
INTP0, INTP1	External interrupt input	TI:	Timer input
P00 to P02:	Port 0	V_{DD0} to V_{DD2}:	Power supply
P20 to P27:	Port 2	V_{LOAD}:	Negative power supply
P30 to P37:	Port 3	V_{SS0}, V_{SS1}:	Ground
P40 to P47:	Port 4	X1, X2:	Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	INTP0
P01				INTP1
P02				TI
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	$\overline{SCK3}$
P21				SO3
P22, P23				—
P24				BUSY
P25				SO1
P26				SI1
P27				$\overline{SCK1}$
P30 to P37	Output	Port 3. P-ch open-drain 8-bit high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by mask option.	Output	FIP24 to FIP31
P40 to P47	Output	Port 4. P-ch open-drain 8-bit high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by mask option.	Output	FIP32 to FIP39
P50 to P57	I/O	Port 5. P-ch open-drain 8-bit high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units).	Input	FIP40 to FIP47
P60 to P64	I/O	Port 6. P-ch open-drain 5-bit high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units).	Input	FIP48 to FIP52

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00
INTP1				P01
TI	Input	8-bit remote control timer 9 (TM9) timer input	Input	P02
$\overline{SCK3}$	I/O	Serial interface serial clock input/output	Input	P20
SO3	Output	Serial interface serial data output	Input	P21
BUSY	Input	Serial interface automatic transmit/receive busy signal input	Input	P24
SO1	Output	Serial interface serial data output	Input	P25
SI1	Input	Serial interface serial data input	Input	P26
$\overline{SCK1}$	I/O	Serial interface serial clock input/output	Input	P27
FIP0 to FIP23	Output	VFD controller/driver high-tolerance large current output. A pull-down resistor can be incorporated to V_{LOAD} in 1-bit units by a mask option.	Output	—
FIP24 to FIP31				P30 to P37
FIP32 to FIP39				P40 to P47
FIP40 to FIP47		VFD controller/driver high-tolerance large current output. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units).	Input	P50 to P57
FIP48 to FIP52				P60 to P64
V_{LOAD}	—	Connecting pull-down resistor for VFD controller/driver	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for system clock oscillation	—	—
X2	—		—	—
ANI0 to ANI3	Input	A/D converter analog input	Input	—
AV_{DD}	—	A/D converter analog power supply/reference voltage input. Make the same potential as V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential. Make the same potential as V_{SS1}.	—	—
V_{DD0}	—	Positive power supply for ports	—	—
V_{DD1}	—	Positive power supply except for ports, analog block, and VFD controller/driver	—	—
V_{DD2}	—	Positive power supply for VFD controller/driver	—	—
V_{SS0}	—	Ground potential for ports	—	—
V_{SS1}	—	Ground potential except for ports and analog block	—	—
IC	—	Internally connected. Connect directly to V_{SS1}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

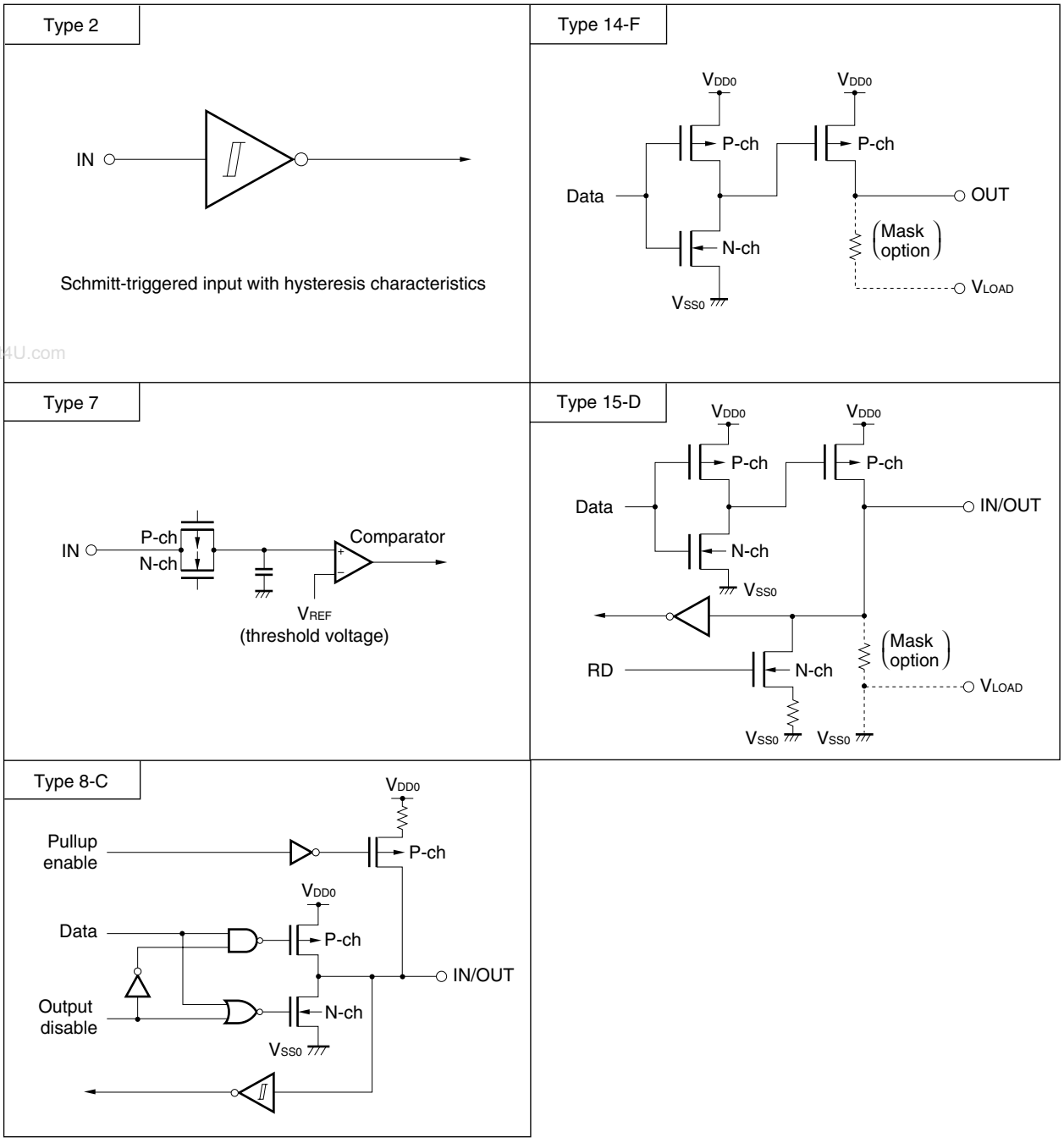
The I/O circuit type of each pin and the recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, see **Figure 3-1**.

★ **Table 3-1. Types of Pin I/O Circuits**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor.
P01/INTP1			Output: Leave open.
P02/TI			
P20/$\overline{SCK3}$			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P21/SO3			Output: Leave open.
P22, P23			
P24/BUSY			
P25/SO1			
P26/SI1			
P27/$\overline{SCK1}$			
P30/FIP24 to P37/FIP31	14-F	Output	Leave open.
P40/FIP32 to P47/FIP39			
P50/FIP40 to P57/FIP47	15-D	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P60/FIP48 to P64/FIP52			Output: Leave open.
FIP0 to FIP23	14-F	Output	Leave open.
$\overline{RESET}$	2	Input	—
ANI0 to ANI3	7		Connect to V_{DD0} or V_{SS0}.
AV_{DD}	—	—	Connect to V_{DD1}.
AV_{SS}			Connect to V_{SS1}.
V_{LOAD}			
IC			Connect directly to V_{SS1}.

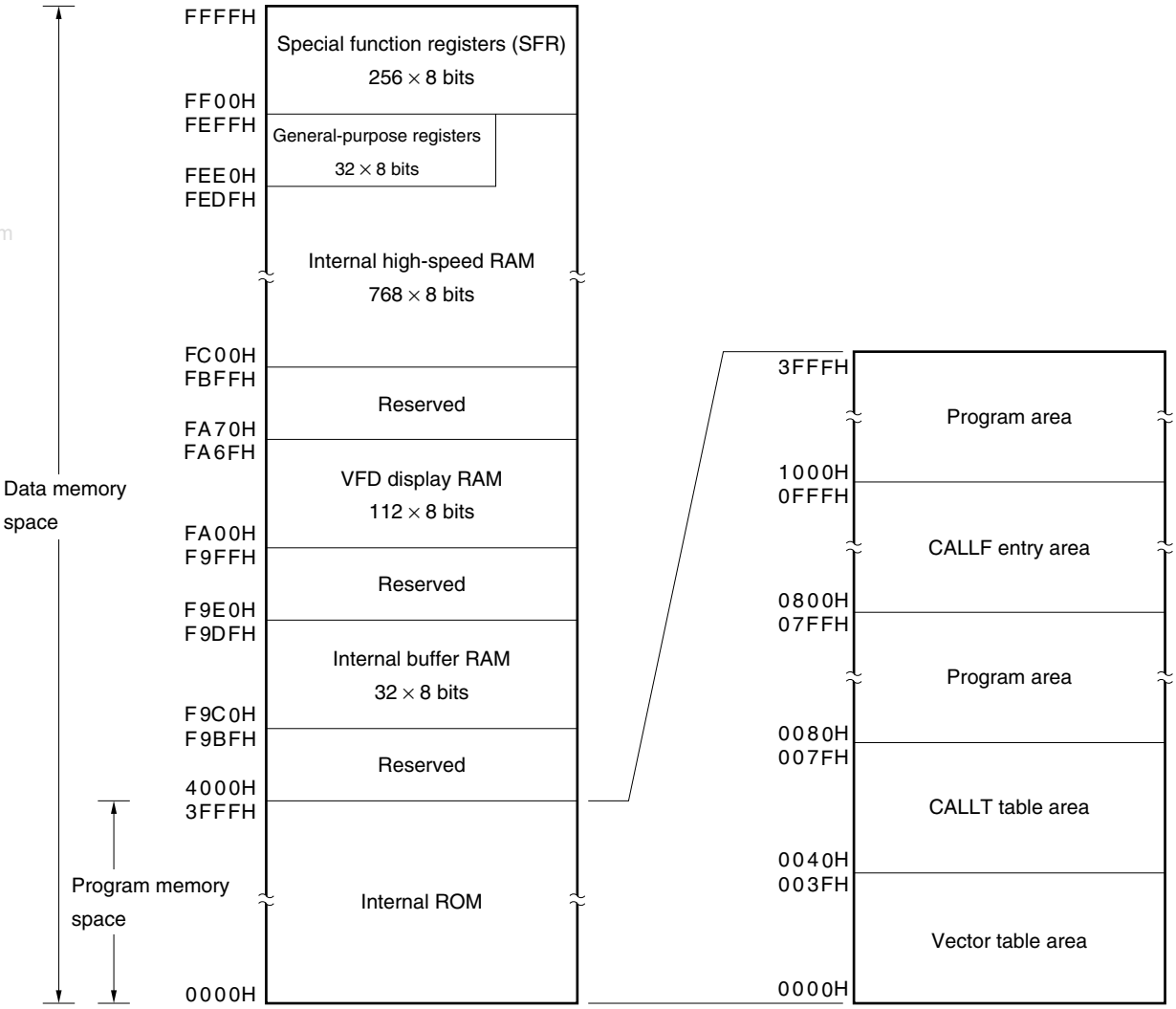
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

The memory map of the μPD780232 is shown in Figure 4-1.

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Port

There are three kinds of I/O ports.

- CMOS I/O (ports 0, 2): 11
- P-ch open-drain output (ports 3, 4): 16
- P-ch open-drain I/O (ports 5, 6): 13

Total: 40

Table 5-1. Port Functions

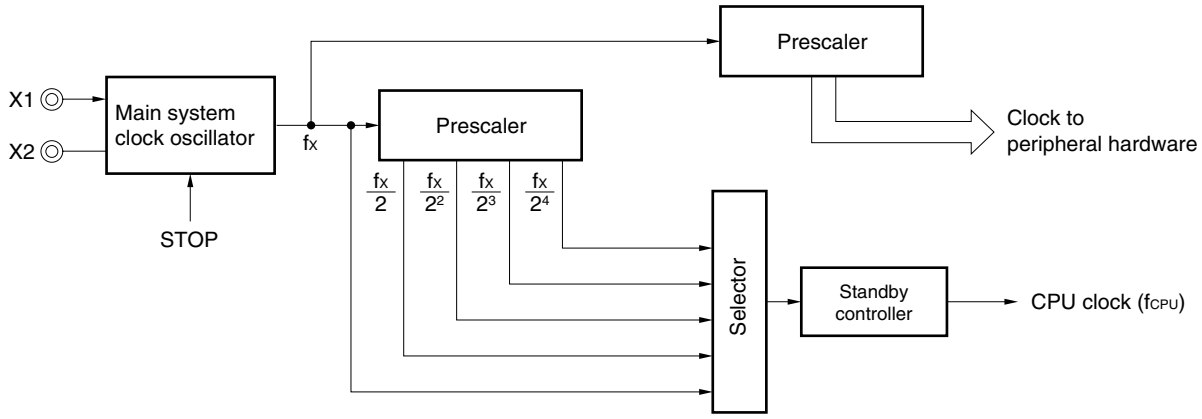
Name	Pin Name	Function
Port 0	P00 to P02	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip resistor can be specified by software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip resistor can be specified by software.
Port 3	P30 to P37	P-ch open-drain high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by a mask option.
Port 4	P40 to P47	P-ch open-drain high-tolerance output port. A pull-down resistor can be incorporated in 1-bit units to V_{LOAD} by a mask option.
Port 5	P50 to P57	P-ch open-drain high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units).
Port 6	P60 to P64	P-ch open-drain high-tolerance I/O port. Input/output can be specified in 1-bit units. A pull-down resistor can be incorporated in 1-bit units by a mask option (Connection to V_{LOAD} or V_{SS0} can be specified in 1-bit units).

5.2 Clock Generator

The minimum instruction execution time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0 MHz operation with main system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

Four timer/event counter channels are incorporated.

- 8-bit remote control timer: 1 channel
- 8-bit timer: 2 channels
- Watchdog timer: 1 channel

Table 5-2. Timer/Event Counter Operations

		8-Bit Remote Control Timer	8-Bit Timer	Watchdog Timer
Operation mode	Interval timer	—	2 channels	1 channel
Function	Pulse width measurement	1 input	—	—
	Interrupt source	3	2	1

Figure 5-2. Block Diagram of 8-Bit Remote Control Timer (TM9)

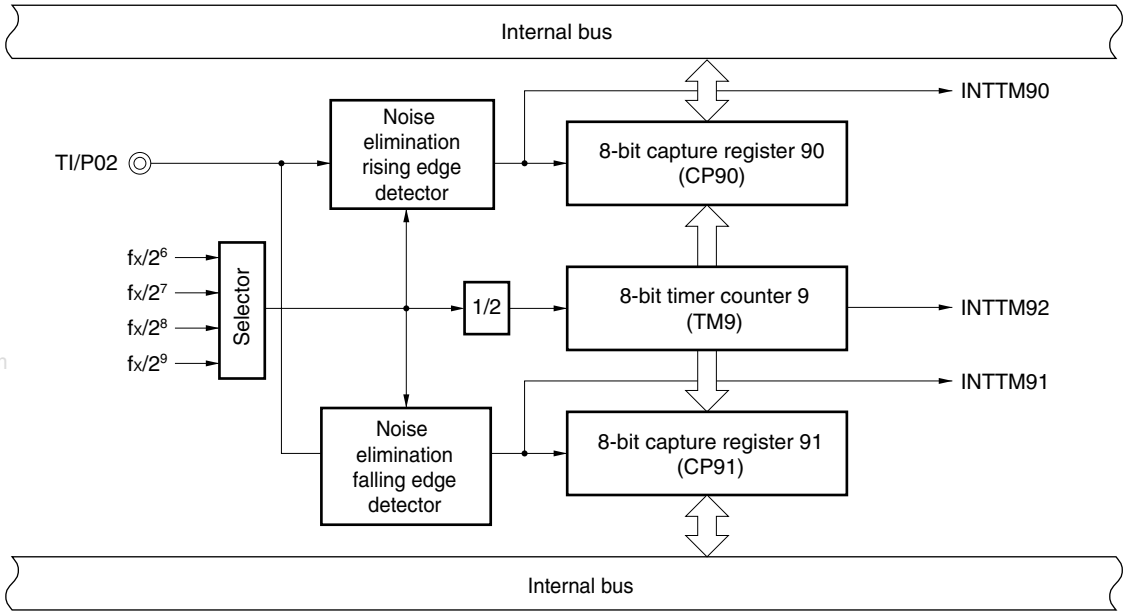


Figure 5-3. Block Diagram of 8-Bit Timer (TM80)

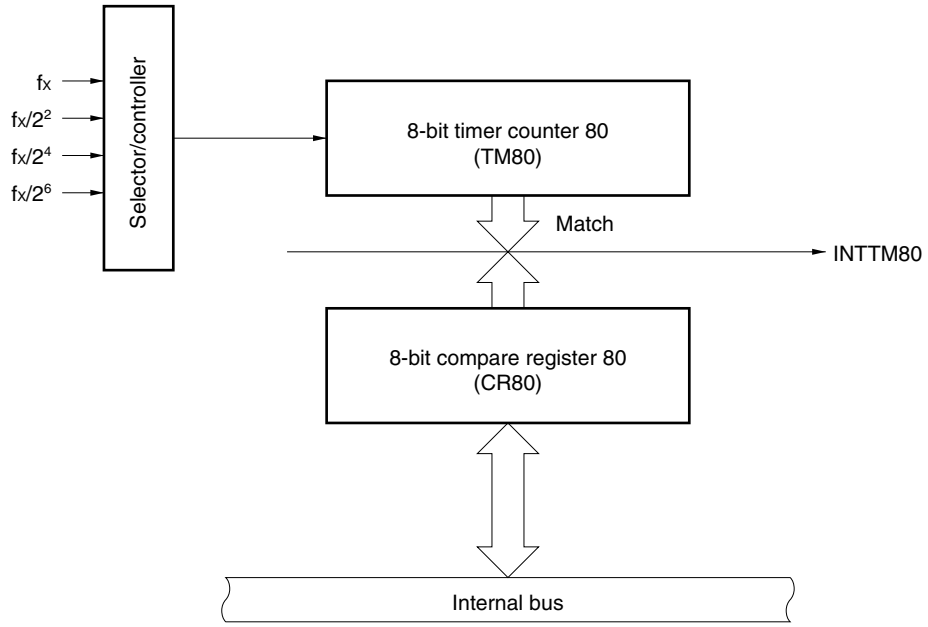
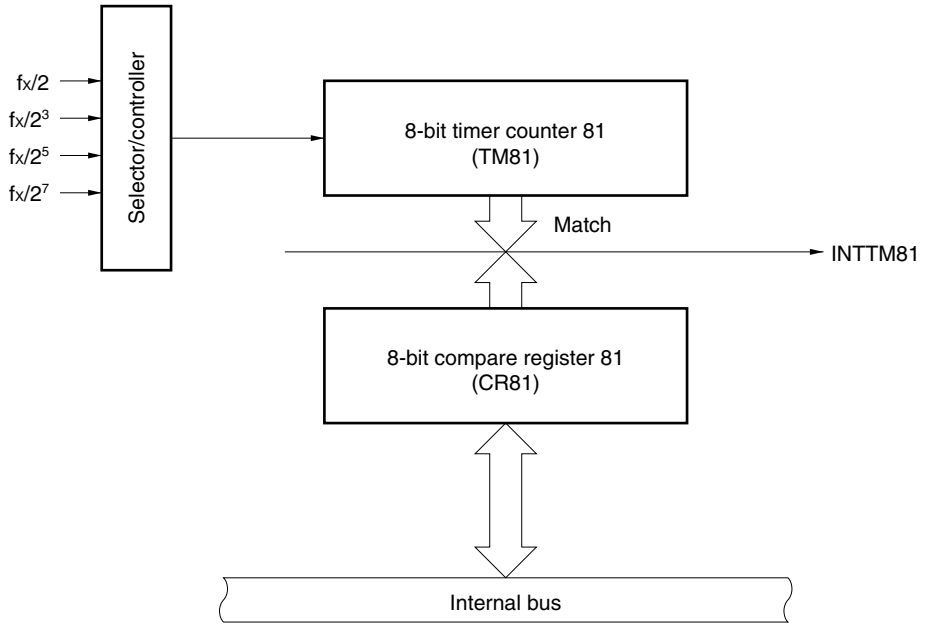
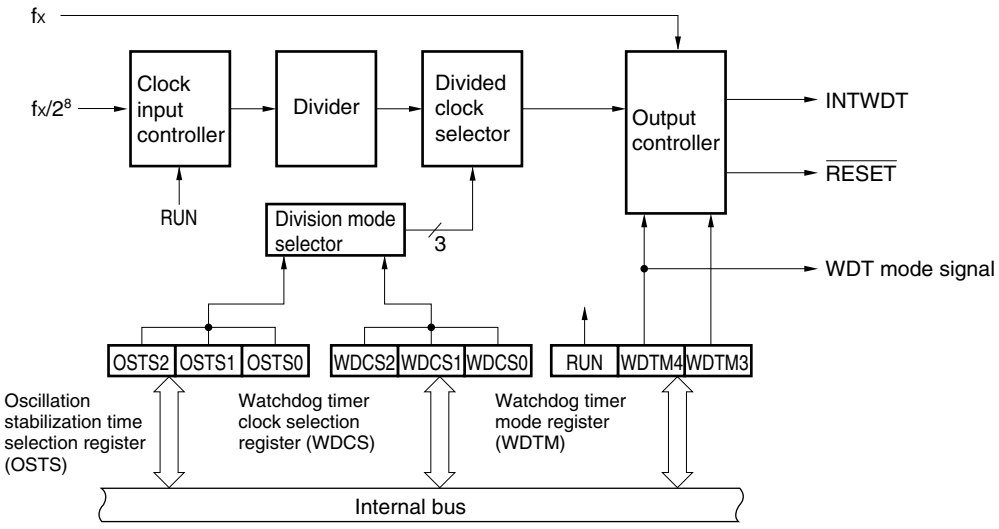


Figure 5-4. Block Diagram of 8-Bit Timer (TM81)



★ **Figure 5-5. Watchdog Timer Block Diagram**

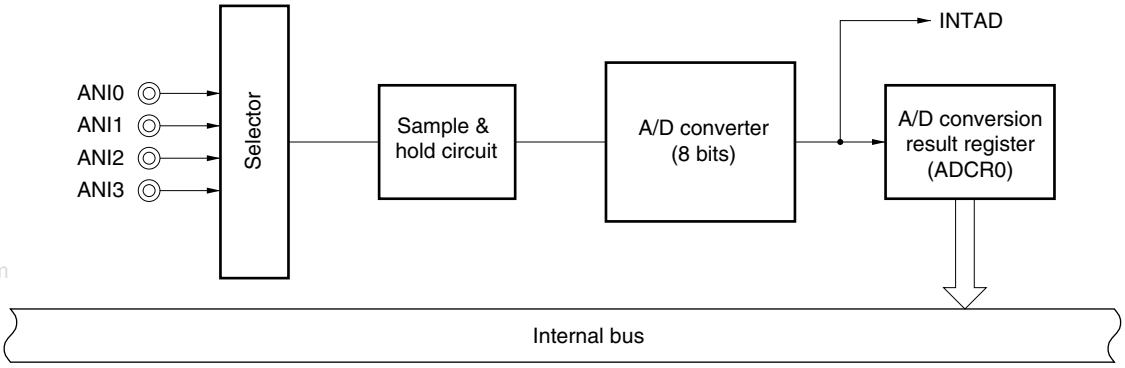


5.4 A/D Converter

An 8-bit resolution 4-channel A/D converter is incorporated.

A/D conversion can be started by software only.

Figure 5-6. A/D Converter Block Diagram



5.5 Serial Interface

Two clocked serial interface channels are incorporated.

Serial interface SIO1 operates in the 3-wire serial mode (with automatic transmit/receive function), in which MSB first/LSB first switching is possible.

Serial interface SIO3 operates in the 2-wire serial mode (transmit only) in which the first bit is fixed to MSB.

Figure 5-7. Serial Interface SIO1 Block Diagram

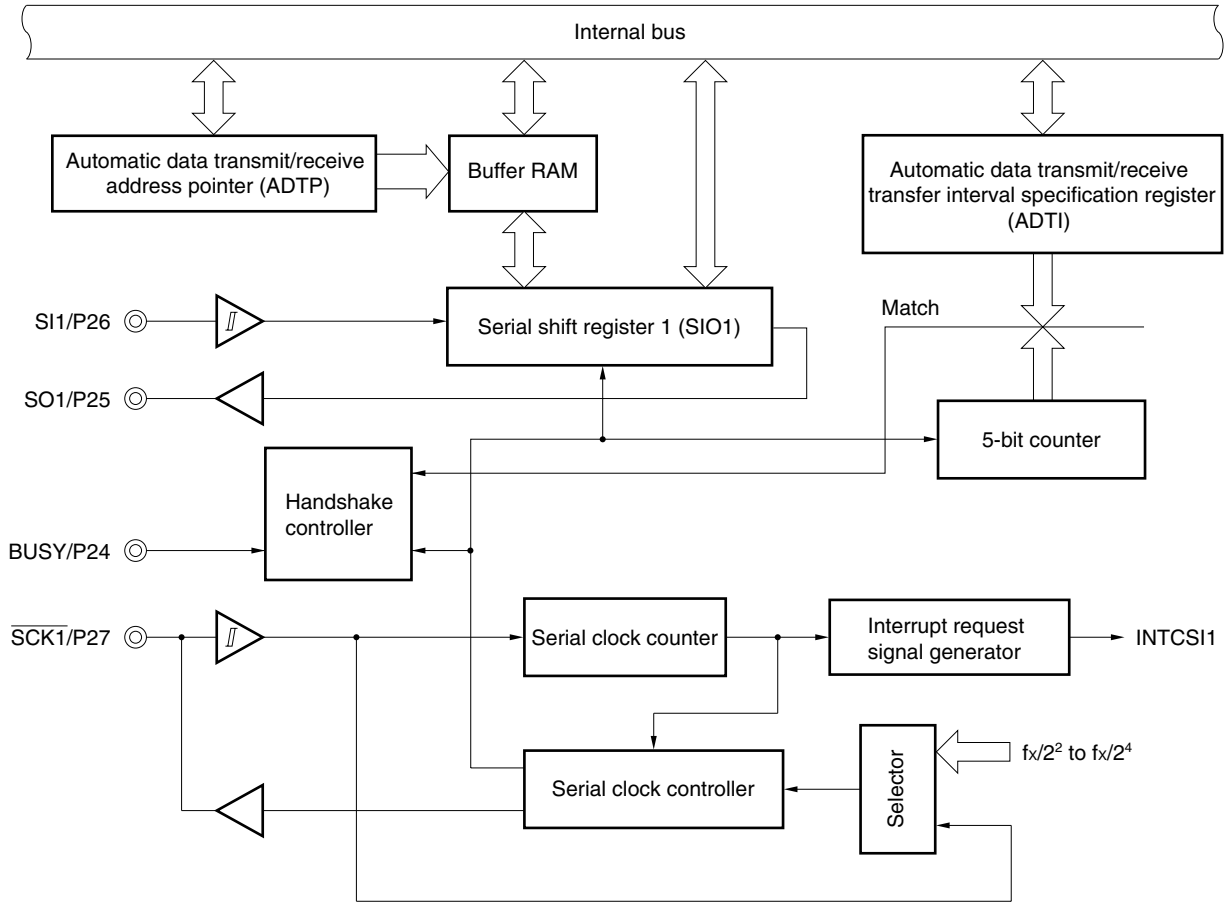
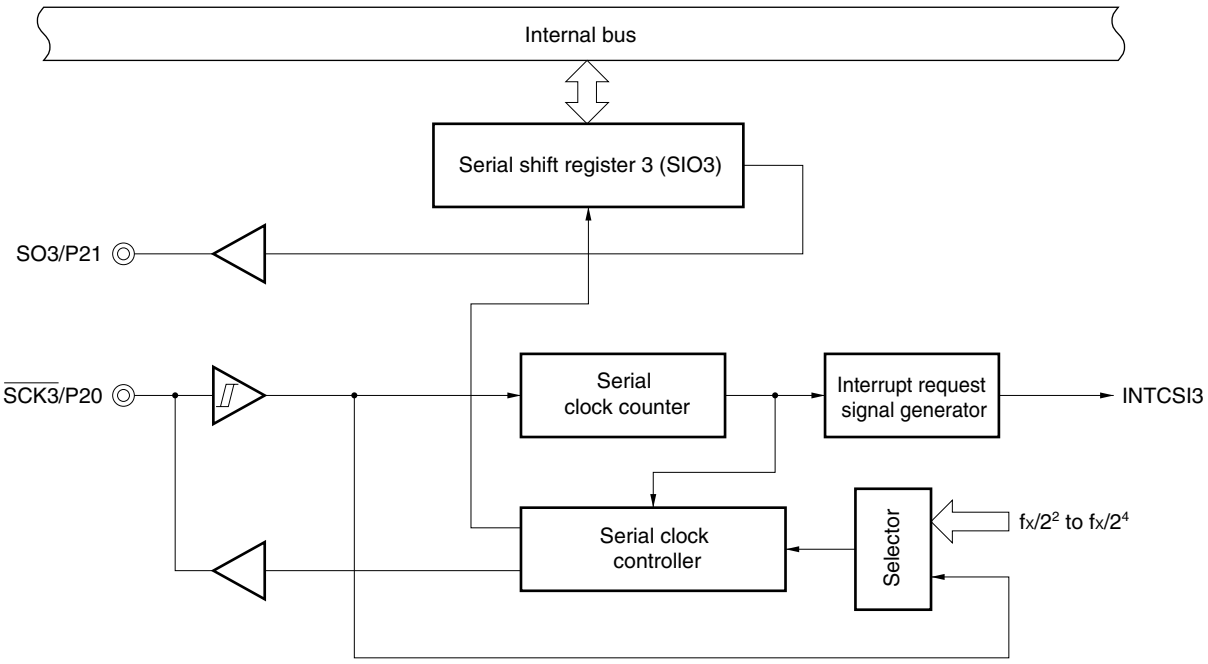


Figure 5-8. Serial Interface SIO3 Block Diagram

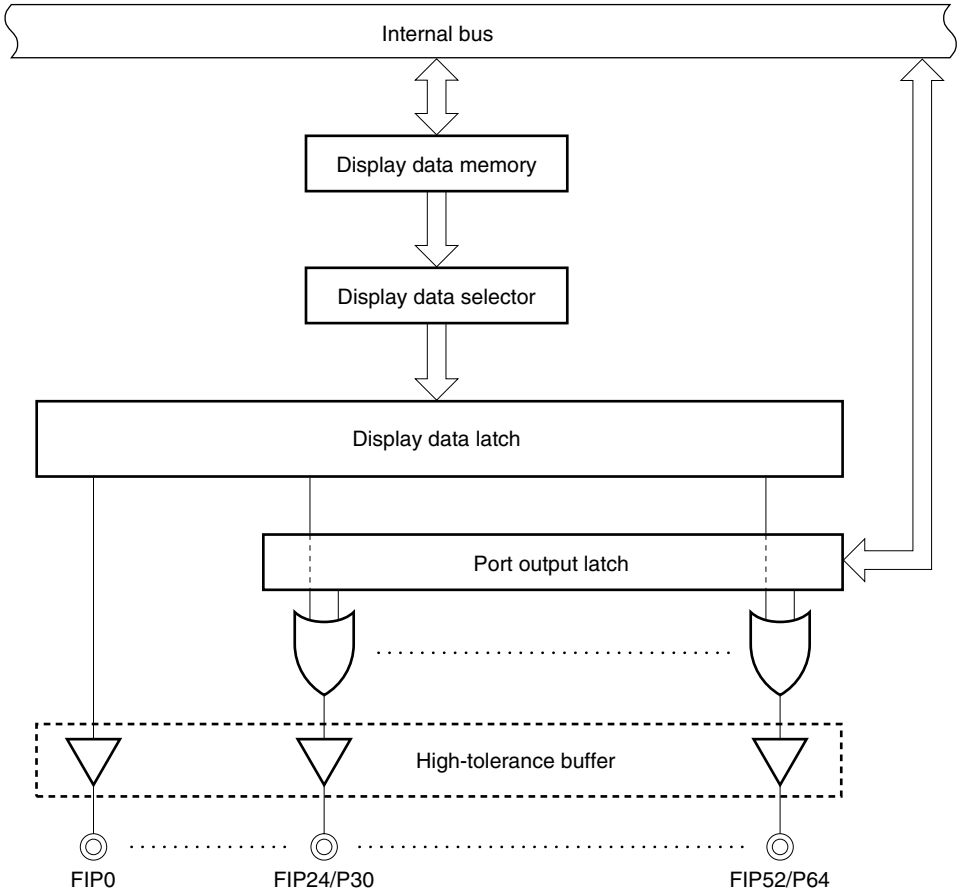


5.6 VFD Controller/Driver

A VFD controller/driver with the following functions is incorporated.

(a) Total number of display outputs: 53. Output of 16 patterns is enabled.
(b) 112-byte display RAM is provided to enable display signal output by reading display data automatically (direct memory access (DMA)).
(c) A port pin that is not used for VFD display can be used as an output port or an I/O port (except for FIP0 to FIP23, which are VFD output-only pins).
(d) The luminance can be adjusted in 8 levels using display mode register 1 (DSPM1).
(e) Hardware taking into consideration the key scan application is incorporated.
(f) Whether the key scan timing is inserted or not is selectable.
(g) A high-tolerance output buffer (VFD driver) that can drive the VFD directly is incorporated.
(h) VFD output pins can incorporate a pull-down resistor, set by a mask option.

Figure 5-9. VFD Controller/Driver Block Diagram



6. INTERRUPT FUNCTIONS

There are 3 types of interrupt functions.

- Non-maskable: 1
- Maskable: 12
- Software: 1

Table 6-1. Interrupt Source List

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTTM90	Remote control timer input rising edge detection	Internal	000AH	(B)
	4	INTTM91	Remote control timer input falling edge detection		000CH	
	5	INTTM92	Remote control timer overflow		000EH	
	6	INTKS	Key scan timing from VFD controller/driver		0010H	
	7	INTCSI1	Serial interface SIO1 transfer end		0012H	
	8	INTCSI3	Serial interface SIO3 transfer end		0014H	
	9	INTTM80	TM80 and CR80 match		0016H	
	10	INTTM81	TM81 and CR81 match		0018H	
	11	INTAD	A/D conversion end		001AH	
Software	—	BRK	BRK instruction execution	—	003EH	(D)

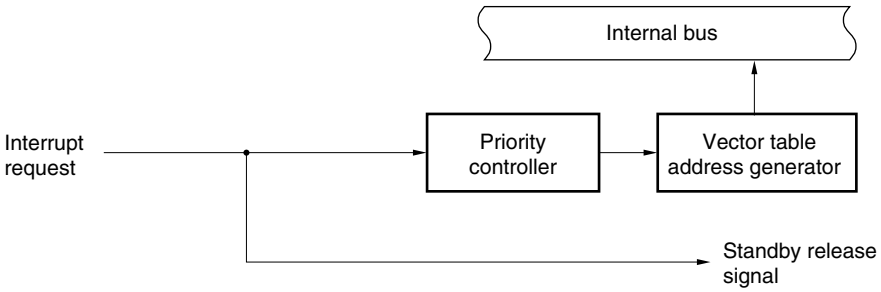
Notes 1. Default Priority is the priority order when more than one maskable interrupt request is generated simultaneously. 0 is the highest priority and 11 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

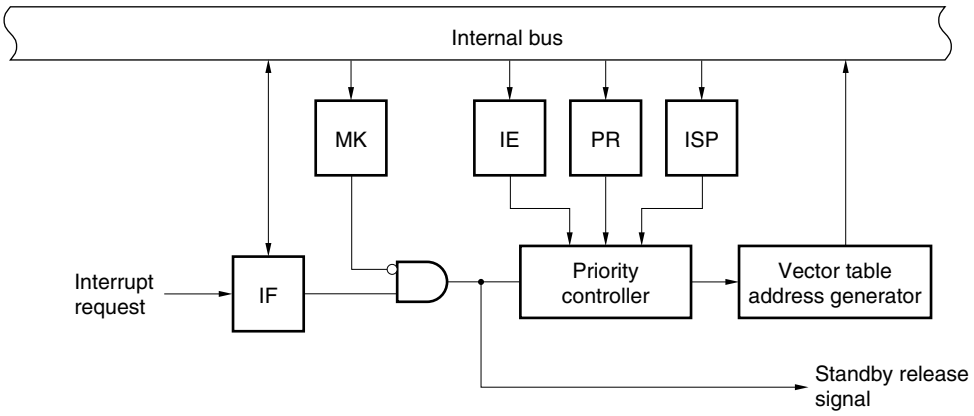
★ **Remark** Two watchdog timer interrupt sources (INTWDT) are available: a non-maskable interrupt and a maskable interrupt (internal), either of which can be selected.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0, INTP1)

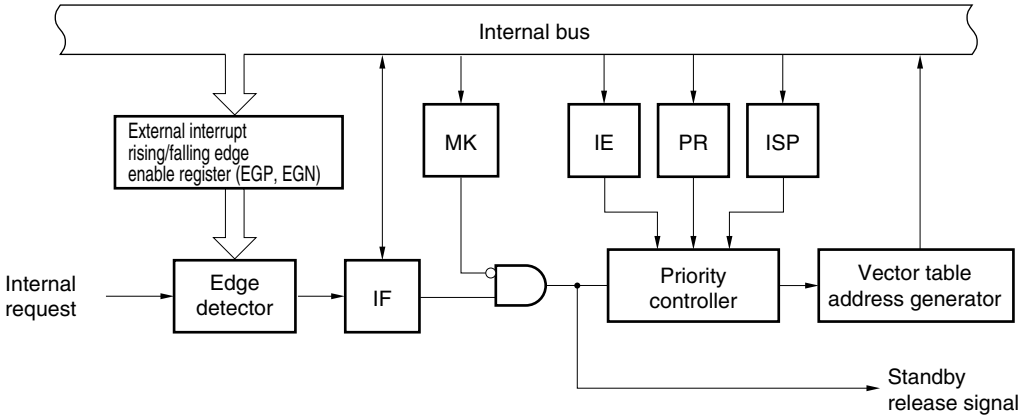
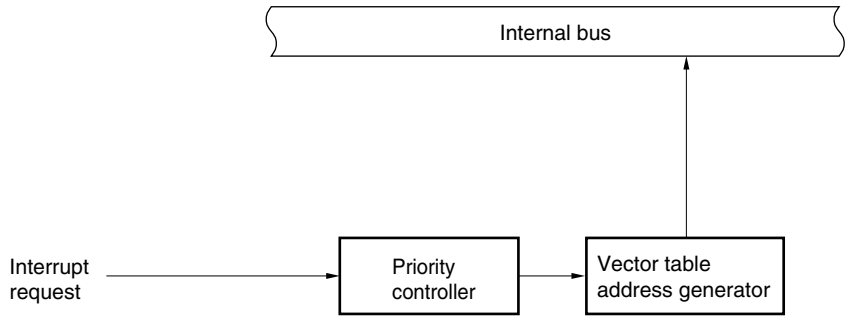


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) Software interrupt

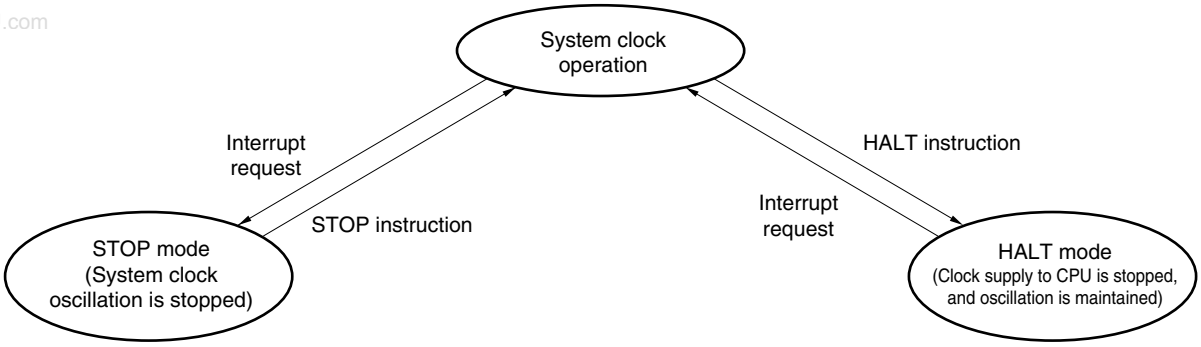


7. STANDBY FUNCTION

The standby function is a function to reduce the current consumption. The following two types of standby functions are available.

- HALT mode: Halts the CPU operating clock and enables a reduction in the average current consumption by intermittent operation with normal operation.
- STOP mode: Halts the system clock oscillation. Halts all operations with the system clock and sets an ultra-low power consumption state.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two types of resetting methods are available.

- External reset by the $\overline{\text{RESET}}$ input
- Internal reset by watchdog timer loop detection

★ 9. MASK OPTION

The mask options for the μPD780232 are shown in Table 9-1.

Table 9-1. Pin Mask Option Selection

Pin Name	Mask Option
FIP 0 to FIP23, P30/FIP24 to P37/FIP31, P40/FIP32 to P47/FIP39	An on-chip pull-down resistor can be specified for V_{LOAD} in 1-bit units.
P50/FIP40 to P57/FIP47, P60/FIP48 to P64/FIP52	An on-chip pull-down resistor can be specified for V_{LOAD} or V_{SS0} in 1-bit units.

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

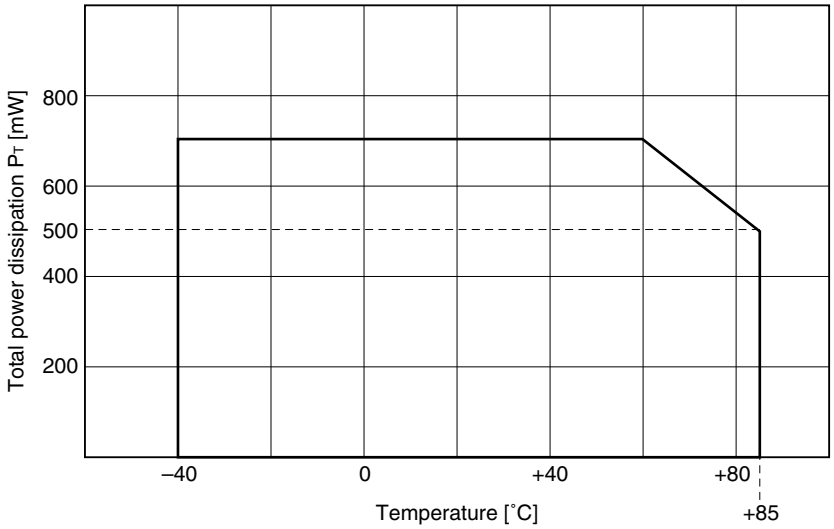
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{LOAD}			V_{DD} – 45 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{RESET}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64	P-ch open drain	V_{DD} – 45 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}			V_{DD} – 45 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL} **Note 1**	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T **Note 2**	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Notes 1. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Notes 2. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780232 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) × I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

The following shows how to calculate total power consumption for the example in Figure 11-1.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids × 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 36.4\ \text{mW}$$

Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

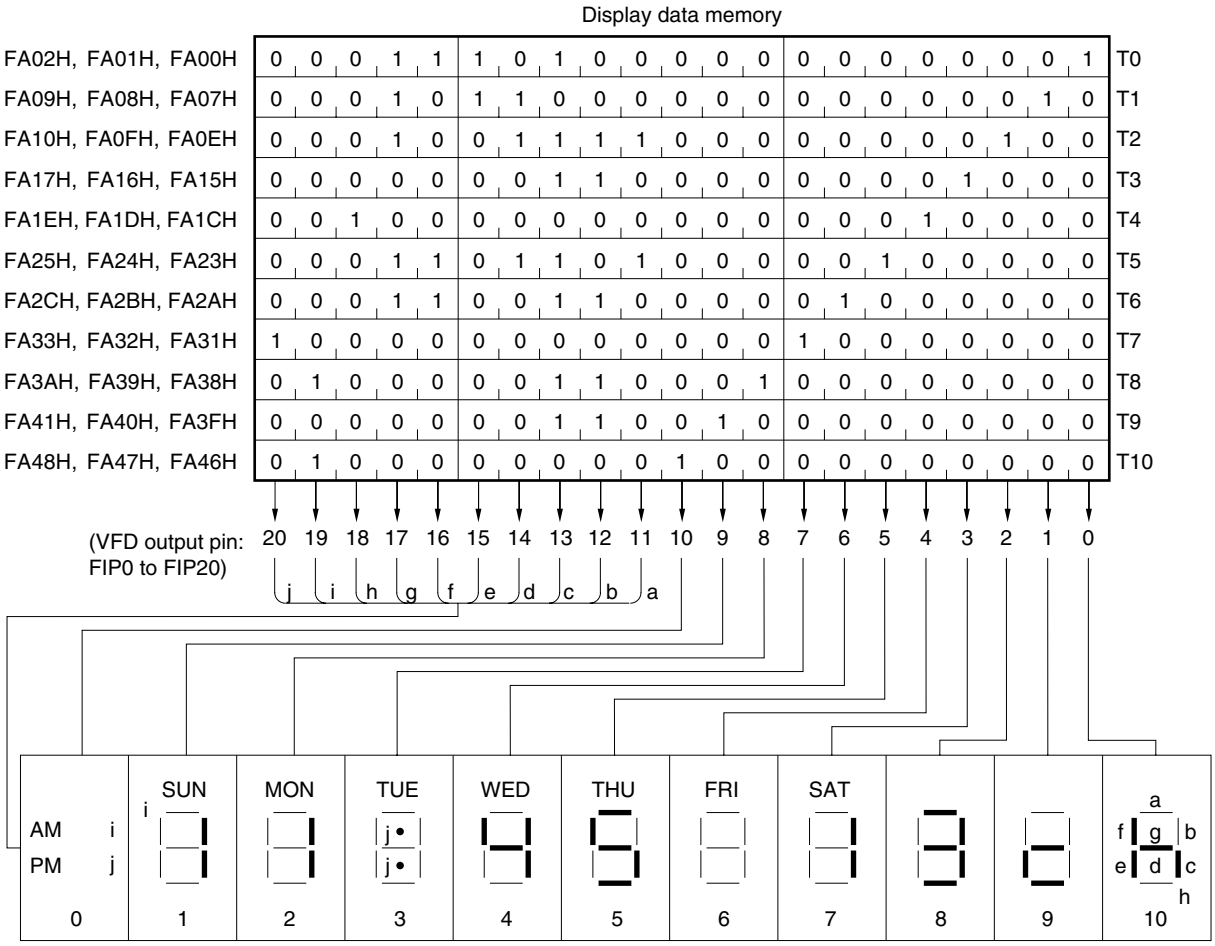
$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

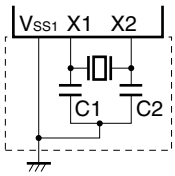
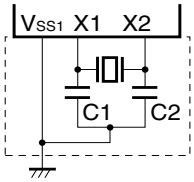
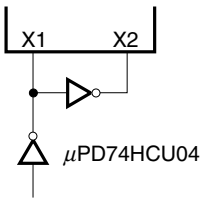
In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption.

However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

Figure 11-1. Display Example of 10 Segments-11 Digits



System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**				10	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System Clock: Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB 1000J	1.00	150	150	4.5	5.5
	CSA2.00MG040	2.00	100	100		
	CST2.00MG040		On-chip	On-chip		
	CSA3.58MG	3.58	30	30		
	CST3.58MGW		On-chip	On-chip		
	CSTS0358MG06					
	CSA4.19MG	4.19	30	30		
	CST4.19MGW		On-chip	On-chip		
	CSTS0419MG06					
	CSA5.00MG	5.00	30	30		
	CST5.00MGW		On-chip	On-chip		
	CSTS0500MG03					

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIH3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52				–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_2	P50 to P57, P60 to P64		15	35	90	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52	V_{OD} – V_{LOAD} = 40 V	30	60	135	kΩ
Power supply current[Note]	I_{DD1}	5 MHz crystal oscillation operation mode	PCC = 00H		7	14	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode			1.5	4.5	mA
	I_{DD3}	STOP mode			1	30	μA

Note Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

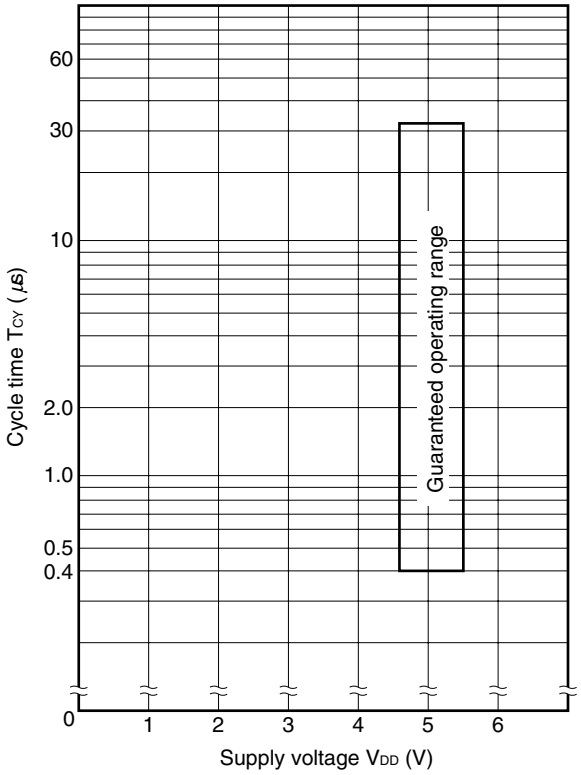
2. PCC: Processor clock control register

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/ low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2[Note]			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF[Note]			300	ns

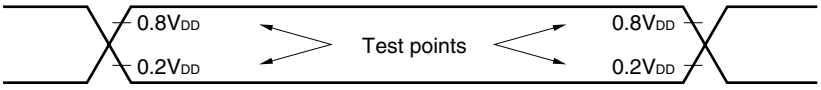
Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

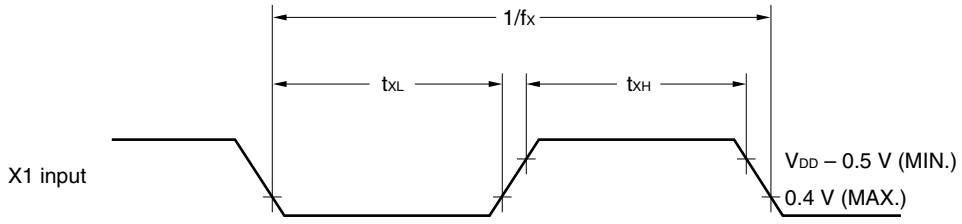
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF[Note]			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

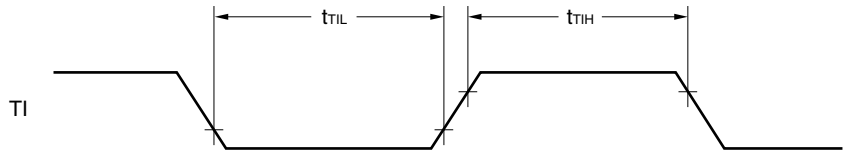
AC Timing Test Points (Excluding X1 Input)



Clock Timing

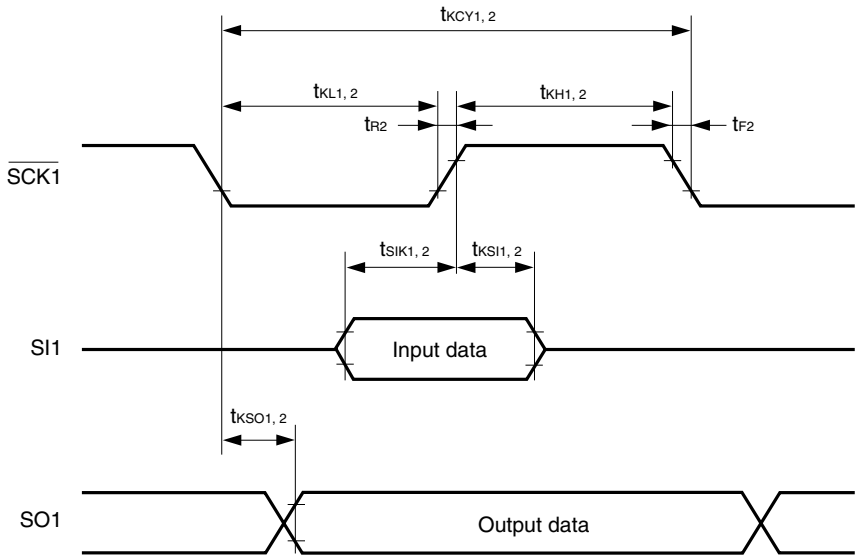


TI Timing

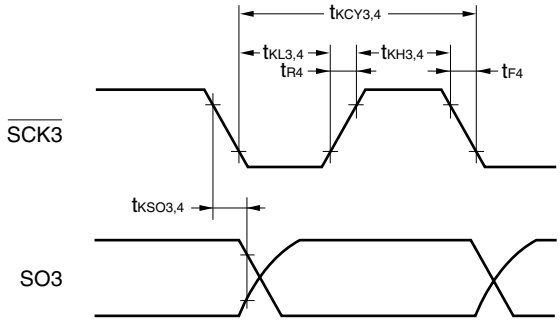


Serial Transfer Timing

3-wire serial mode:



2-wire serial mode:



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error[Note 1]					±1.0	%
Conversion time[Note 2]	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

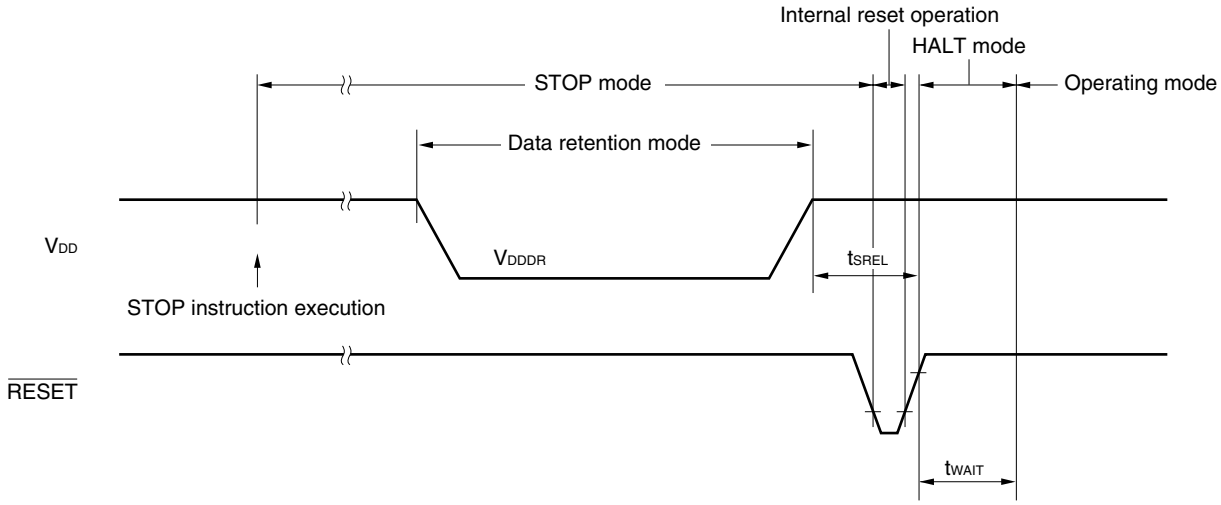
2. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

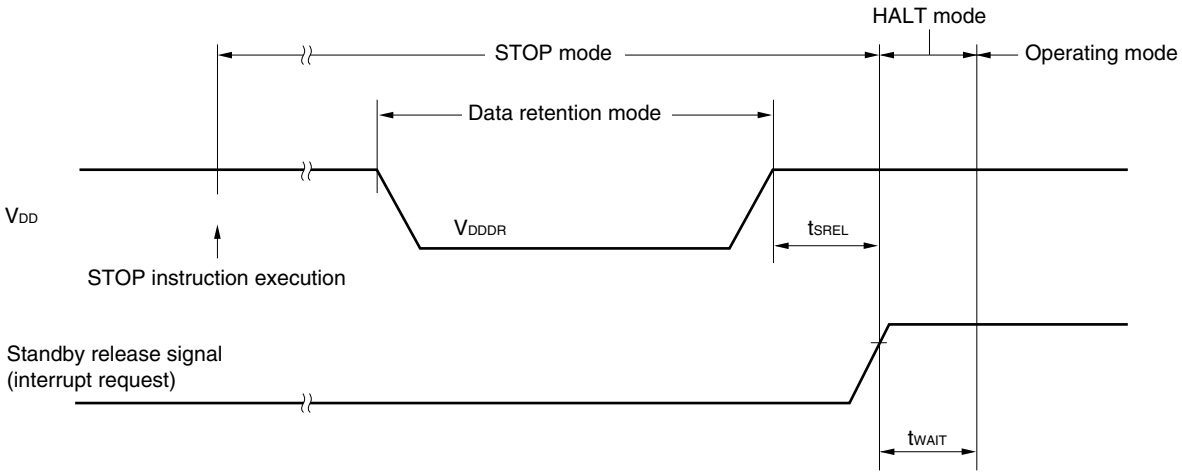
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

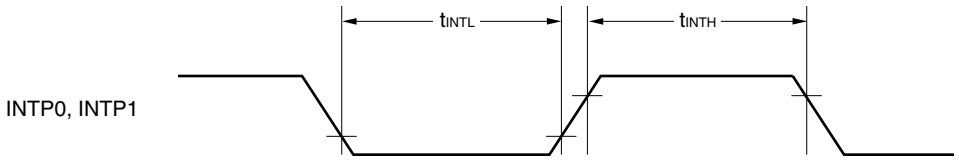
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



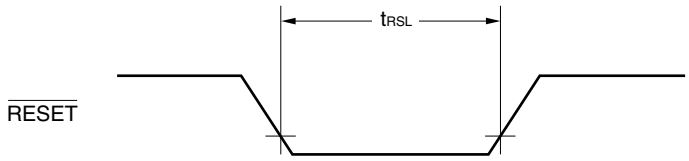
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

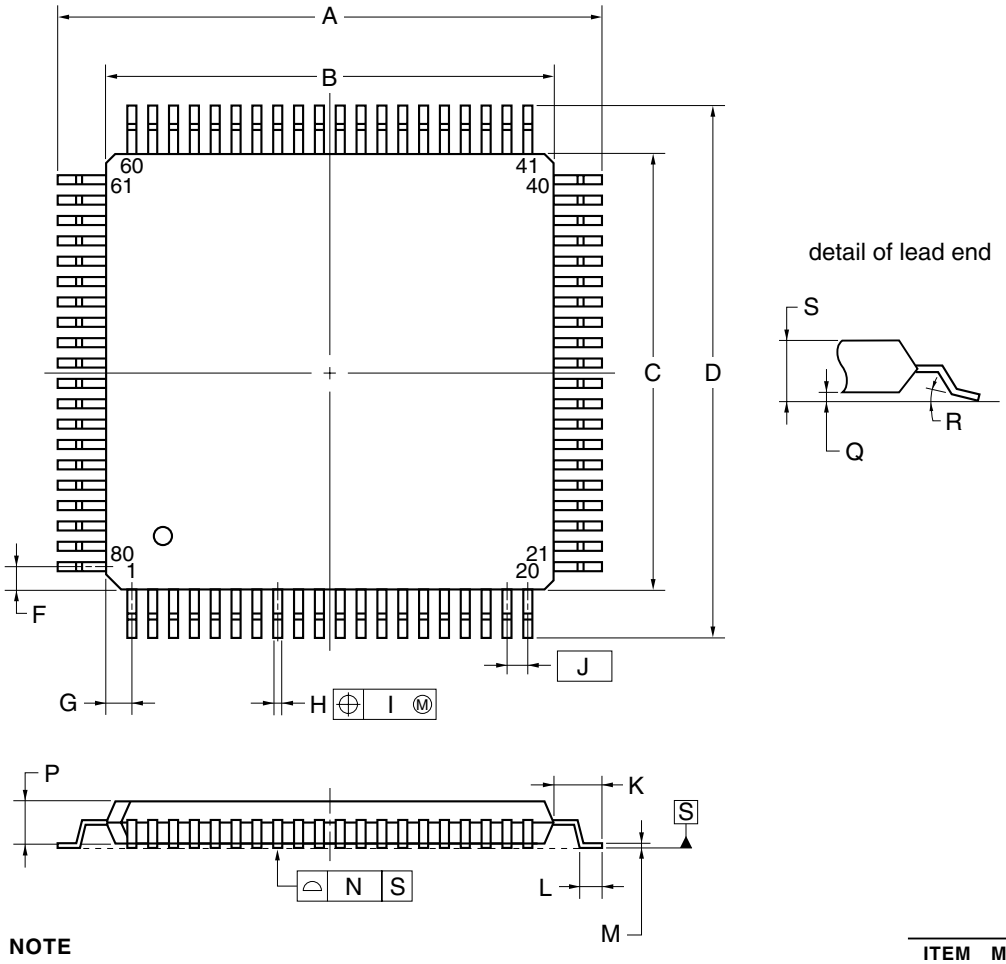


$\overline{\text{RESET}}$ Input Timing



12. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

★ 13. RECOMMENDED SOLDERING CONDITIONS

The μPD780232 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

μPD780232GC-×××-8BT: 80-pin plastic QFP (14 × 14)

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780232.
Also refer to **(6) Notes on using development tools**.

(1) Software Package

SP78K0	Software package common to 78K/0 Series

(2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780233	Device file for μPD780232 Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(3) Flash Memory Writing Tools

★ Flashpro III (FL-PR3, PG-FP3)	Dedicated flash programmer for on-chip flash memory microcontrollers
FA-80GC	Adapter for flash memory writing. Used by connecting to Flashpro III. • For 80-pin plastic QFP (GC-8BT type)

(4) Debugging Tools

- **When in-circuit emulator IE-78K0-NS(-A) is used**

IE-78K0-NS(-A)	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
★ IE-78K0-NS-PA	Performance board to enhance/extend the functions of the IE-78K0-NS
IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
★ IE-70000-CD-IF-A	PC card and interface cable required when notebook-type PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when IBM PC/AT™ compatible is used as host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Adapter required when PC incorporating PCI bus is used as host machine
★ IE-780233-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate the μPD780232 Subseries
NP-80GC ★ NP-80GC-TQ ★ NP-H80GC-TQ	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the NP-80GC and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
★ TGC-080SBP	Conversion adapter to connect the NP-80GC-TQ or NP-H80GC-TQ and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780233	Device file for μPD780232 Subseries

- **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
★ IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
★ IE-70000-PC-IF-C	Adapter required when IBM PC/AT compatible is used as host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Adapter required when PC incorporating PCI bus is used as host machine
IE-70000-R-SV3	Interface adapter and cable required when EWS is used as host machine
★ IE-780233-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate the μPD780232 Subseries
IE-78K0-R-EX1	Emulation probe conversion board required when using IE-780232-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the EP-78230GC-R and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780233	Device file for μPD780232 Subseries

(5) Real-Time OSs

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

★ **(6) Notes on using development tools**

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780233.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780233.
- The FL-PR3, FA-80GC, NP-80GC, NP-80GC-TQ, and NP-H80GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd (+81-45-475-4191).
- The TGK-080SBP is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact: Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronics Department (TEL +81-6-6244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	—
ID78K0	√	—
SM78K0	√	—
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780232 Subseries User's Manual	U13364E
μPD780232 Data Sheet	This manual
μPD78F0233 Data Sheet	U13322E
78K/0 Series Instructions User's Manual	U12326E
★ 78K/0, 78K/0S Series Flash Memory Write Application Note	U14458E

★ Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
PG-FP3 Flash Memory Programmer		U13502E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78K0-NS-A In-Circuit Emulator		U14889E
IE-78001-R-A In-Circuit Emulator		U14142E
IE-78K0-R-EX1 In-Circuit Emulator		To be prepared
IE-780233-NS-EM4 Emulation Board		U14666E
EP-78230 Emulation Probe		EEU-1515
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Parts User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Guide	U11649E
	Reference	U11539E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-time OS	Fundamentals	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamentals	U12257E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Package - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-3067-5800
Fax: 01-3067-5899

NEC Electronics (France) S.A.
Madrid Office
Madrid, Spain
Tel: 091-504-2787
Fax: 091-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

J01.2

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

- **The information in this document is current as of February, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).