NEC

MOS INTEGRATED CIRCUIT

μPD7566A, 7566A(A)

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD7566A is a product of the μPD7554, 7564 sub-series which is a low-end, low-cost version of the μPD7500 series microcomputers. This 4-bit single-chip microcomputer has fewer ports than the other products in the μPD7500 series, in order to reduce the package size, and is especially ideal for temperature control applications, as well as for application systems, such as air conditioners, microwave ovens, refrigerators, rice cooker, washing machines, and cassette deck controllers. Some of the output pins for the microcomputer can be used to directly drive triacs and LEDs.

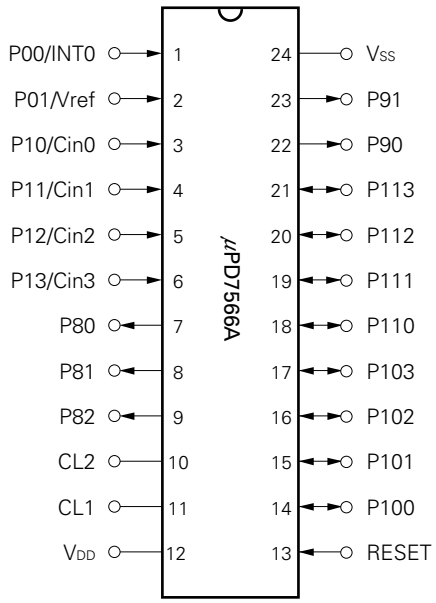
In addition, various I/O circuits can be selected by mask options, so that the number of necessary external circuits can be significantly reduced.

A detailed function description is provided in the following user's manual.
Be sure to read this manual when designing your system.
μPD7556, 7566 User's Manual: IEM-1111D

FEATURES

- 45 instructions (subset of the μPD7500H SET B)
- Instruction cycle: 2.86 microseconds (700 kHz, at 5V) with ceramic oscillator
- Program memory (ROM): 1,024 words x 8 bits
- Data memory (RAM): 64 words x 4 bits
- Test sources: 1 external and 1 internal
- 8-bit timer/event counter
- 19 I/O lines (total output current: 100 mA)
  - . Five pins can be used to directly drive triacs and LEDS
    : P80 to P82, P90 to P91
  - . Eight pins can be used to directly drive LEDs
    : P100 to P103, P110 to P113
  - . Four comparator input pins: P10/Cin 0 to P13/Cin 3
  - . Mask option functions available on all ports
- Standby functions (STOP/HALT)
- Data memory contents can be retained on a low voltage
- Internal ceramic oscillator for system clock oscillation
- CMOS
- Low-power dissipation
- Single power source (2.7 to 6.0V)

PIN CONFIGURATION (Top View)



APPLICATIONS ★

μPD7566A : Air conditioner, microwave oven, refrigerator, audio equipment controller, etc.
μPD7566A(A) : Automotive and transportation equipments, etc.

The quality level and absolute maximum ratings of the μPD7566A and the μPD7566A(A) differ.
Except where specifically noted, explanations here concern the μPD7566A as a representative product.
If you are using the μPD7566A(A), use the information presented here after checking the functional differences.

The information in this document is subject to change without notice.

The ★ mark shows major revised points.

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ORDERING INFORMATION

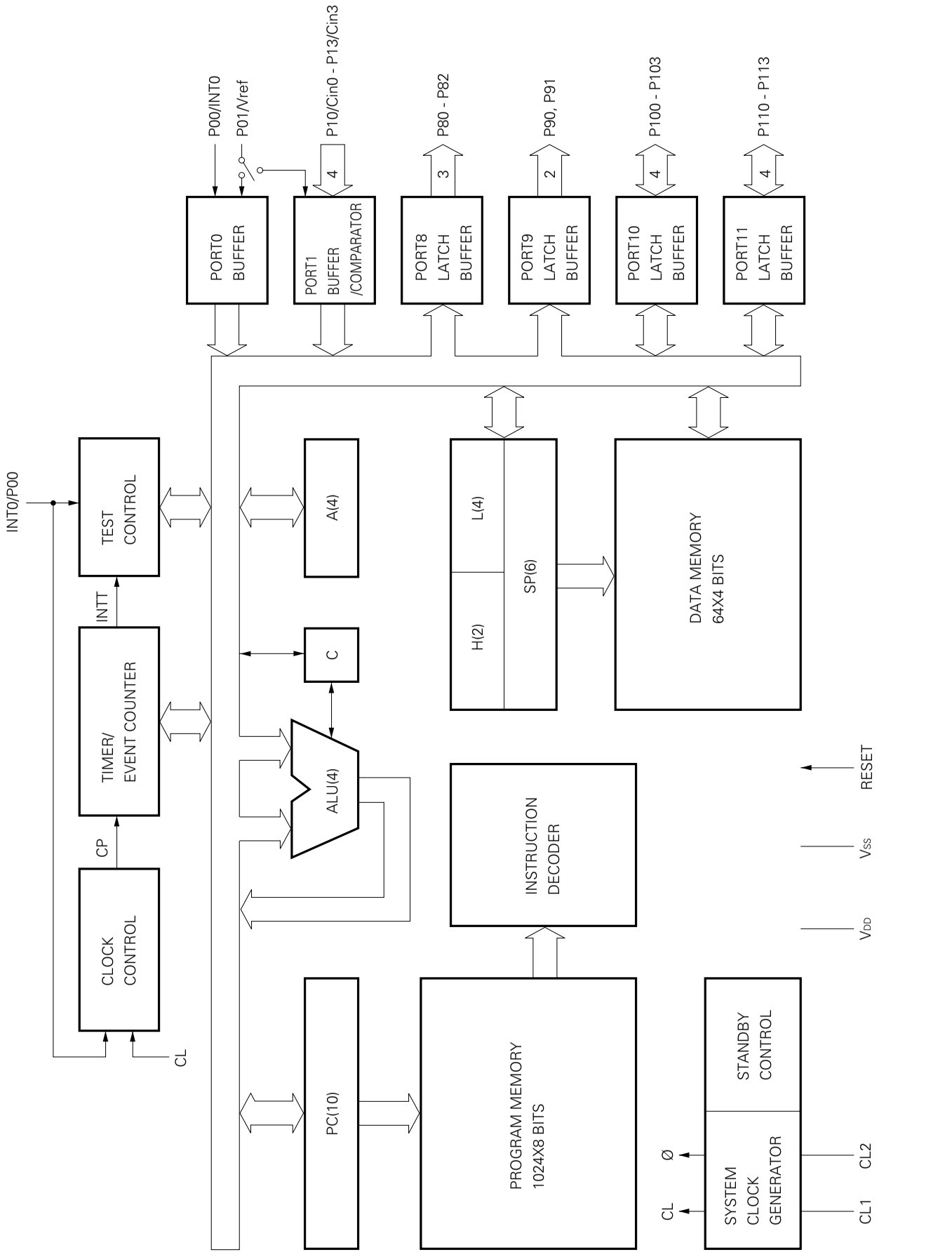
	Part Number	Package	Quality Grade
	μPD7566ACS-xxx	24-pin plastic shrink DIP (300 mil)	Standard
	μPD7566AG-xxx	24-pin plastic SOP (300 mil)	Standard
★	μPD7566ACS(A)-xxx	24-pin plastic shrink DIP (300 mil)	Special
★	μPD7566AG(A)-xxx	24-pin plastic SOP (300 mil)	Special

Caution Be sure to specify mask options when placing your order.

Remark xxx indicates ROM code number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

μPD7566A BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT FUNCTIONS

Pin Name	Input/ Output	Shared with:	Function	At Reset	I/O Circuit Type
P00	Input	INT0	2-bit input port (PORT 0). P00 is also used to input count clocks (event pulses).	Input	S
P01		Vref			T
P10-P13	Input	Cin0 - Cin3	4-bit input port (PORT 1)	Input	U
P80-P82	Output	-	3-bit output port (PORT 8). High-current (15 mA), and medium-voltage (9V) output	High impedance	O
P90, P91	Output	-	2-bit output port (PORT 9). High-current (15 mA), and medium-voltage (9V) output		
P100 - P103	Input/ Output	-	4-bit I/O port (PORT 10). Medium-current (10 mA), and medium-voltage (9V) I/O	High impedance or high-level output	P
P110- P113	Input Output	-	4-bit I/O port (PORT 11). Medium-current (10 mA), and medium-voltage (9V) I/O		

1.2 OTHER FUNCTIONS

Pin Name	Input/ Output	Shared with:	Function	At Reset	I/O Circuit Type
INT0	Input	P00	Edge-detecting testable input pin (rising edge)	Input	S
Vref	Input	P01	Comparator reference voltage input pin (Whether this pin is used as P01 or as Vref is specified by a mask option.)	Input	T
Cin0-Cin3	Input	P10-P13	4-bit comparator input pins (Whether these pins are used as digital input pins (P10 to P13) or as comparator input pins (Cin0 to Cin3) is specified by the mask option for each bit.	Input	U
CL1			A ceramic oscillator is connected across these pins.		
CL2					
RESET			System reset input pin (high-level active). A pull-down resistor can be interconnected to this pin by a mask option.		R
V_{DD}			Power pin		
V_{SS}			GND pin		

1.3 MASK OPTIONS FOR PINS ★

The following mask options are available. These mask options can be selected in bit units.

Pin Name	Mask Option
P00	① No internally provided resistor ② Pull-down resistor internally provided ③ Pull-up resistor internally provided
P01/V_{ref}	① External V_{ref} input ② No internally provided resistor (CMOS input) ③ Pull-down resistor internally provided (CMOS input) ④ Pull-up resistor internally provided (CMOS input)
P10/Cin0	① Comparator input ② No internally provided register ③ Pull-down resistor internally provided (CMOS input) ④ Pull-up resistor internally provided (CMOS input)
P11/Cin1	① Comparator input ② No internally provided register ③ Pull-down resistor internally provided (CMOS input) ④ Pull-up resistor internally provided (CMOS input)
P12/Cin2	① Comparator input ② No internally provided register ③ Pull-down resistor internally provided (CMOS input) ④ Pull-up resistor internally provided (CMOS input)
P13/Cin3	① Comparator input ② No internally provided register ③ Pull-down resistor internally provided (CMOS input) ④ Pull-up resistor internally provided (CMOS input)
P80	① N-channel open-drain output ② CMOS (push-pull) output
P81	① N-channel open-drain output ② CMOS (push-pull) output
P82	① N-channel open-drain output ② CMOS (push-pull) output
P90	① N-channel open-drain output ② CMOS (push-pull) output
P91	① N-channel open-drain output ② CMOS (push-pull) output
P100	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P101	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P102	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P103	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P110	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P111	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P112	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
P113	① N-channel open-drain I/O ② Push-pull I/O ③ N-channel open-drain I/O with pull-up resistor internally provided
RESET	① Pull-down resistor is not internally provided ② Pull-down resistor is internally provided
Internal V_{ref} setting [Note]	① Internal bias is not provided ② A 1/2 V_{DD} internal bias is applied to V_{ref}

Note When any of pins P10-P13 is specified as "① comparator", and "① internal bias is not provided" is specified for the internal V_{ref} setting, specify "① external V_{ref} input" for pin P01.
When none of pins P10-P13 is specified as "① comparator", specify "① internal bias is not provided" for the internal V_{ref} setting.

There is no mask option for PROM products. For more information, see the μPD75P66 Data Sheet (IC-7518).

1.4 NOTES ON USING THE P00/INT0, AND RESET PINS

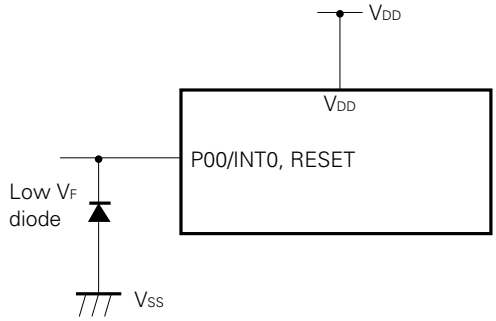
In addition to the functions described in 1.1, 1.2, and 1.3, an exclusive function for setting the test mode, in which the internal functions of the μPD7566A are tested, is provided to the P00/INT0 and RESET pins.

If a voltage less than V_{SS} is applied to either of these pins, the μPD7566A is put into test mode. Therefore, even when the μPD7566A is in normal operation, if noise less than the V_{SS} is input into any of these pins, the μPD7566A will enter the test mode, and this will cause problems for normal operation.

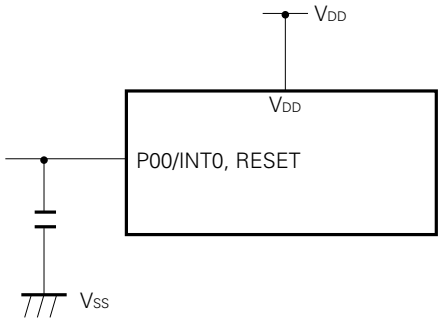
As an example, if the wiring to the P00/INT0 pin or the RESET pin is long, stray noise may be picked up and the above mentioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- **Connect a diode having a low V_F across P00/INT0 and RESET, and V_{SS}.**



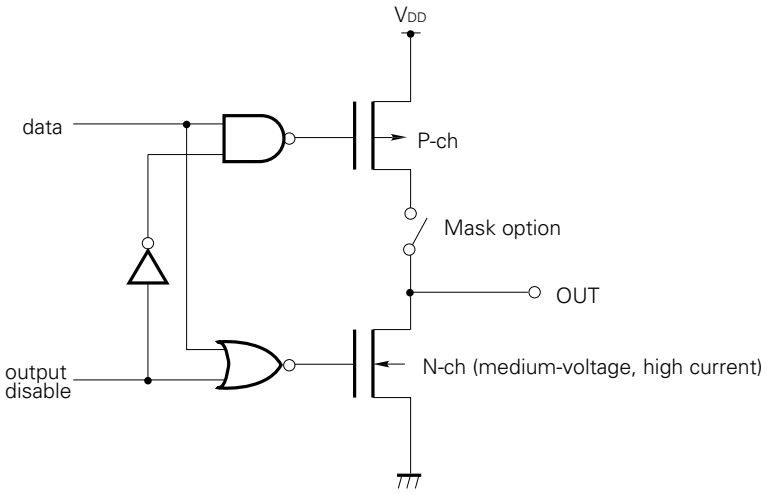
- **Connect a capacitor across P00/INT0 and RESET, and V_{SS}.**



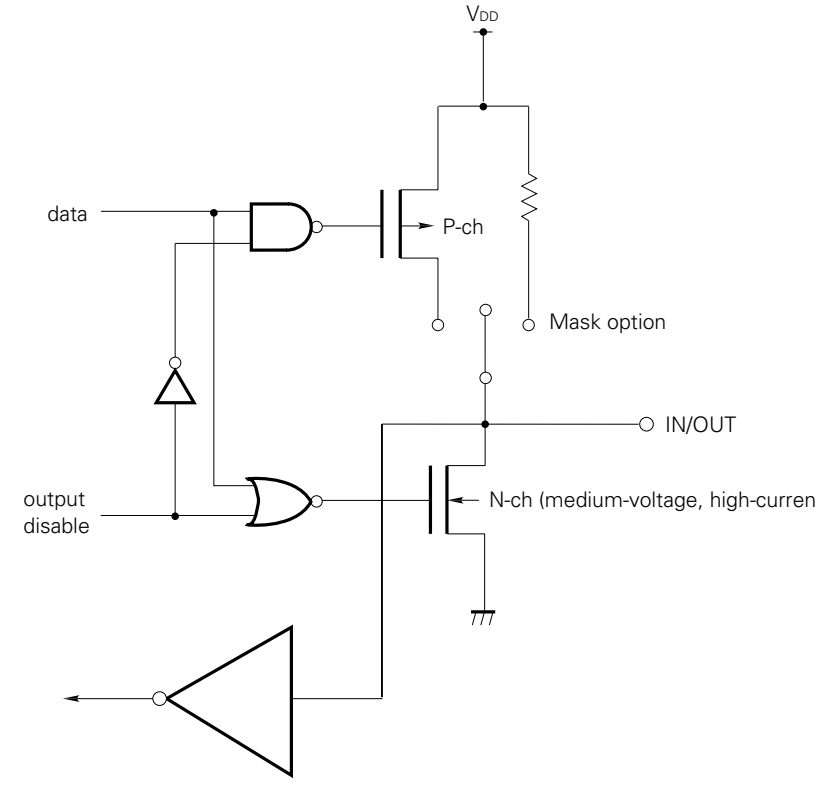
1.5 PIN I/O CIRCUITS

Schematic drawings of the I/O circuits for the microcomputer's pins are shown below.

(1) Type O

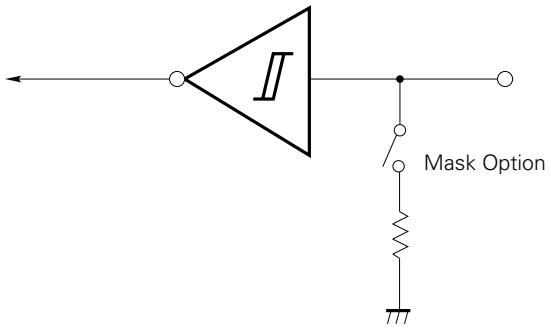


(2) Type P

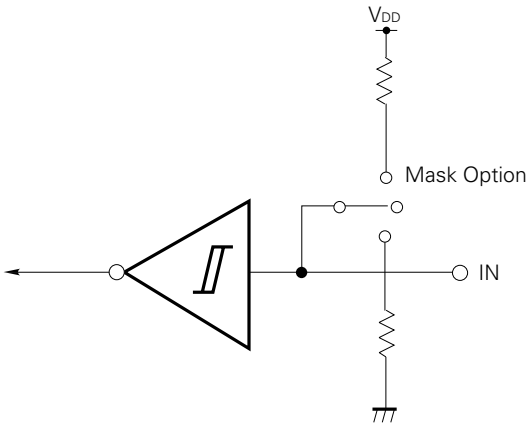


Medium-voltage, input buffer

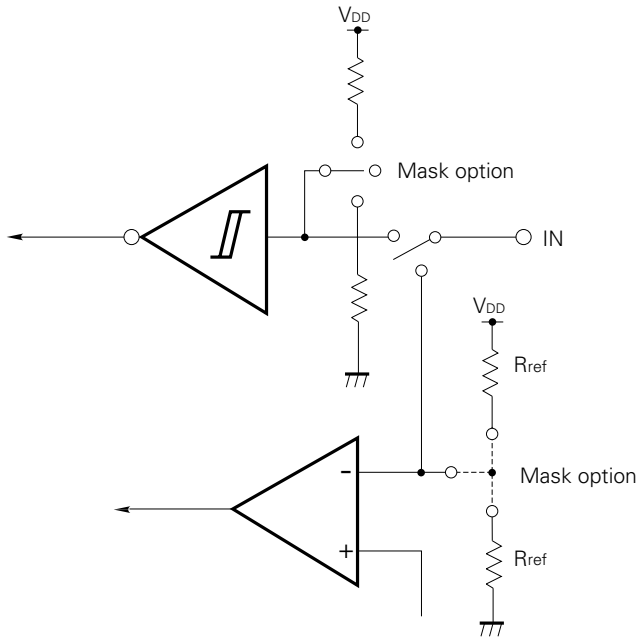
(3) Type R



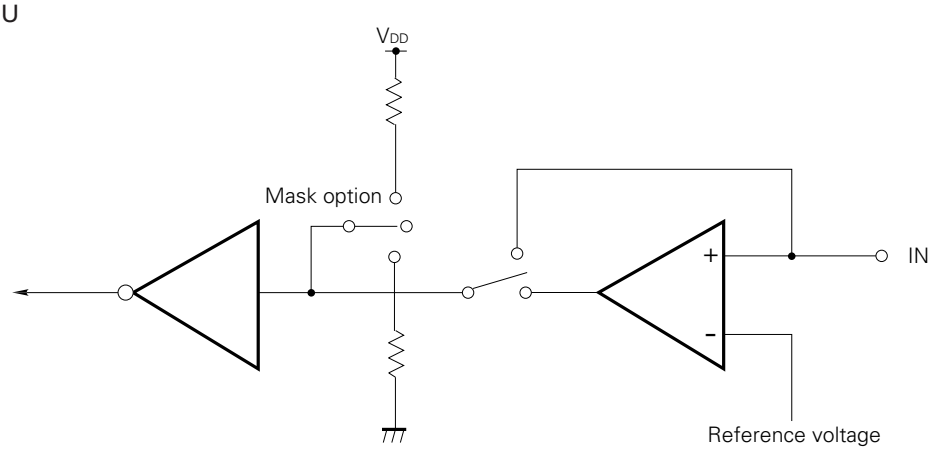
(4) Type S



(5) Type T



(6) Type U



1.6 RECOMMENDED PROCESSING OF UNUSED PINS

Pin	Recommended Processing
P00/INT0	Connect to V_{SS}
P01/V_{ref}	Connect to V_{SS} or V_{DD}
P10-P13	
P80-P82	Open
P90, P91	
P100-P103	Input : Connect to V_{SS} or V_{DD}
P110-P113	Output: Open

1.7 I/O PORT OPERATIONS

(1) P00, P01 (Port 0)

Port 0 is a 2-bit input port and consists of pins P00 and P01. These pins are multiplexed, and P00 can also input count clocks or testable signal (INT0), while P01 is used, when so specified by a mask option, to input a reference voltage (Vref) to the internal comparator.

To input a count clock from P00, set bits 2 and 1 (CM2 and 1) for the clock mode register to "01" (see 2.10, Clock Control Circuit).

To allow P00 to serve as INT0, set the SM3 flag to 1.

Whether P01 is used to input a reference voltage (Vref) to the comparator is specified by a mask option. In this case, the port function for the P01 pin cannot be used. The data on P00 and P01 can be loaded to the lower 2 bits (A0 and A1) of the accumulator at any time, by executing a port input instruction (IPL, L = 0).

(2) P10/Cin 0 to P13/Cin 3 (Port 1)

Port 1 is a 4-bit input port consisting of these four pins, which can also be used to input analog voltages to the comparator, when so specified by mask options.

To input analog voltages through Port 1, a comparator must be connected to each bit of the port by a mask option, and a port input instruction (IPL, L = 1) must be executed.

The analog voltage input through these pins to the comparator is always compared with a reference voltage input through the Vref pin. It takes up to 3 machine cycles to accomplish this comparison. Therefore, to change the voltage applied to the Vref pin by port output to form an A/D converter by using a resistor ladder, wait for 3 machine cycles after executing a port output (OPL) instruction. Then carry out an input (IPL, L = 1) instruction to obtain the result of the comparison.

If the output instruction is executed during a 3 machine cycle period that precedes the IPL instruction (L = 1), which inputs the comparison result, the comparator accuracy may be degraded. For this reason, do not execute the OPL instruction during 3 machine cycles immediately before the IPL instruction is executed.

```
Example: LHLI    0AH   ;  L = 10
         OPL           ;  Port 10 output (Vref is changed)
         NOP
         NOP
         LHLI    1     ;  L = 1
         IPL           ;  Input of comparison result
```

(3) P80 to P82 (Port 8), and P90 to P91 (Port 9)

Pins 80 to P82 constitute a 3-bit output port with output latch, Port 8, while P90 to P91 form a 2-bit output port with output latch, Port 9.

When a port output instruction (OPL, L = 8, or L = 9) is executed, the contents of the accumulator are latched on the output latches, and, at the same time, output to these ports.

Each bit in Ports 8 and 9 can be set or reset by SPBL or RPBL instruction.

Two output modes can be selected for Ports 8 and 9 by a mask option: CMOS (push-pull) or N-channel open-drain mode.

The N-channel open-drain output mode is useful for interfacing a circuit operating on a supply voltage different from that to the microcomputer, because the output buffer in this mode can withstand an applied 9V.

(4) P100 to P103(Port 10), and P110 to P113 (Port 11).....Pseudo-bidirectional I/O

Pins P100 to P103 constitute a 4-bit I/O port with output latches, Port 10, while P110 to P113 form Port 11, which is a 4-bit I/O port with output latches.

When a port output instruction (OPL, L = 10 or L11) is executed, the accumulator contents are latched to the output latches and, at the same time, output to either of these ports.

Data once written to the output latch and the state of the output buffer are retained until an output instruction that manipulates Port 10 or 11 is executed next, or until the RESET signal is input. Therefore, the states of the output latches and output buffer will not be changed, even when an input instruction is executed to these ports.

Each bit of Ports 10 and 11 can be set or reset by SPBL or RPBL instruction. Three input modes can be selected for Ports 10 and 11 by mask options: N-channel open-drain I/O, N-channel open-drain I/O with pull-up resistors connected, and CMOS (push-pull) modes.

The N-channel open-drain mode is useful for interfacing a circuit operating on a supply voltage different from that fed to the microcomputer, because the I/O buffer in this mode can withstand a 9V application.

If the CMOS (push-pull) I/O mode has been selected and an output instruction has once been executed, the ports cannot return to the input mode. However, the pin states can be checked by executing a port input (IPL) instruction.

In the N-channel open-drain mode, regardless of whether the pull-up resistors are connected or not, the ports are set in the input mode, when high-level signals are output to them, and the data on the 4 bits of each port can be loaded to the accumulator. Thus, the port serves as a pseudo-bidirectional port.

The three I/O modes are selected under the following conditions:

① CMOS I/O
   i) To use all the 4-bits as input port pins
   ii) To use port pins as output pins from which no medium-voltage output is required

② N-channel open-drain I/O
   i) To use port pins in applications where inputting outputting a medium-voltage is required
   ii) To use some port pins as input pins and the others as output pins
   iii) To alternately input and output data through one port pin

③ N-channel open-drain I/O with pull-up resistor connected
   i) To use some port pins as input pins and the other, as output pins in applications where pull-up resistors are required
   ii) To alternately input and output data through one port pin in application where a pull-up resistor is required

Caution To use port pins as input pins in modes ② and ③ above, it is necessary to write "1" to the output latch in advance and to turn off the N-channel transistor.

2. INTERNAL FUNCTIONAL BLOCKS

2.1 PROGRAM COUNTER (PC) ..... 10 BITS

This is a 10-bit binary counter that retains the address information for the program memory (ROM).

Fig. 2-1 Program Counter

PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PC

Normally, each time an instruction has been executed, the PC contents are automatically incremented by the number of bytes for the instruction.

When a call instruction has been executed, the current contents of the PC (i.e., return address) are saved to the stack, and a new call address is loaded to the PC. When a return instruction has been executed, the contents of the stack (i.e., return address) are loaded to the PC. When a jump instruction has been executed, immediate data that indicates the jump destination is loaded to some or all of the bits for the PC.

When a skip instruction has been executed, the PC contents are incremented by 2 or 3 during 1 machine cycle, depending on the number of bytes for the instruction to be executed next. All the PC bits are cleared to 0, when the RESET signal has been input.

2.2 STACK POINTER (SP) ..... 6 BITS

This is a 6-bit register. When port of the data memory is used as a last-in, first-out (LIFO) stack area, the SP retains the first address for the stack.

Fig. 2-2 Stack Pointer

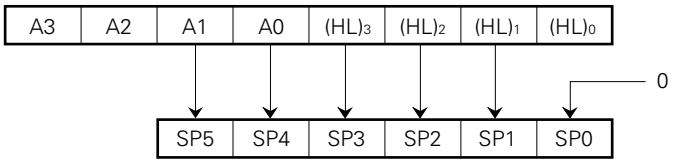
SP5	SP4	SP3	SP2	SP1	SP0	SP

The SP contents are decremented when a call instruction has been executed, and are incremented when a return instruction has been executed.

To obtain a stack area, the SP must be initialized by TAMSP instruction. Note, however, that 0 is is unconditionally loaded to the LSB for the SP (i.e., bit SP0) when TAMSP instruction has been executed. Stacking operation begins with decrementing the SP contents. Therefore, the highest address for the stack area +1 is set in the SP.

If the highest address for the stack area is 3FH, which is the highest address in the data memory, the initial values for the SP5 to 0 bits must be 00H. However, keep the data to be stored in AM to 40H when TAMSP instruction is executed, so that the microcomputer can be easily emulated by μPD7500H (EVAKIT-7500B).

Fig. 2-3 Executing TAMSP Instruction



The SP contents cannot be read.

Caution The SP contents are undefined, when the RESET signal has been input. Therefore, make sure that the SP is initialized at the beginning of the program.

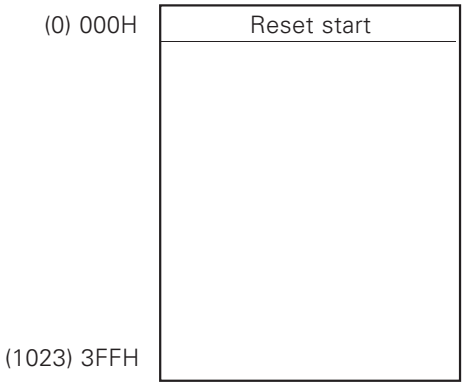
```
Example: LHLI    00H
         LAI     0
         ST
         LAI     4
         TAMSP           ; SP = 40H
```

2.3 PROGRAM MEMORY (ROM) ..... 1,024 WORDS X 8 BITS

This is a mask programmable ROM, consisting of 1,024 words by 8 bits. The ROM is addressed by the program counter (PC). The program is stored in the program memory.

Address 000H in this memory is a reset start address.

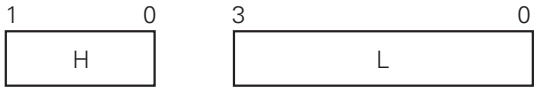
Fig. 2-4 Program Memory Map



2.4 GENERAL-PURPOSE REGISTERS

Two general-purpose registers, H (2 bits) and L (4 bits), are available. Each of these registers can be manipulated independently from the other. In addition, these registers can be used as a pair register (HL). The pair register serves as a data pointer to address the data memory.

Fig. 2-5 General-Purpose Registers

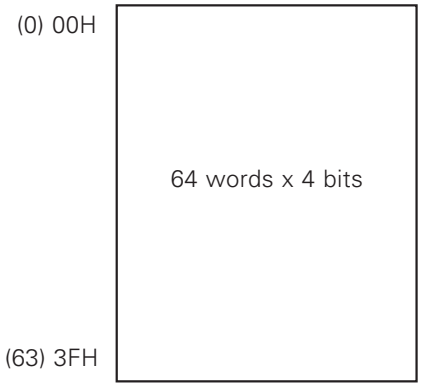


The L register is also used to specify an I/O port or mode register, when an input/output instruction (IPL or OPL) is executed. This register is also used to specify the port bit to be set or reset by SPBL or RPBL instruction.

2.5 DATA MEMORY (RAM) ..... 64 WORDS X 4 BITS

The data memory is static RAM configured of 64 words by 4 bits, and is used to store various data and as a stack area. The data memory is also used in pairs with the accumulator, making it possible to process 8-bit data.

Fig. 2-6 Data Memory Map



The data memory can be addressed in the following three addressing modes:

- Direct: In this mode, the data memory is directly addressed by the immediate data for an instruction.
- Register indirect: The data memory is indirectly addressed by the contents of pair register HL (including autoincrement and autodecrement).
- Stack: The data memory is indirectly addressed by the contents of the stack pointer (SP).

Any space in the data memory can be used as stack. The boundary of the stack is determined by initializing the SP by TAMSP instruction. After that, the stack area is automatically accessed by call and return instructions.

When a call instruction is executed, the contents of the PC and program status word (PSW) are stored in stack, as illustrated below.

Stack area

	3			0
SP - 4	0	0	PC9	PC8
SP - 3	PSW[Note]			
SP - 2	PC3 - PC0			
SP - 1	PC7 - PC4			

Note Bit 1 of PSW is always 0.

When a return instruction has been executed, the PC contents are restored, but the PSW contents are not.

The data memory contents can be retained on a low supply voltage in the STOP mode.

2.6 ACCUMULATOR (A) ..... 4 BITS

This is a 4-bit register which plays a central role, when an arithmetic operation is performed. The accumulator can also be used in pairs with a data memory address, indicated by pair register HL, to process 8-bit data.

Fig. 2-7 Accumulator

A3	A2	A1	A0	A

2.7 ARITHMETIC LOGIC UNIT (ALU) ..... 4 BITS

This is a 4-bit arithmetic operation circuit that carries out operations such as binary addition, logic operations, increment, decrement and comparison, as well as bit manipulation.

2.8 PROGRAM STATUS WORD (PSW) ..... 4 BITS

The PSW consists of two skip flags (SK1 and SK0) and a carry flag (C). Bit 1 of this register is always 0.

Fig. 2-8 Program Status Word

3	2	1	0	
SK1	SK0	0	C	PSW

(1) Skip flags (SK1 and SK0)

These flags retain the following skip conditions:

- String effect by LAI instruction
- String effect by LHLI instruction
- Establishment of skip conditions by instructions other than string-effect instructions

The skip flags are automatically set or reset each time an instruction has been executed.

(2) Carry flag (C)

This flag is set to 1, when an addition instruction (ACSC) is executed, and a carry is consequently generated from the bit 3 of the ALU. If a carry is not generated, the carry flag is cleared to 0. In addition, the carry flag can also be set by SC instruction, and cleared by RC instruction. The content of the flag can be tested by SKC instruction.

The PSW contents are automatically stored in the stack area when a call instruction is executed, and are not restored even when a return instruction is implemented. When the RESET signal is input, the SK1 and SK0 flags are cleared to 0, and the C flag content becomes undefined.

2.9 SYSTEM CLOCK GENERATOR

The system clock generator consists of a ceramic oscillator, a 1/2 frequency divider, standby mode (STOP/HALT) control circuit, and other circuits.

The ceramic oscillator can oscillate, when an external ceramic oscillator is connected across pins CL1 and CL2.

The signal output by the internal ceramic oscillator is a system clock (CL), which is then divided in two to create a CPU clock (ø).

The standby mode control circuit mainly consists of a STOP flip-flop and HALT flip-flop.

The STOP flip-flop is set by a STOP instruction, stopping the clock supply. When the ceramic oscillator is operating, this flip-flop stops the oscillator, setting the microcomputer in the STOP mode.

The STOP flip-flop is reset when a high-level RESET signal is input. As a result, the ceramic oscillator resumes its operation, and the clocks supply is started, when the RESET signal later goes low.

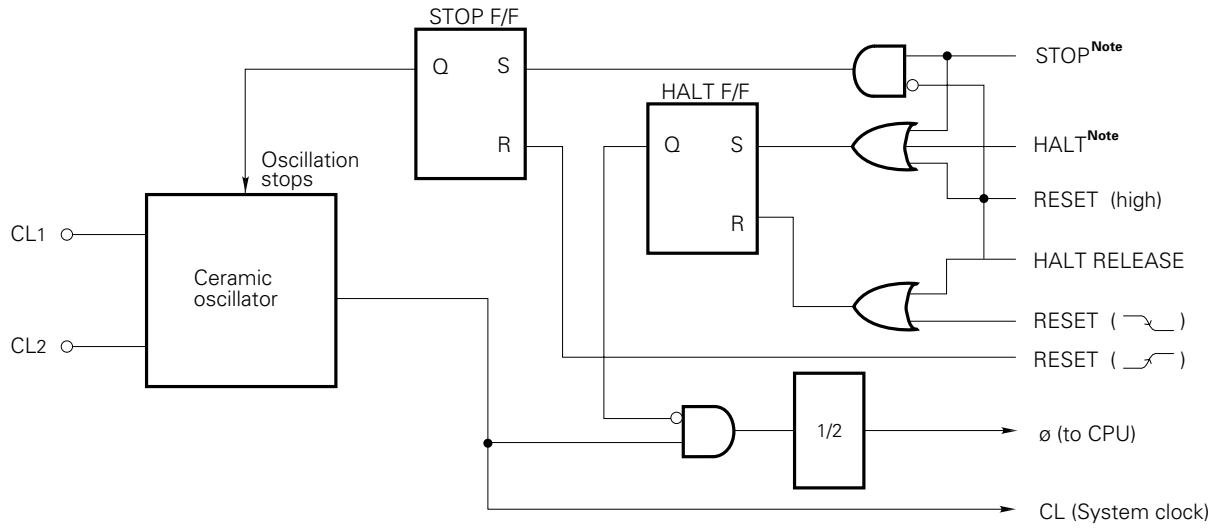
The HALT flip-flop is set by a HALT instruction, disabling the input of the 1/2 frequency divider, which generates CPU clock ø, and thereby stopping only CPU clock ø (HALT mode).

The HALT flip-flop is reset by the HALT RELEASE or the falling of RESET input (which becomes active when one of the test request flags has been set), allowing the supply of ø to be started.

The HALT flip-flop remains set even while the RESET signal is active (high-level), and operates in the same manner as in the HALT mode.

When Power-ON Reset is performed, the ceramic oscillator starts at the rising edge of the RESET signal. After the oscillator has started, however, a specific period is required for the oscillator to stabilize. To present the CPU from malfunctioning due to anstable clock, the HALT flip-flop is set to suppress the CPU clock ø while the RESET signal is high. Therefore, the high-level width of the RESET signal must be greater than the time required for the ceramic oscillator you use to stabilize.

Fig. 2-9 System Clock Generator

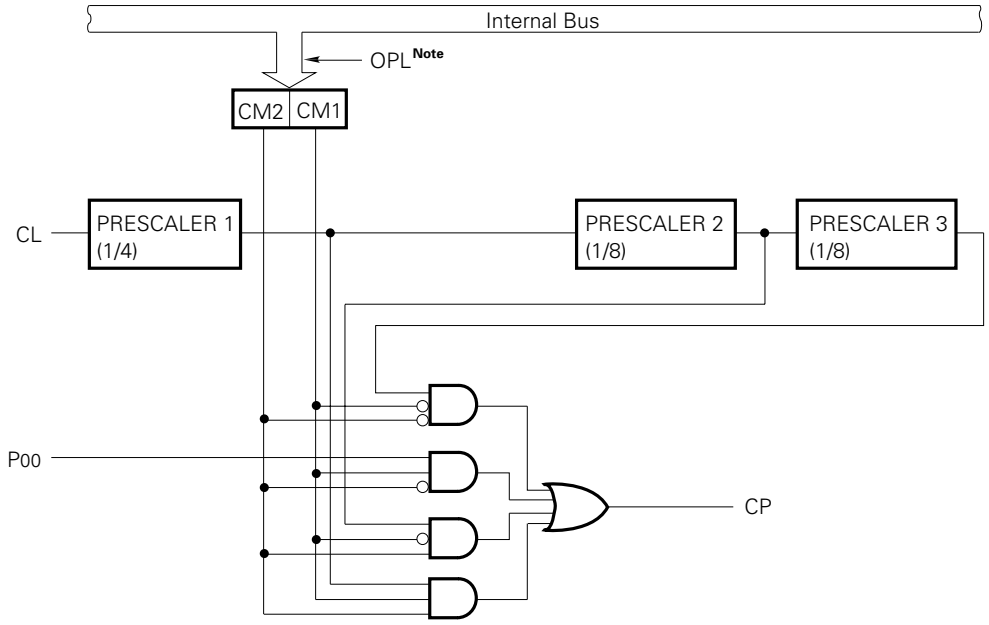


Note indicates that an instruction has been executed.

2.10 CLOCK CONTROL CIRCUIT

The clock control circuit consists of a 2-bit clock mode register (made up of bits CM2 and 1), three prescalers (1, 2, and 3), and a multiplexer. This circuit inputs the output from the system clock generator (i.e., CL). An event pulse (from pin P00) selects a clock source and prescaler, as specified by the clock mode register, and supplies a count pulse (CP) to the timer/event counter.

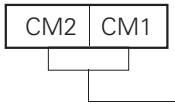
Fig. 2-10 Clock Control Circuit



Note indicates that an instruction has been executed.

A code is set in the clock mode register by an OPL (L = 12) instruction.

Fig. 2-11 Clock Mode Register Format



Clock mode register

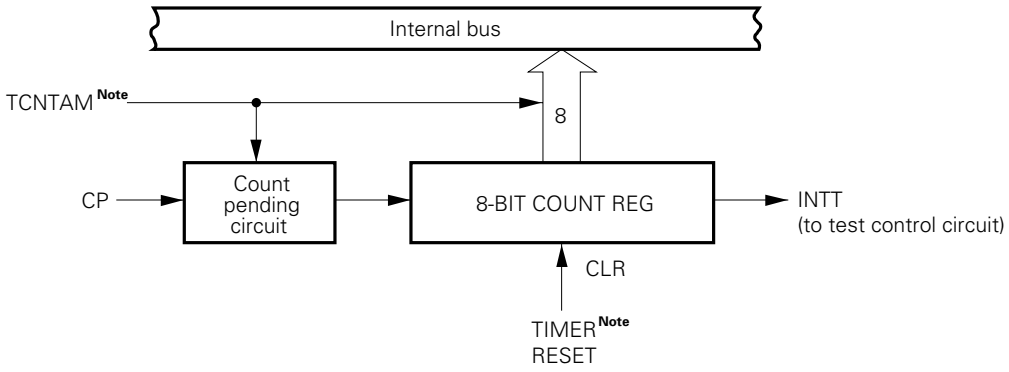
CM2	CM1	Count pulse frequency (CP)
0	0	CL x 1/256
0	1	P00
1	0	CL x 1/32
1	1	CL x 1/4

Caution When setting a code in the clock mode register by the OPL instruction, be sure to clear the bit 0 (which corresponds to CM0 of EVAKIT-7500B (μPD7500) during emulation) for the accumulator to 0.

2.11 TIMER/EVENT COUNTER

The timer/event counter mainly consists of an 8-bit count register.

Fig. 2-12 Timer/Event Counter



Note indicates that an instruction has been executed.

The 8-bit count register is a binary up-counter. The contents of this counter are incremented each time a count pulse (CP) is input to the counter, and are cleared to 00H when TIMER instruction has been executed, when the RESET signal has been input, or when overflow (i.e., counting from FFH to 00H) has occurred in the counter.

The following four count pulses can be selected by the clock mode register (see **2.10 Clock Control Circuit**).

$$\text{CP: CL} \times \frac{1}{4}\text{, CL} \times \frac{1}{32}\text{, CL} \times \frac{1}{256}\text{, P00}$$

The count register always counts up as long as the count pulse is input to it. Therefore, the TIMER instruction clears the contents of the count register to 00H and triggers a timer operation.

The count register contents are incremented in synchronization with CP (or the rising edge of the P00 signal, when an external clock is selected). When the number of counts reaches 256, the count value is returned from FFH to 00H. At this time, the count register generates an overflow signal (INTT), setting the INTT test flag (INTT RQF).

The count register then starts counting up from 00H.

Whether or not an overflow has occurred can be learned by testing the INT RQF flag, using the SKI instruction.

When the timer/event counter operates as a timer, the reference time for the timer is determined by the CP frequency. The accuracy of the measured time is determined, when the system clock is selected, by the system clock oscillation frequency. If the signal input through the P00 pin is selected as the clock, the accuracy is determined by the frequency of the signal input to the P00 pin.

The contents of the count register can always be made ready by TCNTAM instruction. By using this instruction, the current time for the timer can be checked, or it can be determined how many event pulses have been generated so far by inputting the event pulses to the P00 pin and counting them (event counter operation).

The count pending circuit is to ignore changes in the count pulses (CPs) while TCNTAM instruction is executed. This is necessary because, when TCNTAM instruction is used to read the contents of the count register, unstable data may be read while the present count is being updated.

The timer/event counter operates using the system clocks (CL) or the signals input to the P00 pin as count pulses. Therefore, the timer/event counter can be used to release the HALT mode, in which the supply of the CPU clock ø is stopped (see **3. STANDBY FUNCTIONS**).

2.12 TEST CONTROL CIRCUIT

The test control circuit consists of two test flags, a flag called SM3, and a test request flag control circuit. The test request flags, INT0 RQF and INTT RQF, are set by two kinds of test sources (external test input (INT0) and timer overflow (INTT)). The SM3 flag determines whether or not inputting signals to the INT0 pin is enabled. The test request flag control circuit checks the contents of the test request flags, when an SKI instruction is executed, and resets the flags.

The SM3 flag is set by an OPL (L = 0FH) instruction (corresponding to A3). When this flag is 1, the INT0 input is enabled.

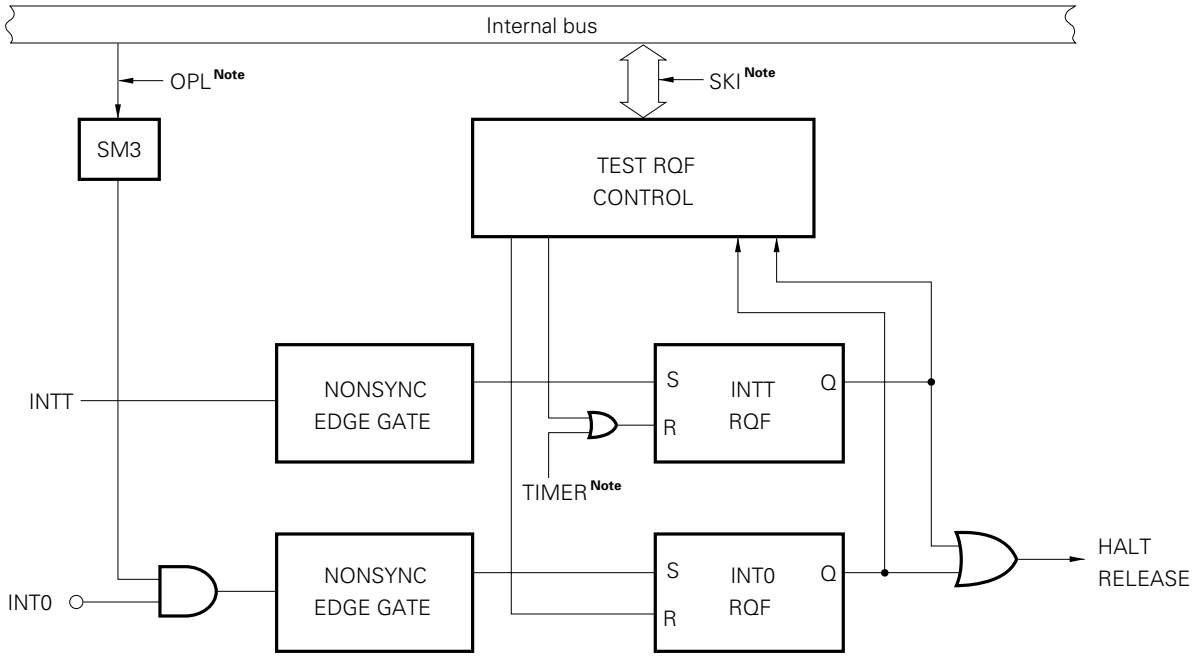
The INT0 RQF flag is set when the rising edge is detected on the INT0 pin, and is reset by an SKI instruction.

The INTT RQF flag is set when an overflow occurs in the timer, and is reset by an SKI or TIMER instruction.

The signals output by the test request flags are used to release the HALT modes. If one of or both the flags were to be set, the HALT modes are released.

When the RESET signal is input, both the test request flags and SM3 flag are reset. Therefore, INT0 input is disabled as the initial condition after the RESET signal has been applied.

Fig. 2-13 Test Control Circuit



Note indicates that an instruction has been executed.

3. STANDBY FUNCTIONS

The μPD7566A can be set in two standby modes (STOP and HALT), in which the power dissipation for the microcomputer can be reduced while the program stands by. The STOP mode is set by a STOP instruction, while the HALT mode is set by a HALT Instruction. In the STOP mode, the supply of all the clocks is stopped, but the supply of only the CPU clock ø is stopped in the HALT mode. When the HALT mode is set, program execution is stopped, but the contents of all the registers and data memory, immediately before the HALT mode has been set, are retained. The timer/event counter can operate even in the HALT mode.

The STOP mode is released only by the input of the RESET signal. The HALT mode can be released by setting either or both the test request flags (INTT RQF and INT0 RQF), or by inputting the RESET signal. Therefore, the standby mode cannot be set, even when the STOP or HALT instruction is executed while one of the test request flags is set. To set the standby mode, when it is possible that one of the test request flags is set, execute an SKI instruction in advance to reset the test request flag.

3.1 STOP MODE

The STOP mode can be set any time by executing the STOP instruction, unless either or both the test request flags are set.

In this mode, the data memory contents are retained, but all other functions are stopped and become invalid, except for the RESET signal, which is used to release the STOP mode. Consequently, the power dissipation for the microcomputer is minimized.

Caution In the STOP mode, the CL1 pin is internally short-circuited to V_{DD} (high level) to prevent the leakage current from the ceramic oscillator.

3.2 HALT MODE

In this mode, only the 1/2 frequency divider for the system clock generator is stopped. Consequently, the supply of system clock (CL) is not stopped and only the CPU clock (ø) is stopped. The operation of the CPU, which calls for the CPU clock, is therefore stopped.

However, the clock control circuit is not stopped. The clock control circuit can therefore input the CL signal generated by the system clock generator and event pulses input from an external source through the P00 pin, can supply both the clocks to the timer/event counter as count pulses (CPs). The timer/event counter can therefore operate on both the count pulses and its operation will not be interrupted.

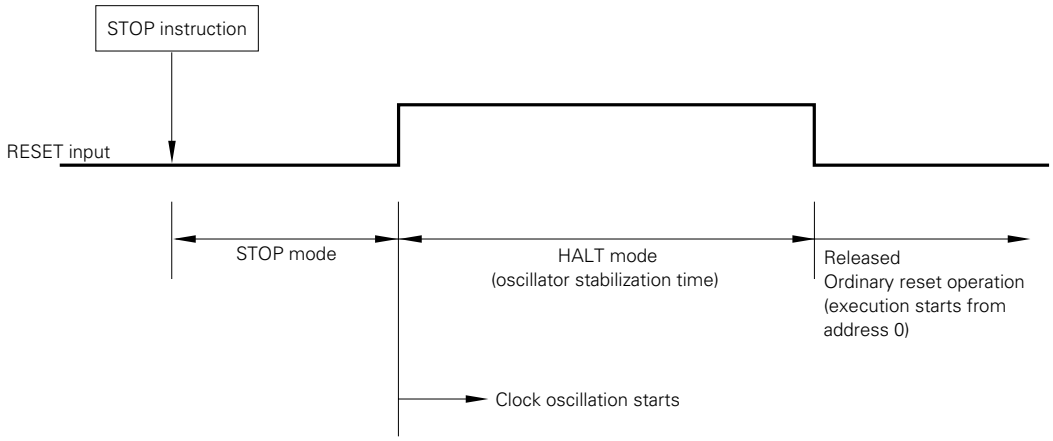
3.3 RELEASING STOP MODE BY USING RESET INPUT

When the RESET signal becomes high in the STOP mode, the HALT mode is set, and at the same time, ceramic oscillation starts.

When the RESET signal goes low, the HALT mode is released followed by ordinary RESET operation. After that, the CPU starts executing the program from address 0. The STOP mode is thus released.

The contents of the data memory are retained even while the mode is released, that the contents of registers become undefined.

Fig. 3-1 STOP Mode Release Timing



Caution The STOP mode is not released by setting the test request flags.

3.4 RELEASING HALT MODE BY USING TEST REQUEST FLAGS

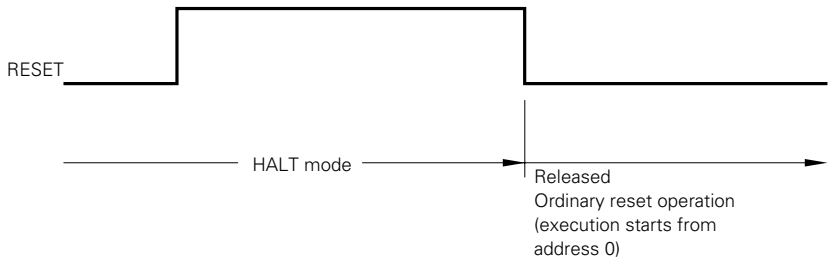
The HALT is released when either or both of the test request flags (INTT RQF and INT0 RQF) are set, and program execution is resumed, starting from the instruction next to the HALT instruction.

The contents of the registers and data memory, which have been retained during the HALT mode, are not affected by the release of the HALT mode.

3.5 RELEASING HALT MODE BY USING RESET INPUT

When the RESET signal is input, the HALT mode is unconditionally released, as illustrated in Fig. 3-2.

Fig. 3-2 HALT Mode Release Timing by RESET Input



While the RESET signal is active (high level), the HALT mode continues. When the RESET signal goes low, the HALT mode is released. Ordinary resetting operation is then accomplished. Then, the program is executed starting from address 0.

The contents of the data memory, retained during the HALT mode, are not affected by the RESET signal. However, the contents of the registers are affected and become undefined.

4. RESET FUNCTION

The microcomputer is reset and initialized as follows, when an active-high RESET signal is input to the RESET pin:

4.1 INITIALIZATION

(1) The program counter (PC9 to PC0) is cleared to 0.
(2) The skip flags (SK1 and SK0) for the program status word are reset to 0.
(3) The count register for the timer/event counter is cleared to 00H.
(4) The clock control circuit is initialized as follows:
- Clock mode register (bits CM2 and 1) = 0

$$\rightarrow CP = CL \times \frac{1}{256}$$

- Prescalers 1, 2, and 3 = 0

(5) The SM3 flag is reset to 0, disabling the external test input (INT0).
(6) The test request flags (INTT RQF and INT0 RQF) are reset to 0.
(7) The contents of the data memory and the following registers will become undefined.
Stack pointer (SP)
Accumulator (A)
Carry flag (C)
General-purpose registers (H and L)
Output latches for ports
(8) The output buffers for all the ports are turned off and enter the output high-impedance state.
The I/O ports are set in the input mode.

Caution When the RESET signal is used to released the standby mode, the contents of the data memory do not become undefined, but are retained.

When the RESET signal is removed, the program is executed starting from address 000H. However, initialize or reinitialize the contents for the registers by program.

5. INSTRUCTION SET

(1) Operand representation format and description

addr	10-bit immediate data or label
caddr caddr1	10-bit immediate data or label Immediate data 100H-107H, 140H-147H or label Immediate data 180H-187H, 1C0H-1C7H or label
mem	6-bit immediate data or label
n5 n4 n2	5-bit immediate data or label 4-bit immediate data or label 2-bit immediate data or label
bit	2-bit immediate data or label
pr	HL-, HL+, HL

(2) Legend for "Operation" column

A	:	Accumulator
H	:	H register
L	:	L register
HL	:	Pair register (HL)
pr	:	Pair register (HL-, HL+, HL)
SP	:	Stack pointer
PC	:	Program counter
C	:	Carry flag
PSW	:	Program status word
CT	:	Count register
In	:	Immediate data corresponding to n5, n4, or n2
Pn	:	Immediate data corresponding to addr, caddr, or caddr1
Bn	:	Immediate data corresponding to bit
Dn	:	Immediate data corresponding to mem
Rn	:	Immediate data corresponding to pr
(xx)	:	Contents addressed by xx
xH	:	Hexadecimal data

(3) Selection of port/mode register

IPL Instruction

L	Port
0	Port 0
1	Port 1
AH	Port 10
BH	Port 11

OPL Instruction

L	Port/mode register
8	Port 8
9	Port 9
AH	Port 10
BH	Port 11
CH	Clock mode register
FH	SM3 flag

RPBL; SPBL Instruction

L	FH	EH	DH	CH	BH	AH	9	8	5	4	2	1	0
Bit	3	2	1	0	3	2	1	0	1	0	2	1	0
Port	Port 11				Port 10				Port 9		Port 8		

(4) Selection of addressing mode by pair register

pr	R_1	R_0
HL-	0	0
HL+	0	1
HL	1	0

Instructions	Mnemonic	operand	OP Code B1	OP Code B2	Operation		Skip Condition
Load/Store	LAI	n4	0 0 0 1 I_3 I_2 I_1 I_0		A ← n4	Loads n4 to accumulator	String-effect LAI
	LHI	n2	0 0 1 0 1 0 I_1 I_0		H ← n2	Loads n2 to register H	
	LAM	pr	0 1 0 1 0 0 R_1 R_0		A ← (pr) pr = HL-, HL+, HL	Loads memory contents addressed by pr to accumulator	L = FH (HL-) L = 0 (HL+)
	LHLI	n5	1 1 0 I_4 I_3 I_2 I_1 I_0		H ← 0 I_4, L ← $I_{3\text{-}0}$	Loads n5 to registerpair HL	String-effect LHLI
	ST		0 1 0 1 0 1 1 1		(HL) ← A	Stores accumulator contents to memory addressed by HL	
	STII	n4	0 1 0 0 I_3 I_2 I_1 I_0		(HL) ← n4, L ← L+1	Stores n4 in memory addressed by HL and then increments L register contents	
	XAL		0 1 1 1 1 0 1 1		A ↔ L	Exchanges accumulator contents with L register contents	
	XAM	pr	0 1 0 1 0 1 R_1 R_0		A ↔ (pr) pr = HL-, HL+, HL	Exchanges accumulator contents with contents of memory addressed by pr	L = FH (HL-) L = 0 (HL+)
Arithmetic Operation	AISC	n4	0 0 0 0 I_3 I_2 I_1 I_0		A ↔ A + n4	Adds accumulator contents to n4	Carry
	ASC		0 1 1 1 1 1 0 1		A ← A + (HL)	Adds accumulator contents to contents of memory addressed by HL	Carry
	ACSC		0 1 1 1 1 1 0 0		A, C ← A + (HL) + C	Adds accumulator contents to contents of memory addressed by HL with carry flag	Carry
	EXL		0 1 1 1 1 1 1 0		A ← A ∀ (HL)	Exclusive-ORs accumulator contents with contents of memory addressed by HL	
Accumulator/ Carry Flag Manipulation	CMA		0 1 1 1 1 1 1 1		A ← $\bar{A}$	Complements accumulator contents	
	RC		0 1 1 1 1 0 0 0		C ← 0	Resets carry flag	
	SC		0 1 1 1 1 0 0 1		C ← 1	Sets carry flag	
Increment/ Decrement	ILS		0 1 0 1 1 0 0 1		L ← L + 1	Increments L register contents	L = 0
	IDRS	mem	0 0 1 1 1 1 0 1	0 0 D_5 D_4 D_3 D_2 D_1 D_0	(mem) ← (mem) + 1	Increments contents of memory addressed by mem	(mem) = 0
	DLS		0 1 0 1 1 0 0 0		L ← L - 1	Decrements L register contents	L = FH
	DDRS	mem	0 0 1 1 1 1 0 0	0 0 D_5 D_4 D_3 D_2 D_1 D_0	(mem) ← (mem) - 1	Decrements contents of memory addressed by mem	(mem) = FH
Memory bit Manipulation	RMB	bit	0 1 1 0 1 0 B_1 B_0		$(HL)_{bit}$ ← 0	Resets bit, specified by $B_{1\text{-}0}$, of memory addressed by HL	
	SMB	bit	0 1 1 0 1 1 B_1 B_0		$(HL)_{bit}$ ← 1	Sets bit, specified by $B_{1\text{-}0}$, of memory addressed by HL	

Instructions	Mnemonic	operand	OP Code B1	OP Code B2	Operation		Skip Condition
Jump	JMP	addr	0 0 1 0 0 0 P_9 P_8	P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0	$PC_{9-0} \leftarrow P_{9-0}$	Jumps to address indicated by P_{9-0}	
	JCP	addr	1 0 P_5 P_4 P_3 P_2 P_1 P_0		$PC_{5-0} \leftarrow P_{5-0}$	Jumps to address specified by P_{5-0} which replaces PC_{5-0}	
Subroutine/ Stack Control	CALL	caddr	0 0 1 1 0 0 P_9 P_8	P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0	(SP-1)(SP-2)(SP-4)$\leftarrow PC_{9-0}$ (SP-3)$\leftarrow$ PSW, SP$\leftarrow$ SP - 4 $PC_{9-0} \leftarrow P_{9-0}$	Saves contents of PC and PSW to stack, decrements SP by 4, and calls address indicated by caddr	
	CAL	caddr1	1 1 1 P_4 P_3 P_2 P_1 P_0		(SP-1)(SP-2)(SP-4)$\leftarrow PC_{9-0}$ (SP-3) $\leftarrow$ PSW, SP $\leftarrow$ SP - 4 $PC_{9-0} \leftarrow$ 0 1 $P_4P_3$0 0 0 $P_2P_1P_0$	Saves contents of PC and PSW to stack, decrements SP by 4, and calls address indicated by caddr1	
	RT		0 1 0 1 0 0 1 1		$PC_{9-0} \leftarrow$ (SP)(SP+2)(SP+3) SP $\leftarrow$ SP + 4	Restores contents of stack memory to PC and increments SP by 4	
	RTS		0 1 0 1 1 0 1 1		$PC_{9-0} \leftarrow$ (SP)(SP+2)(SP+3) SP $\leftarrow$ SP + 4 then skip unconditionally	Restores contents of stack memory to PC, increments SP by 4, and skips unconditionally	Unconditionally
	TAMSP		0 0 1 1 1 1 1 1	0 0 1 1 0 0 0 1	$SP_{5-4} \leftarrow A_{1-0}$ $SP_{3-1} \leftarrow (HL)_{3-1}$, $SP_0 \leftarrow 0$	Transfers lower 2 bits of accumulator to SP_{5-4}, and higher 3 bits of contents of memory, addressed by HL, to SP_{3-1}	
Skip	SKC		0 1 0 1 1 0 1 0		Skip if C = 1	Skips if carry flag is 1	C = 1
	SKABT	bit	0 1 1 1 0 1 B_1 B_0		Skip if A_{bit} = 1	Skips if bit, specified by B_{1-0}, of accumulator is 1	A_{bit} = 1
	SKMBT	bit	0 1 1 0 0 1 B_1 B_0		Skip if $(HL)_{bit}$ = 1	Skips if bit, specified by B_{1-0}, of memory addressed by HL is 1	$(HL)_{bit}$ = 1
	SKMBF	bit	0 1 1 0 0 0 B_1 B_0		Skip if $(HL)_{bit}$ = 0	Skips if bit, specified by B_{1-0}, of memory addressed by HL is 0	$(HL)_{bit}$ = 0
	SKAEM		0 1 0 1 1 1 1 1		Skip if A = (HL)	Skips if accumulator contents are equal to contents of memory addressed by HL	A = (HL)
	SKAEI	n4	0 0 1 1 1 1 1 1	0 1 1 0 I_3 I_2 I_1 I_0	Skip if A = n4	Skips if accumulator contents are equal to n4	A= n4
	SKI	n2	0 0 1 1 1 1 1 1	0 1 0 0 0 0 I_1 I_0	Skip if INT RQF = 1 Then reset INT RQF	Skips if INT RQF is 1, and then clears INT RQF to 0	INT RQF = 1

Instructions	Mnemonic	operand	OP Code B1	OP Code B2	Operation		Skip Condition
Timer Control	TIMER		0 0 1 1 1 1 1 1	0 0 1 1 0 0 1 0	Start Timer	Starts timer operation	
	TCNTAM		0 0 1 1 1 1 1 1	0 0 1 1 1 0 1 1	A ← CT_{7-4} (HL) ← CT_{3-0}	Transfers higher 4 bits of count register to accumulator, and lower 4 bits to memory addressed by HL	
Input/Output	IPL		0 1 1 1 0 0 0 0		A ← Port (L)	Loads contents of port specified by L register to accumulator	
	IP1		0 1 1 1 0 0 0 1		A ← Port 1	Inputs contents of port to accumulator	
	OPL		0 1 1 1 0 0 1 0		Port/Mode reg.(L) ← A	Outputs accumulator contents to port or mode register specified by L register	
	RPBL Note		0 1 0 1 1 1 0 0		Port bit (L) ← 0	Resets bits of port 8, 10, or 11 specified by L register	
	SPBL Note		0 1 0 1 1 1 0 1		Port bit (L) ← 1	Sets bits of port 8, 10, or 11 specified by L register	
CPU Control	HALT		0 0 1 1 1 1 1 1	0 0 1 1 0 1 1 0	Set Halt mode	Sets HALT mode	
	STOP		0 0 1 1 1 1 1 1	0 0 1 1 0 1 1 1	Set Stop Mode	Sets STOP mode	
	NOP		0 0 0 0 0 0 0 0		No operation	Performs nothing but waits for 1 machine cycle	

Note Although the SPBL and RPBL instructions are to set or reset a specified bit, they also output port contents (in 4-bit units) including the specified bit as soon as the specified bit has been set or reset (the contents of the output latch are output to pins other than the specified bit). Before executing these instructions, initialize the contents of the output latch by executing the OPL instruction.

6. ELECTRICAL SPECIFICATIONS

μPD7566A: ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Condition		Rating	Unit
Supply Voltage	V_{DD}			-0.3 to + 7.0	V
Input Voltage	V_I	Other than ports 10 and 11		-0.3 to V_{DD} + 0.3	V
		Ports 10 and 11	**Note 1**	-0.3 to V_{DD} + 0.3	V
			Note 2	-0.3 to +11	V
Output Voltage	V_O	Other than ports 8 to 11		-0.3 to V_{DD} + 0.3	V
		Ports 8 to 11	**Note 1**	-0.3 to V_{DD} + 0.3	V
			Note 2	-0.3 to +11	V
High-Level Output Current	I_{OH}	1 pin		-5	mA
		Total of all pins		-15	mA
Low-Level Output Current	I_{OL}	1 pin	Ports 8 and 9	30	mA
			Others	15	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			-10 to +70	°C
Storage Temperature	T_{stg}			-65 to +150	°C
Power Dissipation	P_d	T_a = 70°C	Shrink DIP	480	mW
			Mini-flat	250	

Note 1. CMOS input/output or N-channel open-drain output with pull-up resistor connected

2. N-channel open-drain input/output

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product. ★

★ **μPD7566A(A): ABSOLUTE MAXIMUM RATINGS** (T_a = 25°C)

Item	Symbol	Condition		Rating	Unit
Supply Voltage	V_{DD}			-0.3 to + 7.0	V
Input Voltage	V_I	Other than ports 10 and 11		-0.3 to V_{DD} + 0.3	V
		Ports 10 and 11	**Note 1**	-0.3 to V_{DD} + 0.3	V
			Note 2	-0.3 to +11	V
Output Voltage	V_O	Other than ports 8 to 11		-0.3 to V_{DD} + 0.3	V
		Ports 8 to 11	**Note 1**	-0.3 to V_{DD} + 0.3	V
			Note 2	-0.3 to +11	V
High-Level Output Current	I_{OH}	1 pin		-5	mA
		Total of all pins		-15	mA
Low-Level Output Current	I_{OL}	1 pin	Ports 8 and 9	30	mA
			Others	15	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C
Power Dissipation	P_d	T_a = 85°C	Shrink DIP	350	mW
			Mini-flat	195	

Note 1. CMOS input/output or N-channel open-drain output with pull-up resistor connected

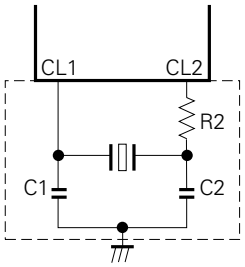
2. N-channel open-drain input/output

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

CAPACITANCE (T_a = 25°C, V_{DD} = 0V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz 0V at pins other than measured pin	P00, P01, P10 to P13			15	pF
Output Capacitance	C_{OUT}		$C_{in}0$ to $C_{in}3$			15	pF
Input/Output Capacitance	C_{IO}		Ports 8 and 9			35	pF
			Ports 10 and 11			35	pF

OSCILLATOR CHARACTERISTICS (μPD7566A : T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0V
μPD7566A(A) : T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0V)

Oscillator	External Circuit	Item	Condition	MIN.	TYP.	MAX.	Unit
Ceramic Oscillator Note		Oscillation frequency (f_{CC})	V_{DD} = 4.5 to 6.0V	290	700	710	kHz
			V_{DD} = 4.0 to 6.0V	290	500	510	kHz
			V_{DD} = 3.5 to 6.0V	290	400	410	kHz
			V_{DD} = 2.7 to 6.0V	290	300	310	kHz
		Oscillation stabilization time (t_{OS})	After the minimum value of the operating voltage range has been reached	20			ms

Note The following ceramic oscillators are recommended:

Manufacturer	Product Name	Recommended Constants			Operating Voltage Range [V]	
		C1 [pF]	C2 [pF]	R2 [kΩ]	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSB300D	330	330	6.8	2.7	6.0
	CSB400P	220	220	6.8	3.5	6.0
	CSB500E	100	100	6.8	4.0	6.0
	CSB700A	100	100	6.8	4.5	6.0
Kyoto Ceramic Co., Ltd.	KBR-300B	470	470	0	2.7	6.0
	KBR-400B	330	330	0	3.5	6.0
	KBR-500B	220	220	0	4.0	6.0
	KBR-680B	220	220	0	4.5	6.0
Toko Inc.	CRK-400	120	120	12	3.5	6.0
	CRK-500	100	100	12	4.0	6.0
	CRK-680	82	82	12	4.5	6.0

Caution 1. Locate the oscillation circuit as close as possible to the CL1 and CL2 pins.

2. Do not route any other signal lines in the area enclosed by the dotted Line.

DC CHARACTERISTICS (μPD7566A : T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0V; μPD7566A(A) : T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than ports 10 and 11		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 10 and 11[Note 1]		0.7V_{DD}		9	V
Low-Level Input Voltage	V_{IL}			0		0.3V_{DD}	V
High-Level Output Voltage	V_{OH}	Ports 8 to 11	V_{DD} = 4.5 to 6.0V, I_{OH} = -1 mA	V_{DD}-2.0			V
			I_{OH} = -100 μA	V_{DD}-1.0			V
Low-Level Output Voltage	V_{OL}	Ports 10 and 11	V_{DD} = 4.5 to 6.0V, I_{OL} = 1.6 mA			0.4	V
			V_{DD} = 4.5 to 6.0V, I_{OL} = 10 mA			2.0	V
			I_{OL} = 400 μA			0.5	V
		Port 8 and 9	V_{DD} = 4.5 to 6.0V, I_{OL} = 15 mA			2.0	V
			I_{OL} = 600 μA			0.5	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}				3	μA
	I_{LIH2}	V_{IN} = 9V, Ports 10 and 11[Note 1]				10	μA
Low-Level Input Leakage Current	I_{LIL}	V_{IN} = 0V				-3	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}				3	μA
	I_{LOH2}	V_{OUT} = 9V, Ports 8, 9, 10 and 11[Note 1]				10	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0V				-3	μA
Resistor Interconnected To Input Pin (Pull-Up, Pull-Down)		Ports 0 and 1, RESET		23.5	47	70.5	kΩ
Resistor Interconnected To Output Pin (Pull-Up)		Ports 10 and 11		7.5	15	22.5	kΩ
Supply Current[Note 2]	I_{DD1}	Operation mode	V_{DD} = 5V±10%, f_{CC} = 700 kHz		650	2200	μA
			V_{DD} = 3V±10%, f_{CC} = 300 kHz		120	360	μA
	I_{DD2}	HALT mode	V_{DD} = 5V±10%, f_{CC} = 700 kHz		450	1500	μA
			V_{DD} = 3V±10%, f_{CC} = 300 kHz		65	200	μA
	I_{DD3}	STOP mode	V_{DD} = 5V±10%		0.1	10	μA
			V_{DD} = 3V±10%		0.1	5	μA

Note 1. With N-channel open-drain input/output selected

2. Excluding current flowing through internal pull-up and pull-down resistors, comparator, and internal bias resistor

COMPARATOR CHARACTERISTICS (μPD7566A : T_a = -10 to +70°C, V_{DD} = 3.0 to 6.0V; μPD7566A(A) : T_a = -40 to +85°C, V_{DD} = 3.0 to 6.0V)

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Ccomparator Current Dissipation[Note]			Cin 0 to Cin 3, 1 circuit V_{DD} = 5V±10%	25	50	100	μA	★
Comparator Input	Input Voltage Range	Vcin Vref		0		V_{DD}	V	
	Response Time			2		4	t_{CY}	
	Resolution		V_{DD} =5V±10%		10	50	mV	
						100	mV	
	Input Leakage Current					±3	μA	
	Internal Bias Resistor	R_{ref}		50	100	200	kΩ	★

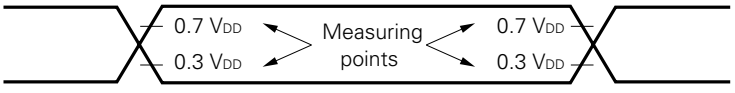
Note Excluding current flowing through internal bias resistor

AC CHARACTERISTICS (μPD7566A : T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0V; μPD7566A(A) : T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Internal Clock Cycle Time	t_{CY}[Note]	V_{DD} =4.5 to 6.0V		2.8		6.9	μs
				6.4		6.9	μs
P00 Event Input Frequency	f_{P0}	duty = 50%	V_{DD} = 4.5 to 6.0V	0		710	kHz
				0		350	kHz
P00 Input Rise and Fall Time	t_{P0R}, t_{P0F}					0.2	μs
P00 Input High- and Low-Level Widths	t_{P0H}, t_{P0L}	V_{DD} = 4.5 to 6.0V		0.7			μs
				1.45			μs
INT0 High- and Low-Level Widths	t_{I0H}, t_{I0L}			10			μs
Reset High- and Low-Level Widths	t_{RSH}, t_{RSL}			10			μs

Note t_{CY} = 2/f_{CC} (Refer to the characteristic curve for the power requirement not listed above.)

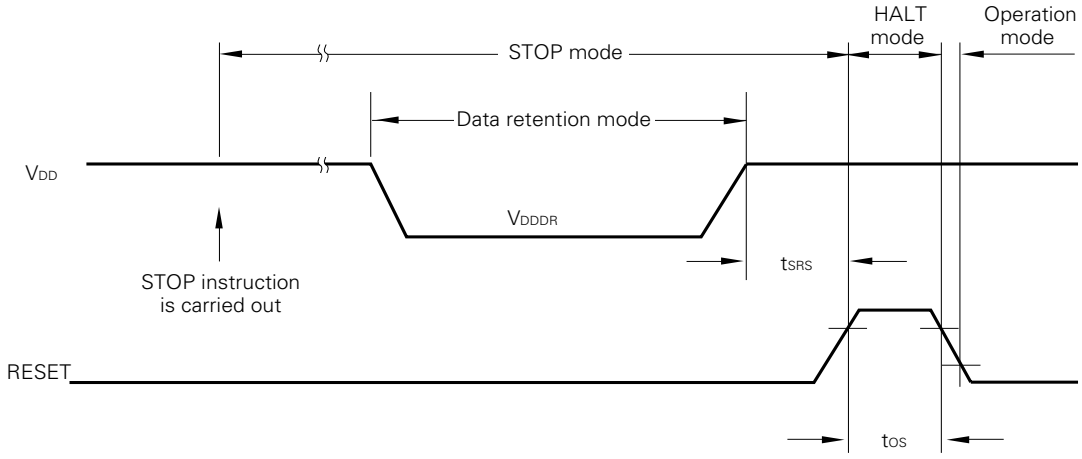
AC TIMING MEASURING POINTS (other than CL1 input)



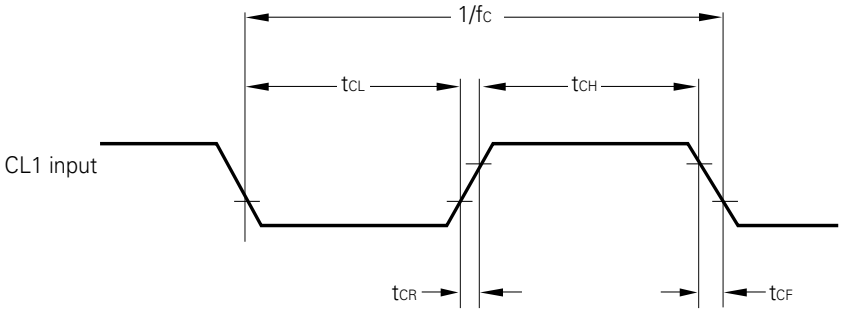
DATA MEMORY DATA RETENTION CHARACTERISTICS IN STOP MODE (μPD7566A : T_a = -10 to +70°C, μPD7566A(A): T_a = -40 to +85°C)

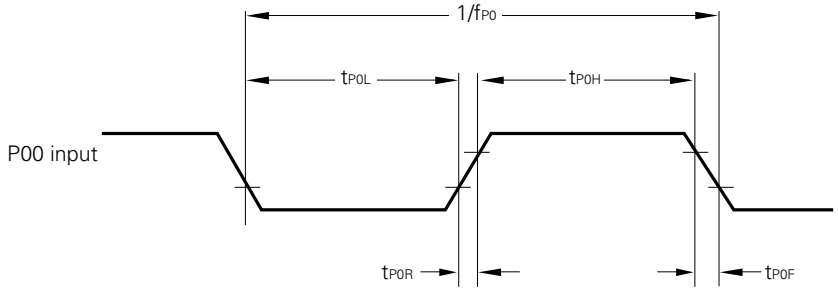
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage for Data Retention	V_{DDDR}		2.0		6.0	V
Supply Current for Data Retention	I_{DDDR}	V_{DDDR} = 2.0V		0.1	5	μA
Reset Setup Time	t_{SRS}		0			μs
Oscillation Stabilization Time	t_{OS}	After V_{DD} reached 4.5V	20			ms

DATA RETENTION TIMING

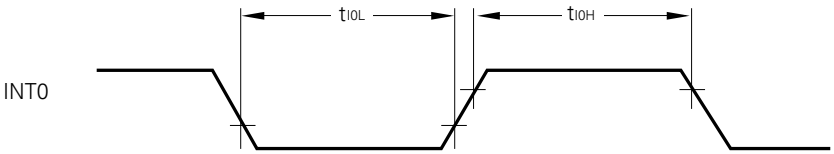


CLOCK TIMING

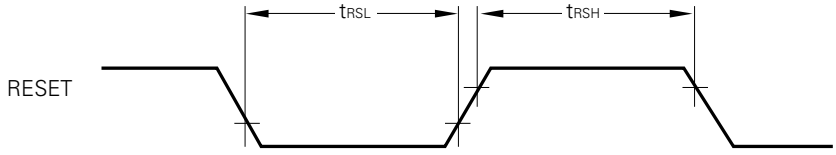




TEST INPUT TIMING



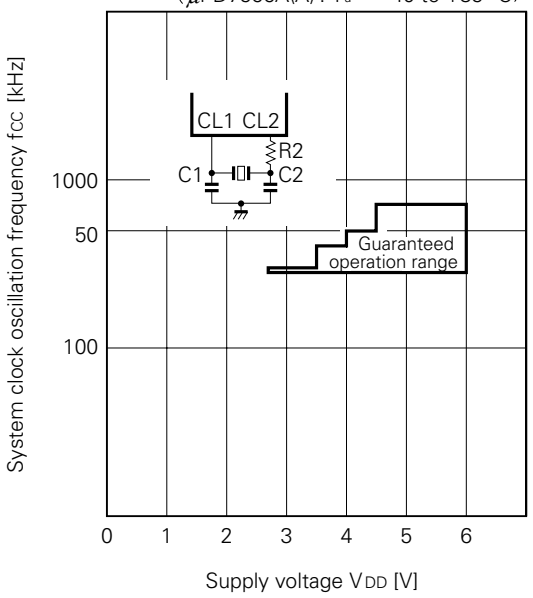
RESET INPUT TIMING



7. CHARACTERISTIC DATA

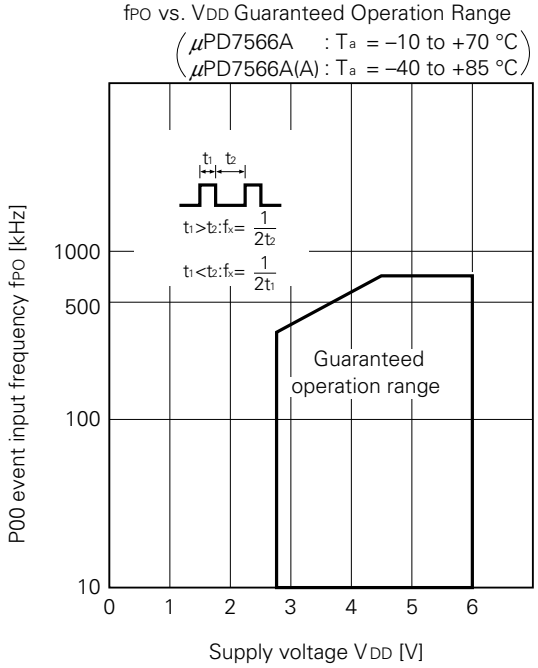
fCC vs. VDD Guaranteed Operation Range

(μPD7566A : Ta = –10 to +70 °C
μPD7566A(A) : Ta = –40 to +85 °C)

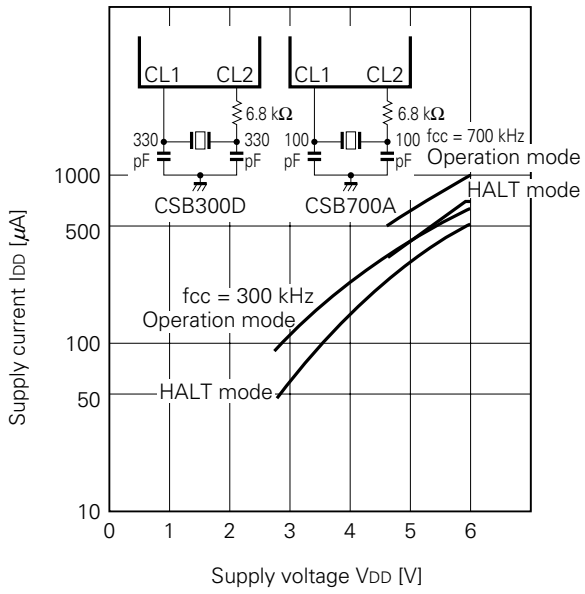


fPO vs. VDD Guaranteed Operation Range

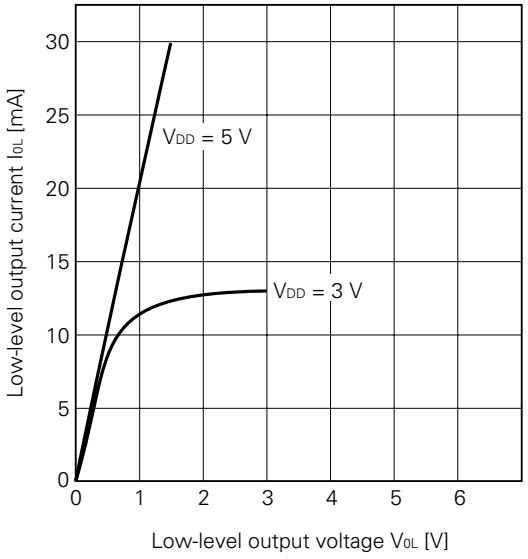
(μPD7566A : Ta = –10 to +70 °C
μPD7566A(A) : Ta = –40 to +85 °C)



I_{DD} vs. V_{DD} Characteristic Example
(Reference Value)
(T_a = 25°C)



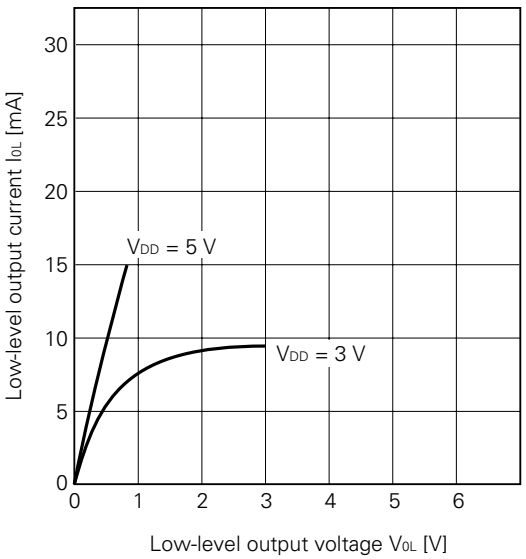
I_{OL} vs. V_{OL} Characteristic Example (Ports 8 and 9)
(Reference Value)
(T_a = 25°C)



Caution The absolute maximum rating is 30 mA per pin.

I_{OL} vs. V_{OL} Characteristic Example (Ports 10 and 11)
(Reference Value)

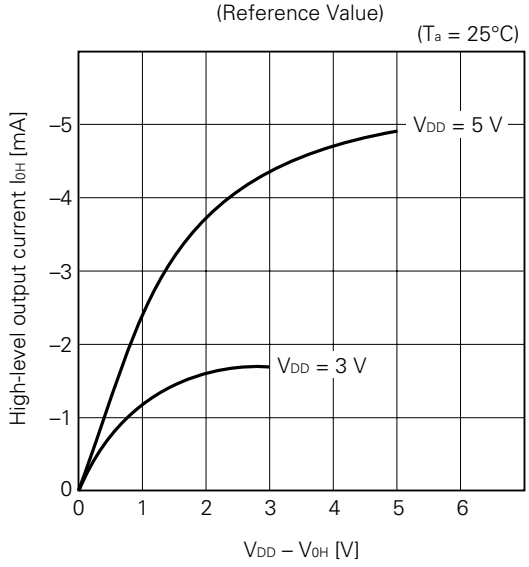
(T_a = 25°C)



Caution The absolute maximum rating is 15 mA per pin.

I_{OH} vs. V_{OH} Characteristic Example
(Reference Value)

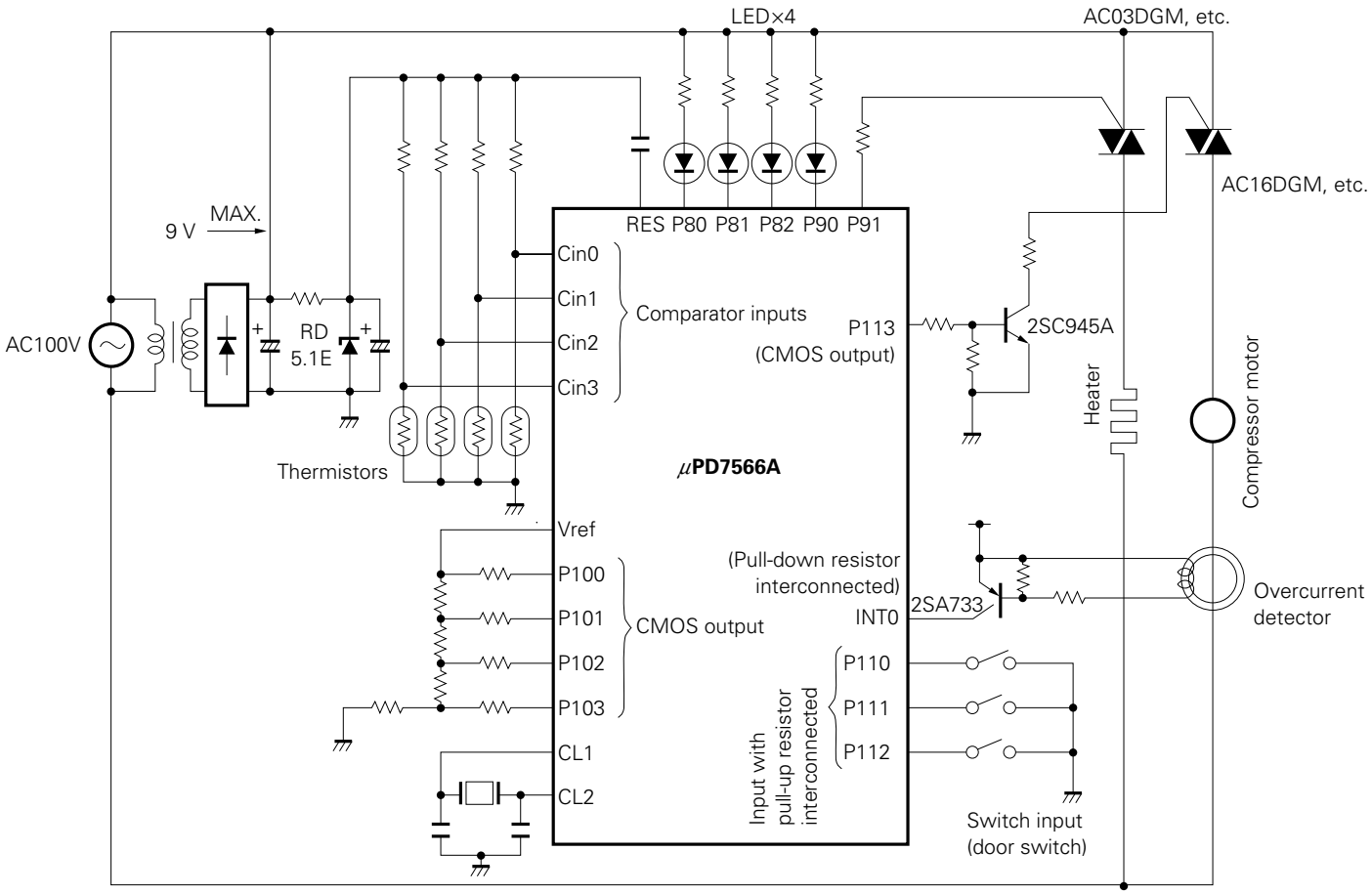
(T_a = 25°C)



Caution The absolute maximum rating is –5 mA per pin.

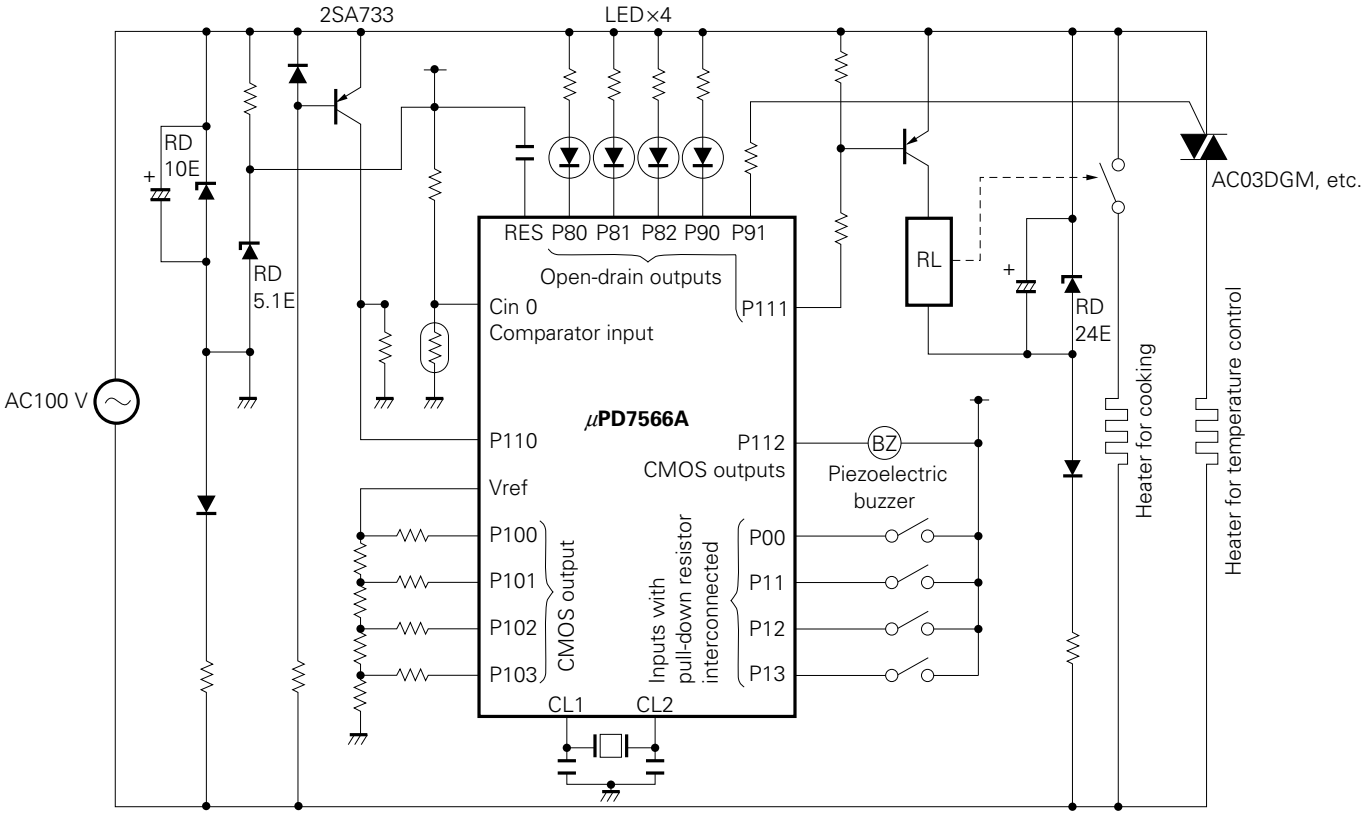
8. APPLICATION CIRCUITS

(1) Refrigerator and Air Conditioner

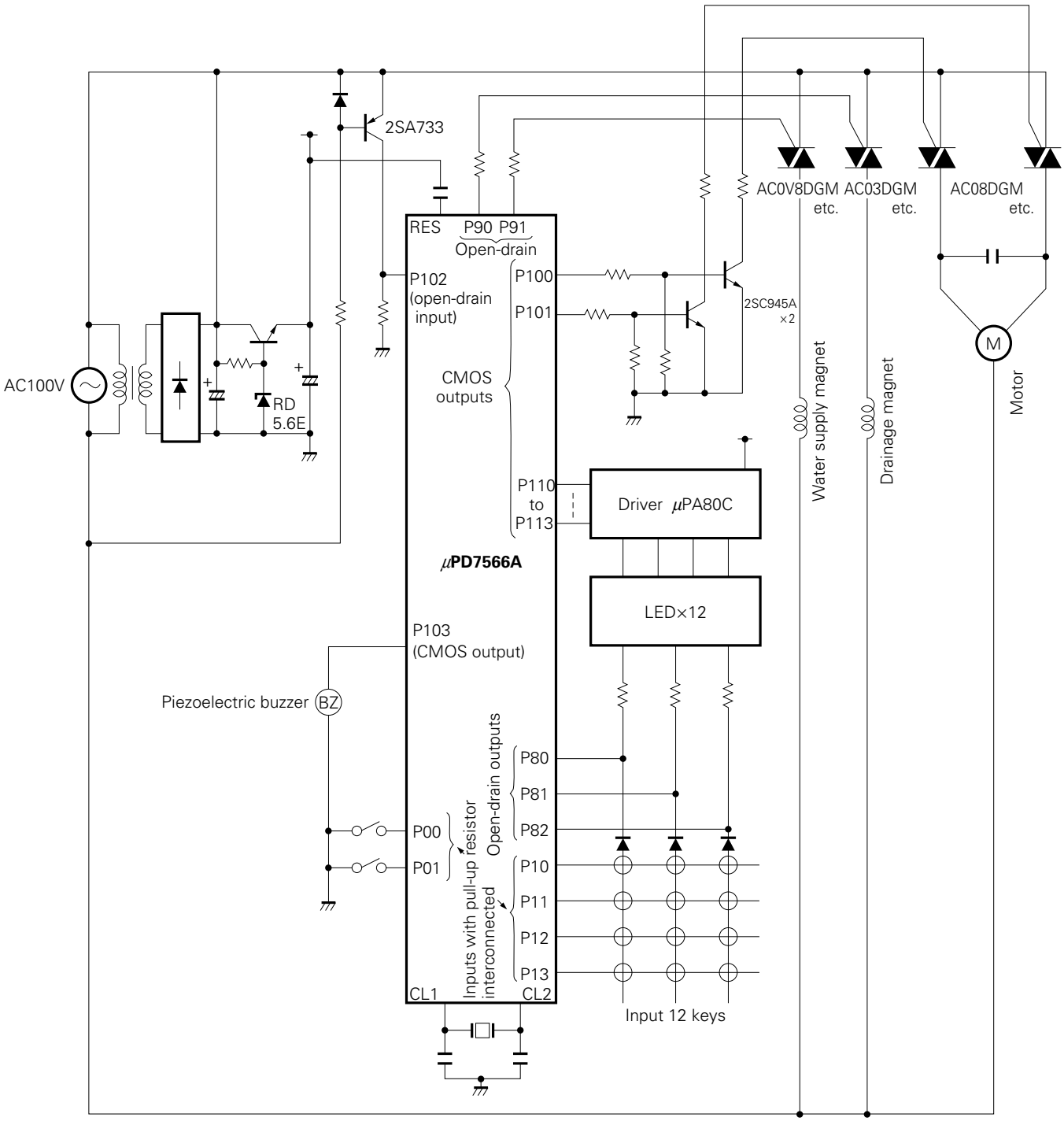


The above example shows a circuit for a refrigerator. A circuit for an air conditioner can be implemented by replacing only the heater with a fan motor.

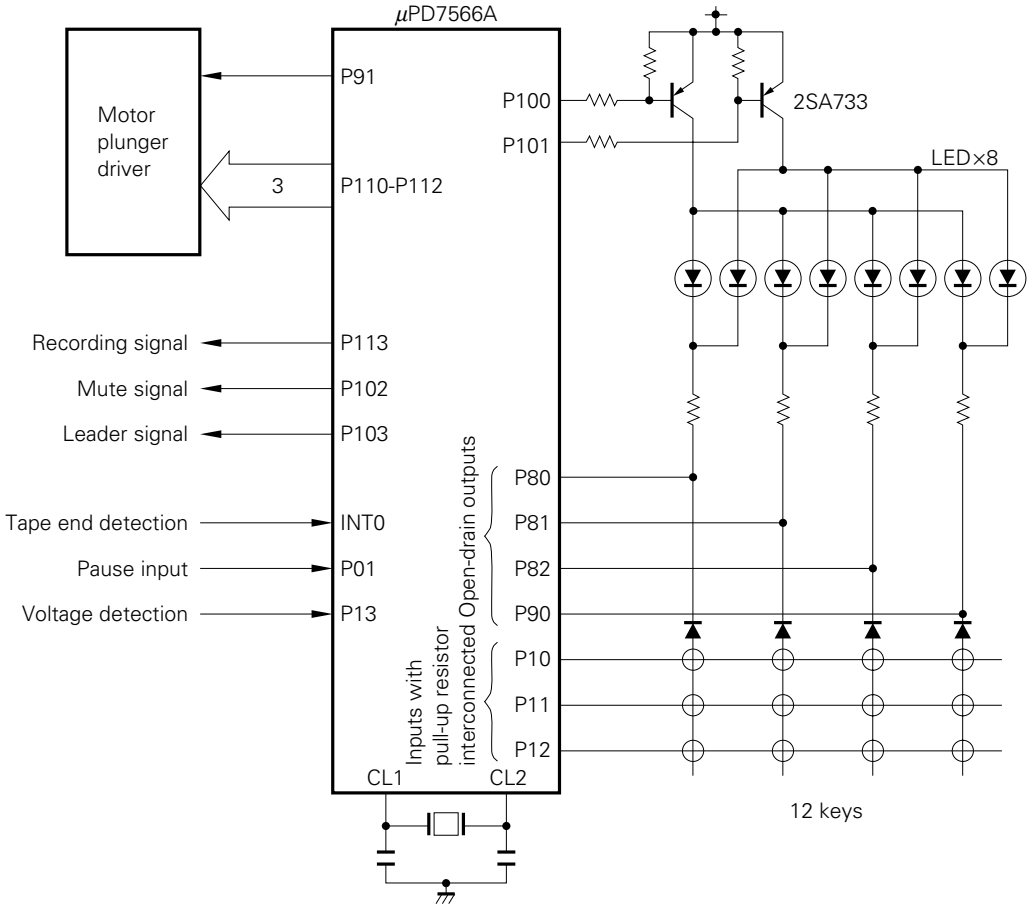
(2) Rice Cooker



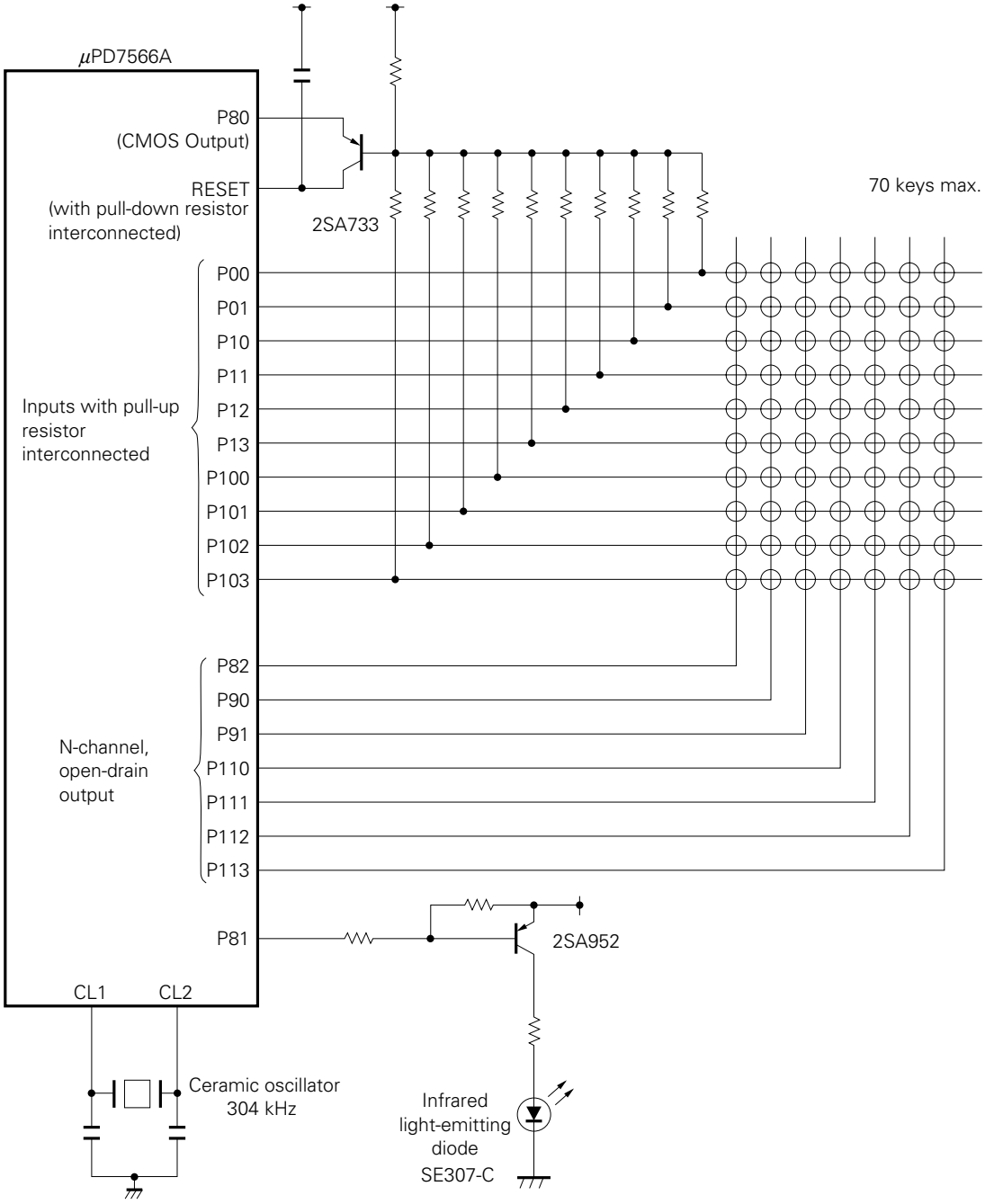
(3) Washing Machine



(4) Cassette Deck Controller



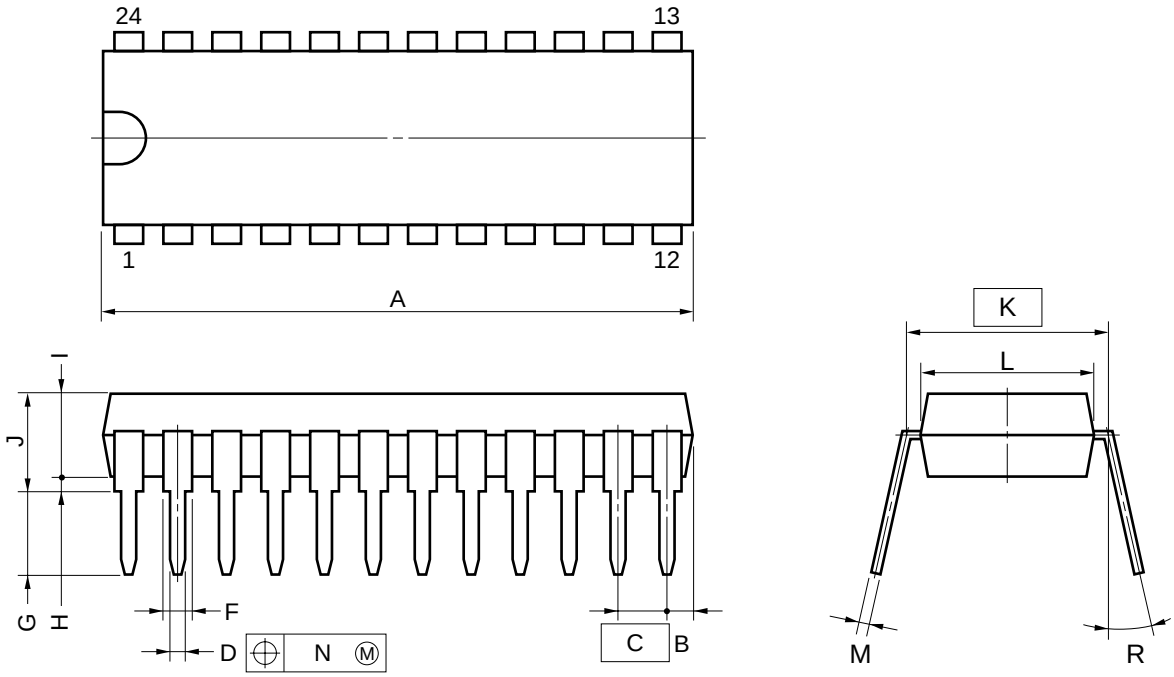
(5) Remote Controller



9. PACKAGE DRAWINGS

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (1/2)

24 PIN PLASTIC SHRINK DIP (300 mil)



NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

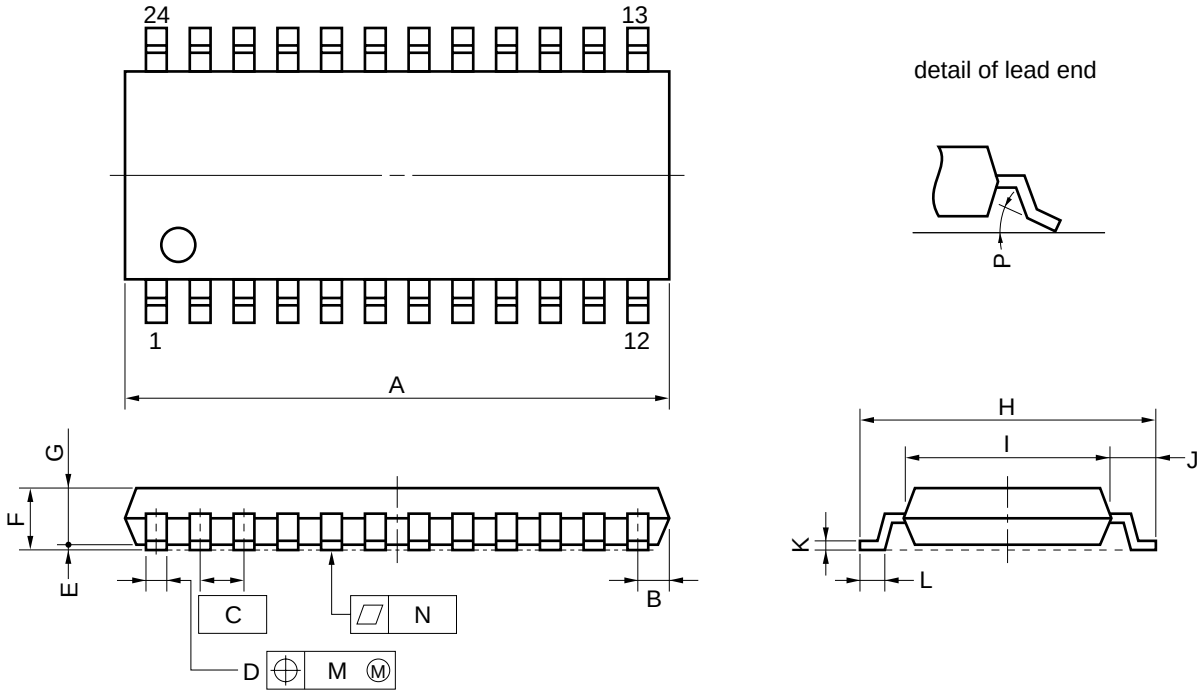
ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S24C-70-300B-1

★ **Caution Dimensions of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (1/2).**

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (2/2)

24 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P24GM-50-300B-4

Caution Dimensions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (2/2). ★

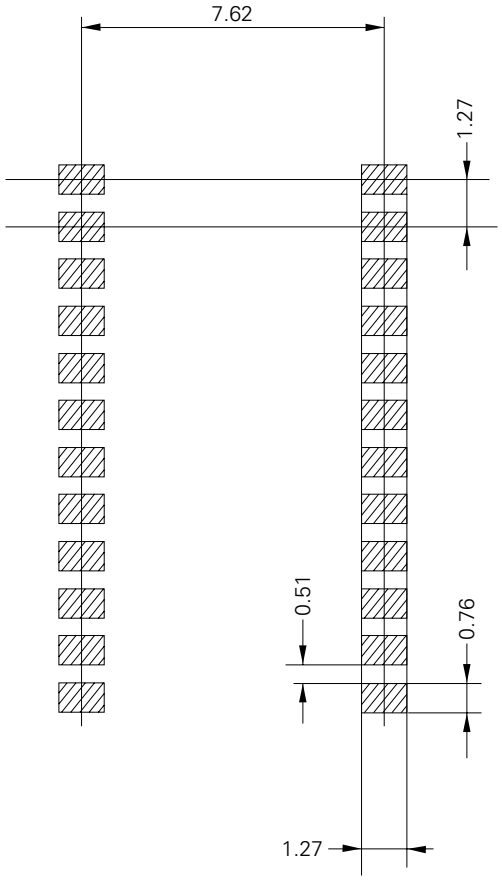
DRAWINGS OF ES PRODUCT PACKAGES (1/2)

ES 24 PIN SHRINK DIP (REFERENCE) (UNIT: mm)

DRAWINGS OF ES PRODUCT PACKAGES (2/2)

ES 24 PIN CERAMIC SOP (REFERENCE) (UNIT: mm)

10. RECOMMENDED PC BOARD PATTERN FOR SOP (REFERENCE) (UNIT: mm)



- The pattern shown above conforms to the Integrated Circuit Dimensions Rule (IC-74-2) stipulated by the Electric Industry Association of Japan (EIAJ).
- The dimensions of this pattern are applicable to all the products called flat DIP (mini-flat) "form A 300 mil type".
- If there is a possibility that solder bridges could be formed, shorten the pitch (0.76 mm) between pads, without changing the length for each pad (1.27 mm).

11. RECOMMENDED SOLDERING CONDITIONS ★

For the μPD7566A, soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document "Semiconductor device mounting technology manual" (IEI-1207).

For other soldering methods, please consult with NEC sales personnel.

Table 11-1 Soldering Conditions of Surface Mount Type

μPD7566AG-XXX: 24-pin plastic SOP (300 mil)
μPD7566AG(A)-XXX: 24-pin plastic SOP (300 mil)

Soldering Method	Soldering Conditions	Recommended Conditions Reference Code
Infrared Reflow	Package peak temperature 230°C, Time: 30 secondes max. (210°C min.), Number of soldering operations: 1,	IR30-00-1
VPS	Package peak temperature 215°C, Time: 40 seconds max. (200°C min.), Number of soldering operations: 1	VP15-00-1
Wave Soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Preparatory heating temperature: 120°C max. (Package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., Time: 3 seconds max. (Per side)	–

Caution Do not use one soldering method in combination with another (however, pin partial heating can be performed with other soldering methods).

Table 11-2 Soldering Conditions of Through-Hole Type

μPD7566ACS-XXX: 24-pin plastic shrink DIP (300 mil)
μPD7566ACS(A)-XXX: 24-pin plastic shrink DIP (300 mil)

Soldering Method	Soldering Conditions
Wave Soldering (Only for pin part)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Pin Partial Heating	Pin temperature: 300°C max., Time: 3 seconds max. (Per pin)

Caution The wave soldering must be performed at the pin part only. Note that the solder must not be directly contacted to the package body.

★ APPENDIX A. COMPARISON FOR μPD7566A SUB-SERIES PRODUCTS

Item \ Product		μPD7556	μPD75P56	μPD7556A	μPD7556A(A)	μPD7566	μPD75P66	μPD7566A	μPD7566A(A)
Instruction Cycle/System Clock (5 V)	RC	4 μs/500 kHz				–			
	External	2.86 μs/700 kHz				–			
	Ceramic	–				2.86 μs/700 kHz			
Instruction Set		45 (SET B)							
ROM		1024 × 8							
RAM		64 × 4							
I/O Ports	Total	20	14 or 15	20		19	14	19	
	Port 0	P00, P01	P00	P00, P01		P00, P01	P00	P00, P01	
	Port 1	P10-P13	–	P10-P13		P10-P13	–	P10-P13	
	Port 8	P80-P82, P83/CL2	P80-P82, P83(CL2)	P80-P82, P83/CL2		P80-P82			
	Breakdown Voltage Limit	12 V		9 V		12 V		9 V	
	Port 9, 10, 11	P90, P91, P100-P103, P110-P113							
	Breakdown Voltage Limit	12 V		9 V		12 V		9 V	
Timer/Event Counter		8 bits							
Comparator		4 channels							
Supply Voltage Range		2.5-6.0 V	4.5-6.0 V	2.0-6.0 V	2.7-6.0 V	2.7-6.0 V	4.5-6.0 V	2.7-6.0 V	2.7-6.0 V
Package		24-pin plastic shrink DIP 24-pin plastic SOP							

APPENDIX B. DEVELOPMENT SUPPORT TOOLS

The following development support tools are available for developing a system in which the μPD7566A is employed.

Language Processor

μPD7550, 7560 Series Absolute Assembler	This absolute assembler is a program which converts a program written in mnemonic to object code, so that it can be executed by microcomputer. In addition, this absolute assembler is provided with a function which automatically performs branch instruction optimization.			
	Host machine	OS	Media	Order code (Product name)
	PC-9800 series	MS-DOS™ Ver.3.10 to Ver.5.00A Note	3.5"2HD	μS5A13AS7554
			5.25" 2HD	μS5A10AS7554
	IBM PC/AT™	PC DOS™ (Ver.3.1)	5.25" 2HC	μS7B10AS7554

PROM Programming Tool

Hardware	PG-1500	PROM programmer that can easily program typical PROMs of 256K to 4M bits or single-chip microcomputers with built-in PROMs in the stand-alone mode or remotely from the host machine by connecting the accessory boards and separately sold program adapters.			
	PA-75P56CS	PROM programmer adapter to be connected to the PG-1500 for programming the μPD75P56 or the μPD75P66.			
Software	PG-1500 Controller	Allows controlling the PG-1500 connected to the host machine via the serial and parallel interface, from the host machine.			
		Host machine	OS	Media	Order code (Product name)
		PC-9800 series	MS-DOS Ver.3.10 to Ver.5.00A Note	3.5"2HD	μS5A13PG1500
				5.25" 2HD	μS5A10PG1500
		IBM PC/AT	PC DOS (Ver.3.1)	5.25" 2HC	μS7B10PG1500

Note Although Ver. 5.00/5.00A is provided with a task swap function, this function cannot be used with this software.

Remark The operations of the assembler and PG-1500 controller are guaranteed only on the above host machine and OS.

Debugging Tool

Hardware	EVAKIT-7500B	The EVAKIT-7500B is an evaluation board which can be used commonly with the μPD7500 series products. For system development with the μPD7566A, the and the EV-7554A option EVAKIT-7500B board are used together. Although the EVAKIT-7500B can operate in the stand-alone mode, the EVAKIT-7500B has 2 serial interface channels on its board to which a console, such as RS-232C, etc., can be connected for debugging. Additionally, the EVAKIT-7500B has real-time tracing function, so that the conditions of the program counter and the output ports can be traced on a real-time basis. The EVAKIT-7500B also has a PROM programmer for effective debugging.			
	EV-7554A	The EV-7554A is used together with the EVAKIT-7500B to evaluate the μPD7566A.			
	SE-7554A	The SE-7554A is a simulation board for evaluating a system by mounting the program, developed by the EVAKIT-7500B, in place of the μPD7566A.			
Software	EVAKIT-7500 Control Program (EVAKIT controller)	The EVAKIT-7500 control program controls the EVAKIT-7500B from the host machine by connecting the EVAKIT-7500B to the host machine via the RS-232C.			
		Host machine	OS	Media	Order code (Product name)
		PC-9800 series	MS-DOS Ver.3.10 to Ver.5.00A[Note]	3.5"2HD	μS5A13EV7500-P01
				5.25" 2HD	μS5A10EV7500-P01
		IBM PC series	PC DOS (Ver.3.1)	5.25" 2D	μS7B11EV7500-P01

Note Although Ver. 5.00/5.00A is provided with a task swap function, this function cannot be used with this software.

★ **Caution It is not possible to internally mount a pull-up resistor in a port in the EVAKIT-7500B. When evaluating, arrange to have a pull-up resistor mounted in the user system.**

Remark Operations of the EVAKIT controller are guaranteed on the above listed host machines with the listed operating system.

APPENDIX C. RELATED DOCUMENTS ★

DOCUMENT RELATED TO DEVICE

Document Name	Document No.
User's Manual	IEU-1111D
μPD7500-series Selection Guide	IF-1027G

DOCUMENT RELATED TO DEVELOPMENT TOOL

Document Name			Document No.
Hardware	EVAKIT-7500B User's Manual		EEU-1017C
	EV-7554A User's Manual		EEU-1034A
	PG-1500 User's Manual		EEU-1335B
Software	μPD7550, 7560-series Abusolute Assembler User's Manual		EEM-1006
	EVAKIT-7500 Control Program User's Manual	MS-DOS base	EEM-1356
		PC DOS base	EEM-1049
	PG-1500 Controller User's Manual		EEU-1291B

OTHER RELATED DOCUMENT

Document Name	Document No.
Package Manual	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-1209A
NEC Semiconductor Device Reliability/Quality Control System	IEI-1203A
Static Electricity Discharge (ESD) Guarantee Guide	IEI-1201
Semiconductor Device Quality Guarantee Guide	MEI-1202
Microcomputer-Related Product Guide -Third Party Product	**Note**

Remark These documents above are subject to change without notice. Be sure to use the latest document for designing.

Note To be published.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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