



SURFACE-MOUNT NPN POWER TRANSISTORS

D70F2T1

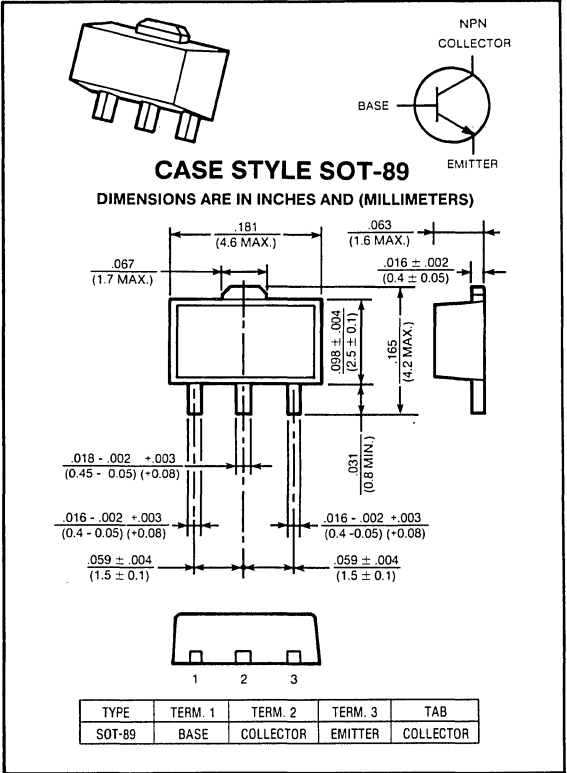
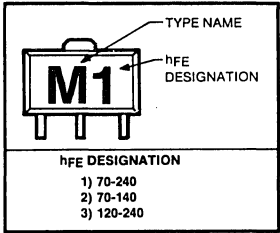
**50 VOLTS
2 AMP, 500 mWATTS**

Designed for power amplifier applications, power switching applications.

Features:

- Low saturation voltage
: $V_{CE(sat)} = 0.5V$ (Max.) ($I_C = 1A$)
- High speed switching time: $t_{stg} = 1.0\mu s$ (Typ.)
- $P_D = 1 \sim 2W$ (Mounted on ceramic substrate)
- Small flat package
- Complementary to D71F2T1
- See page 840 for mounting and handling considerations.

MARKING SYSTEM



maximum ratings ($T_A = 25^\circ C$) (unless otherwise specified)

RATING	SYMBOL	D70F2T1	UNITS
Collector-Emitter Voltage	V_{CEO}	50	Volts
Collector-Base Voltage	V_{CBO}	50	Volts
Emitter Base Voltage	V_{EBO}	5	Volts
Collector Current — Continuous	I_C	2	A
Base Current — Continuous	I_B	0.4	A
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$ @ $T_C = 25^\circ C^{(1)}$	P_D	500 1000	mWatts
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

thermal characteristics⁽²⁾

- (1) Mounted on ceramic substrate ($250mm^2 \times 0.8t$).
(2) See page 841 for thermal considerations.

electrical characteristics ($T_A = 25^\circ\text{C}$) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
----------------	--------	-----	-----	-----	------

off characteristics

Collector-Emitter Breakdown Voltage ($I_C = 10\text{mA}$, $I_E = 0$)	$V_{(BR)CEO}$	50	—	—	Volts
Collector Cutoff Current ($V_{CB} = 50\text{V}$, $I_E = 0$)	I_{CBO}	—	—	0.1	μA
Emitter Cutoff Current ($V_{EB} = 5\text{V}$, $I_C = 0$)	I_{EBO}	—	—	0.1	μA

on characteristics

DC Current Gain ⁽³⁾ ($I_C = 0.5\text{A}$, $V_{CE} = 2\text{V}$) ($I_C = 2.0\text{A}$, $V_{CE} = 2\text{V}$)	h_{FE}	70 20	— —	240 —	—
Collector-Emitter Saturation Voltage ($I_C = 1\text{A}$, $I_B = 0.05\text{A}$)	$V_{CE(sat)}$	—	—	0.5	V
Base-Emitter Saturation Voltage ($I_C = 1\text{A}$, $I_B = 0.05\text{A}$)	$V_{BE(sat)}$	—	—	1.2	Volts

switching characteristics

Turn-on Time	$V_{CC} = 30\text{V}$ $I_{B1} = -I_{B2} = 0.05\text{A}$ Duty Cycle $\leq 1\%$	t_{on}	—	0.1	—	μs
Storage Time		t_{stg}	—	1.0	—	
Fall Time		t_f	—	0.1	—	

(3) See page 44, for h_{FE} ranges.

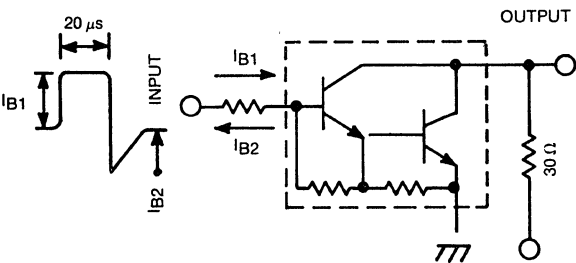


FIG. 1 SWITCHING TIME TEST CIRCUIT

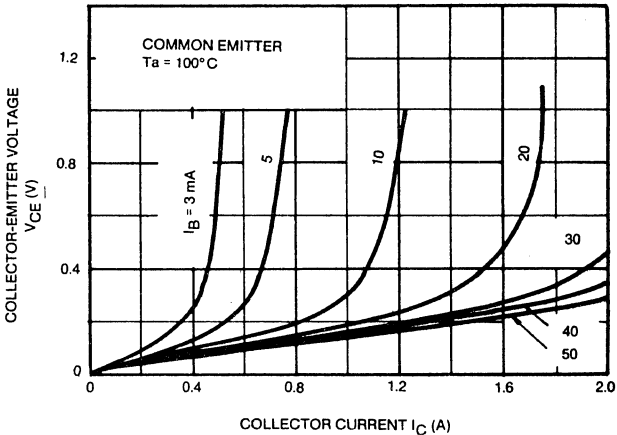


FIG. 2 $V_{CE} - I_C$

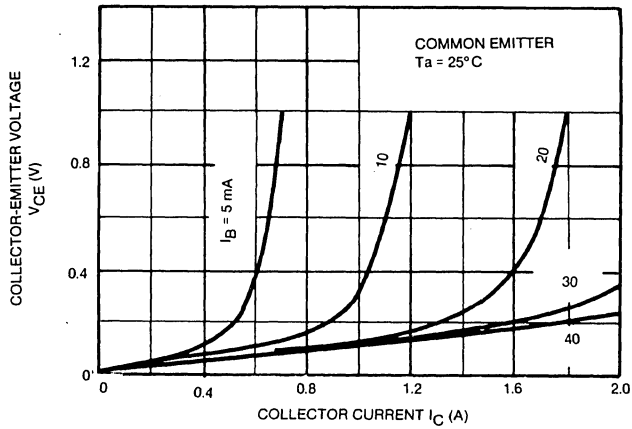


FIG. 3 $V_{CE} - I_C$

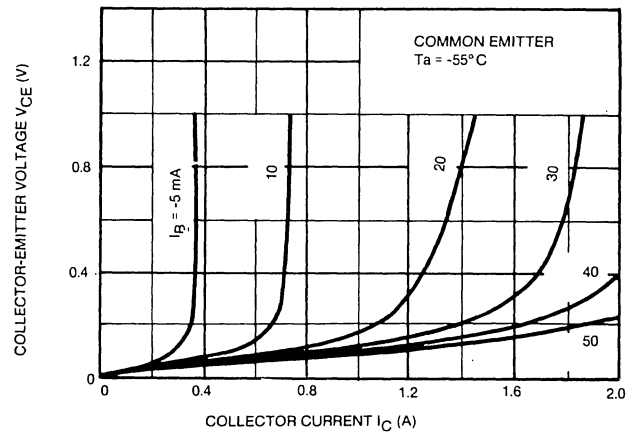


FIG. 4 $V_{CE} - I_C$

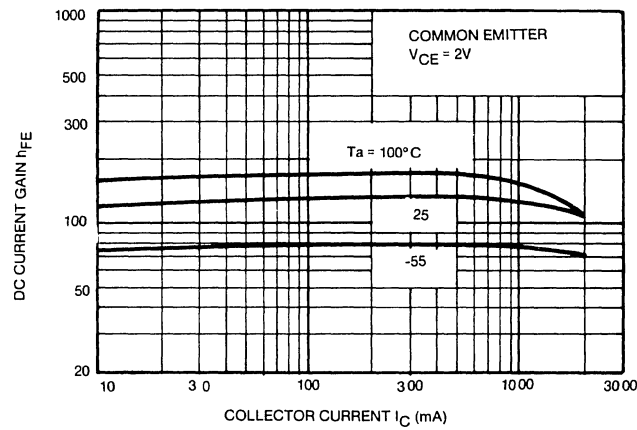


FIG. 5 $h_{FE} - I_C$

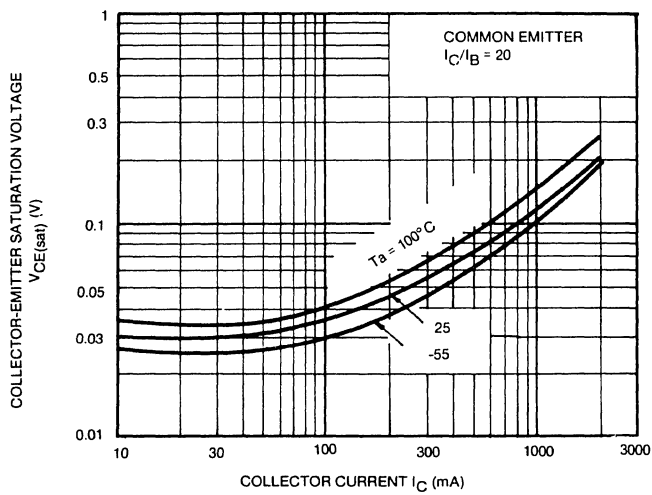


FIG. 6 $V_{CE(sat)} - I_C$

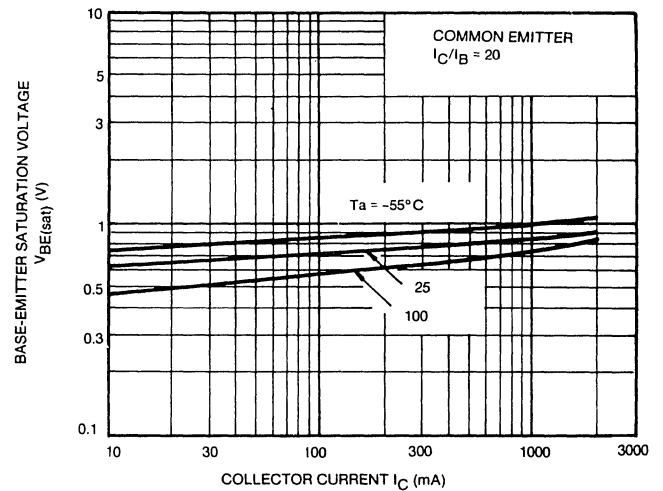


FIG. 7 $V_{BE(sat)} - I_C$

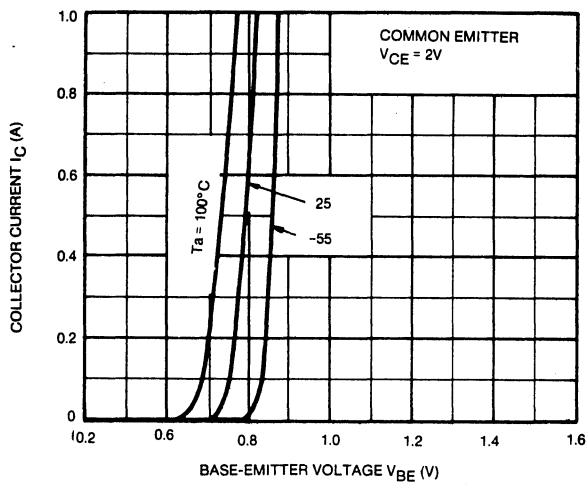


FIG. 8 $I_C - V_{BE}$

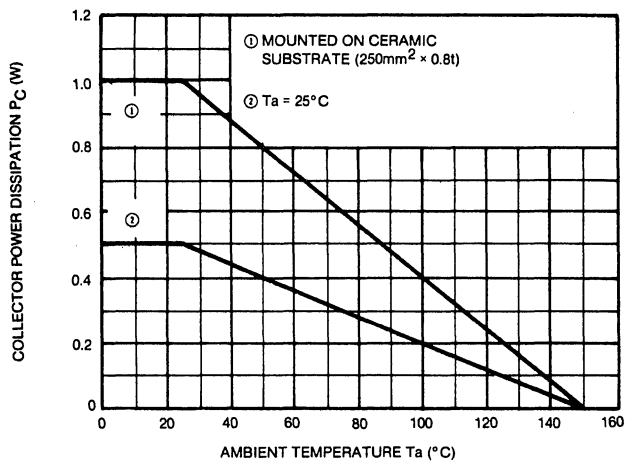


FIG. 10 $P_C - T_a$

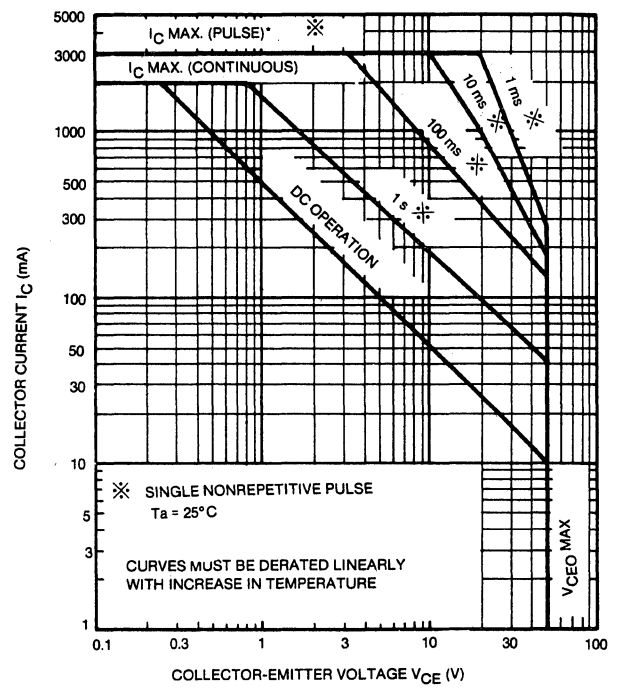


FIG. 9 SAFE OPERATING AREA