μPD4361
65,536 x 1-Bit
Static CMOS RAM

Description

The μPD4361 is a 65,536-word by 1-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD4361 a high-speed device that requires very low power and no clock or refreshing.

The device is packaged in a 22-pin plastic DIP and 22-pin ceramic leadless chip carrier and has two types of access times, address and chip select. In addition, the μPD4361C-L features low-power data retention.

Features

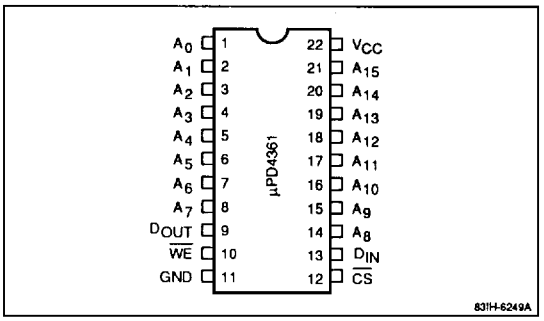
- 65, 536 x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Data retention current of 50 μA max available from -L versions only
- Standard 22-pin plastic DIP and ceramic LCC
- Standard JEDEC pin configurations

Ordering Information

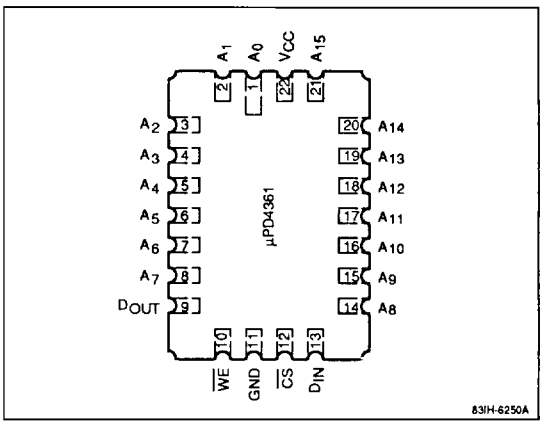
Part Number	Access Time (max)	Package
μPD4361C-45	45 ns	22-pin plastic DIP
C-55	55 ns	
C-70	70 ns	
μPD4361C-45L	45 ns	
C-55L	55 ns	
C-70L	70 ns	
μPD4361K-40	40 ns	22-pin ceramic LCC
K-45	45 ns	
K-55	55 ns	

Pin Configurations

22-Pin Plastic DIP



22-Pin Ceramic LCC



Pin Identification

Symbol	Function
A_0 - A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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New speeds to 12 ns will be available in 1991.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR} (Note 2)	0 to +70°C
Storage temperature, T_{STG} (Note 3)	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 20 ns maximum pulse.

(2) T_{OPR} for 4361K = −10 to +85°C.

(3) T_{STG} for 4361K = −65 to +150°C.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High-Z	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 20 ns maximum pulse.

Capacitance

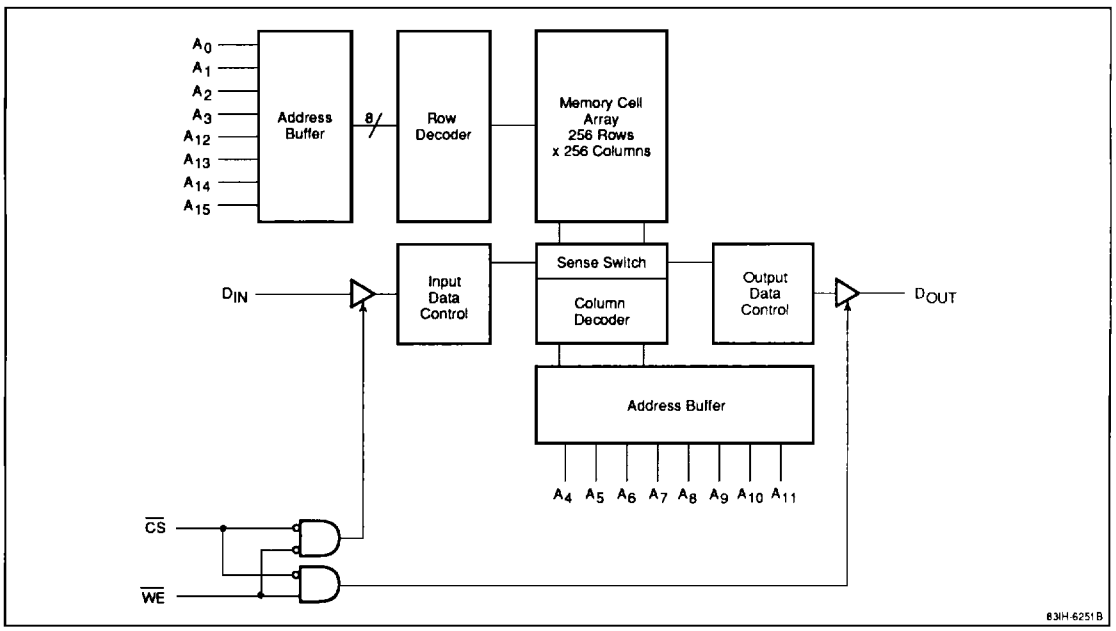
T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			5	pF
Output capacitance	C_{DOUT}			7	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Operating supply current	I_{CC}			120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD4361-40		μPD4361-45		μPD4361-55		μPD4361-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation											
Read cycle time	t_{RC}	40		45		55		70		ns	(Note 2)
Address access time	t_{AA}		40		45		55		70	ns	
Chip select access time	t_{ACS}		40		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		5		ns	
Chip select to output in low-Z	t_{LZ}	5		5		5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{HZ}	0	22	0	25	0	30	0	30	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	27	0	30	0	40	0	40	ns	
Write Operation											
Write cycle time	t_{WC}	40		45		55		70		ns	(Note 2)
Chip select to end of write	t_{CW}	37		40		50		60		ns	
Address valid to end of write	t_{AW}	37		40		50		60		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	23		25		30		40		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	23		25		25		30		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	22	0	25	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

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Low V_{CC} Data Retention Characteristics (for -L Version Only)

T_A = 0 to 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or 0 V $\leq V_{IN} \leq 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or 0 V $\leq V_{IN} \leq 0.2$ V
Chip deselect to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Data Retention Timing

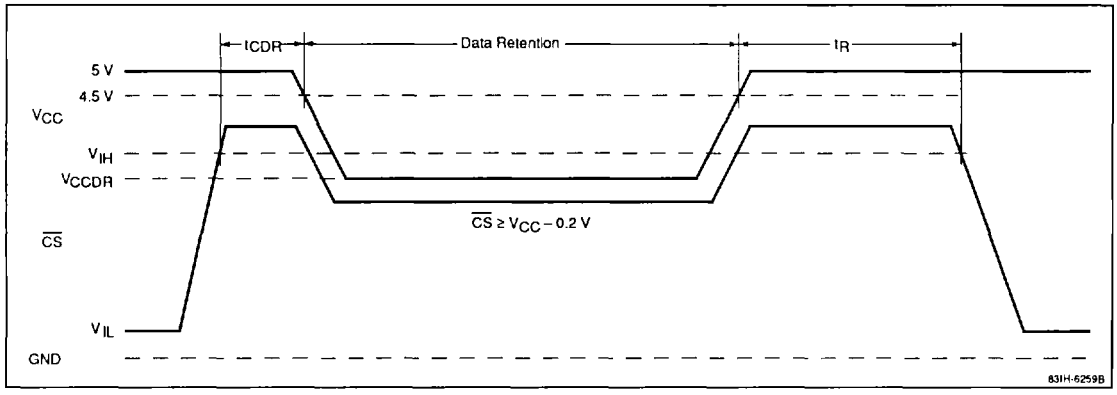


Figure 1. Output Load

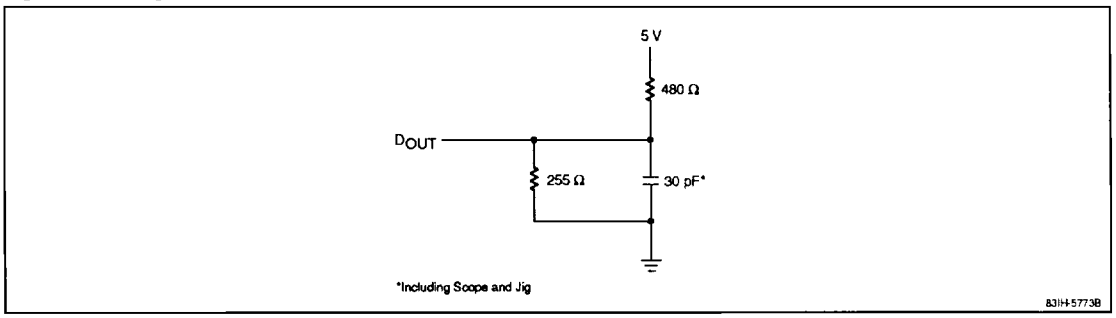
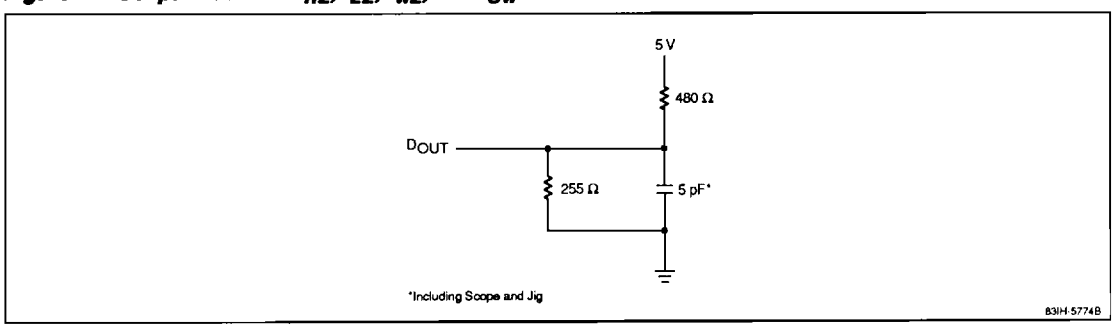


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



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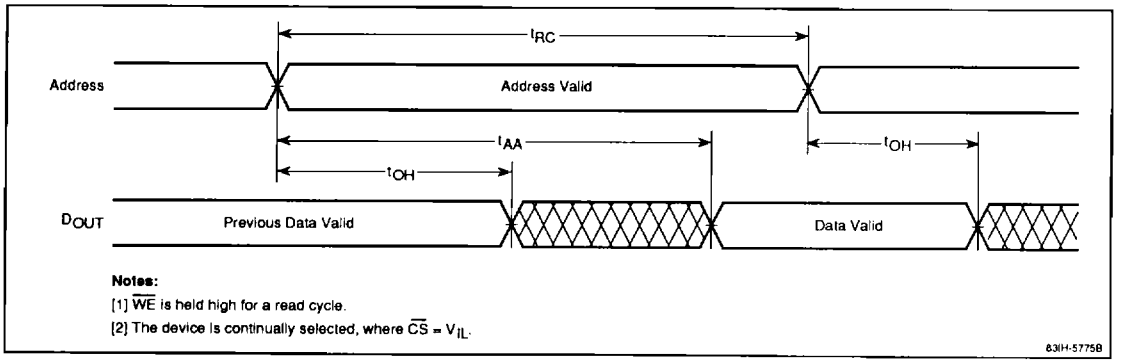
Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS}$ = V_{IL}.

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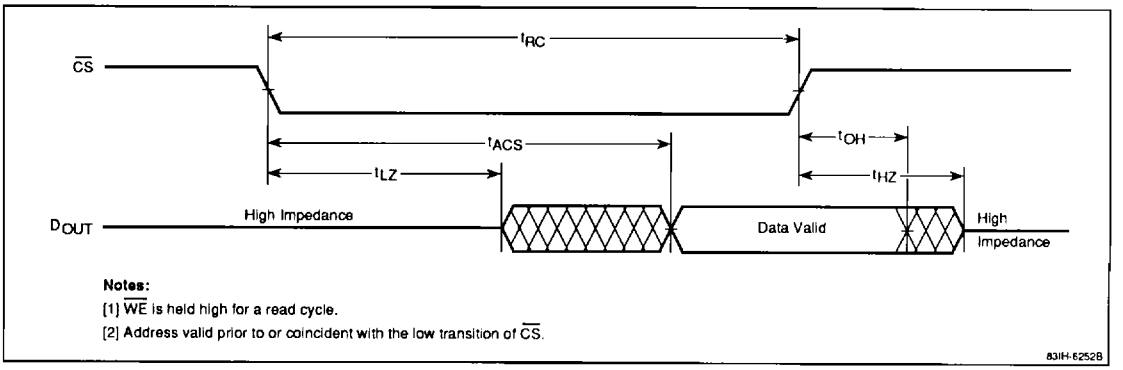
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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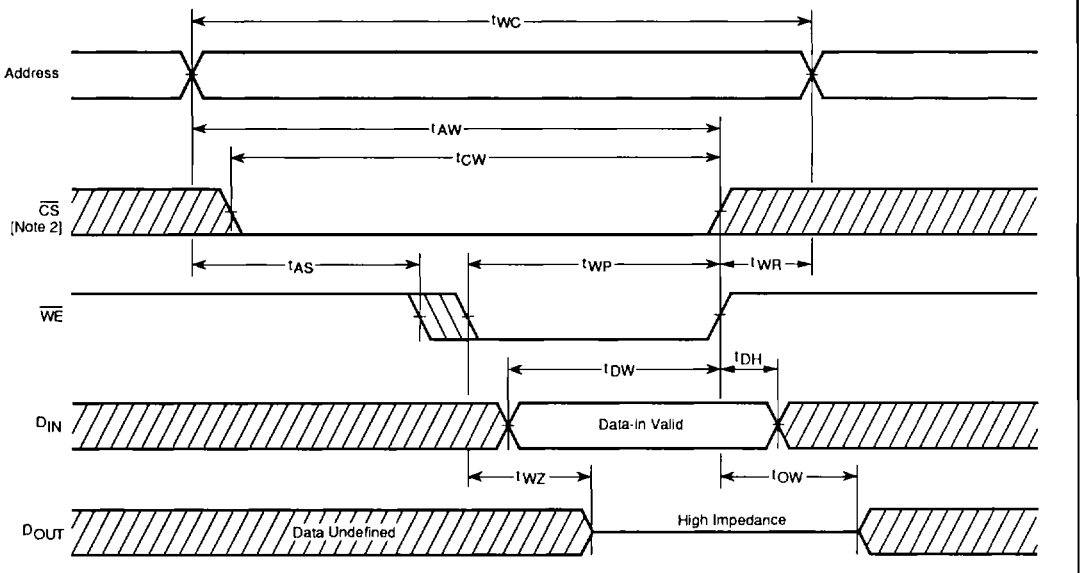
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{CS}$ and $\overline{WE}$ go high simultaneously, the outputs remain in high impedance.

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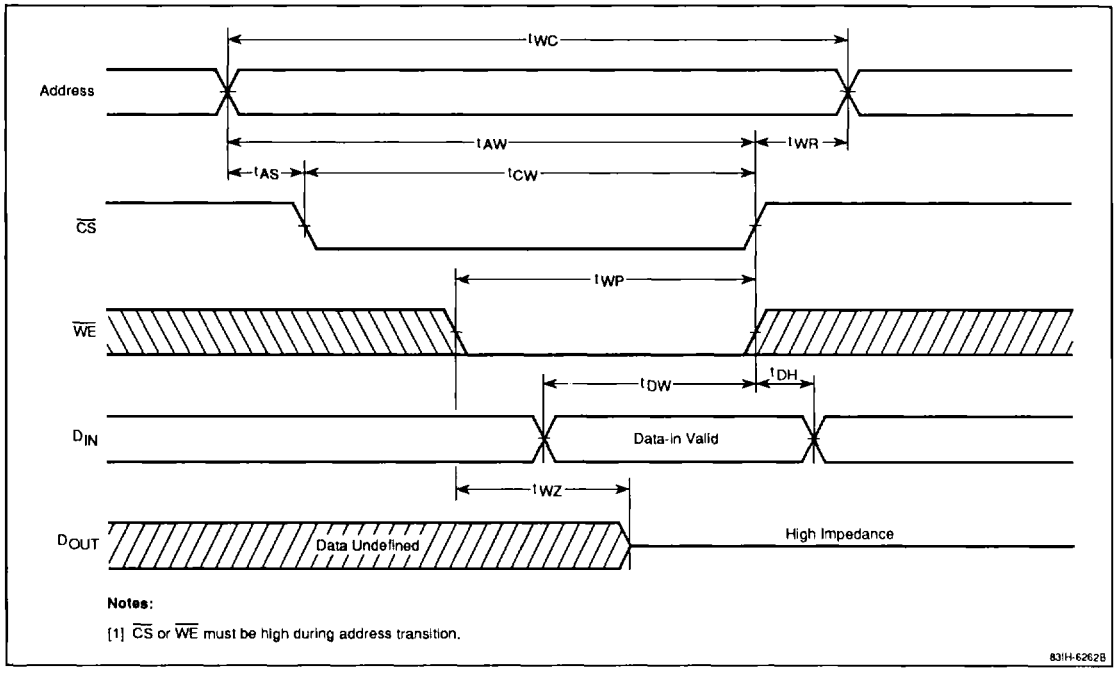
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

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