



DESCRIPTION

It is built in dual auto-reverse preamplifier, dual OCL power amplifier, and a ripple filter.

Power amplifier stage

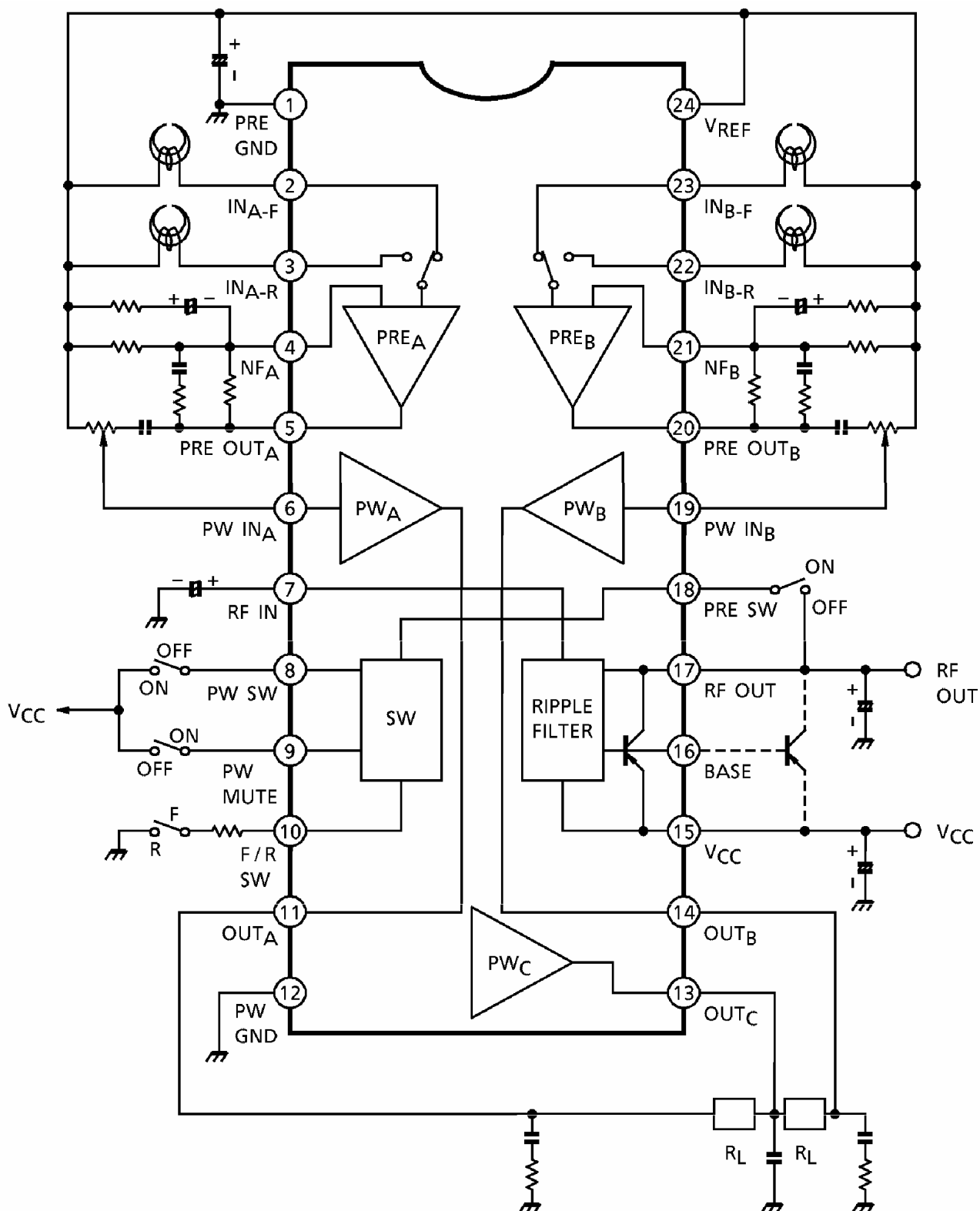
- ### Preamplifier stage

- Auto-reverse with F/R control switch.
- Input coupling condenser-less
- Low noise : $V_{ni}=1.3\mu V_{rms}$ (Typ.)
- Built-in a preamplifier mute.
- Built-in input capacitor for reducing buzz noise.

- Built-in a ripple filter.
- Built-in a power switch.
- Low quiescent current : $I_{CCQ}=11.5\text{mA(Typ.)}$ ($V_{CC}=3\text{V}$, $T_a=25^\circ\text{C}$)
- Operating supply voltage range: $V_{CC}(\text{opr})=1.8\sim 4.5\text{V}(T_a=25^\circ\text{C})$

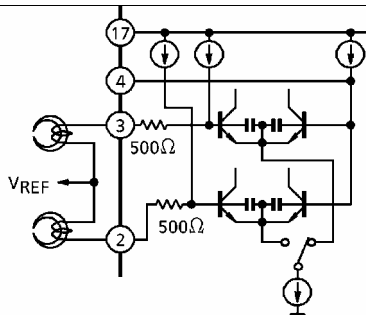
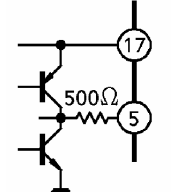
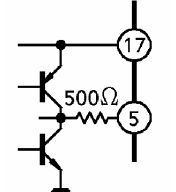
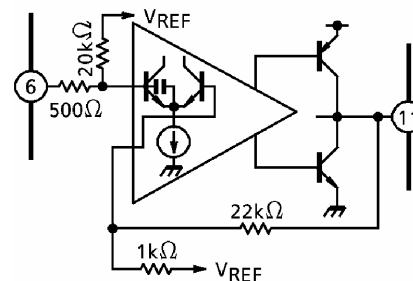
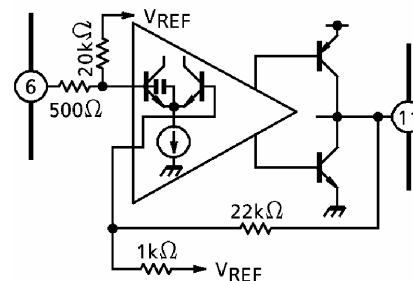
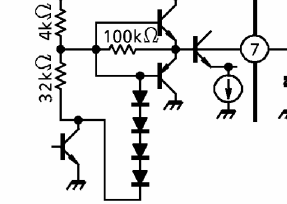
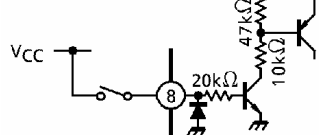
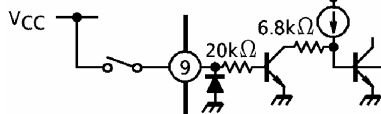
The drawing shows the mechanical specifications for the CHMC SXXX D2002 component. The top view shows a rectangular component with dimensions 13.0 ± 0.2 mm in width and 7.6 ± 0.3 mm in height. It features 24 pins on the top edge and 12 pins on the bottom edge. The pin pitch is 1.0 mm. The side view shows a height of 7.62 mm (300 mil) and a width of 13.5 mm. A detail view shows the pin profile with dimensions: 0.15 ± 0.02 mm for the pin height, 0.1 ± 0.02 mm for the pin width, and 0.50 ± 0.05 mm for the base width.

BLOCK DIAGRAM



TERMINAL EXPLANATION

Terminal voltage: typical terminal voltage at no signal with test circuit ($V_{CC}=3V$, $T_a=25^{\circ}C$)

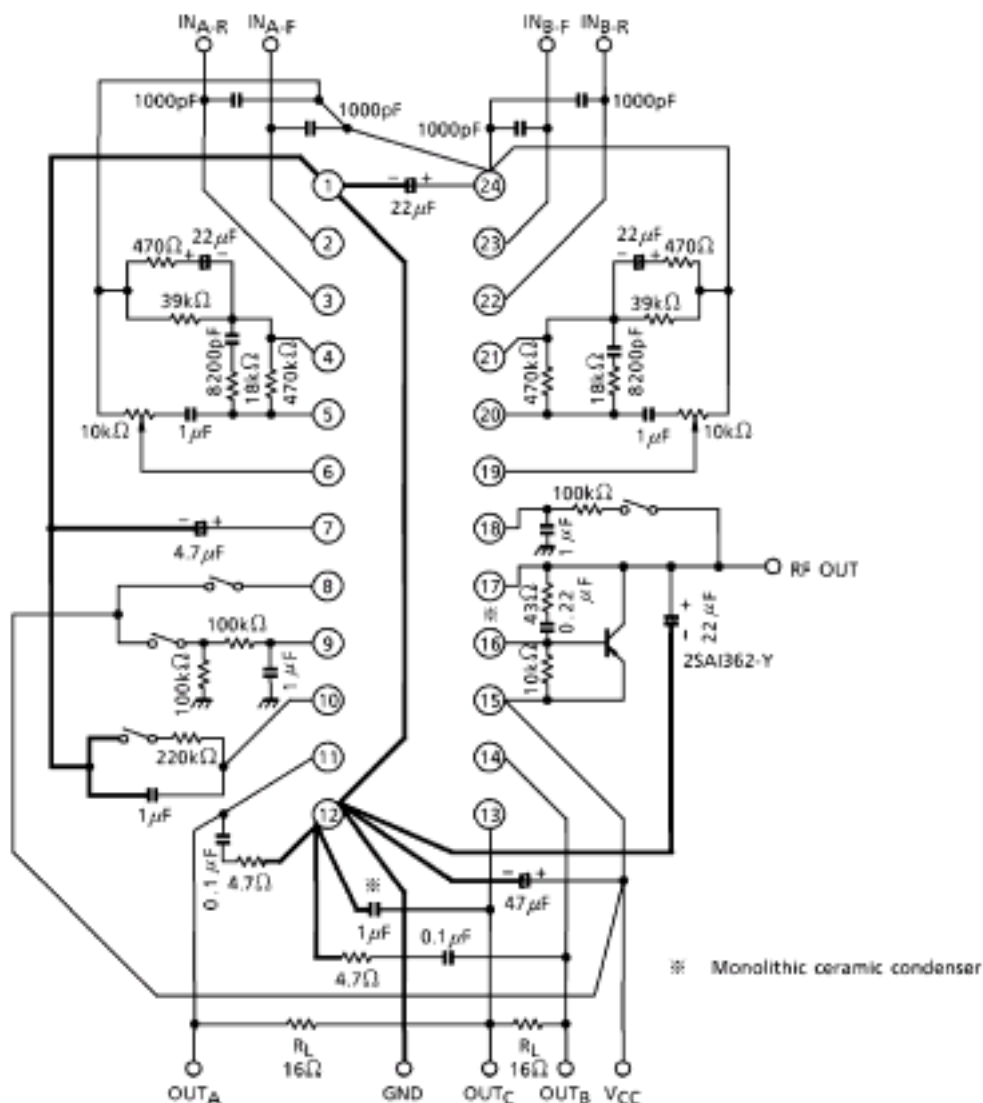
Terminal		Function	Internal circuit	Terminal Voltage (V)
NO.	Name			
1	Pre GND	The GND, except the power drive stage.	-	0
2	INA-F	Input of preamplifier. F/R SW (OPEN:  /  PIN “L” :  /  PIN)		1.3
3	INA-R			
22	INB-R			
23	INB-F			
4	NFA	NF of preamplifier		1.3
21	NFB			
5	PRE OUTA	Output of preamplifier		1.3
20	PRE OUTB			
6	PW INA	Input of power amplifier		1.3
19	PW INB			
11	OUTA	Output of power amplifier		1.3
14	OUTB			
7	RF IN	Ripple filter terminal		2.6
8	PW SW	Power on/off switch. (V_{CC} : power on Open or GND: power off)		-
9	PW MUTE	Muting switch for power amplifier. (V_{CC} : power amp. On Open or GND: power amp. Off)		-

TERMINAL EXPLANATION

Terminal voltage: typical terminal voltage at no signal with test circuit ($V_{CC}=3V$, $T_a=25^{\circ}C$)

Terminal		Function	Internal circuit	Terminal Voltage (V)
NO.	Name			
10	F/R SW	Forward/Reverse mode switch. (OPEN : Forward mode "L" level : Reverse mode This terminal can't be connected with GND line directly. In case of reverse mode, a resistor ($R=180k\Omega\sim270k\Omega$) should be connected to GND		-
12	PW GND	GND for power drive stage	-	0
13	OUTc	Output terminal of center power amplifier.		1.3
15	Vcc	-	-	3
16	BASE	Base of an external PNP transistor for ripple filter.		2.3
17	RF OUT	Ripple filter output. Ripple filter circuit supplies internal circuit except power amplifier circuit with power source.		2.6
18	PRE SW	Muting switch for preamplifier. (V17(RF OUT) : Preamp. Off OPEN : Preamp. On) This terminal can't be connected with GND line directly. In case that terminal is connected with GND line, a resistor ($R \geq 10k\Omega$) should be connected to GND.		-
24	VREF	Reference voltage. Preamplifier and power amplifier operate on this reference.		1.3

AN EXAMPLE OF PATTERN LAYOUT



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V _{cc}	6	V
Output Current	Power	I _{o(peak)}	60	mA
	Ripple Filter	I _{RF}	30	
Power Dissipation		P _{D(note)}	400	mW
Operating Temperature		T _{opr}	-25~75	°C
Storage Temperature		T _{stg}	-55~150	°C

(Note) Derated above Ta=25°C in the proportion of 3.2mW/°C.

ELECTRICAL CHARACTERISTICS

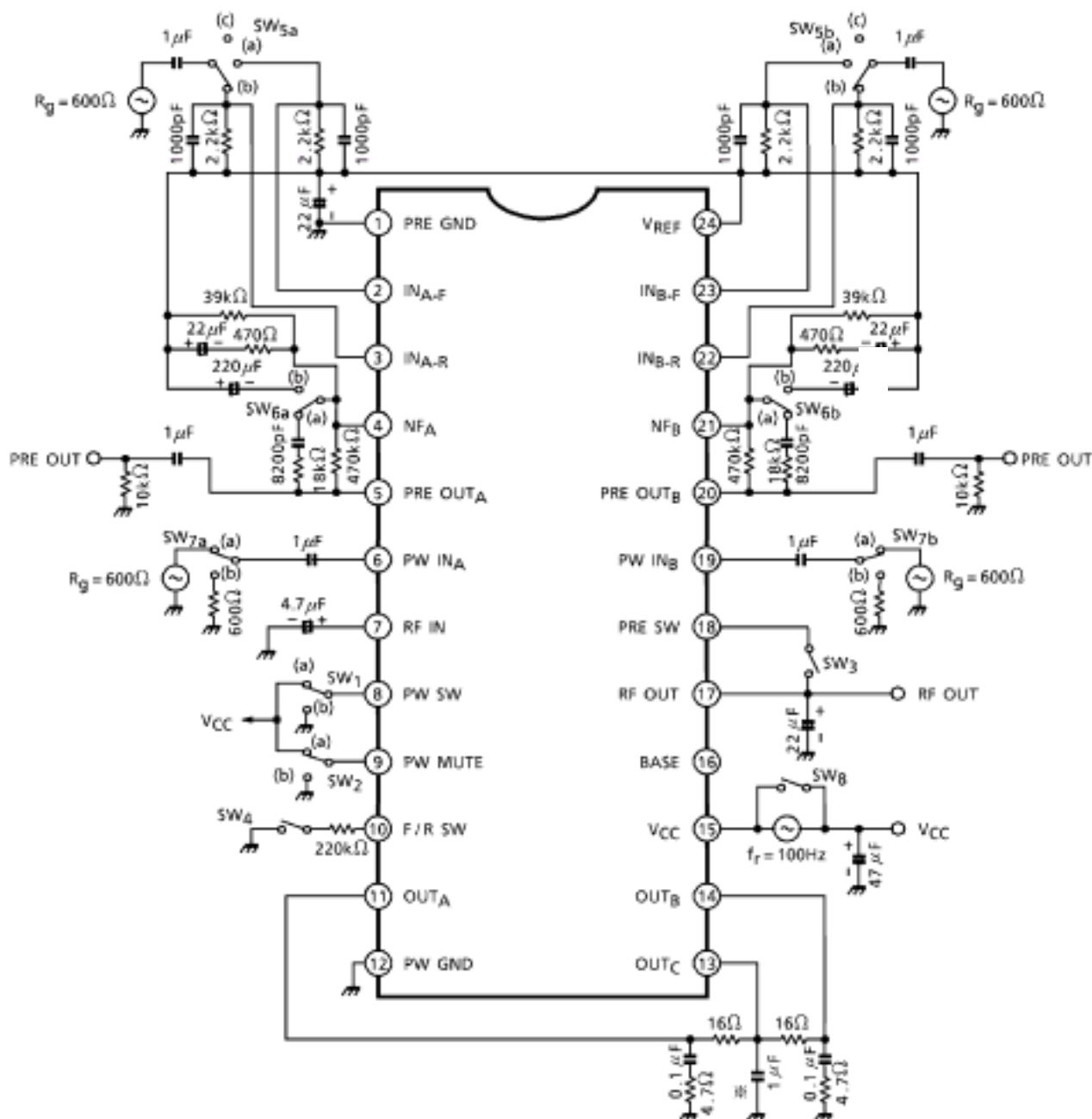
(Unless otherwise specified: Ta=25°C, Vcc=3V; f=1kHz, SW1: a, SW2: a, SW3: OPEN SW8: ON

Preamplifier stage: Rg=2.2kΩ, RL=10kΩ, SW2: OPEN SW4: ON/OPEN, SW5: a/b, SW6: a

Power amplifier stage: Rg=600Ω, RL=16Ω, SW3: ON SW7: a)

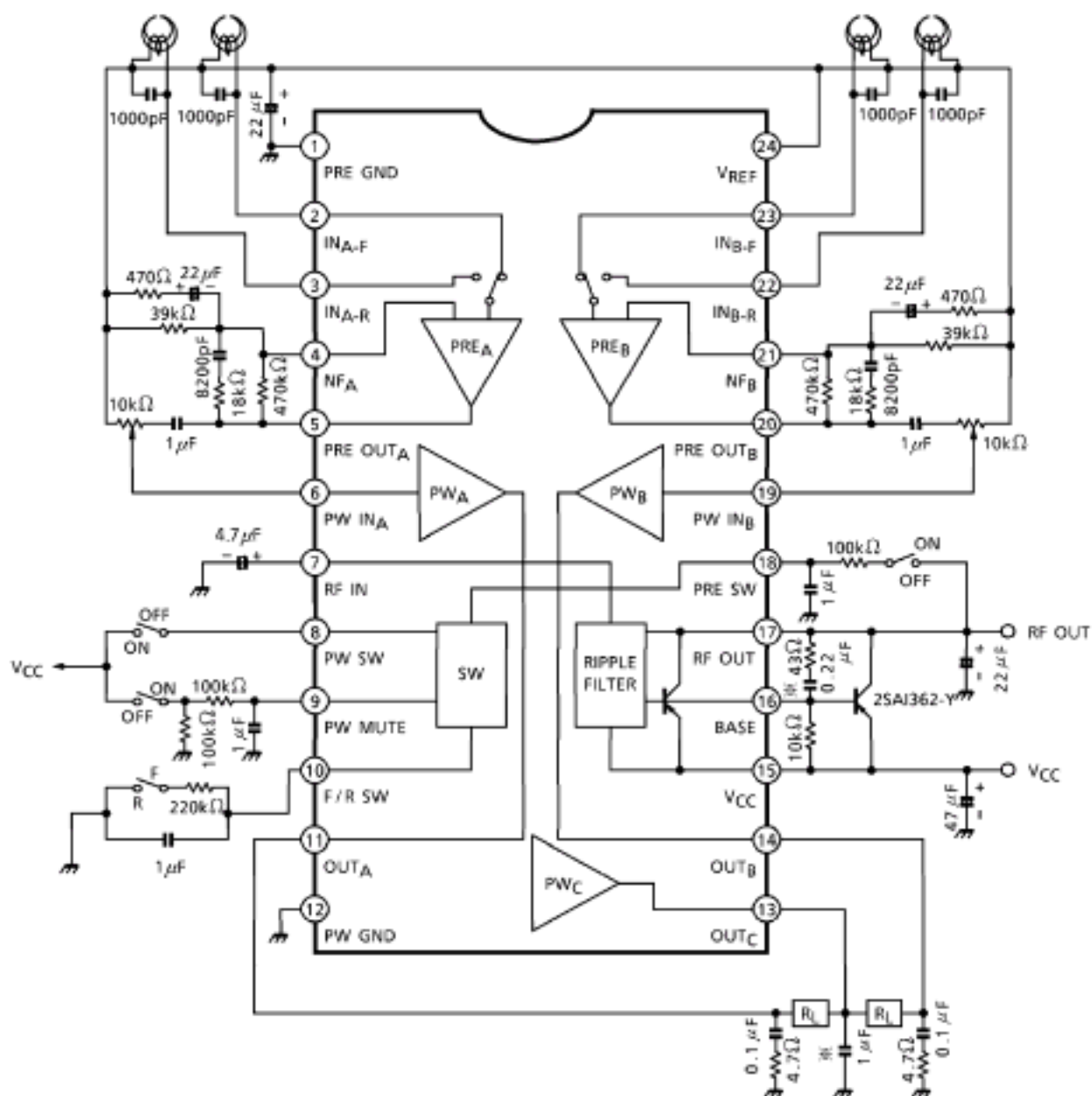
Characteristics		Symbol	Test conditions		Min	Typ	Max	Unit
Quiescent Current		ICCQ1	Power off, SW1 :b SW2: b SW3: ON				5	μA
		ICCQ2	Power amp. Off , Sw2: b			5	9	mA
		ICCQ3	Vin=0			11.5	16.5	
Power amplifier stage	Voltage Gain	Gv	Vo=-12dBV		25	27	29	dB
	Channel Balance	CB				0	1.5	
	Output Power	Po1	THD=10%	RL=16Ω	35	50		mW
		Po2		RL=32Ω		33		
	Total Harmonic Distortion	THD1	Po=1mW			0.2	0.8	%
	Output Noise Voltage	Vno	Rg=600Ω, SW7: b			22	40	μVrms
	Ripple Rejection Ratio	RR1	fr=100Hz, Vr=-22dBV SW8:OPEN		45	62		dB
	Cross Talk (CH-A/CH-B)	CT1	Vo=-12dBV		35	42		
	Power Muting Attenuation	ATT1	Vo=-12dBV, SW2: a→b			80		
Preamplifier stage	Open Loop Voltage Gain	Gvo	Vo=-12dBV, SW6: b		70	80		dB
	Closed Loop Voltage Gain	Gvc	Vo=-12dBV			35		
	Maximum Output Voltage	Vom	THD=1%		600	850		mVrms
	Total Harmonic Distortion	THD2	Vo=-12dBV			0.02	0.1	%
	Equivalent Input Noise Voltage	Vni	Rg=2.2kΩ, SW5 : c BPF=20Hz~20kHz NAB(Gv=35dB, f=1kHz)			1.3	2.8	μVrms
	Cross Talk (CH-A/CH-B)	CT2	Vo=-12dBV			70		dB
	Cross Talk (Forward/Reverse)	CT3				70		
	Pre Muting Attenuation	ATT2	Vo=-12dBV, SW3: OPEN→ON			80		
Ripple Filter Output Voltage		VRF	Vcc=2V, IRF=0mA		1.76	1.8		V
Ripple Rejection Ratio of Ripple Filter Output		RR2	Vcc=2V, IRF=10mA fr=100Hz, Vr=-22dBV SW8 :OPEN		45	53		dB
Power On/off Switch	Power On Current	I8	Vcc=1.8V, V24 ≥ 0.5V		5			μA
	Power Off Voltage	V8	Vcc=1.8V, V24 ≤ 0.3V		0		0.3	V
Power Amp. Mute Switch	Mute Off Current	I9	Vcc=1.8V, ATT1 ≤ 3dB		5			μA
	Mute On Voltage	V9	Vcc=1.8V, ATT1 ≥ 60dB		0		0.3	V

TEST CIRCUIT



Monolithic ceramic condenser

APPLICATION CIRCUIT



Monolithic ceramic condenser

CHARACTERISTICS CURVES

Unless otherwise specified: $V_{CC}=3V$, $f=1kHz$, $T_a=25^{\circ}C$ Power amplifier stage : $R_g=600\Omega$, $R_L=16\Omega$, preamplifier stage : $R_g=2.2k\Omega$, $R_L=10k\Omega$

