NEC

MOS INTEGRATED CIRCUIT

μPD16857

MONOLITHIC 6 channel H-BRIDGE DRIVER

DESCRIPTION

μPD16857 is monolithic 6 channel H-bridge driver employing power MOS FETs in the output stages. The MOS FETs in the output stage lower the saturation voltage and power consumption as compared with conventional drivers using bipolar transistors.

In addition, a low-voltage malfunction prevention circuit is also provided that prevents the IC from malfunctioning when the supply voltage drops. A 30-pin plastic shrink SOP package is adopted to help create compact and slim application sets.

In the output stage H bridge circuits, two low-ON resistance H-bridge circuits for driving actuators, and another three channels for driving sled motors and tilt control, and another channel for driving loading motor are provided, making the product ideal for applications in DVD-ROM/DVD-RAM.

FEATURES

- Six H-bridge outputs employing power MOS FETs.
- High speed PWM drive corresponding: Operating input frequency 120 kHz (MAX.)
- Low voltage malfunction prevention circuit: Operating control block voltage under 2.5 V (TYP.)
- Loading into 38-pin shrink SOP (300 mil).

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Control block supply voltage	V_{DD}		–0.5 to +6.0	V
Output block supply voltage	V_M		–0.5 to +13.5	V
Input voltage	V_{IN}		–0.5 to V_{DD}+0.5	V
Output current	$I_{D(pulse)}$	PW ≤ 5 ms, Duty ≤ 20 %	±1.0	A/ch
Power consumption[Note]	P_T		1.0	W
Peak junction temperature	$T_{CH(MAX)}$		150	°C
Storage temperature range	T_{stg}		–55 to +150	°C

Note When mounted on a glass epoxy board (10 cm × 10 cm × 1 mm, 15 % copper foil)

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Document No. S13908EJ1V0DS00 (1st edition)
Date Published July 1999 N CP(K)
Printed in Japan

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Control block supply voltage	V_{DD} **Note**		3.0	3.3	3.6	V
Output block supply voltage	V_M		10.8	12	13.2	V
Output current (pulse)	$I_{D(pulse)}$	PW < 5 ms, Duty < 10 %	–0.6		0.6	A
Operating frequency	f_{IN}				120	kHz
Operating temperature range	T_A		0		75	°C
Peak junction temperature	$T_{CH(MAX)}$				125	°C

Note The low-voltage malfunction prevention circuit (UVLO) operates when V_{DD} is 2.1 V TYP.

CHARACTERISTICS

T_A = 25 °C and the other parameters are within their recommended operating ranges as described above unless otherwise specified.

The parameters other than changes in delay time are when the current is ON.

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_M pin current (OFF state)	I_M	V_M = 13.2 V			50	μA
V_{DD} pin current	I_{DD}	V_{DD} = 3.6 V			200	μA
High level input current	I_{IH}	V_{IN} = V_{DD}			0.15	mA
Low level input current	I_{IL}	V_{IN} = 0, IN and SEL pins	–2.0			μA
High level input voltage	V_{IH}	V_{DD} = 3.3 V, V_M = 12 V	0.7V_{DD}		V_{DD}	V
Low level input voltage	V_{IL}	IN and SEL pins	–0.3		0.3V_{DD}	V
H-bridge ON resistance (ch1, 3, 5, 6)	R_{ONa}	V_{DD} = 3.3 V, V_M = 12 V upper + lower		2.5	3.5	Ω
H-bridge ON resistance (ch2, 4)	R_{ONb}			1.5	2.0	Ω
H-bridge switching current without load (ch1, 3, 5, 6) **Note**	$I_{sa(AVE)}$	V_{DD} = 3.3 V, V_M = 12 V 100 kHz switching			3.0	mA
H-bridge switching current without load (ch2, 4) **Note**	$I_{sb(AVE)}$				4.5	mA

Note Average value of the current consumed internally by an H-bridge circuit when the circuit is switched without load.

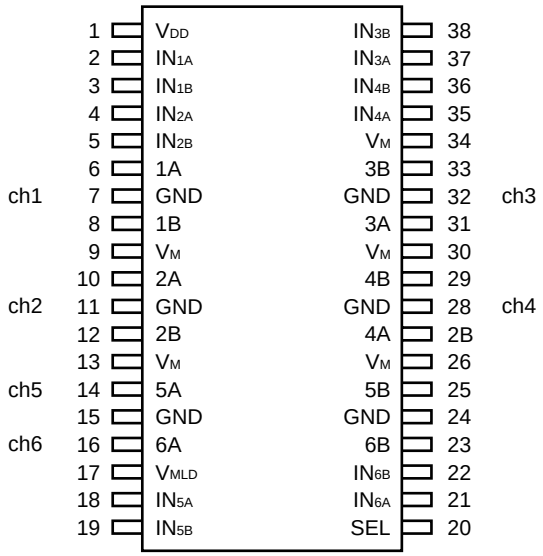
CHARACTERISTICS

T_A = 25 °C and the other parameters are within their recommended operating ranges as described above unless otherwise specified.

The parameters other than changes in delay time are when the current is ON.

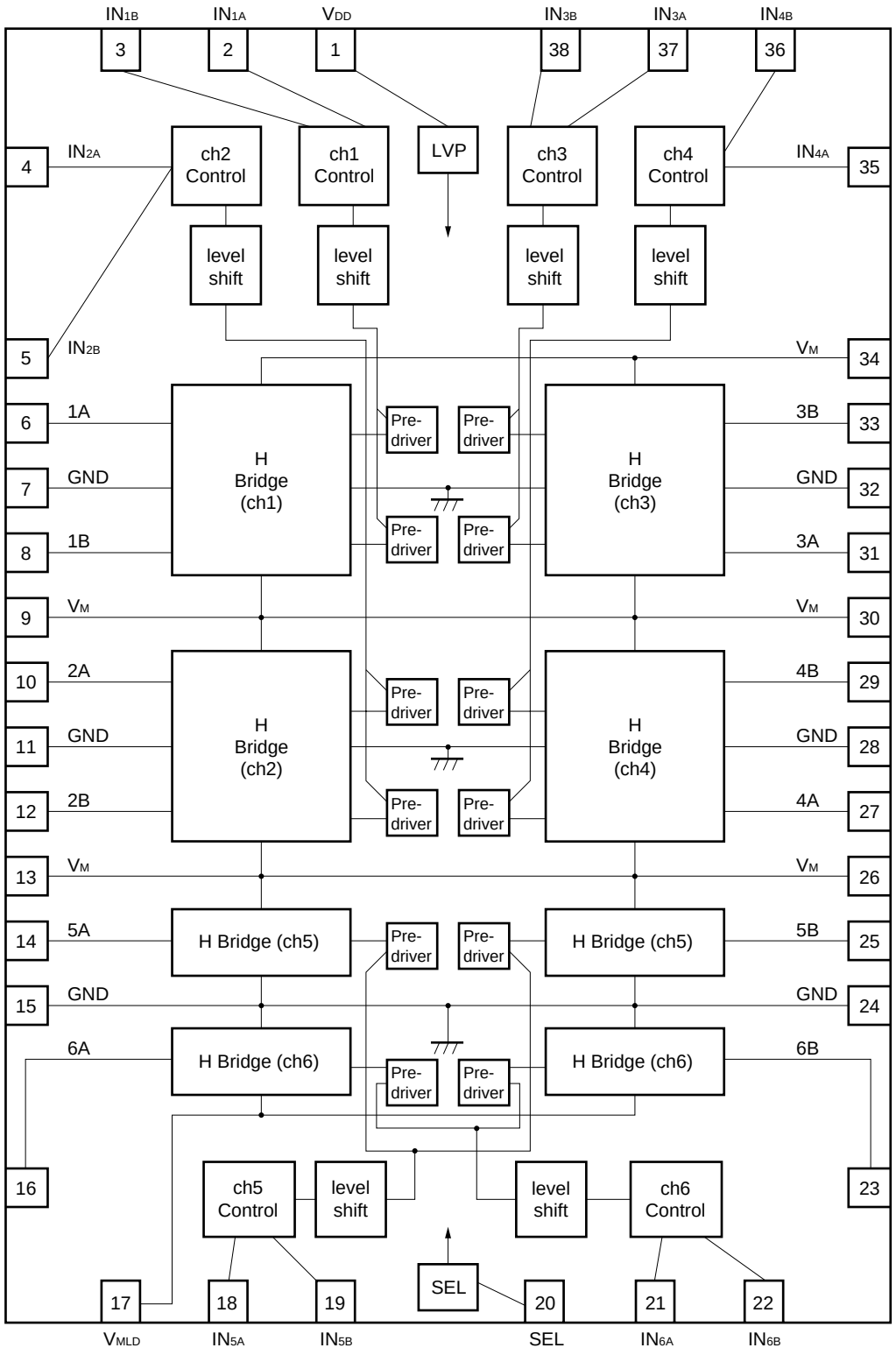
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
(ch1, 3, 5 1A, 1B, 3A, 3B, 5A, 5B output)						
Rise time	t_{TLHa}				200	ns
Rising delay time	t_{PLHa}	V_{DD} = 3.3 V			350	ns
Change in rising delay time	Δt_{PLHa}	V_M = 12 V			110	ns
Fall time	t_{THLa}	R_L(load) = 20 Ω			200	ns
Falling delay time	t_{PHLa}	100 kHz switching			350	ns
Change in falling delay time	Δt_{PHLa}				130	ns
(ch1, 3, 5 1A-1B, 3A-3B, 5A-5B)						
Rising delay time differential	$t_{PLHa(A-B)}$	V_{DD} = 3.3 V, V_M = 12 V			50	ns
Falling delay time differential	$t_{PHLa(A-B)}$	R_L = 20 Ω, 100 kHz SW			50	ns
(ch2, 4 2A, 2B, 4A, 4B output)						
Rise time	t_{TLHb}				200	ns
Rising delay time	t_{PLHb}	V_{DD} = 3.3 V			350	ns
Change in rising delay time	Δt_{PLHb}	V_M = 12 V			110	ns
Fall time	t_{THLb}	R_L(load) = 10 Ω			200	ns
Falling delay time	t_{PHLb}	100 kHz switching			350	ns
Change in falling delay time	Δt_{PHLb}				130	ns
(ch2, 4 2A-2B, 4A-4B)						
Rising delay time differential	$t_{PLHb(A-B)}$	V_{DD} = 3.3 V, V_M = 12 V			50	ns
Falling delay time differential	$t_{PHLb(A-B)}$	R_L = 10 Ω, 100 kHz SW			50	ns
(ch6 6A, 6A output)						
Rise time	t_{TLHC}	V_{DD} = 3.3 V		100		ns
Rising delay time	t_{PLHC}	V_M = 12 V			1.0	μs
Fall time	t_{THLC}	R_L(load) = 20 Ω		100		ns
Falling delay time	t_{PHLC}	100 kHz switching			1.0	μs

PIN CONNECTION



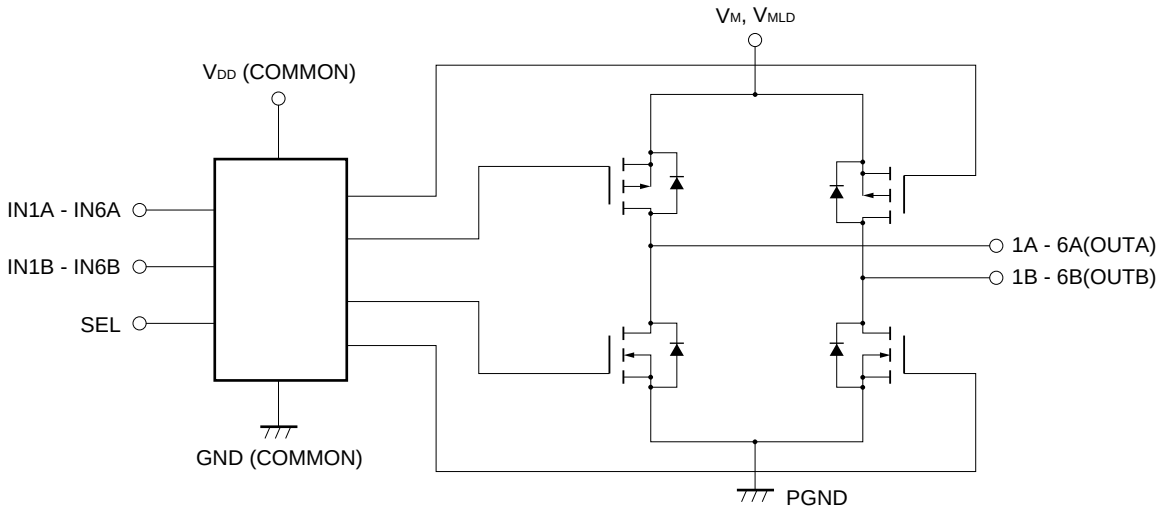
Pin No.	Pin name	Pin function	Pin No.	Pin name	Pin function
1	V_{DD}	Control block supply voltage pin (3.3 V input)	20	SEL	Output enable pin
2	IN_{1A}	ch1 input pin	21	IN_{6A}	ch6 input pin
3	IN_{1B}	ch1 input pin	22	IN_{6B}	ch6 input pin
4	IN_{2A}	ch2 input pin	23	6B	ch6 output pin
5	IN_{2B}	ch2 input pin	24	GND	Ground pin
6	1A	ch1 output pin	25	5B	ch5 output pin
7	GND	Ground pin	26	V_M	Output block supply voltage pin (12 V input)
8	1B	ch1 output pin	27	4A	ch4 output pin
9	V_M	Output block supply voltage pin (12 V input)	28	GND	Ground pin
10	2A	ch2 output pin	29	4B	ch4 output pin
11	GND	Ground pin	30	V_M	Output block supply voltage pin (12 V input)
12	2B	ch2 output pin	31	3A	ch3 output pin
13	V_M	Output block supply voltage pin (12 V input)	32	GND	Ground pin
14	5A	ch5 output pin	33	3B	ch3 output pin
15	GND	Ground pin	34	V_M	Output block supply voltage pin (12 V input)
16	6A	ch6 output pin	35	IN_{4A}	ch4 input pin
17	V_{MLD}	Output block supply voltage pin (12 V input)	36	IN_{4B}	ch4 input pin
18	IN_{5A}	ch5 input pin	37	IN_{3A}	ch3 input pin
19	IN_{5A}	ch5 input pin	38	IN_{3B}	ch3 input pin

BLOCK DIAGRAM



Remark Plural terminal (V_M, V_{MLD}, GND) is not only 1 terminal and connect all terminals.

FUNCTION TABLE

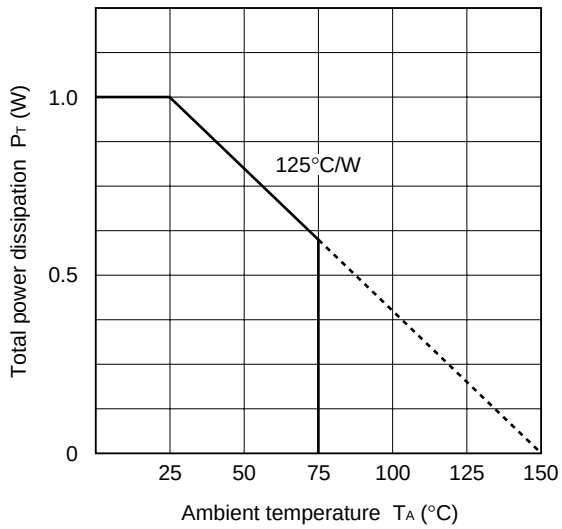


INPUT			OUTPUT	
IN1A - IN6A	IN1A - IN6A	SEL	1A - 6A	1B - 6B
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H
X	X	L	Z	Z

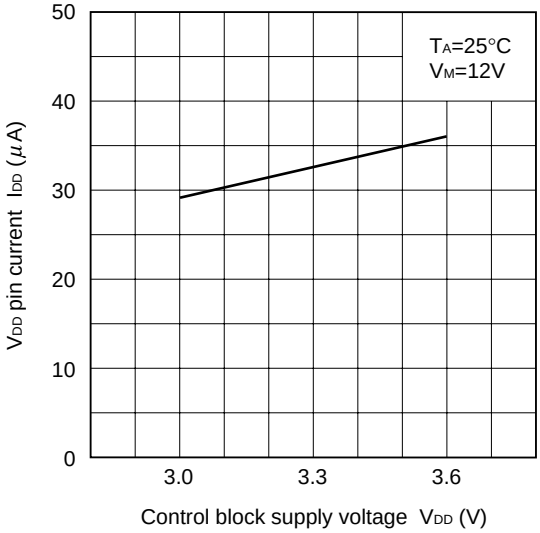
X: Don't care Z: High impedance

TYPICAL CHARACTERISTICS

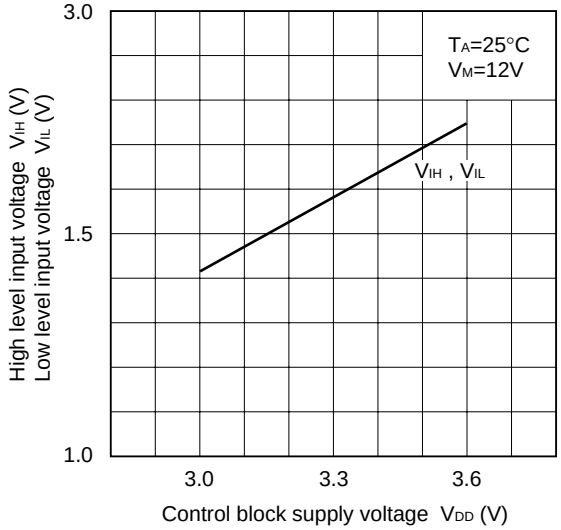
P_T vs. T_A characteristics



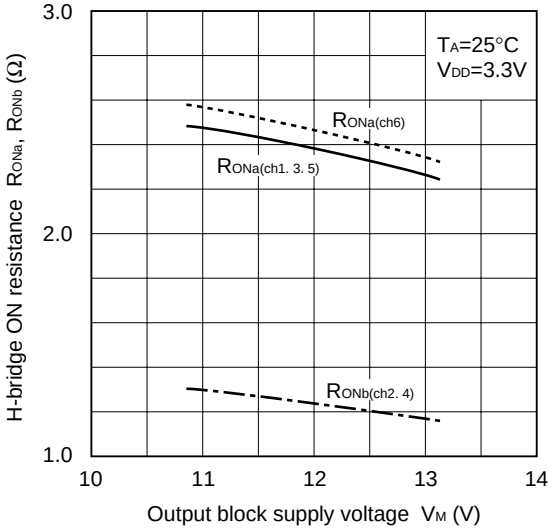
I_{DD} vs. V_{DD} characteristics



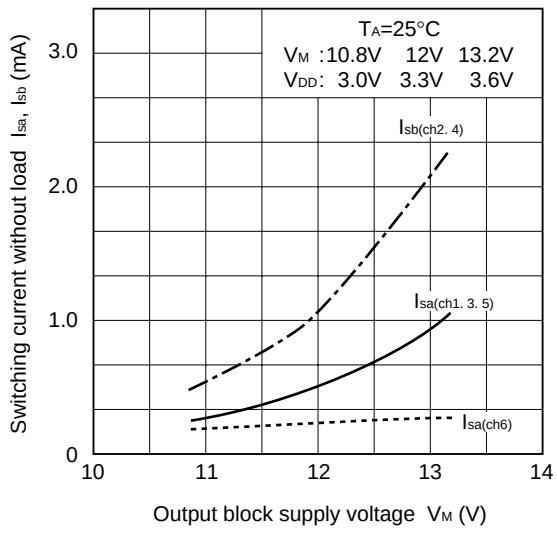
V_{IH} vs. V_{IL}-V_{DD} characteristics



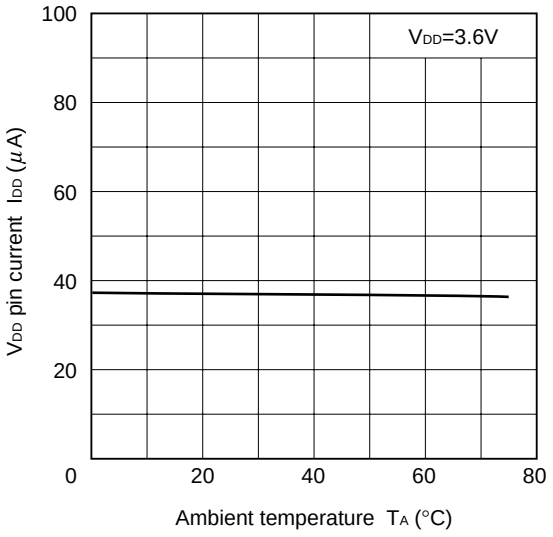
R_{ON} vs. V_M characteristics



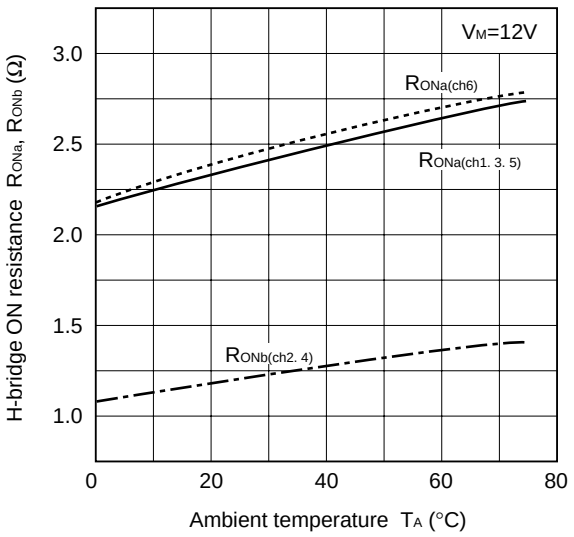
I_{sa}, I_{sb}. vs. V_{DD} characteristics



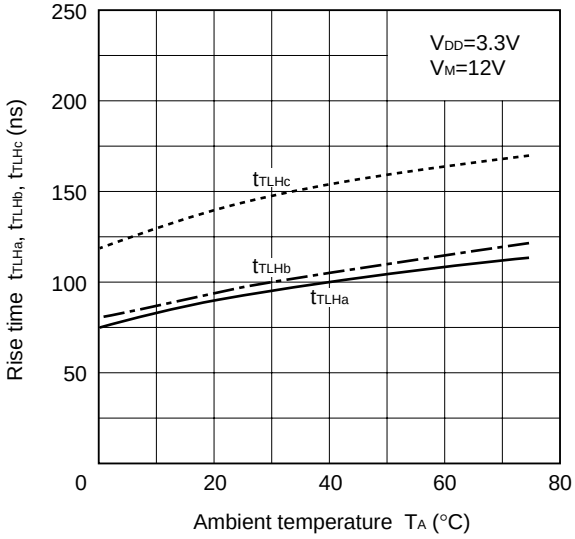
I_{DD} vs. T_A characteristics



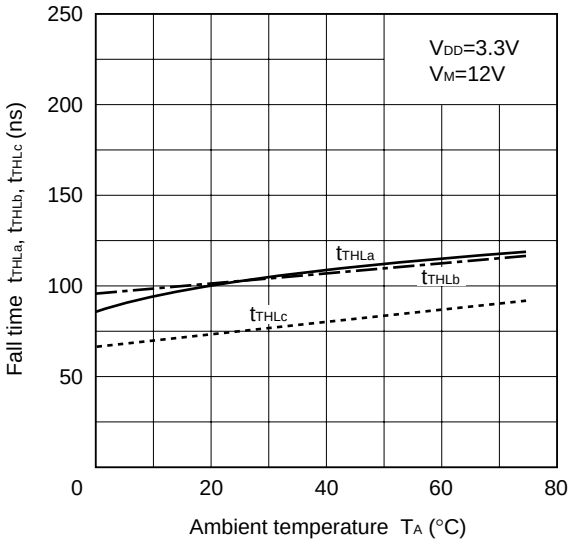
R_{ON} vs. T_A characteristics



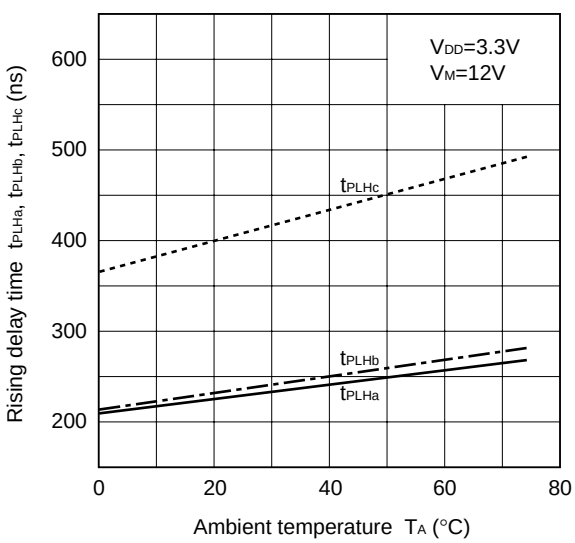
t_{TLHa}, t_{TLHb}, t_{TLHc}, vs. T_A characteristics



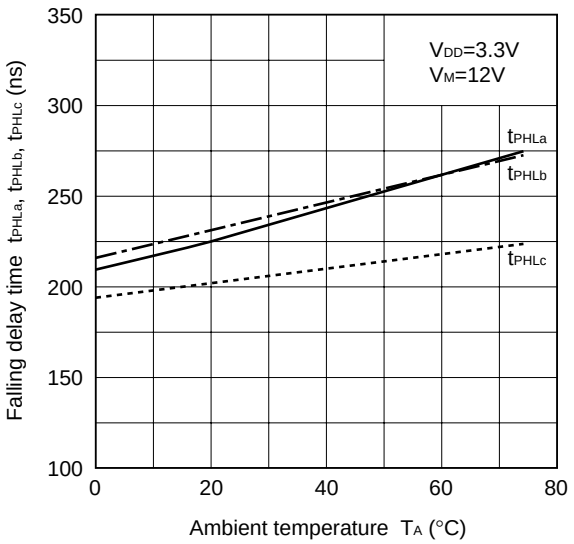
t_{THLa}, t_{THLb}, t_{THLc} vs. T_A characteristics



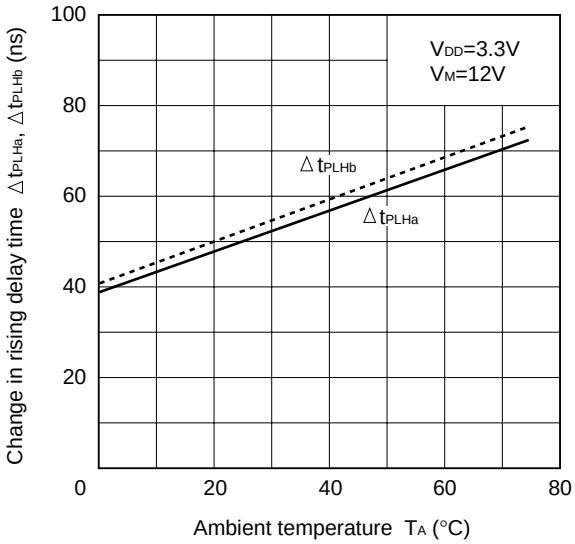
t_{PLHa}, t_{PLHb}, t_{PLHc}, vs. T_A characteristics



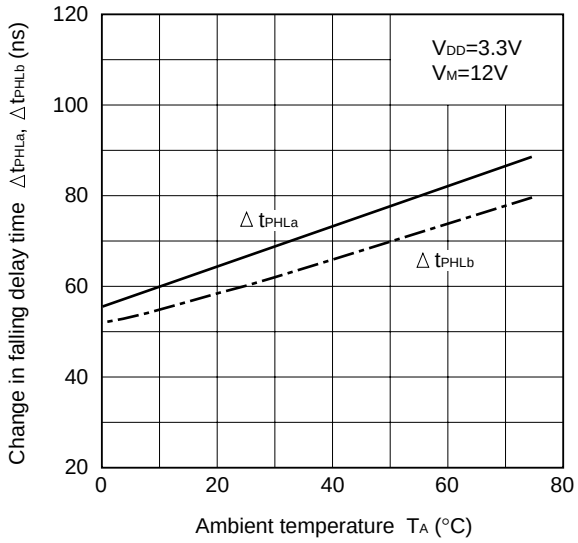
t_{PHLa}, t_{PHLb}, t_{PHLc} vs. T_A characteristics



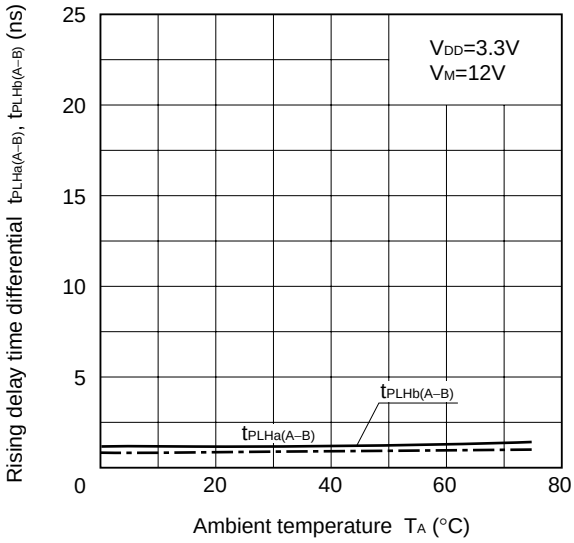
$\triangle t_{PLHa}$, $\triangle t_{PLHb}$, vs. T_A characteristics



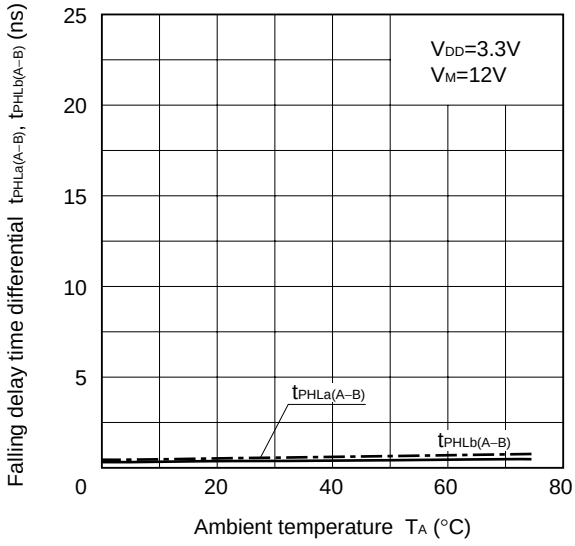
△tPHLa, △tPHLc, vs. TA characteristics



tPLHa(A–B), tPLHb(A–B), vs. TA characteristics



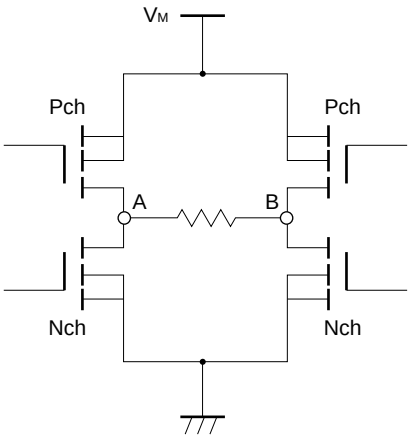
tPHLa(A–B), tPHLb(A–B), vs. TA characteristics



ABOUT SWITCHING OPERATION

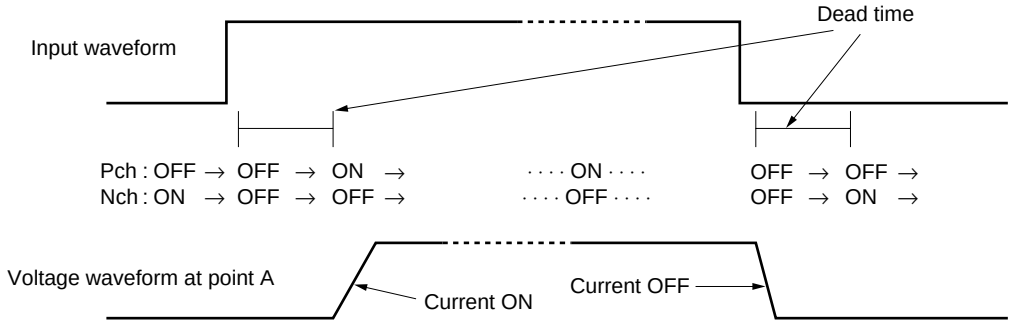
When output A is switched as shown in the figure on the right, a dead time (time during which both Pch and Nch are off) elapses to prevent through current. Therefore, the waveform of output A (rise time, fall time, and delay time) changes depending on whether output B is fixed to the high or low level.

The output voltage waveforms of A in response to an input waveform where output B is fixed to the low level (1) or high level (2) are shown below.



(1) Output B: Fixed to low level

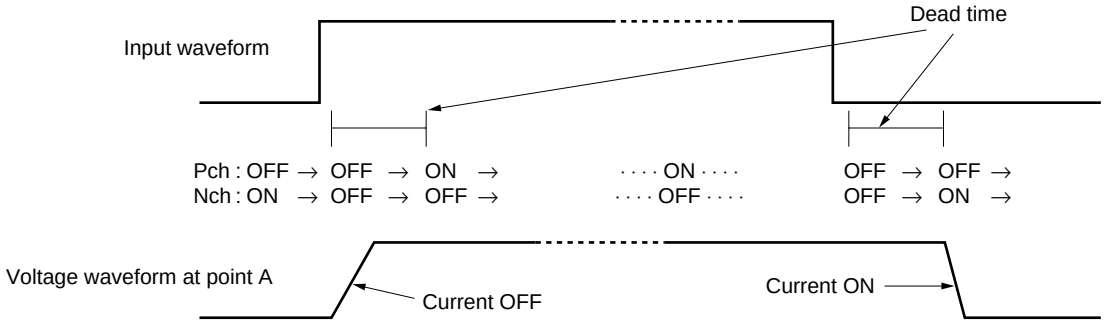
Output A: Switching operation (Operations of Pch switch and Nch switch are shown.)



Output A goes into high-impedance state and is in an undefined status during the dead time period. But, because output B is pulled down by the load, a low level is output to A.

(2) Output B: Fixed to high level

Output A: Switching operation (Operations of Pch switch and Nch switch are shown.)



Output A goes into high-impedance state and is in an undefined status during the dead time period. But, because output B is pulled up by the load, a high level is output to A.

The switching characteristics shown on the preceding pages are specified as follow (“output at one side” means output B for H-bridge output A, or output A for output B).

[Rise time]

Rise time when the output at one side is fixed to the low level (specified on current ON).

[Fall time]

Fall time when the output at one side is fixed to the high level (specified on current ON).

[Rising delay time]

Rising delay time when the output at one side is fixed to the low level (specified on current ON).

[Falling delay time]

Falling delay time when the output at one side is fixed to the high level (specified on current ON).

[Change in rising delay time]

Change (difference) in the rising delay time between when the output at one side is fixed to the low level and when the output at the other side is fixed to the high level.

[Change in falling delay time]

Change (difference) in the falling delay time between when the output at one side is fixed to the low level and when the output at the other side is fixed to the high level.

[Rising delay time differential]

Difference in rising delay time between output A and output B.

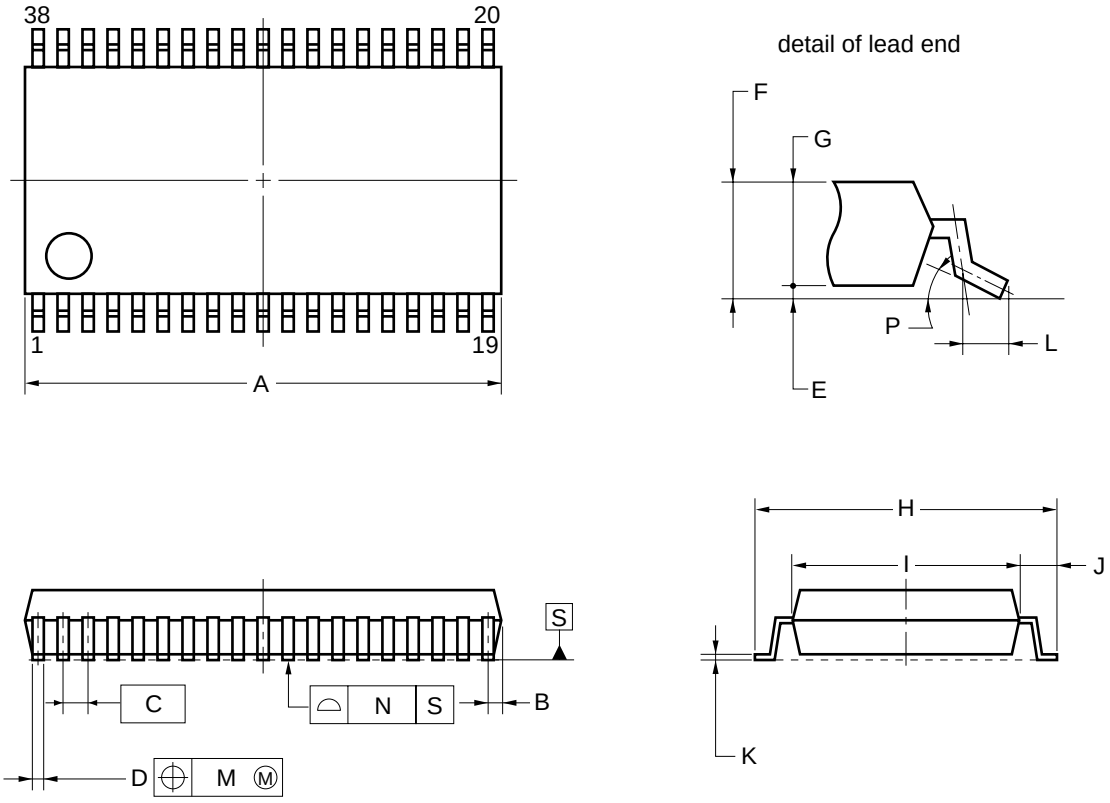
[Falling delay time differential]

Difference in falling delay time between output A and output B.

Caution Because this LSI switches a high current at high speeds, surge may occur due to the V_M and GND wiring and inductance and degrade the performance of the LSI.
On the PWB, keep the pattern width of the V_M and GND lines as wide and short as possible, and insert the bypass capacitors between V_M and GND at location as close to the LSI as possible.
Connect a low inductance magnetic capacitor (4700 pF or more) and an electrolytic capacitor of 10 μF or so, depending on the load current, in parallel.

PACKAGE DIMENSION

38-PIN PLASTIC SSOP (300 mil)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.7±0.3
B	0.65 MAX.
C	0.65 (T.P.)
D	$0.37^{+0.05}_{-0.1}$
E	0.125±0.075
F	1.675±0.125
G	1.55
H	7.7±0.2
I	5.6±0.2
J	1.05±0.2
K	$0.2^{+0.1}_{-0.05}$
L	0.6±0.2
M	0.10
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P38GS-65-BGG

RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Soldering Method	Soldering Conditions	Recommended Condition symbol
Infrared reflow	Package peak temperature: 235 °C; Time: 30 secs. max. (210 °C min.); Number of times: 3 times max.; Number of day: none; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% max.) is recommended	IR35-00-3
VPS	Package peak temperature: 215 °C; Time: 40 secs. max. (200 °C min.); Number of times: 3 times max.; Number of day: none; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% max.) is recommended.	VP15-00-3
Wave soldering	Package peak temperature: 260 °C; Time: 10 secs. max.; Number of times: once; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% max.) is recommended.	WS60-00-1

Caution Do not use two or more soldering methods in combination.

[MEMO]

[MEMO]

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