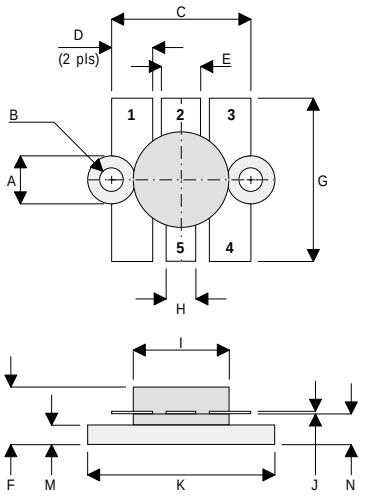
TetraFET

D1204UK

ROHS COMPLIANT METAL GATE RF SILICON FET

MECHANICAL DATA



DT

PIN 1 SOURCE (COMMON) PIN 2 GATE

PIN 3 SOURCE (COMMON) PIN 4 SOURCE (COMMON)

PIN 5 DRAIN

DIM	mm	Tol.	Inches	Tol.
A	6.35 DIA	0.13	0.250 DIA	0.005
B	3.17 DIA	0.13	0.125 DIA	0.005
C	18.41	0.25	0.725	0.010
D	5.46	0.13	0.215	0.005
E	5.21	0.13	0.205	0.005
F	7.62	MAX	0.300	MAX
G	21.59	0.38	0.850	0.015
H	3.94	0.13	0.155	0.005
I	12.70	0.13	0.500	0.005
J	0.13	0.03	0.005	0.001
K	24.76	0.13	0.975	0.005
M	2.59	0.13	0.102	0.005
N	4.06	0.25	0.160	0.010

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 30W – 12.5V – 175MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **LOW NOISE**
- **HIGH GAIN – 10 dB MINIMUM**

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1 MHz to 200 MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	117W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	30A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions			Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0	I_D = 100mA		40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 12.5V	V_{GS} = 0				1	mA
I_{GSS}	Gate Leakage Current	V_{GS} = 20V	V_{DS} = 0				1	µA
$V_{GS(th)}$	Gate Threshold Voltage*	I_D = 10mA	V_{DS} = V_{GS}		1		7	V
g_{fs}	Forward Transconductance*	V_{DS} = 10V	I_D = 3A		2.4			S
G_{PS}	Common Source Power Gain	P_O = 30W			10			dB
η	Drain Efficiency	V_{DS} = 12.5V	I_{DQ} = 0.6A		50			%
VSWR	Load Mismatch Tolerance	f = 175MHz			20:1			—
C_{iss}	Input Capacitance	V_{DS} = 0	V_{GS} = –5V	f = 1MHz			180	pF
C_{oss}	Output Capacitance	V_{DS} = 12.5V	V_{GS} = 0	f = 1MHz			120	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 12.5V	V_{GS} = 0	f = 1MHz			12	pF

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 1.5°C / W

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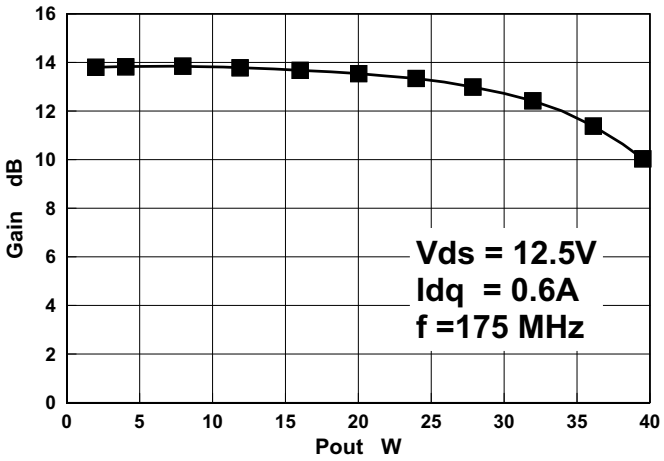

Figure 1- Gain vs. Power Output

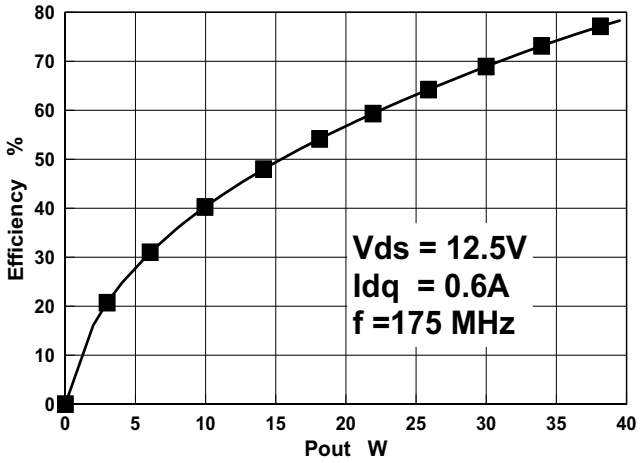

Figure 2 - Efficiency vs Power Output

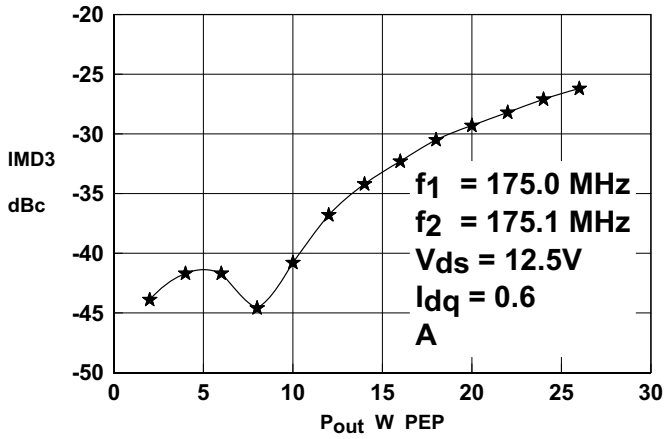

Figure 3 - IMD vs Power Output

OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175	2.2 + j3.8	1.4 - j1.8

Typical S Parameters

! V_{DS} = 12.5V, I_{DQ} = 0.6A

MHZ S MA R 50

Freq	S11		S21		S12		S22	
MHz	mag	ang	mag	ang	mag	ang	mag	ang
50	0.78	-167.2	17.2	76.0	0.011	0.0	0.72	-164.2
100	0.82	-171.7	7.7	57.9	0.008	3.9	0.78	-167.6
150	0.87	-174.9	4.5	44.5	0.006	31.6	0.84	-170.3
200	0.90	-178.2	2.9	34.2	0.008	63.1	0.88	-173.3
250	0.93	178.6	2.0	26.2	0.012	75.9	0.91	-176.2
300	0.94	175.4	1.5	19.9	0.016	79.6	0.93	-178.9
350	0.96	172.5	1.1	14.8	0.020	80.1	0.95	178.5
400	0.96	169.6	0.9	10.5	0.025	79.2	0.96	176.1
450	0.97	166.9	0.7	7.1	0.029	77.7	0.97	173.8
500	0.97	164.3	0.6	4.2	0.033	76.0	0.97	171.7

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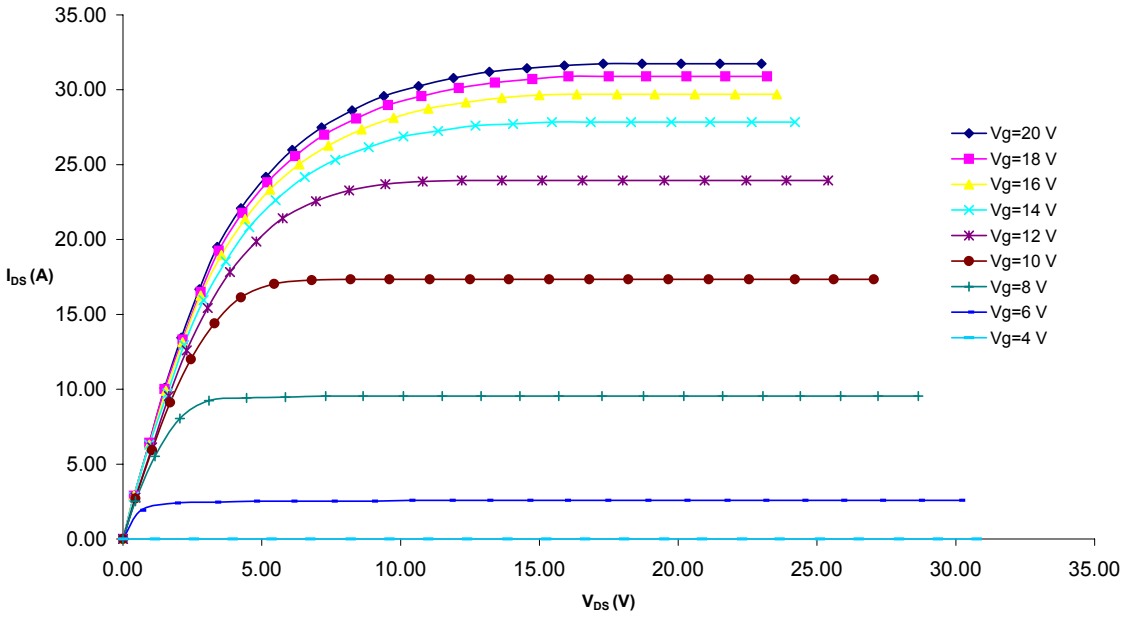

Figure 4 – Typical IV Characteristics.

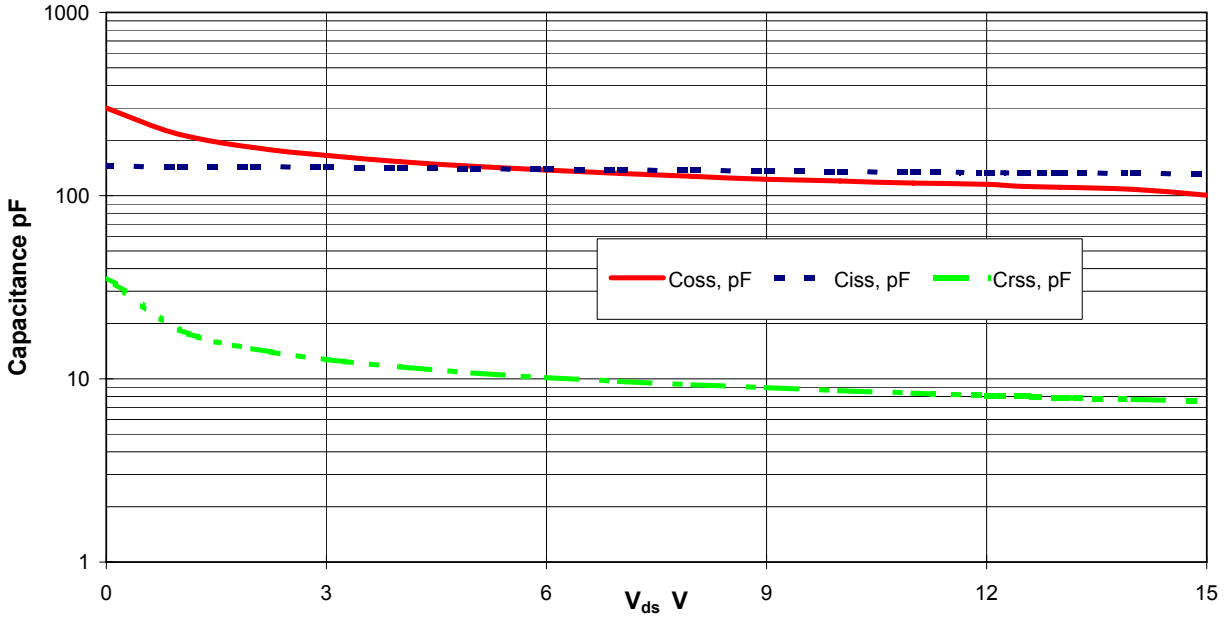

Figure 5 – Typical CV Characteristics.

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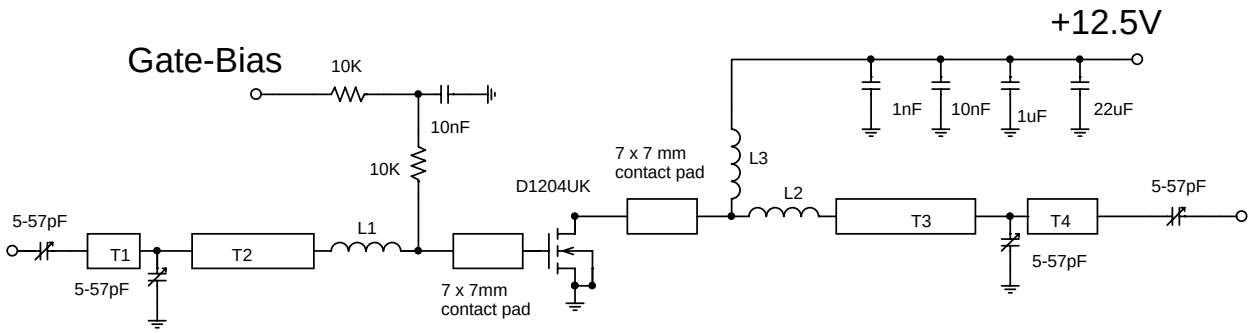

D1204UK 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/glass, Er=2.5

All microstrip lines W=4.4mm

T1 8mm

T2 22mm

T3 18mm

T4 4.5mm

L1 Hairpin loop 16swg 15.5mm dia

L2 Hairpin loop 16swg 10mm dia

L3 11 turns 18swg enamelled copper wire, 10mm i.d.

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