CYT9174
2.0A Bus Termination Regulator

Description

The CYT9174 regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage, which is adjusted by two external voltage divider resistors. The regulator is capable of sourcing or sinking up to 2.0A of current while regulating an output voltage to within 2% (DDR 1 or DDR 2) or less.

The CYT9174, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed back-plane designs. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

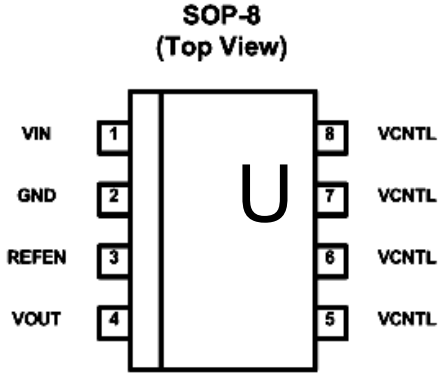
Features

- Support Both DDR 1 ($1.25V_{TT}$) and DDR 2 ($0.9V_{TT}$) Requirements
- SOP-8 Packages
- Capable of Sourcing and Sinking Current 2.0A
- Current-limiting Protection
- Thermal Protection
- Current-shoot-through protection
- Integrated Power MOSFETs
- Generates Termination Voltages for SSTL-2
- High Accuracy Output Voltage at Full-Load
- Adjustable Vout by External Resistors
- Minimum External Components
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

Application

- DDR Memory Termination
- Active Termination Buses
- Supply Splitter

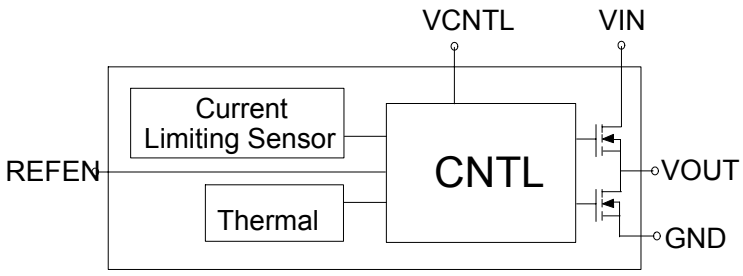
Pin Configuration



Pin Description

Pin Name	Pin function
V_{IN}	Power Input
GND	Ground
V_{CNTL}	Gate Drive Voltage
REFEN	Reference Voltage input and Chip Enable
V_{OUT}	Output Voltage

Block Diagram



Absolute Maximum Rating (1)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	6	V
Power Dissipation	P_D	Internally Limited	--
ESD Rating	--	3	KV
Storage Temperature Range	T_S	-65 to 150	°C
Lead Temperature (Soldering, 5 sec.)	T_{LEAD}	260	°C
Package Thermal Resistance	Θ_{JC}	15.7	ºC/W

Electrical Characteristics

V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REFEN}=1.25V, C_{OUT}=10μF (Ceramic)), T_A=25ºC, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Offset Voltage (2)	V_{OS}	I_{OUT} = 0A	-20	-5	20	mV
Load Regulation (DDR 1/2)	$\|\Delta V_{LOAD}\|$	I_L : 0A→2.0A	--	0.5	2	%
		I_L : 0A→-2.0A	--	0.5	2	
Input Voltage Range (DDR 1/2)	V_{IN}	Keep V_{CNTL}≥V_{IN} on operation power on and power off sequences	1.6	2.5/1.8	--	V
	V_{CNTL}		--	3.3	6	
Current In Shutdown Mode	I_{SHDN}	V_{REFEN} ＜0.2V, R_L = 180Ω	--	1	90	μA
Short Circuit Protection						
Current limit	I_{LIMIT}		--	2.5	--	A
Quiescent Current	I_Q	I_L=2.0A	--	1.4	3	mA
Over Temperature Protection						
Thermal Shutdown Temperature	T_{CASE}	3.3V ≤ V_{CNTL} ≤5 V	--	100	--	ºC
Thermal Shutdown Hysterresis		Guaranteed by design	--	30	--	
Shutdown Function						
Shutdown Threshold Trigger		Output=High	0.8	--	--	V
		Output=Low	--	--	0.2	

Note 1: Exceeding the absolute maximum rating may damage the device.

Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}

Application Information

Internal parasitic diode

Avoid forward-bias internal parasitic diode, V_{OUT} to V_{CNTL}, and V_{OUT} to V_{IN}, the V_{OUT} should not be forced same voltage respect to ground on this pin while the V_{CNTL} or V_{IN} is disappeared.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V.

In addition to item1, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

Thermal Consideration

CYT9174 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous normal load conditions however, the maximum junction temperature rating of 150°C must not be exceeded. Higher continuous currents or ambient temperature require additional heatsinking. Heat sinking to the IC package must consider the worst case power dissipation which may occur.

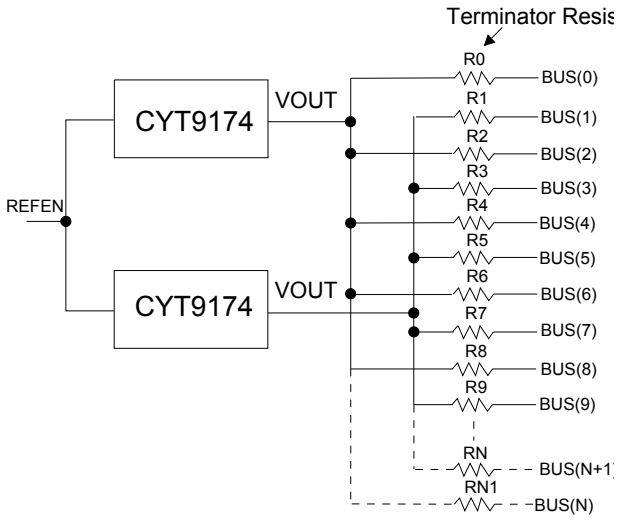
It should also be noted that with the V_{CNTL} equal to 5V, the point of thermal shutdown will be degraded by approx. 20°C compared to the V_{CNTL} equipped with 3.3V. It is highly recommended that to use the 3.3V rail acting as the V_{CNTL} so as to minimize the thermal concern of the CYT9174 in the SOP-8 package.

Layout Consideration

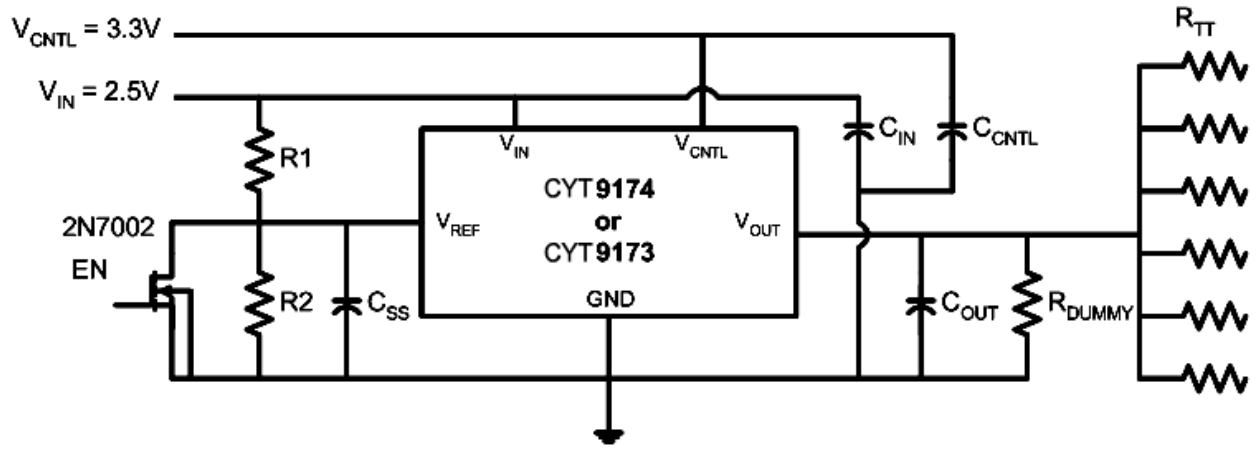
The CYT9174 regulator is packaged in thermally enhanced plastic SOP-8 package. This small footprint package is unable to convectively dissipate the heat generated when the regulator is operating at high current levels. In order to control die operating temperatures, the PC board layout should allow for maximum possible copper area at the V_{CNTL} pins of the CYT9174.

The multiple V_{CNTL} pins on the SOP-8 package are internally connected, but lowest thermal resistance will result if these pins are tightly connected on the PC board. This will also aid heat dissipation at high power levels.

If the large copper around the IC is unavailable, a buried layer may be used as a heat spreader, Use via to conduct the heat into the buried or backside of PCB layer. The via should be small enough to retain solder when the board is wave-soldered.



Application Diagram



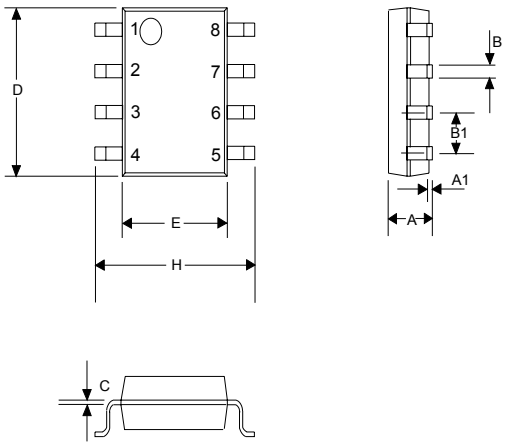
$R_1 = R_2 = 100K\Omega$, $R_{TT} = 50\Omega/33\Omega/25\Omega$

$C_{OUT, min}$ = 10μF(Ceramic) + 1000μF under the worst case testing condition

R_{DUMMY} = 1KΩ as for V_{OUT} discharge when V_{IN} is not present but V_{CNTL} is present

C_{SS} = 1μF, C_{IN} = 470μF(Low ESR), C_{CNTL} = 47μF

Outline Drawing SOP-8



DIMENSIONS				
DIM[N]	INCHES		MM	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
B	0.0130	0.0200	0.33	0.51
B1	0.050 BSC		1.27 BSC	
C	0.0075	0.0098	0.19	0.25
D	0.1890	0.1968	4.80	5.00
H	0.2284	0.2440	5.80	6.20
E	0.1497	0.1574	3.80	4.00