

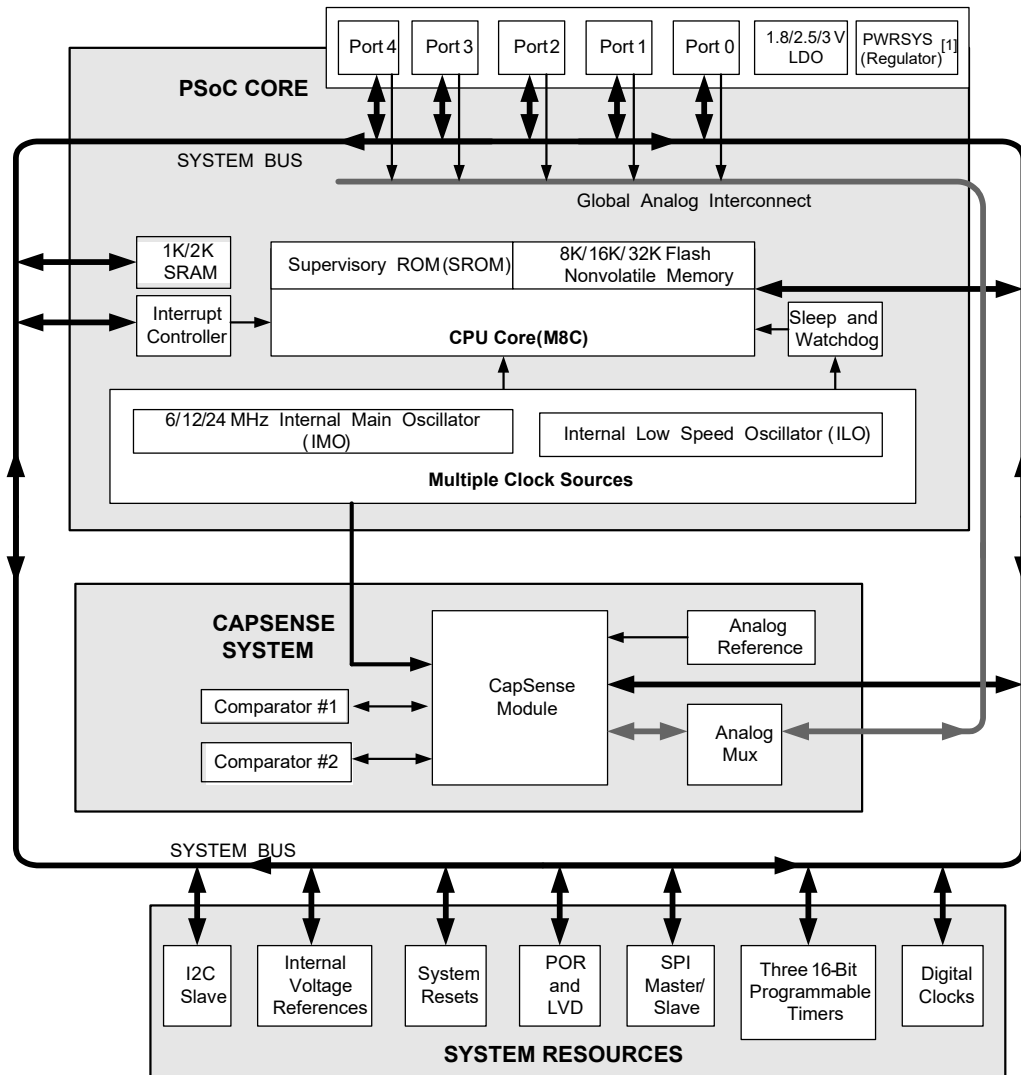
1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors

Features

- **QuietZone™ Controller**
 - Patented Capacitive Sigma Delta PLUS (CSD PLUS™) sensing algorithm for robust performance
 - High Sensitivity (0.1 pF) and best-in-class SNR performance to support:
 - Overlay thickness of 15 mm for glass and 5 mm plastic
 - Proximity Solutions
 - Superior noise immunity performance against conducted and radiated noise and ultra low radiated emissions
 - Standardized user modules for overcoming noise
- **Low power CapSense® block with SmartSense Auto-tuning**
 - Low average power consumption –
 - 28 µA/sensor in run time (wake-up and scan once every 125 ms)
 - SmartSense_EMC_PLUS Auto-Tuning
 - Sets and maintains optimal sensor performance during run time
 - Eliminates system tuning during development and production
 - Compensates for variations in manufacturing process
- **Driven shield available on five GPIO pins**
 - Delivers best-in class water tolerant designs
 - Robust proximity sensing in the presence of metal objects
 - Supports longer trace lengths
 - Max load of 100 pF (3 MHz)
- **Powerful Harvard-architecture processor**
 - M8C CPU with a max speed of 24 MHz
- **Operating Range: 1.71 V to 5.5 V**
 - Standby Mode 1.1 µA (Typ)
 - Deep Sleep 0.1 µA (Typ)
- **Operating Temperature range: –40 °C to +85 °C**
- **Flexible on-chip memory**
 - 8 KB flash, 1 KB SRAM
 - 16 KB flash, 2 KB SRAM
 - 32 KB flash, 2 KB SRAM
 - 50,000 flash erase/write cycles
 - Read while Write with EEPROM emulation
 - In-system programming simplifies manufacturing process
- **4 Clock Sources**
 - Internal main oscillator (IMO): 6/12/24 MHz
 - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
 - External 32 KHz Crystal Oscillator
 - External Clock Input
- **Programmable pin configurations**
 - Up to 34 general-purpose I/Os (GPIOs)
 - Dual mode GPIO (Analog and Digital)
 - High sink current of 25 mA per GPIO
 - Max sink current 120 mA for all I/Os combined
 - Source Current
 - 5 mA on ports 0 and 1
 - 1 mA on ports 2, 3 and 4
 - Configurable internal pull-up, high-Z and open drain modes
 - Selectable, regulated digital I/O on port 1
 - Configurable input threshold on port 1
- **Versatile Analog functions**
 - Internal analog bus supports connection of multiple sensors to form ganged proximity sensor
 - Internal Low-Dropout voltage regulator for high power supply rejection ratio (PSRR)
- **Additional system resources**
 - I²C Slave:
 - Selectable to 50 kHz, 100 kHz, or 400 kHz
 - Selectable Clock stretch or Forced Nack Mode
 - I²C wake from sleep with Hardware address match
 - 12 MHz (Configurable) SPI master and slave
 - Three 16-bit timers
 - Watchdog and sleep timers
 - Integrated supervisory circuit
 - 10-bit incremental analog-to-digital converter (ADC) with internal voltage reference
 - Two general-purpose high speed, low power analog comparators
- **Complete development tools**
 - Free development tool (PSoC Designer™)
- **Sensor and Package options**
 - 10 Sensing Inputs – 16-pin QFN, 16-pin SOIC
 - 16 Sensing Inputs – 24-pin QFN
 - 24 Sensing Inputs – 30-pin WLCSP
 - 25 Sensing Inputs – 32-pin QFN
 - 31 Sensing Inputs – 48-pin QFN

Errata: For information on silicon errata, see “[Errata](#)” on page 38. Details include trigger conditions, devices affected, and proposed workaround.

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

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PSoC® Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the “Logic Block Diagram” on page 2, consists of three main areas:

- The core
- CapSense analog system
- System resources

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20x37/47/67/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 34 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 31 inputs^[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

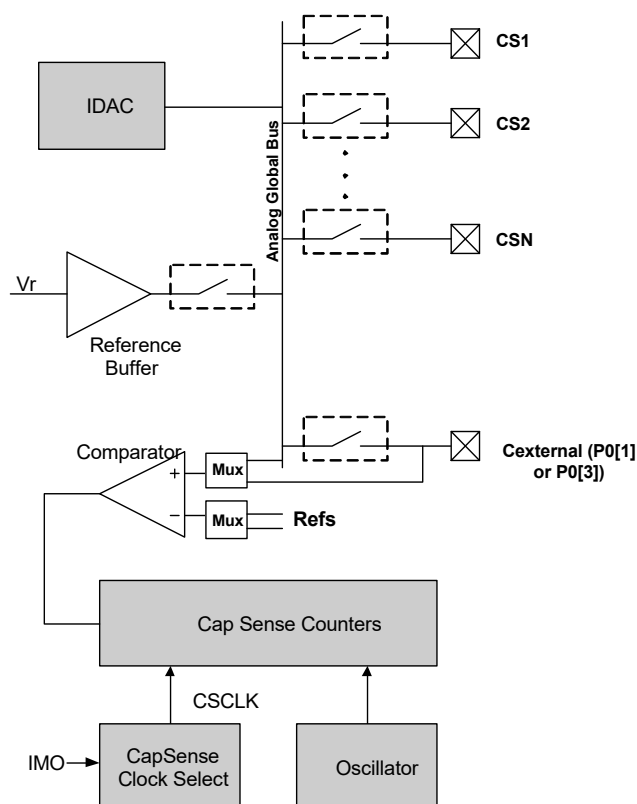
SmartSense™ Auto-tuning

SmartSense auto-tuning is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters of each sensor during run time. SmartSense auto-tuning allows engineers to go from prototyping to mass production without retuning for manufacturing variations in PCB and/or overlay material properties.

Note

2. 34 GPIOs = 31 pins for capacitive sensing + 2 pins for I²C + 1 pin for modulator capacitor.

Figure 1. CapSense System Block Diagram



Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the [I2CSBUF User Module datasheet](#).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See "Development Kits" on page 32.

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

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Designing with PSoC Designer

The PSoC development process can be summarized in the following four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate and Verify

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

Pinouts

The CY8C20x37/47/67/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O and connection to the common analog bus. However, V_{SS} , V_{DD} , and XRES are not capable of digital I/O.

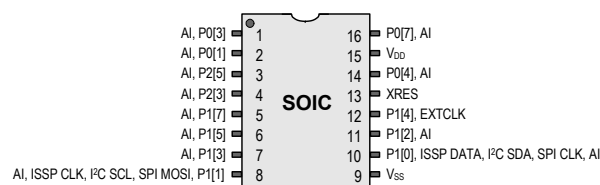
16-pin SOIC (10 Sensing Inputs)

Table 1. Pin Definitions – CY8C20237-24SXI, CY8C20247/S-24SXI [3]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|----------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P0[3] | Integrating Input |
| 2 | I/O | I | P0[1] | Integrating Input |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P1[7] | I2C SCL, SPI SS |
| 6 | I/O | I | P1[5] | I2C SDA, SPI MISO |
| 7 | I/O | I | P1[3] | |
| 8 | I/O | I | P1[1] | ISSP CLK ^[4] , I2C SCL, SPI MOSI |
| 9 | Power | | V_{SS} | Ground connection ^[7] |
| 10 | I/O | I | P1[0] | ISSP DATA ^[4] , I2C SDA, SPI CLK ^[5] |
| 11 | I/O | I | P1[2] | Driven Shield Output (optional) |
| 12 | I/O | I | P1[4] | Optional external clock (EXTCLK) |
| 13 | INPUT | | XRES | Active high external reset with internal pull-down ^[6] |
| 14 | I/O | I | P0[4] | |
| 15 | Power | | V_{DD} | Supply voltage |
| 16 | I/O | I | P0[7] | |

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20237-24SXI, CY8C20247/S-24SXI Device



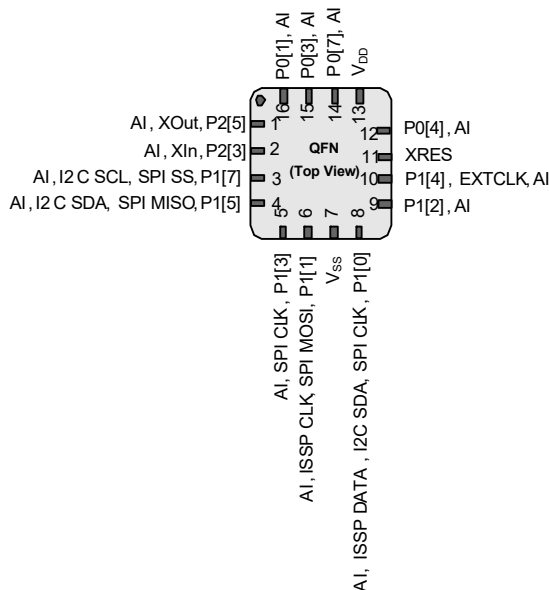
Notes

- 13 GPIOs = 10 pins for capacitive sensing+2 pins for I2C + 1 pin for modulator capacitor.
- On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.
- The internal pull down is 5KOhm.
- All VSS pins should be brought out to one common GND plane.

16-pin QFN (10 Sensing Inputs)^[8]
Table 2. Pin Definitions – CY8C20237, CY8C20247/S^[9]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 4 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 5 | IOHR | I | P1[3] | SPI CLK |
| 6 | IOHR | I | P1[1] | ISSP CLK ^[10] , I ² C SCL, SPI MOSI |
| 7 | Power | | V _{SS} | Ground connection ^[13] |
| 8 | IOHR | I | P1[0] | ISSP DATA ^[10] , I ² C SDA, SPI CLK ^[11] |
| 9 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 10 | IOHR | I | P1[4] | Optional external clock (EXTCLK) |
| 11 | Input | | XRES | Active high external reset with internal pull-down ^[12] |
| 12 | IOH | I | P0[4] | |
| 13 | Power | | V _{DD} | Supply voltage |
| 14 | IOH | I | P0[7] | |
| 15 | IOH | I | P0[3] | Integrating input |
| 16 | IOH | I | P0[1] | Integrating input |

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20237, CY8C20247/S Device

Notes

8. No center pad.
9. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
10. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. The internal pull down is 5KOhm.
13. All VSS pins should be brought out to one common GND plane.

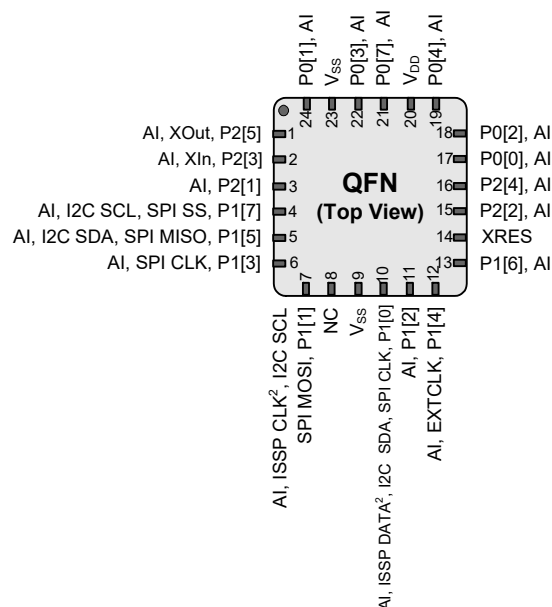
24-pin QFN (16 Sensing Inputs)^[14]
Table 3. Pin Definitions – CY8C20337, CY8C20347/S^[15]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK ^[16] , I ² C SCL, SPI MOSI |
| 8 | | | NC | No connection |
| 9 | Power | | V _{SS} | Ground connection ^[19] |
| 10 | IOHR | I | P1[0] | ISSP DATA ^[16] , I ² C SDA, SPI CLK ^[17] |
| 11 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 12 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 13 | IOHR | I | P1[6] | |
| 14 | Input | | XRES | Active high external reset with internal pull-down ^[18] |
| 15 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 16 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 17 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 18 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 19 | IOH | I | P0[4] | |
| 20 | Power | | V _{DD} | Supply voltage |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[3] | Integrating input |
| 23 | Power | | V _{SS} | Ground connection ^[19] |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

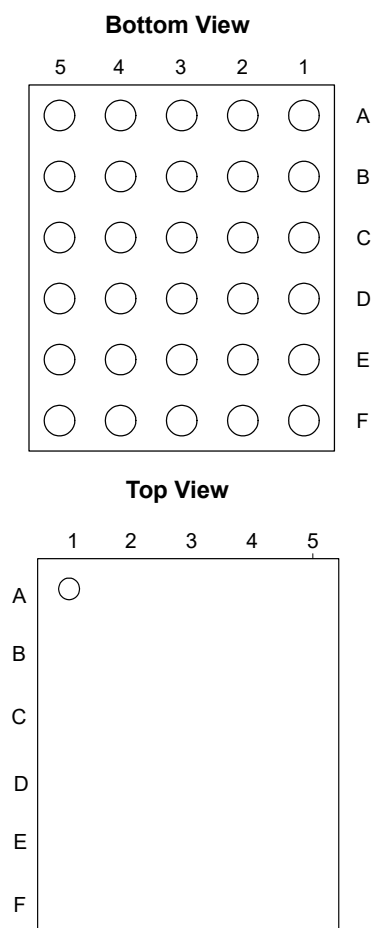
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. 19 GPIOs = 16 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
16. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
17. Alternate SPI clock.
18. The internal pull down is 5KOhm.
19. All VSS pins should be brought out to one common GND plane.

Figure 4. CY8C20337, CY8C20347/S Device


30-ball WLCSP (24 Sensing Inputs)
Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP) ^[20]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| A1 | IOH | I | P0[2] | Driven Shield Output (optional) |
| A2 | IOH | I | P0[6] | |
| A3 | Power | | V _{DD} | Supply voltage |
| A4 | IOH | I | P0[1] | Integrating Input |
| A5 | I/O | I | P2[7] | |
| B1 | I/O | I | P4[2] | |
| B2 | IOH | I | P0[0] | Driven Shield Output (optional) |
| B3 | IOH | I | P0[4] | |
| B4 | IOH | I | P0[3] | Integrating Input |
| B5 | I/O | I | P2[5] | Crystal Output (Xout) |
| C1 | I/O | I | P2[2] | Driven Shield Output (optional) |
| C2 | I/O | I | P2[4] | Driven Shield Output (optional) |
| C3 | I/O | I | P0[7] | |
| C4 | IOH | I | P3[2] | |
| C5 | I/O | I | P2[3] | Crystal Input (Xin) |
| D1 | I/O | I | P2[0] | |
| D2 | I/O | I | P3[0] | |
| D3 | I/O | I | P3[1] | |
| D4 | I/O | I | P3[3] | |
| D5 | I/O | I | P2[1] | |
| E1 | Input | | XRES | Active high external reset with internal pull-down ^[21] |
| E2 | IOHR | I | P1[6] | |
| E3 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| E4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| E5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| F1 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| F2 | IOHR | I | P1[0] | ISSP DATA ^[22] , I ² C SDA, SPI CLK ^[23] |
| F3 | Power | | V _{SS} | Supply ground ^[24] |
| F4 | IOHR | I | P1[1] | ISSP CLK ^[22] , I ² C SCL, SPI MOSI |
| F5 | IOHR | I | P1[3] | SPI CLK |

LEGEND: A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20767, CY8C20747 30-ball WLCSP

Notes

20. 27 GPIOs = 24 pins for capacitive sensing + 2 pins for I²C + 1 pin for modulator capacitor.

21. The internal pull down is 5KOhm.

22. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.

23. Alternate SPI clock.

24. All VSS pins should be brought out to one common GND plane.

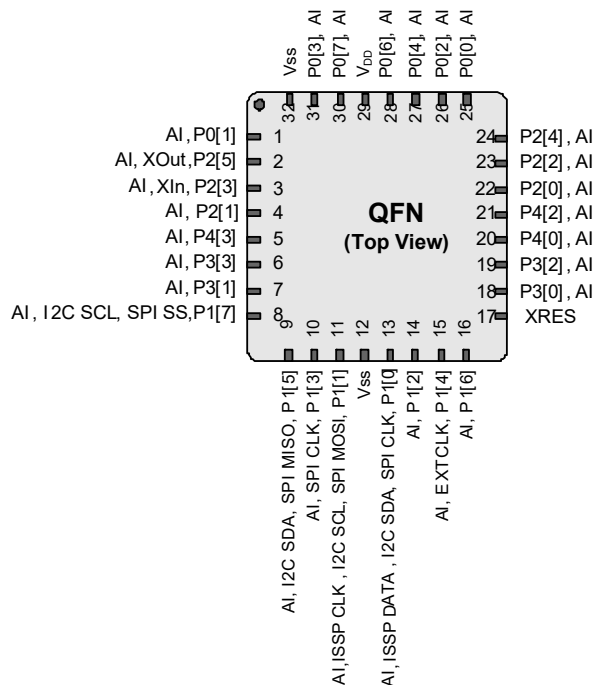
32-pin QFN (25 Sensing Inputs)^[25]
Table 5. Pin Definitions – CY8C20437, CY8C20447/S, CY8C20467/S^[26]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating input |
| 2 | I/O | I | P2[5] | Crystal output (XOut) |
| 3 | I/O | I | P2[3] | Crystal input (XIn) |
| 4 | I/O | I | P2[1] | |
| 5 | I/O | I | P4[3] | |
| 6 | I/O | I | P3[3] | |
| 7 | I/O | I | P3[1] | |
| 8 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 9 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 10 | IOHR | I | P1[3] | SPI CLK. |
| 11 | IOHR | I | P1[1] | ISSP CLK ^[27] , I ² C SCL, SPI MOSI. |
| 12 | Power | | V _{SS} | Ground connection ^[30] |
| 13 | IOHR | I | P1[0] | ISSP DATA ^[27] , I ² C SDA, SPI CLK ^[28] |
| 14 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down ^[29] |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P4[0] | |
| 21 | I/O | I | P4[2] | |
| 22 | I/O | I | P2[0] | |
| 23 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 24 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 25 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 26 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 27 | IOH | I | P0[4] | |
| 28 | IOH | I | P0[6] | |
| 29 | Power | | V _{DD} | |
| 30 | IOH | I | P0[7] | |
| 31 | IOH | I | P0[3] | Integrating input |
| 32 | Power | | V _{SS} | Ground connection ^[30] |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

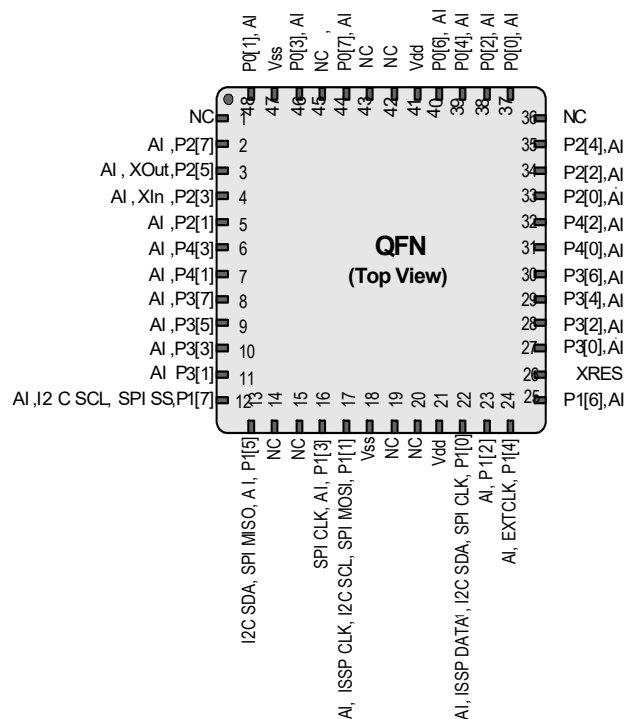
Notes

25. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
26. 28 GPIOs = 25 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
27. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
28. Alternate SPI clock.
29. The internal pull down is 5KOhm.
30. All VSS pins should be brought out to one common GND plane.

Figure 6. CY8C20437, CY8C20447/S, CY8C20467/S Device


48-pin QFN (31 Sensing Inputs)^[31]
Table 6. Pin Definitions – CY8C20637, CY8C20647/S, CY8C20667/S ^[32]

| Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|
| 1 | | | NC | No connection |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 13 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 14 | | | NC | No connection |
| 15 | | | NC | No connection |
| 16 | IOHR | I | P1[3] | SPI CLK |
| 17 | IOHR | I | P1[1] | ISSP CLK ^[33] , I ² C SCL, SPI MOSI |
| 18 | Power | | V _{SS} | Ground connection ^[36] |
| 19 | | | NC | No connection |
| 20 | | | NC | No connection |
| 21 | Power | | V _{DD} | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA ^[33] , I ² C SDA, SPI CLK ^[34] |
| 23 | IOHR | I | P1[2] | Driven Shield Output (optional) |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull-down ^[35] |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | Driven Shield Output (optional) |
| 35 | I/O | I | P2[4] | Driven Shield Output (optional) |
| 36 | | | NC | No connection |
| 37 | IOH | I | P0[0] | Driven Shield Output (optional) |
| 38 | IOH | I | P0[2] | Driven Shield Output (optional) |
| 39 | IOH | I | P0[4] | |

Figure 7. CY8C20637, CY8C20647/S, CY8C20667/S Device


| Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|--|
| 40 | IOH | I | P0[6] | |
| 41 | Power | | V _{DD} | Supply voltage |
| 42 | | | NC | No connection |
| 43 | | | NC | No connection |
| 44 | IOH | I | P0[7] | |
| 45 | | | NC | No connection |
| 46 | IOH | I | P0[3] | Integrating input |
| 47 | Power | | V _{SS} | Ground connection ^[36] |
| 48 | IOH | I | P0[1] | Integrating input |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

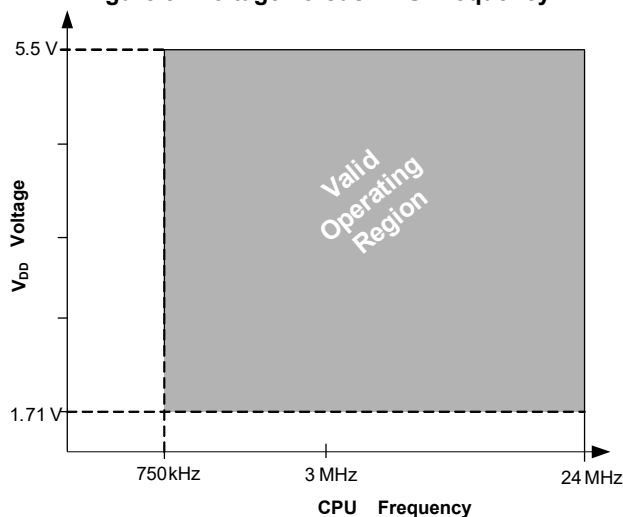
Notes

31. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
32. 34 GPIOs = 31 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.
33. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
34. Alternate SPI clock.
35. The internal pull down is 5KOhm.
36. All VSS pins should be brought out to one common GND plane.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x37/47/67/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 8. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--|---|-----------------------|-----|-----------------------|-------|
| T _{STG} | Storage temperature | Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | -55 | +25 | +125 | °C |
| V _{DD} | Supply voltage relative to V _{SS} | — | -0.5 | — | +6.0 | V |
| V _{IO} | DC input voltage | — | V _{SS} - 0.5 | — | V _{DD} + 0.5 | V |
| V _{IOZ} | DC voltage applied to tristate | — | V _{SS} - 0.5 | — | V _{DD} + 0.5 | V |
| I _{MIO} | Maximum current into any port pin | — | -25 | — | +50 | mA |
| ESD | Electro static discharge voltage | Human body model ESD | 2000 | — | — | V |
| LU | Latch up current | In accordance with JESD78 standard | — | — | 200 | mA |

Operating Temperature

Table 8. Operating Temperature

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|------------------------------|---|-----|-----|------|-------|
| T _A | Ambient temperature | — | -40 | — | +85 | °C |
| T _C | Commercial temperature range | — | 0 | — | 70 | °C |
| T _J | Operational die temperature | The temperature rise from ambient to junction is package specific. See the Thermal Impedances on page 31 . The user must limit the power consumption to comply with this requirement. | -40 | — | +100 | °C |

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Chip-Level Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------------------|---|--|------|------|------|-------|
| V_{DD} [37, 38, 39] | Supply voltage | See Table 14 on page 17. | 1.71 | – | 5.50 | V |
| I_{DD24} | Supply current, IMO = 24 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 2.88 | 4.00 | mA |
| I_{DD12} | Supply current, IMO = 12 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.71 | 2.60 | mA |
| I_{DD6} | Supply current, IMO = 6 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.16 | 1.80 | mA |
| I_{SB0} [40, 41, 42, 43] | Deep sleep current | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 0.10 | 1.1 | μA |
| I_{SB1} [40, 41, 42, 43] | Standby current with POR, LVD and sleep timer | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 1.07 | 1.50 | μA |
| I_{SB12C} [40, 41, 42, 43] | Standby current with I ² C enabled | Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz | – | 1.64 | – | μA |

Notes

37. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
 - a. Bring the device out of sleep before powering down.
 - b. Assume that V_{DD} falls below 100 mV before powering back up.
 - c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
 - d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the [Technical Reference Manual](#). In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected and resets the device when V_{DD} goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD} , the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
40. **Errata:** When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,80h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the [“Errata”](#) on page 38.
41. **Errata:** When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the [“Errata”](#) on page 38.
42. **Errata:** If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the [“Errata”](#) on page 38.
43. **Errata:** Device wakes up from sleep when an analog interrupt is trigger. For more information, see the [“Errata”](#) on page 38.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 10. 3.0 V to 5.5 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|--|---|----------------------|-------|----------------|---------------|
| R_{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | $k\Omega$ |
| V_{OH1} | High output voltage Port 2 or 3 pins | $I_{OH} \leq 10\ \mu\text{A}$, maximum of 10 mA source current in all I/Os | $V_{DD} - 0.20$ | – | – | V |
| V_{OH2} | High output voltage Port 2 or 3 Pins | $I_{OH} = 1\ \text{mA}$, maximum of 20 mA source current in all I/Os | $V_{DD} - 0.90$ | – | – | V |
| V_{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | $I_{OH} < 10\ \mu\text{A}$, maximum of 10 mA source current in all I/Os | $V_{DD} - 0.20$ | – | – | V |
| V_{OH4} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | $I_{OH} = 5\ \text{mA}$, maximum of 20 mA source current in all I/Os | $V_{DD} - 0.90$ | – | – | V |
| V_{OH5} | High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out | $I_{OH} < 10\ \mu\text{A}$, $V_{DD} > 3.1\ \text{V}$, maximum of 4 I/Os all sourcing 5 mA | 2.85 | 3.00 | 3.30 | V |
| V_{OH6} | High output voltage Port 1 pins with LDO regulator enabled for 3 V out | $I_{OH} = 5\ \text{mA}$, $V_{DD} > 3.1\ \text{V}$, maximum of 20 mA source current in all I/Os | 2.20 | – | – | V |
| V_{OH7} | High output voltage Port 1 pins with LDO enabled for 2.5 V out | $I_{OH} < 10\ \mu\text{A}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os | 2.35 | 2.50 | 2.75 | V |
| V_{OH8} | High output voltage Port 1 pins with LDO enabled for 2.5 V out | $I_{OH} = 2\ \text{mA}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os | 1.90 | – | – | V |
| V_{OH9} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH} < 10\ \mu\text{A}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os | 1.60 | 1.80 | 2.10 | V |
| V_{OH10} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | $I_{OH} = 1\ \text{mA}$, $V_{DD} > 2.7\ \text{V}$, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| V_{OL} | Low output voltage | $I_{OL} = 25\ \text{mA}$, $V_{DD} > 3.3\ \text{V}$, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| V_{IL} | Input low voltage | – | – | – | 0.80 | V |
| V_{IH} | Input high voltage | – | $V_{DD} \times 0.65$ | – | $V_{DD} + 0.7$ | V |
| V_H | Input hysteresis voltage | – | – | 80 | – | mV |
| I_{IL} | Input leakage (Absolute Value) | – | – | 0.001 | 1 | μA |
| C_{PIN} | Pin capacitance | Package and pin dependent Temp = 25°C | 0.50 | 1.70 | 7 | pF |
| $V_{ILLVT3.3}$ | Input Low Voltage with low threshold enable set, Enable for Port1 [44] | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.8 | V | – | – |
| $V_{IHLVT3.3}$ | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.4 | – | – | V |
| $V_{ILLVT5.5}$ | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.8 | V | – | – |
| $V_{IHLVT5.5}$ | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.7 | – | – | V |

Note

44. **Errata:** Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S VDD. For more information see item #7 in “Errata” on page 38.

Table 11. 2.4 V to 3.0 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|--|--|------------------------|------|-----------------------|-------|
| R _{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 pins | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.20 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 Pins | I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.40 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.20 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.50 | – | – | V |
| V _{OH5A} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} < 10 μA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| V _{OH6A} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| V _{OL} | Low output voltage | I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| V _{IL} | Input low voltage | – | – | – | 0.72 | V |
| V _{IH} | Input high voltage | – | V _{DD} × 0.65 | – | V _{DD} + 0.7 | V |
| V _H | Input hysteresis voltage | – | – | 80 | – | mV |
| I _{IL} | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| C _{PIN} | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| V _{ILLVT2.5} | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.7 | V | – | |
| V _{IHLVT2.5} | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.2 | | – | V |

Table 12. 1.71 V to 2.4 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--|---|------------------------|------|-----|-------|
| R _{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 pins | I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.20 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 pins | I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.50 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.20 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} - 0.50 | – | – | V |

Table 12. 1.71 V to 2.4 V DC GPIO Specifications (continued)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------|--------------------------------|--|----------------------|------|----------------------|-------|
| V_{OL} | Low output voltage | $I_{OL} = 5$ mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.40 | V |
| V_{IL} | Input low voltage | – | – | – | $0.30 \times V_{DD}$ | V |
| V_{IH} | Input high voltage | – | $0.65 \times V_{DD}$ | – | – | V |
| V_H | Input hysteresis voltage | – | – | 80 | – | mV |
| I_{IL} | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| C_{PIN} | Capacitive load on pins | Package and pin dependent temp = 25 °C | 0.50 | 1.70 | 7 | pF |

Table 13. GPIO Current Sink and Source Specifications

| Supply Voltage | Mode | Port 0/1 per I/O (max) | Port 2/3/4 per I/O (max) | Total Current Even Pins (max) | Total Current Odd Pins (max) | Units |
|----------------|--------|------------------------|--------------------------|-------------------------------|------------------------------|-------|
| 1.71–2.4 | Sink | 5 | 5 | 20 | 30 | mA |
| | Source | 2 | 0.5 | $10^{[45]}$ | | mA |
| 2.4–3.0 | Sink | 10 | 10 | 30 | 30 | mA |
| | Source | 2 | 0.2 | $10^{[45]}$ | | mA |
| 3.0–5.0 | Sink | 25 | 25 | 60 | 60 | mA |
| | Source | 5 | 1 | $20^{[45]}$ | | mA |

DC Analog Mux Bus Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC Analog Mux Bus Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------|---|------------|-----|-----|-----|----------|
| R_{SW} | Switch resistance to common analog bus | – | – | – | 800 | Ω |
| R_{GND} | Resistance of initialization switch to V_{SS} | – | – | – | 800 | Ω |

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC Comparator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------|--|-------------------------------------|-----|-----|-----|---------|
| V_{LPC} | Low power comparator (LPC) common mode | Maximum voltage limited to V_{DD} | 0.2 | – | 1.8 | V |
| I_{LPC} | LPC supply current | – | – | 10 | 80 | μ A |
| V_{OSLPC} | LPC voltage offset | – | – | 2.5 | 30 | mV |

Note

45. Total current (odd + even ports)

Comparator User Module Electrical Specifications

Table 16 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$.

Table 16. Comparator User Module Electrical Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|--------------------------|-------------------------------------|-----|-----|-----|---------------|
| T_{COMP} | Comparator response time | 50 mV overdrive | – | 70 | 100 | ns |
| Offset | – | Valid from 0.2 V to 1.5 V | – | 2.5 | 30 | mV |
| Current | – | Average DC current, 50 mV overdrive | – | 20 | 80 | μA |
| PSRR | Supply voltage > 2 V | Power supply rejection ratio | – | 80 | – | dB |
| | Supply voltage < 2 V | Power supply rejection ratio | – | 40 | – | dB |
| Input range | – | – | 0.2 | | 1.5 | V |

ADC Electrical Specifications

Table 17. ADC User Module Electrical Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------------|------------------------------|---|---|---|---|----------|
| Input | | | | | | |
| V_{IN} | Input voltage range | – | 0 | – | V_{REFADC} | V |
| C_{IIN} | Input capacitance | – | – | – | 5 | pF |
| R_{IN} | Input resistance | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution | $1/(500\text{fF} \times \text{data clock})$ | $1/(400\text{fF} \times \text{data clock})$ | $1/(300\text{fF} \times \text{data clock})$ | Ω |
| Reference | | | | | | |
| V_{REFADC} | ADC reference voltage | – | 1.14 | – | 1.26 | V |
| Conversion Rate | | | | | | |
| F_{CLK} | Data clock | Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 21 for accuracy | 2.25 | – | 6 | MHz |
| S8 | 8-bit sample rate | Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{Resolution}}/\text{Data Clock})$ | – | 23.43 | – | ksps |
| S10 | 10-bit sample rate | Data clock set to 6 MHz. sample rate = $0.001/(2^{\text{resolution}}/\text{data clock})$ | – | 5.85 | – | ksps |
| DC Accuracy | | | | | | |
| RES | Resolution | Can be set to 8, 9, or 10 bit | 8 | – | 10 | bits |
| DNL | Differential nonlinearity | – | –1 | – | +2 | LSB |
| INL | Integral nonlinearity | – | –2 | – | +2 | LSB |
| E_{OFFSET} | Offset error | 8-bit resolution | 0 | 3.20 | 19.20 | LSB |
| | | 10-bit resolution | 0 | 12.80 | 76.80 | LSB |
| E_{GAIN} | Gain error | For any resolution | –5 | – | +5 | %FSR |
| Power | | | | | | |
| I_{ADC} | Operating current | – | – | 2.10 | 2.60 | mA |
| PSRR | Power supply rejection ratio | PSRR ($V_{DD} > 3.0\text{ V}$) | – | 24 | – | dB |
| | | PSRR ($V_{DD} < 3.0\text{ V}$) | – | 30 | – | dB |

DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC POR and LVD Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|----------------------------------|--|----------------------|------|------|-------|
| V _{POR0} | 1.66 V selected in PSoC Designer | V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog. | 1.61 | 1.66 | 1.71 | V |
| V _{POR1} | 2.36 V selected in PSoC Designer | | – | 2.36 | 2.41 | V |
| V _{POR2} | 2.60 V selected in PSoC Designer | | – | 2.60 | 2.66 | V |
| V _{POR3} | 2.82 V selected in PSoC Designer | | – | 2.82 | 2.95 | V |
| V _{LVD0} | 2.45 V selected in PSoC Designer | – | 2.40 | 2.45 | 2.51 | V |
| V _{LVD1} | 2.71 V selected in PSoC Designer | | 2.64 ^[46] | 2.71 | 2.78 | V |
| V _{LVD2} | 2.92 V selected in PSoC Designer | | 2.85 ^[47] | 2.92 | 2.99 | V |
| V _{LVD3} | 3.02 V selected in PSoC Designer | | 2.95 ^[48] | 3.02 | 3.09 | V |
| V _{LVD4} | 3.13 V selected in PSoC Designer | | 3.06 | 3.13 | 3.20 | V |
| V _{LVD5} | 1.90 V selected in PSoC Designer | | 1.84 | 1.90 | 2.32 | V |
| V _{LVD6} | 1.80 V selected in PSoC Designer | | 1.75 ^[49] | 1.80 | 1.84 | V |
| V _{LVD7} | 4.73 V selected in PSoC Designer | | 4.62 | 4.73 | 4.83 | V |

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Programming Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|---|--|-----------------|-----|------------------------|-------|
| V _{DDIWRITE} | Supply voltage for flash write operations | – | 1.71 | – | 5.25 | V |
| I _{DDP} | Supply current during programming or verify | – | – | 5 | 25 | mA |
| V _{ILP} | Input low voltage during programming or verify | See appropriate “DC GPIO Specifications” on page 15 | – | – | V _{IL} | V |
| V _{IHP} | Input high voltage during programming or verify | See appropriate “DC GPIO Specifications” on page 15 | V _{IH} | – | – | V |
| I _{ILP} | Input current when Applying V _{ILP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 0.2 | mA |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 1.5 | mA |
| V _{OLP} | Output low voltage during programming or verify | – | – | – | V _{SS} + 0.75 | V |
| V _{OHP} | Output high voltage during programming or verify | See appropriate “DC GPIO Specifications” on page 15. For V _{DD} > 3V use V _{OH4} in Table 10 on page 15. | V _{OH} | – | V _{DD} | V |
| Flash _{ENPB} | Flash write endurance | Erase/write cycles per block | 50,000 | – | – | – |
| Flash _{DR} | Flash data retention | Following maximum Flash write cycles; ambient temperature of 55 °C | 20 | – | – | Years |

Notes

46. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
 47. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
 48. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
 49. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC I²C Specifications

Table 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 20. DC I²C Specifications^[50]

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------------------|------------------|---|----------------------|-----|---------------------------------------|-------|
| V _{IL} I ² C | Input low level | $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | $0.25 \times V_{DD}$ | V |
| | | $2.5\text{ V} \leq V_{DD} \leq 3.0\text{ V}$ | – | – | $0.3 \times V_{DD}$ | V |
| | | $1.71\text{ V} \leq V_{DD} \leq 2.4\text{ V}$ | – | – | $0.3 \times V_{DD}$ | V |
| V _{IH} I ² C | Input high level | $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $0.65 \times V_{DD}$ | – | V_{DD}^{+} $0.7\text{ V}^{[51]}$ | V |

Shield Driver DC Specifications

Table 21 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 21. Shield Driver DC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|-------------------------|--|-------|-----|-------|-------|
| V _{Ref} | Reference buffer output | $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.942 | – | 1.106 | V |
| V _{RefHi} | Reference buffer output | $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.104 | – | 1.296 | V |

DC IDAC Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC IDAC Specifications (8-bit IDAC)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|---------------------------|-----|-----|-----|-------|-----------------------|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_INL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 138 | – | 169 | μA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | μA | DAC setting = 64 dec |

Table 23. DC IDAC Specifications (7-bit IDAC)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|---------------------------|-----|-----|-----|-------|-----------------------|
| IDAC_DNL | Differential nonlinearity | –1 | – | 1 | LSB | – |
| IDAC_INL | Integral nonlinearity | –2 | – | 2 | LSB | – |
| IDAC_Current | Range = 4x | 137 | – | 168 | μA | DAC setting = 127 dec |
| | Range = 8x | 138 | – | 169 | μA | DAC setting = 64 dec |

Notes

50. Errata: Pull-up resistors on I²C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C20xx7/S power supply. For more information see item #6 in the "Errata" on page 38.

51. Errata: For more information see item #6 in the "Errata" on page 38.

AC Chip-Level Specifications

Table 24 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Chip-Level Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------------------------|--|---|------|-----|-------|-------|
| F _{IMO24} | IMO frequency at 24 MHz Setting | — | 22.8 | 24 | 25.2 | MHz |
| F _{IMO12} | IMO frequency at 12 MHz setting | — | 11.4 | 12 | 12.6 | MHz |
| F _{IMO6} | IMO frequency at 6 MHz setting | — | 5.7 | 6.0 | 6.3 | MHz |
| F _{CPU} | CPU frequency | — | 0.75 | — | 25.20 | MHz |
| F _{32K1} | ILO frequency | — | 15 | 32 | 50 | kHz |
| F _{32K_U} | ILO untrimmed frequency | — | — | 32 | — | kHz |
| DC _{IMO} | Duty cycle of IMO | — | 40 | 50 | 60 | % |
| DC _{ILO} | ILO duty cycle | — | 40 | 50 | 60 | % |
| SR _{POWER_UP} | Power supply slew rate | V _{DD} slew rate during power-up | — | — | 250 | V/ms |
| t _{XRST} | External reset pulse width at power-up | After supply voltage is valid | 1 | — | — | ms |
| t _{XRST2} | External reset pulse width after power-up ^[52] | Applies after part has booted | 10 | — | — | μs |
| t _{JIT_IMO} ^[53] | 6 MHz IMO cycle-to-cycle jitter (RMS) | — | — | 0.7 | 6.7 | ns |
| | 6 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32 | — | — | 4.3 | 29.3 | ns |
| | 6 MHz IMO period jitter (RMS) | — | — | 0.7 | 3.3 | ns |
| | 12 MHz IMO cycle-to-cycle jitter (RMS) | — | — | 0.5 | 5.2 | ns |
| | 12 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32 | — | — | 2.3 | 5.6 | ns |
| | 12 MHz IMO period jitter (RMS) | — | — | 0.4 | 2.6 | ns |
| | 24 MHz IMO cycle-to-cycle jitter (RMS) | — | — | 1.0 | 8.7 | ns |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32 | — | — | 1.4 | 6.0 | ns |
| | 24 MHz IMO period jitter (RMS) | — | — | 0.6 | 4.0 | ns |

Note

52. The minimum required XRES pulse length is longer when programming the device (see Table 28 on page 23).

53. See the Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

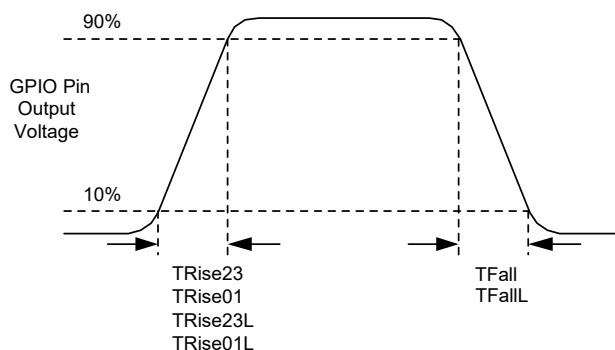
AC General Purpose I/O Specifications

Table 25 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------|--|--|-----|-----|---|-------|
| F_{GPIO} | GPIO operating frequency | Normal strong mode Port 0, 1 | 0 | – | 6 MHz for $1.71\text{ V} < V_{DD} < 2.40\text{ V}$ | MHz |
| | | | 0 | – | 12 MHz for $2.40\text{ V} < V_{DD} < 5.50\text{ V}$ | MHz |
| t_{RISE23} | Rise time, strong mode, Cload = 50 pF Ports 2 or 3 | $V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE23L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3 | $V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90% | 15 | – | 80 | ns |
| t_{RISE01} | Rise time, strong mode, Cload = 50 pF Ports 0 or 1 | $V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90% LDO enabled or disabled | 10 | – | 50 | ns |
| $t_{RISE01L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1 | $V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90% LDO enabled or disabled | 10 | – | 80 | ns |
| t_{FALL} | Fall time, strong mode, Cload = 50 pF all ports | $V_{DD} = 3.0\text{ to }3.6\text{ V}$, 10% to 90% | 10 | – | 50 | ns |
| t_{FALLL} | Fall time, strong mode low supply, Cload = 50 pF, all ports | $V_{DD} = 1.71\text{ to }3.0\text{ V}$, 10% to 90% | 10 | – | 70 | ns |

Figure 9. GPIO Timing Diagram



AC Comparator Specifications

Table 26 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC Low Power Comparator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------|---|--|-----|-----|-----|-------|
| t_{LPC} | Comparator response time, 50 mV overdrive | 50 mV overdrive does not include offset voltage. | – | – | 100 | ns |

AC External Clock Specifications

Table 27 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC External Clock Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------|---|------------|-------|-----|-------|-------|
| F_{OSCEXT} | Frequency (external oscillator frequency) | – | 0.75 | – | 25.20 | MHz |
| | High period | – | 20.60 | – | 5300 | ns |
| | Low period | – | 20.60 | – | – | ns |
| | Power-up IMO to switch | – | 150 | – | – | μs |

AC Programming Specifications

Figure 10. AC Waveform

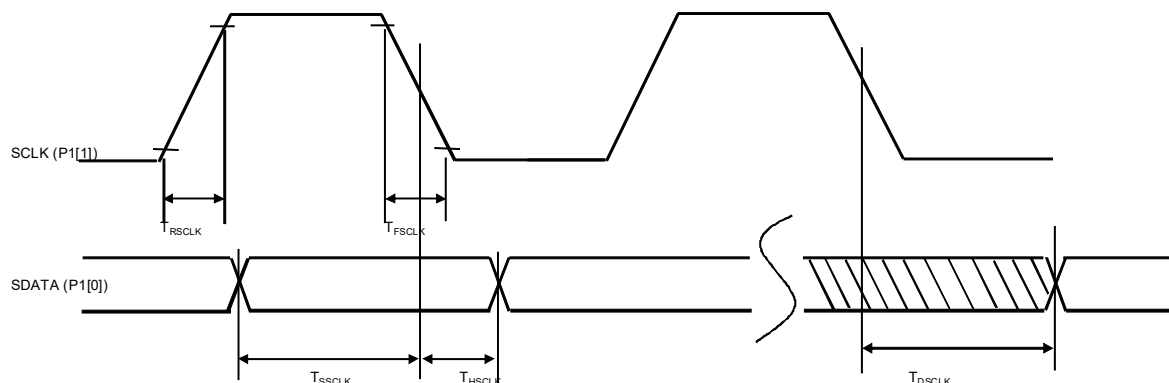


Table 28 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Programming Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------|---|---|-------|-----|-------|---------|
| t_{RSCLK} | Rise time of SCLK | — | 1 | — | 20 | ns |
| t_{FSCLK} | Fall time of SCLK | — | 1 | — | 20 | ns |
| t_{SSCLK} | Data setup time to falling edge of SCLK | — | 40 | — | — | ns |
| t_{HSCLK} | Data hold time from falling edge of SCLK | — | 40 | — | — | ns |
| F_{SCLK} | Frequency of SCLK | — | 0 | — | 8 | MHz |
| t_{ERASEB} | Flash erase time (block) | — | — | — | 18 | ms |
| t_{WRITE} | Flash block write time | — | — | — | 25 | ms |
| t_{DSCLK} | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | — | — | 60 | ns |
| t_{DSCLK3} | Data out delay from falling edge of SCLK | $3.0 \leq V_{DD} \leq 3.6$ | — | — | 85 | ns |
| t_{DSCLK2} | Data out delay from falling edge of SCLK | $1.71 \leq V_{DD} \leq 3.0$ | — | — | 130 | ns |
| t_{XRST3} | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | — | — | μs |
| t_{XRES} | XRES pulse length | — | 300 | — | — | μs |
| $t_{VDDWAIT}^{[54]}$ | V_{DD} stable to wait-and-poll hold off | — | 0.1 | — | 1 | ms |
| $t_{VDDXRES}^{[54]}$ | V_{DD} stable to XRES assertion delay | — | 14.27 | — | — | ms |
| t_{POLL} | SDAT high pulse time | — | 0.01 | — | 200 | ms |
| $t_{ACQ}^{[54]}$ | “Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks. | — | 3.20 | — | 19.60 | ms |
| $t_{XRESINI}^{[54]}$ | “Key window” time after an XRES event, based on 8 ILO clocks | — | 98 | — | 615 | μs |

Note

54. Valid from 5 to 50 °C. See the spec, [CY8C20X66](#), [CY8C20X46](#), [CY8C20X36](#), [CY7C643XX](#), [CY7C604XX](#), [CY8CTST2XX](#), [CY8CTMG2XX](#), [CY8C20X67](#), [CY8C20X47](#), [CY8C20X37](#), [Programming Spec](#) for more details.

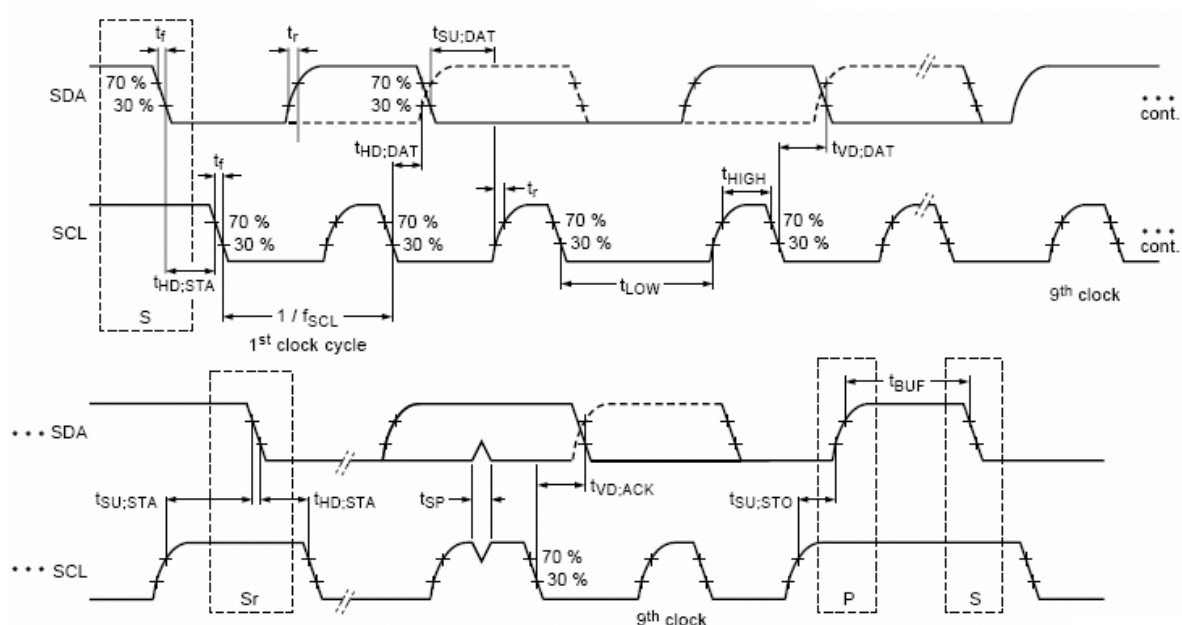
AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|-------------------------------------|---|---------------|------|---------------------|------|-------|
| | | Min | Max | Min | Max | |
| f _{SCL} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{HD;STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | μs |
| t _{LOW} | LOW period of the SCL clock | 4.7 | – | 1.3 | – | μs |
| t _{HIGH} | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | μs |
| t _{SU;STA} | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | μs |
| t _{HD;DAT} ^[55] | Data hold time | 20 | 3.45 | 20 | 0.90 | μs |
| t _{SU;DAT} | Data setup time | 250 | – | 100 ^[56] | – | ns |
| t _{SU;STO} | Setup time for STOP condition | 4.0 | – | 0.6 | – | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | μs |
| t _{SP} | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 38.

56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 30. SPI Master AC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|-------------------------|---|-----------|--------|--------|------------|
| F_{SCLK} | SCLK clock frequency | $V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$ | — — | — — | 6 3 | MHz MHz |
| DC | SCLK duty cycle | — | — | 50 | — | % |
| t_{SETUP} | MISO to SCLK setup time | $V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$ | 60 100 | — — | — — | ns ns |
| t_{HOLD} | SCLK to MISO hold time | — | 40 | — | — | ns |
| t_{OUT_VAL} | SCLK to MOSI valid time | — | — | — | 40 | ns |
| t_{OUT_H} | MOSI high time | — | 40 | — | — | ns |

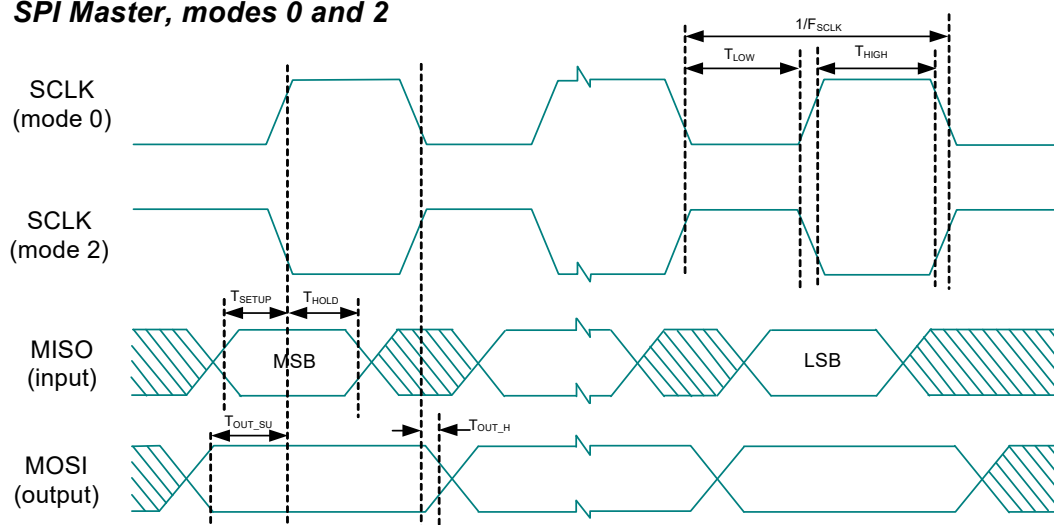
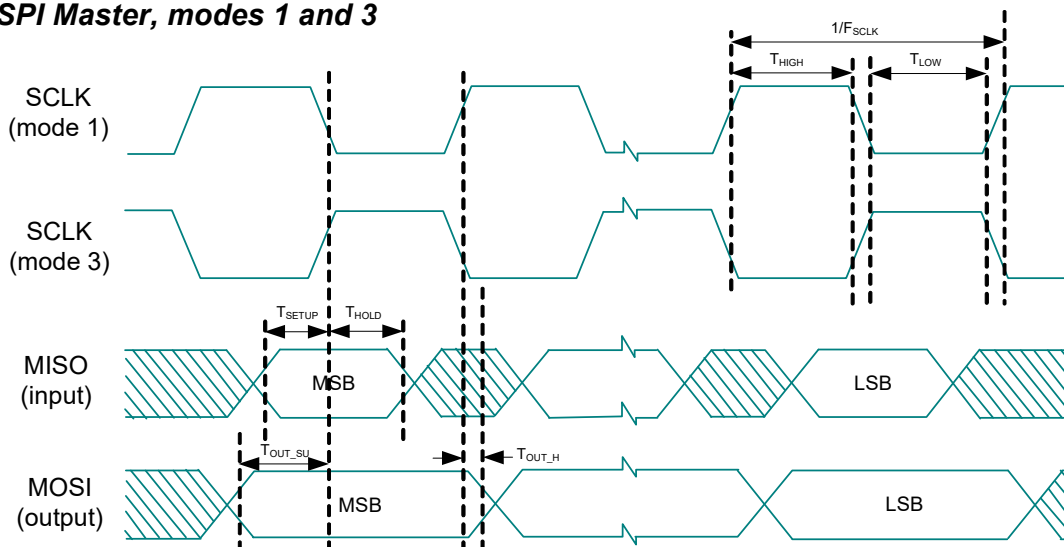
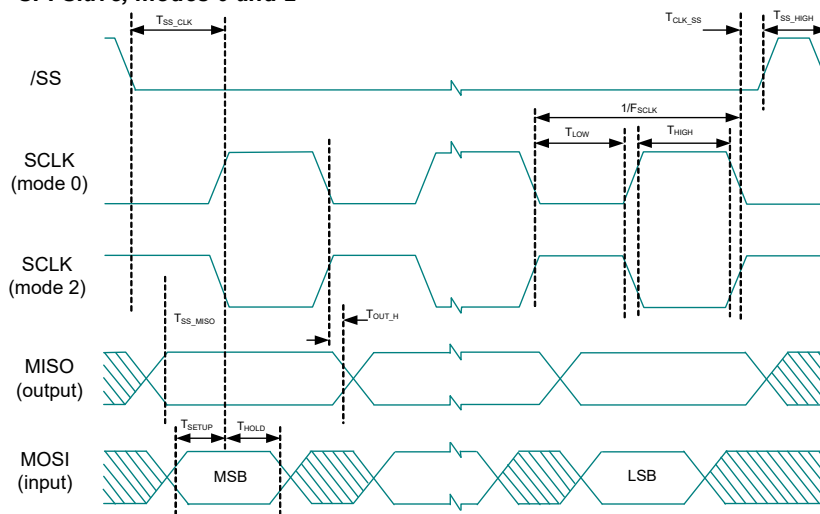
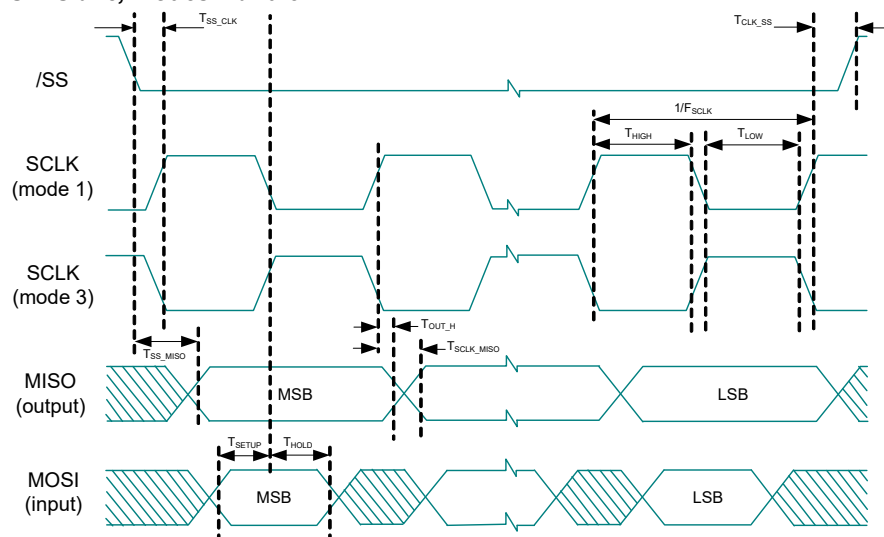
Figure 12. SPI Master Mode 0 and 2
SPI Master, modes 0 and 2

Figure 13. SPI Master Mode 1 and 3
SPI Master, modes 1 and 3


Table 31. SPI Slave AC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--------------------------------|------------|----------|-----|-----|-------|
| F_{SCLK} | SCLK clock frequency | — | — | — | 4 | MHz |
| t_{LOW} | SCLK low time | — | 42 | — | — | ns |
| t_{HIGH} | SCLK high time | — | 42 | — | — | ns |
| t_{SETUP} | MOSI to SCLK setup time | — | 30 | — | — | ns |
| t_{HOLD} | SCLK to MOSI hold time | — | 50 | — | — | ns |
| t_{SS_MISO} | SS high to MISO valid | — | — | — | 153 | ns |
| t_{SCLK_MISO} | SCLK to MISO valid | — | — | — | 125 | ns |
| t_{SS_HIGH} | SS high time | — | 50 | — | — | ns |
| t_{SS_CLK} | Time from SS low to first SCLK | — | $2/SCLK$ | — | — | ns |
| t_{CLK_SS} | Time from last SCLK to SS high | — | $2/SCLK$ | — | — | ns |

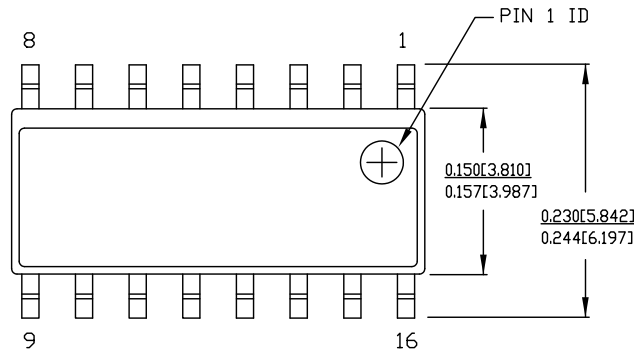
Figure 14. SPI Slave Mode 0 and 2
SPI Slave, modes 0 and 2

Figure 15. SPI Slave Mode 1 and 3
SPI Slave, modes 1 and 3


Packaging Information

This section illustrates the packaging specifications for the CY8C20x37/47/67 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Figure 16. 16-pin (150 Mil) SOIC



NOTE:

1. DIMENSIONS IN INCHES[MM] **MAX.**
2. REFERENCE JEDEC MS-012
3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

| PART # | |
|---------|----------------|
| S16.15 | STANDARD PKG. |
| SZ16.15 | LEAD FREE PKG. |

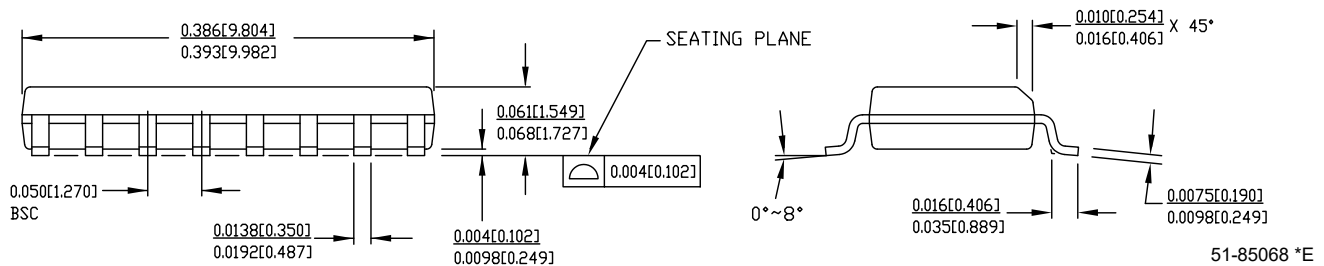
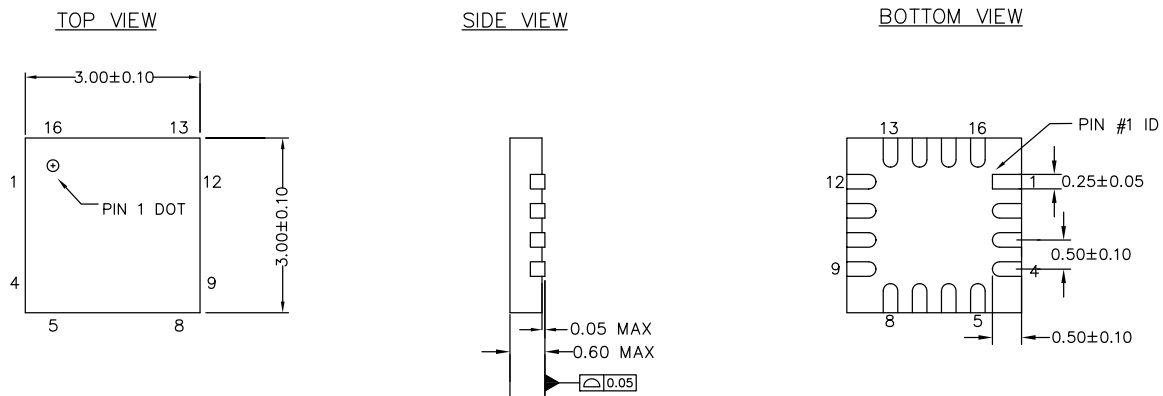


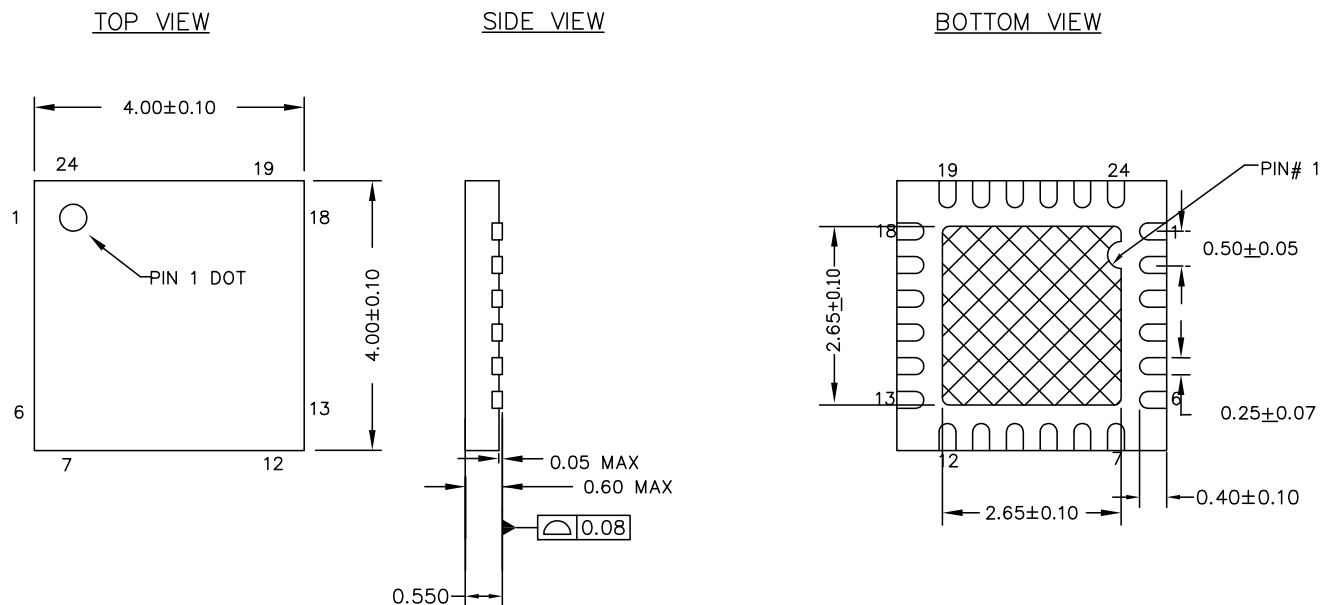
Figure 17. 16-pin Chip-On-Lead (3 x 3 x 0.6 mm) (Sawn) Package Outline, 001-09116




NOTES

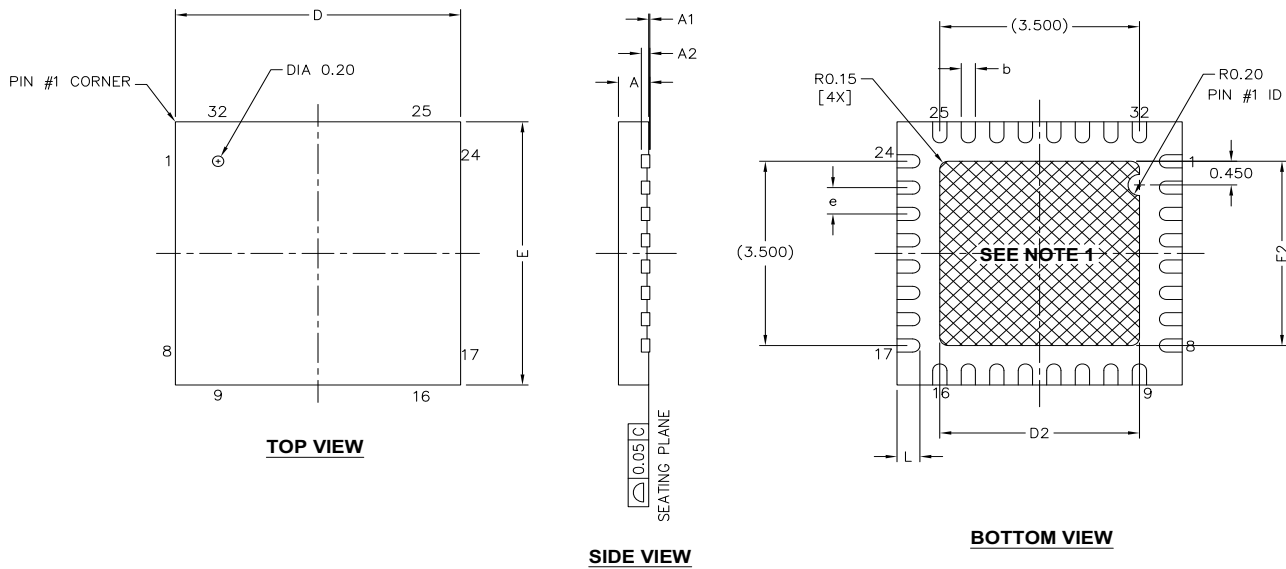
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 18. 24-Pin (4 × 4 × 0.6 mm) QFN

NOTES :


1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *G

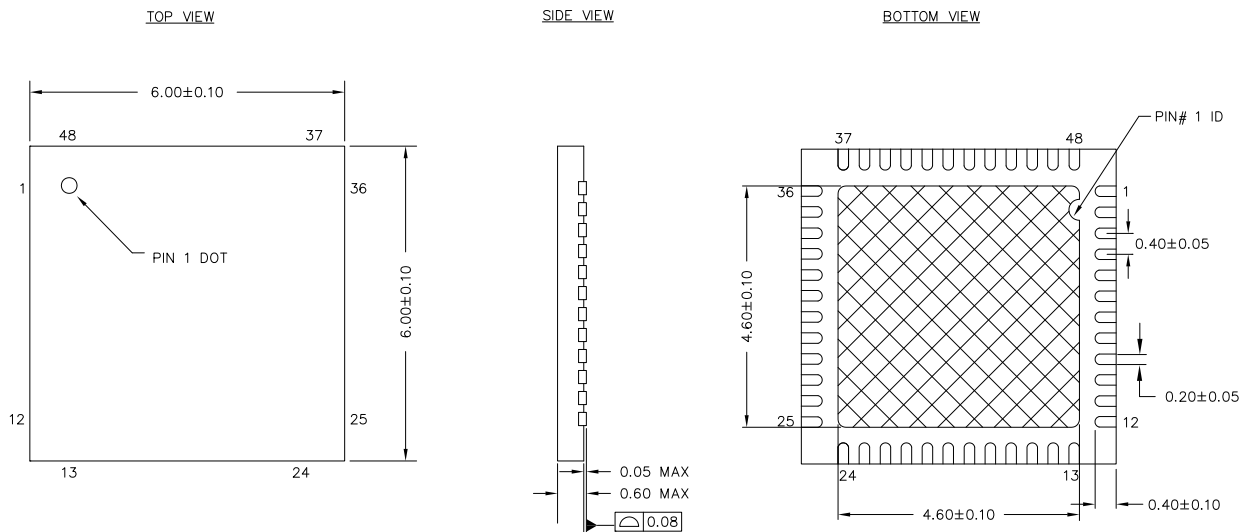
Figure 19. 32-Pin (5 × 5 × 0.6 mm) QFN



| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| A1 | - | 0.020 | 0.045 |
| A2 | 0.15 BSC | | |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.40 | 3.50 | 3.60 |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.25 | 0.30 |
| e | 0.50 TYP | | |

NOTES:

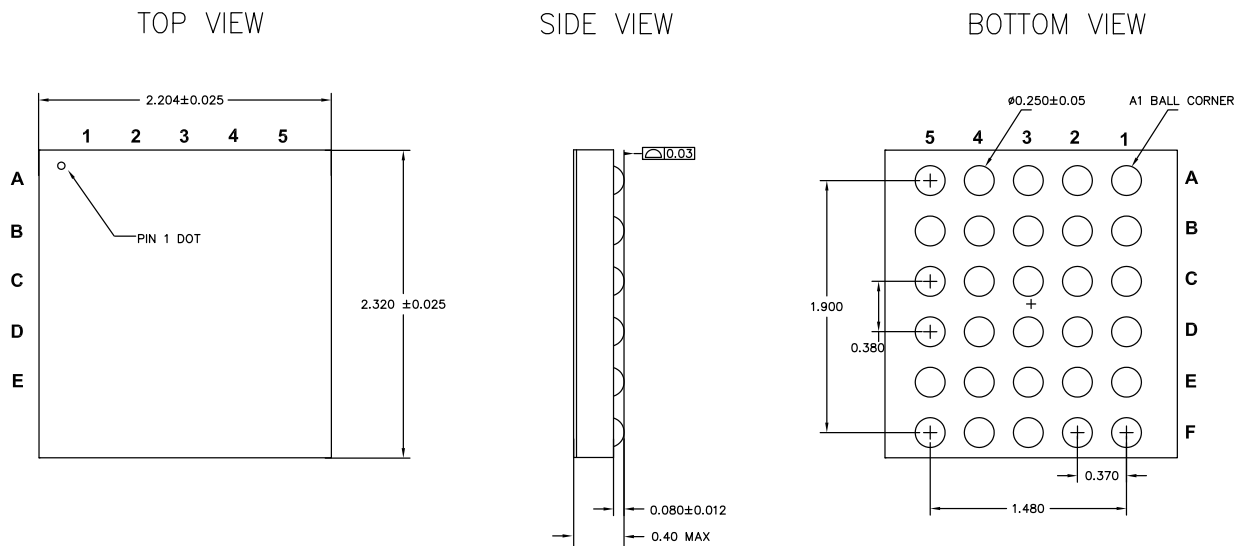
1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *F

Figure 20. 48-Pin (6 × 6 × 0.6 mm) QFN

NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Figure 21. 30-pin WLCSP


- Note: 1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETER
 3. BALL ARRAY IS NOT CENTERED WITH RESPECT TO DIE

001-50669 *D

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 32. Thermal Impedances per Package

| Package | Typical θ_{JA} ^[57] |
|----------------------------|---------------------------------------|
| 16-pin SOIC | 95 °C/W |
| 16-pin QFN | 33 °C/W |
| 24-pin QFN ^[58] | 21 °C/W |
| 32-pin QFN ^[58] | 20 °C/W |
| 48-pin QFN ^[58] | 18 °C/W |
| 30-ball WLCSP | 54 °C/W |

Capacitance on Crystal Pins

Table 33. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|------------|---------------------|
| 32-Pin QFN | 3.2 pF |
| 48-Pin QFN | 3.3 pF |

Solder Reflow Peak Temperature

Table 34 shows the solder reflow temperature limits that must not be exceeded.

Table 34. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5$ °C |
|---------------|------------------------------------|---------------------------------|
| 16-pin SOIC | 260 °C | 30 seconds |
| 16-pin QFN | 260 °C | 30 seconds |
| 24-pin QFN | 260 °C | 30 seconds |
| 32-pin QFN | 260 °C | 30 seconds |
| 48-pin QFN | 260 °C | 30 seconds |
| 30-ball WLCSP | 260 °C | 30 seconds |

Notes

57. $T_J = T_A + \text{Power} \times \theta_{JA}$.

58. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at

<http://www.cypress.com/psocdesigner> and includes a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube in-circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at

<http://www.cypress.com/psocprogrammer>.

Development Kits

All development kits are sold at the [Cypress Online Store](#).

Evaluation Tools

All evaluation tools are sold at the [Cypress Online Store](#).

CY3210-MiniProg1

The **CY3210-MiniProg1 kit** allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The **CY3210-PSoCEval1 kit** features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers are purchased from the [Cypress Online Store](#).

CY3216 Modular Programmer

The [CY3216 Modular Programmer kit](#) features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

CY3207ISSP In-System Serial Programmer (ISSP)

The [CY3207ISSP](#) is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Ordering Information

Table 35 lists the CY8C20x37/47/67/S PSoC devices' key package features and ordering codes.

Table 35. PSoC Device Key Features and Ordering Information

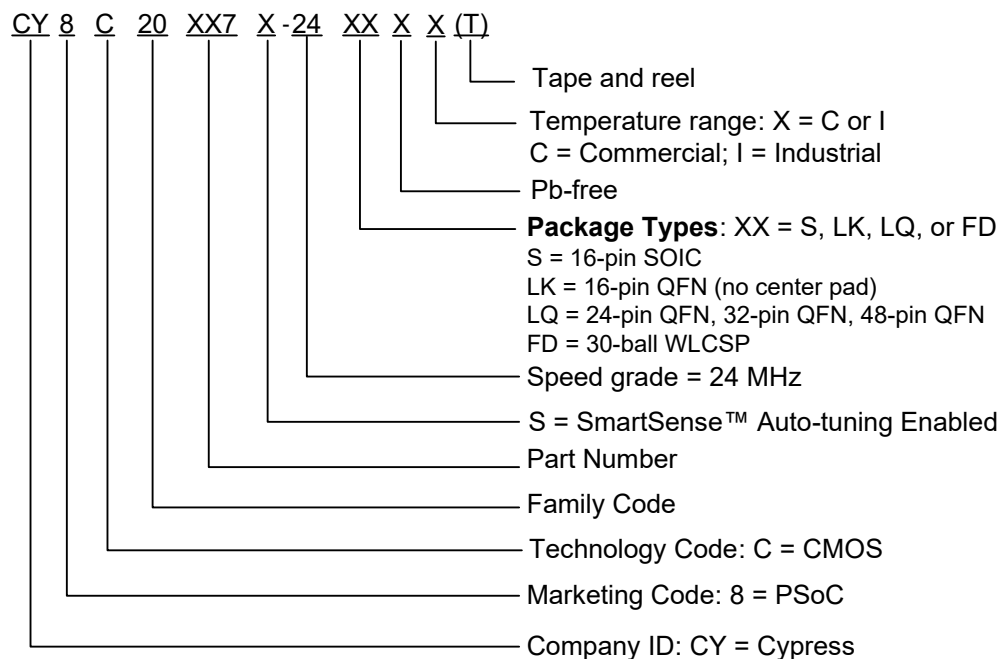
| Ordering Code | Package | Flash (Bytes) | SRAM (Bytes) | CapSense Sensors | Digital I/O Pins | Analog Inputs ^[59] | XRES Pin | ADC |
|--------------------|----------------------------|---------------|--------------|------------------|------------------|-------------------------------|----------|-----|
| CY8C20237-24SXI | 16-pin SOIC | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24SXI | 16-pin SOIC | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXI | 16-pin QFN | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20237-24LKXIT | 16-pin QFN (Tape and Reel) | 8 K | 1 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXI | 16-pin QFN | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20247S-24LKXIT | 16-pin QFN (Tape and Reel) | 16 K | 2 K | 10 | 13 | 13 | Yes | Yes |
| CY8C20337-24LQXI | 24-pin QFN | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20337-24LQXIT | 24-pin QFN (Tape and Reel) | 8 K | 1 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXI | 24-pin QFN | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20347S-24LQXIT | 24-pin QFN (Tape and Reel) | 16 K | 2 K | 16 | 19 | 19 | Yes | Yes |
| CY8C20437-24LQXI | 32-pin QFN | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20437-24LQXIT | 32-pin QFN (Tape and Reel) | 8 K | 1 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXI | 32-pin QFN | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20447S-24LQXIT | 32-pin QFN (Tape and Reel) | 16 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXI | 32-pin QFN | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20467S-24LQXIT | 32-pin QFN (Tape and Reel) | 32 K | 2 K | 25 | 28 | 28 | Yes | Yes |
| CY8C20637-24LQXI | 48-pin QFN | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20637-24LQXIT | 48-pin QFN (Tape and Reel) | 8 K | 1 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXI | 48-pin QFN | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20647S-24LQXIT | 48-pin QFN (Tape and Reel) | 16 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXI | 48-pin QFN | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |
| CY8C20667S-24LQXIT | 48-pin QFN (Tape and Reel) | 32 K | 2 K | 31 | 34 | 34 | Yes | Yes |

Note

⁵⁹. Dual-function Digital I/O Pins also connect to the common analog mux.

Table 35. PSoC Device Key Features and Ordering Information *(continued)*

| Ordering Code | Package | Flash (Bytes) | SRAM (Bytes) | CapSense Sensors | Digital I/O Pins | Analog Inputs ^[59] | XRES Pin | ADC |
|-------------------|------------------------------|---------------|--------------|------------------|------------------|-------------------------------|----------|-----|
| CY8C20767-24FDXC | 30-pin WLCSP | 32 K | 2 K | 24 | 27 | 27 | Yes | Yes |
| CY8C20767-24FDXCT | 30-pin WLCSP (Tape and Reel) | 32 K | 2 K | 24 | 27 | 27 | Yes | Yes |

Ordering Code Definitions


Acronyms

The following table lists the acronyms that are used in this document.

Table 36. Acronyms Used in this Document

| Acronym | Description |
|------------------|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| ESD | electrostatic discharge |
| FSR | full scale range |
| GPIO | general purpose input/output |
| I ² C | inter-integrated circuit |
| ICE | in-circuit emulator |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LED | light-emitting diode |
| LPC | low power comparator |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | million instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debug |
| PCB | printed circuit board |
| POR | power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC | programmable system-on-chip |
| QFN | quad flat no-lead |
| SCLK | serial I ² C clock |
| SDA | serial I ² C data |
| SDATA | serial ISSP data |
| SOIC | small outline integrated circuit |
| SPI | serial peripheral interface |
| SRAM | static random access memory |
| SS | slave select |
| USB | universal serial bus |
| WLCSP | wafer level chip scale package |

Reference Documents

- *Technical reference manual for CY20xx7 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx7*
- *Host Sourced Serial Programming for 20xx7 devices*

Document Conventions

Units of Measure

Table 37 lists all the abbreviations used to measure the PSoC devices.

Table 37. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------------|
| °C | degree Celsius |
| dB | decibel |
| kHz | kilohertz |
| ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Glossary

| | |
|-------------------------------------|---|
| Crosspoint connection | Connection between any GPIO combination via analog multiplexer bus. |
| Differential non linearity | Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. |
| Hold time | Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct. |
| I ² C | It is a serial multi-master bus used to connect low speed peripherals to MCU. |
| Integral nonlinearity | It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level. |
| Latch-up current | Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree Celsius) |
| Power supply rejection ratio (PSRR) | The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device. |
| Scan | The conversion of all sensor capacitances to digital values. |
| Setup time | Period required to prepare a device, machine, process, or system for it to be ready to function. |
| Signal-to-noise ratio | The ratio between a capacitive finger signal and system noise. |
| SPI | Serial peripheral interface is a synchronous serial data link standard. |

Errata

This section describes the errata for the CY8C20xx7/S family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY8C20xx7/S Qualification Status

Product Status: Production released.

CY8C20xx7/S Errata Summary

The following Errata items apply to the CY8C20xx7/S datasheet 001-69257.

1. DoubleTimer0 ISR

■Problem Definition

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0, B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■Scope of Impact

The ISR may be executed twice.

■Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as `“and reg[B0h], FDh”`

■Fix Status

Will not be fixed

■Changes

None

2. Missed GPIO Interrupt

■Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■Parameters Affected

No datasheet parameters are affected.

■Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■Scope of Impact

The GPIO interrupt service routine will not be run.

■Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt. Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0. Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■Fix Status

Will not be fixed

■Changes

None

3. Missed Interrupt During Transition to Sleep

■ Problem Definition

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling sleep mode just prior to an interrupt.

■ Scope of Impact

The relevant interrupt service routine will not be run.

■ Workaround

None.

■ Fix Status

Will not be fixed

■ Changes

None

4. Wakeup from sleep with analog interrupt

■ Problem Definition

Device wakes up from sleep when an analog interrupt is trigger

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ Scope of Impact

Device unexpectedly wakes up from sleep

■ Workaround

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

■ Fix Status

Will not be fixed

■ Changes

None

5. Wake-up from Sleep with Hardware I2C Address match on Pins P1[0], P1[1]

■ Problem Definition

I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL, to wake-up from sleep using I2C hardware address match event.

■ Parameters Affected

$t_{HD;DAT}$ increased to 20 ns from 0 ns

■ Trigger Condition(S)

This is an issue only when all these three conditions are met:

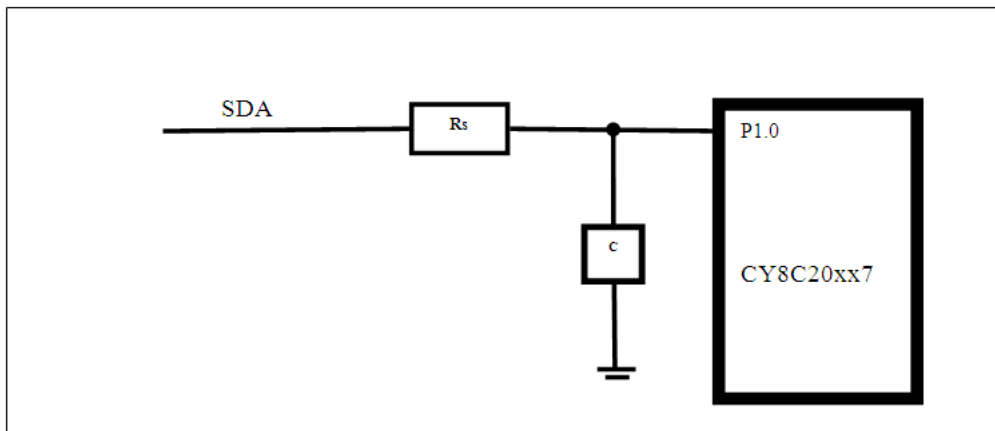
- 1) P1.0 and P1.1 are used as I2C pins,
- 2) Wakeup from sleep with hardware address match feature is enabled, and
- 3) I2C master does not provide 20 ns hold time on SDA with respect to falling edge of SCL.

■ Scope of Impact

These trigger conditions cause the device to never wake-up from sleep based on I2C address match event.

■ Workaround

For a design that meets all of the trigger conditions, the following suggested circuit has to be implemented as a work-around. The R and C values proposed are 100 ohm and 200 pF respectively.



■ Fix Status

Will not be fixed

■ Changes

None

6. I2C Port Pin Pull-up Supply Voltage

■Problem Definition

Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C20xx7/S V_{DD} .

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when the I2C master is powered at a higher voltage than CY8C20xx7/S.

■Scope of Impact

This trigger condition will corrupt the I2C communication between the I2C host and the CY8C20xx7/S CapSense controller.

■Workaround

I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C20xx7/S supply voltage.

■Fix Status

Will not be fixed

■Changes

None

7. Port1 Pin Voltage

■Problem Definition

Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S V_{DD} .

■Parameters Affected

None.

■Trigger Condition(S)

This problem occurs only when port1 pins are at voltage 0.7 V higher than V_{DD} of CY8C20xx7/S.

■Scope of Impact

This trigger condition will not allow CY8C20xx7/S to drive the output signal on port1 pins, input path is unaffected by this condition.

■Workaround

Port1 should not be connected to a higher voltage than V_{DD} of CY8C20xx7/S.

■Fix Status

Will not be fixed

■Changes

None

Document History Page

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257 | | | | |
|---|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 3276782 | DST | 06/27/2011 | New silicon and document |
| *A | 3327230 | DST | 07/28/2011 | Changed 48-pin dimensions to 6 × 6 × 0.6 mm QFN Updated pins name in Table 3 on page 9 and removed USB column and updated dimensions for 48-pin parts in Table 35 on page 34 Updated Figure 20 on page 30 Removed ICE and Debugger sections. Removed CY3215 Development Kit and CY3280-20x66 UCC sections. Updated Ordering Information . |
| *B | 3403111 | YVA | 10/12/2011 | Moved status from Advance to Preliminary. Updated Ordering Information Removed the row named “48-Pin (6 × 6 mm) QFN (OCD)”. Changed all 48-pin ordering code column from CY8C20XXX-24LTxx to CY8C20XXX-24LQxx. Updated 16-pin SOIC and 16-pin QFN package drawings. |
| *C | 3473317 | DST | 12/23/2011 | Updated Features . Updated Pinouts (Removed PSoC in captions of Figure 2 , Figure 3 , Figure 4 , Figure 6 , and Figure 7). Updated DC Chip-Level Specifications under Electrical Specifications (Updated typical value of I _{DD24} parameter from 3.32 mA to 2.88 mA, updated typical value of I _{DD12} parameter from 1.86 mA to 1.71 mA, updated typical value of I _{DD6} parameter from 1.13 mA to 1.16 mA, updated maximum value of I _{SB0} parameter from 0.50 µA to 1.1 µA, added I _{SB12C} parameter and its details). Updated DC GPIO Specifications under Electrical Specifications (Added the parameters namely V _{ILLVT3.3} , V _{IHLVT3.3} , V _{ILLVT5.5} , V _{IHLVT5.5} and their details in Table 10 , added the parameters namely V _{ILLVT2.5} , V _{IHLVT2.5} and their details in Table 11). Added the following sections namely DC I2C Specifications , Shield Driver DC Specifications , and DC IDAC Specifications under Electrical Specifications . Updated AC Chip-Level Specifications (Added the parameter namely t _{JIT_IMO} and its details). Updated Ordering Information (updated Table 35). |
| *D | 3510277 | YVA/DST | 02/16/2012 | Added CY8C20x37/37S/47/47S/67/67S part numbers and changed title to “1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders” Updated Features . Modified comparator blocks in Logic Block Diagram . Replaced SmartSense with SmartSense auto-tuning. Added CY8C20xx7S part numbers in Pin Definitions. Added footnote for Table 20 . Updated Table 21 and Table 22 and added Table 23 . Updated F _{32K1} min value. Updated data hold time min values. Updated CY8C206x7 part information in Table “Emulation and Programming Accessories”. Updated Ordering Information . |
| *E | 3539259 | DST | 03/01/2012 | Changed Datasheet status from Preliminary to Final. Updated all Pinouts to include Driven Shield Output (optional) information. Updated Min value for V _{LPC} Table 15 . Updated Offset and Input range in Table 16 . |

Document History Page (continued)

| Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257 | | | | |
|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *F | 3645807 | DST/BVI | 07/03/2012 | Updated F_{SCLK} parameter in the Table 31, "SPI Slave AC Specifications," on page 26 Changed t_{OUT_HIGH} to t_{OUT_H} in Table 30, "SPI Master AC Specifications," on page 25 Updated Features section, "Programmable pin configurations" bullet: <ul style="list-style-type: none"> ■ Included the following sub-bullet point - 5 mA source current on port 0 and 1 and 1 mA on port 2,3 and 4 ■ Changed the bullet point "High sink current of 25 mA for each GPIO" to "High sink current of 25 mA for each GPIO. Total 120 mA maximum sink current per chip" ■ Added "QuietZone™ Controller" bullet and updated "Low power CapSense® block with SmartSense™ auto-tuning" bullet. Updated package diagrams 001-13937 to *D and 001-57280 to *C revisions. |
| *G | 3800055 | DST | 11/23/2012 | Changed document title. Part named changed from CY8C20xx7 to CY8C20xx7/S Table 20: Update to VIH2C to match Item #6 in K2 Si Errata document (001-75370) Updated package diagrams: 51-85068 to *E 001-09116 to *G 001-13937 to *E 001-42168 to *E 001-57280 to *E |
| *H | 3881332 | SRLI | 02/04/2013 | Updated Features : Added Note "Please contact your nearest sales office for additional details." and referred the same note in "24 Sensing Inputs – 30-pin WLCSP". |
| *I | 3993458 | DST | 05/07/2013 | Updated Electrical Specifications (Updated DC GPIO Specifications (Updated heading of third column as "Port 0/1 per I/O (max)" for Table 13)). Updated Packaging Information : spec 001-09116 – Changed revision from *G to *H (Figure 17). Added Errata . |
| *J | 4081796 | DST | 07/31/2013 | Added Errata footnotes (Note 40, 41, 42, 43, 44). Updated already existing footnotes (Note 50, 51, 55) as Errata footnotes. Updated Electrical Specifications : Updated DC Chip-Level Specifications : Added Note 40, 41, 42, 43 and referred the same notes in I_{SB0} , I_{SB1} , I_{SB12C} parameters. Updated DC GPIO Specifications : Added Note 44 and referred the same note in description of $V_{ILLVT3.3}$ parameter in Table 10 . Updated DC I2C Specifications : Updated Note 50, 51 referred in Table 20 . Updated AC I2C Specifications : Updated Note 55 referred in Table 29 . Updated to new template. |

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|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *K | 4248645 | DST | 01/16/2014 | Updated Pinouts : Updated 32-pin QFN (25 Sensing Inputs)[25] : Updated Figure 6 . Updated Packaging Information : spec 001-09116 – Changed revision from *H to *I. |
| *L | 4404150 | SLAN | 06/10/2014 | Updated Pinouts : Updated 16-pin SOIC (10 Sensing Inputs) : Updated Table 1 : Added Note 6 and referred the same note in description of XRES pin. Updated 16-pin QFN (10 Sensing Inputs)[8] : Updated Table 2 : Added Note 12 and referred the same note in description of XRES pin. Updated 24-pin QFN (16 Sensing Inputs)[14] : Updated Table 3 : Added Note 18 and referred the same note in description of XRES pin. Updated 30-ball WLCSP (24 Sensing Inputs) : Updated Table 4 : Added Note 21 and referred the same note in description of XRES pin. Updated 32-pin QFN (25 Sensing Inputs)[25] : Updated Table 5 : Added Note 29 and referred the same note in description of XRES pin. Updated 48-pin QFN (31 Sensing Inputs)[31] : Updated Table 6 : Added Note 35 and referred the same note in description of XRES pin. Updated Electrical Specifications : Updated DC GPIO Specifications : Updated Table 10 : Updated minimum and maximum values of V_{IH} parameter. Updated Table 11 : Updated minimum and maximum values of V_{IH} parameter. Updated AC Chip-Level Specifications : Updated Table 24 : Removed minimum and maximum values of “ILO untrimmed frequency”. Updated Packaging Information : spec 001-09116 – Changed revision from *I to *J. Completing Sunset Review. |
| *M | 4825924 | SLAN | 07/07/2015 | Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6). Updated Packaging Information : spec 001-13937 – Changed revision from *E to *F. Updated to new template. |
| *N | 5068999 | ARVI | 12/31/2015 | Updated hyperlink of “Technical Reference Manual” in all instances across the document. Updated PSoC® Functional Overview : Updated Additional System Resources : Updated description. Updated Development Tool Selection : Removed “Accessories (Emulation and Programming)”. Removed “Build a PSoC Emulator into Your Board”. |

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|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *O | 5122184 | JFMD | 02/02/2016 | Updated Features : Removed Note "Please contact your nearest sales office for additional details." and its reference. Updated Ordering Information : Updated Table 35 : Updated part numbers. |
| *P | 5742810 | AESATMP9 | 05/19/2017 | Updated logo and copyright. |
| *Q | 6171969 | PRIA | 05/11/2018 | Added Figure 21. 30-pin WLCSP on page 30 . Added information about pull-down resistance value on pins P1[0] and P1[1] in notes 10 , 16 , 22 , 27 and 33 . Corrected typographical error in Table 22 and Table 23 . Updated Figure 18. 24-Pin (4 × 4 × 0.6 mm) QFN: 001-13937 *F to *G and Figure 19. 32-Pin (5 × 5 × 0.6 mm) QFN: 001-42168 *E to *F. |

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