

4-Mbit (512K words × 8 bit) Static RAM

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active and standby currents
 - Active current: $I_{CC} = 38 \text{ mA}$ typical
 - Standby current: $I_{SB2} = 6 \text{ mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 36-pin SOJ and 44-pin TSOP II packages

Functional Description

CY7C1049GN is a high-performance CMOS fast static RAM device organized as 512K words by 8-bits.

Data writes are performed by asserting the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW, while providing the data on I/O₀ through I/O₇ and address on A₀ through A₁₈ pins.

Data reads are performed by asserting the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₇).

All I/Os (I/O₀ through I/O₇) are placed in a high-impedance state during the following events:

- The device is deselected (\overline{CE} HIGH)
- The control signal \overline{OE} is de-asserted

The logic block diagram is on page 2.

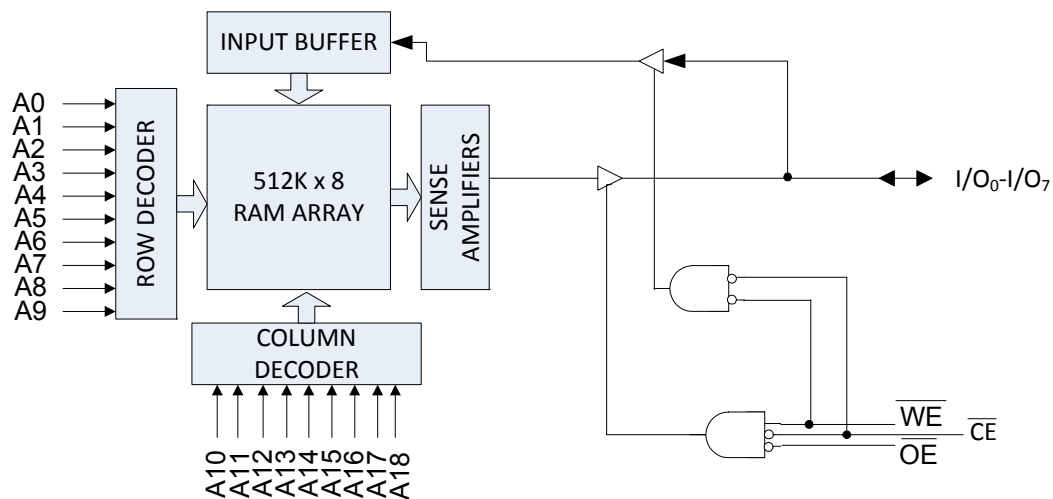
Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns) 10/15	Power Dissipation			
				Operating I _{CC} , (mA)		Standby, I _{SB2} (mA)	
				f = f _{max}			
				Typ ^[1]	Max	Typ ^[1]	Max
CY7C1049GN18	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1049GN30		2.2 V–3.6 V	10	38	45		
CY7C1049GN		4.5 V–5.5 V	10	38	45		

Notes

1. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1049GN

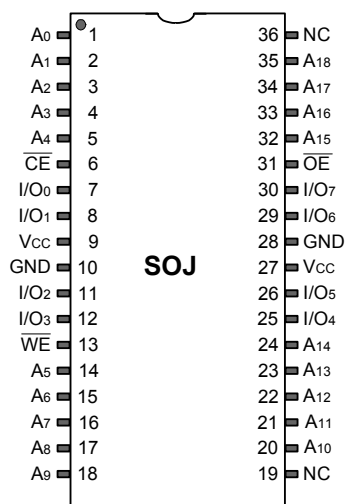


Contents

Pin Configurations	4	Package Diagrams	15
Maximum Ratings	6	Acronyms	16
Operating Range	6	Document Conventions	16
DC Electrical Characteristics	6	Units of Measure	16
Capacitance	7	Document History Page	17
Thermal Resistance	7	Sales, Solutions, and Legal Information	18
AC Test Loads and Waveforms	7	Worldwide Sales and Design Support	18
Data Retention Characteristics	8	Products	18
Data Retention Waveform	8	PSoC® Solutions	18
AC Switching Characteristics	9	Cypress Developer Community	18
Switching Waveforms	10	Technical Support	18
Truth Table	13		
Ordering Information	14		
Ordering Code Definitions	14		

Pin Configurations

Figure 1. 36-pin SOJ pinout ^[2]

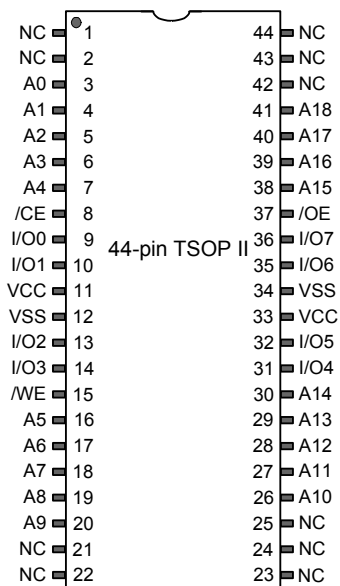


Note

2. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 2. 44-pin TSOP II pinout, Single Chip Enable ^[3]



Notes

- NC pins are not connected internally to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature –65 °C to +150 °C

Ambient temperature
with power applied –55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND ^[4] –0.5 to $V_{CC} + 0.5$ V

DC voltage applied to outputs
in HI-Z State ^[4] –0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[4] –0.5 V to $V_{CC} + 0.5$ V

Current into outputs (in LOW state) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	–	–	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2	–	–	
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	–	–	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	–	–	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5$ ^[6]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	–	–	0.2	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	–	–	0.4	
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	–	–	0.4	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V –	1.4	–	$V_{CC} + 0.2$ ^[4]	V
		2.2 V to 2.7 V –	2	–	$V_{CC} + 0.3$ ^[4]	
		2.7 V to 3.6 V –	2	–	$V_{CC} + 0.3$ ^[4]	
		4.5 V to 5.5 V –	2.2	–	$V_{CC} + 0.5$ ^[4]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V –	–0.2 ^[4]	–	0.4	V
		2.2 V to 2.7 V –	–0.3 ^[4]	–	0.6	
		2.7 V to 3.6 V –	–0.3 ^[4]	–	0.8	
		4.5 V to 5.5 V –	–0.5 ^[4]	–	0.8	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	–1	–	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	–1	–	+1	μA
I_{CC}	Operating supply current	Max V_{CC} , $I_{OUT} = 0 \text{ mA}$, CMOS levels	–	38	45	mA
		$f = 100 \text{ MHz}$		–	40	
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$	–	6	8	mA

Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 2 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V – 2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V – 3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V – 5.5 V), $T_A = 25 \text{ °C}$.
- This parameter is guaranteed by design and not tested.

Capacitance

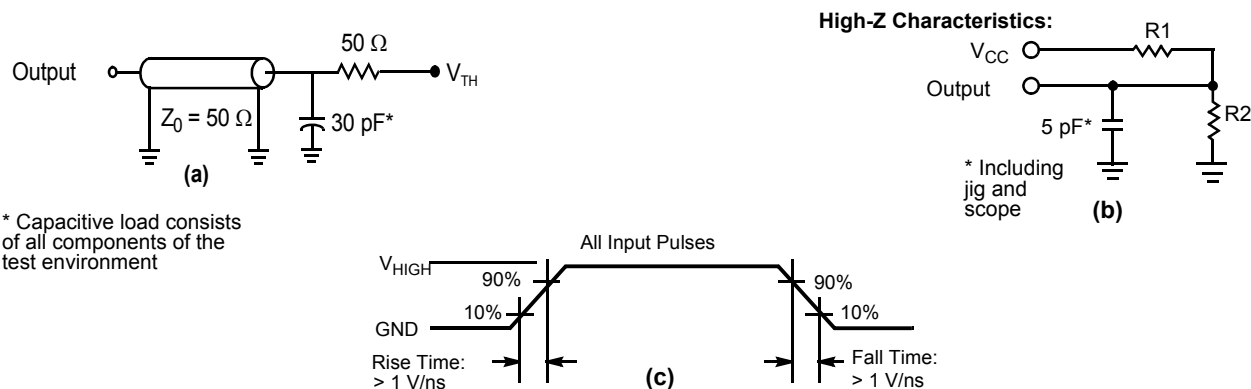
Parameter ^[7]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter ^[7]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	59.52	68.85	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		31.48	15.97	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[8]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a 100- μs ramp time from 0 to $V_{CC}(\text{min})$ and a 100- μs wait time after V_{CC} stabilization.

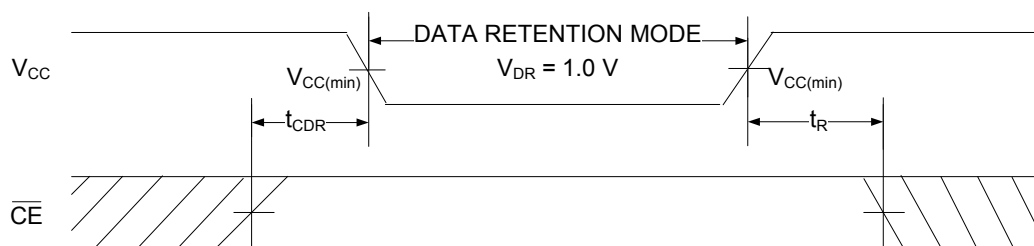
Data Retention Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	V
I_{CCDR}	Data retention current	$V_{CC} = 1.2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}^{[9]}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$, or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}^{[10]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[9, 10]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	–	ns
		$V_{CC} < 2.2\text{ V}$	15	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform ^[9]



Notes

9. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

10. These parameters are guaranteed by design.

AC Switching Characteristics

Over the operating range of -40°C to 85°C

Parameter ^[11]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read cycle time	10	–	15	–	ns
t _{AA}	Address to data	–	10	–	15	ns
t _{OHA}	Data / ERR hold from address change	3	–	3	–	ns
t _{ACE}	\overline{CE} LOW to data	–	10	–	15	ns
t _{DOE}	\overline{OE} LOW to data	–	4.5	–	8	ns
t _{LZOE}	\overline{OE} LOW to low impedance ^[12]	0	–	0	–	ns
t _{HZOE}	\overline{OE} HIGH to HI-Z ^[12]	–	5	–	8	ns
t _{LZCE}	\overline{CE} LOW to low impedance ^[12]	3	–	3	–	ns
t _{HZCE}	\overline{CE} HIGH to HI-Z ^[12]	–	5	–	8	ns
t _{PU}	\overline{CE} LOW to power-up ^[13, 14]	0	–	0	–	ns
t _{PD}	\overline{CE} HIGH to power-down ^[13, 14]	–	10	–	15	ns
Write Cycle ^[14, 15]						
t _{WC}	Write cycle time	10	–	15	–	ns
t _{SCE}	\overline{CE} LOW to write end	7	–	12	–	ns
t _{AW}	Address setup to write end	7	–	12	–	ns
t _{HA}	Address hold from write end	0	–	0	–	ns
t _{SA}	Address setup to write start	0	–	0	–	ns
t _{PWE}	\overline{WE} pulse width	7	–	12	–	ns
t _{SD}	Data setup to write end	5	–	8	–	ns
t _{HD}	Data hold from write end	0	–	0	–	ns
t _{LZWE}	\overline{WE} HIGH to low impedance ^[12]	3	–	3	–	ns
t _{HZWE}	\overline{WE} LOW to HI-Z ^[12]	–	5	–	8	ns

Notes

- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3\text{ V}$) and $V_{CC}/2$ (for $V_{CC} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{CC} < 3\text{ V}$). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 3 on page 7, unless specified otherwise.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{LZOE} , t_{LZCE} , and t_{LZWE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 7. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle pulse width in Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{DS} and t_{HZWE} .

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [16, 17]

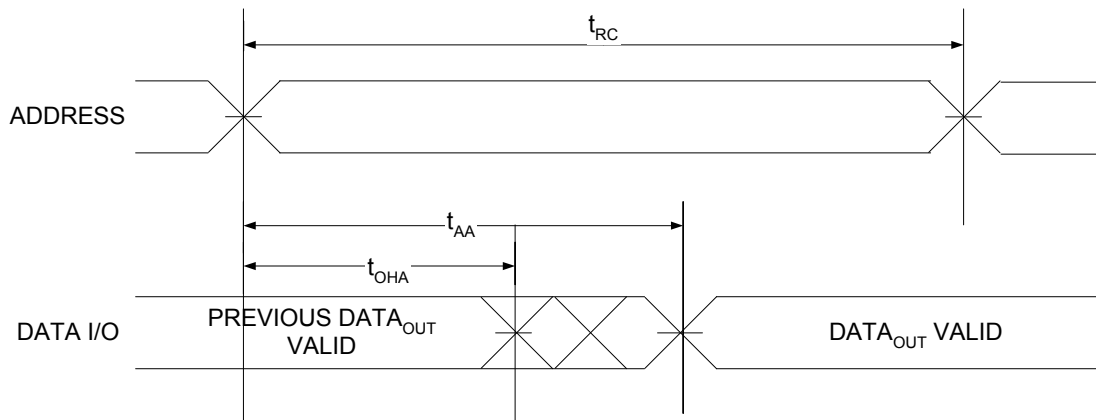
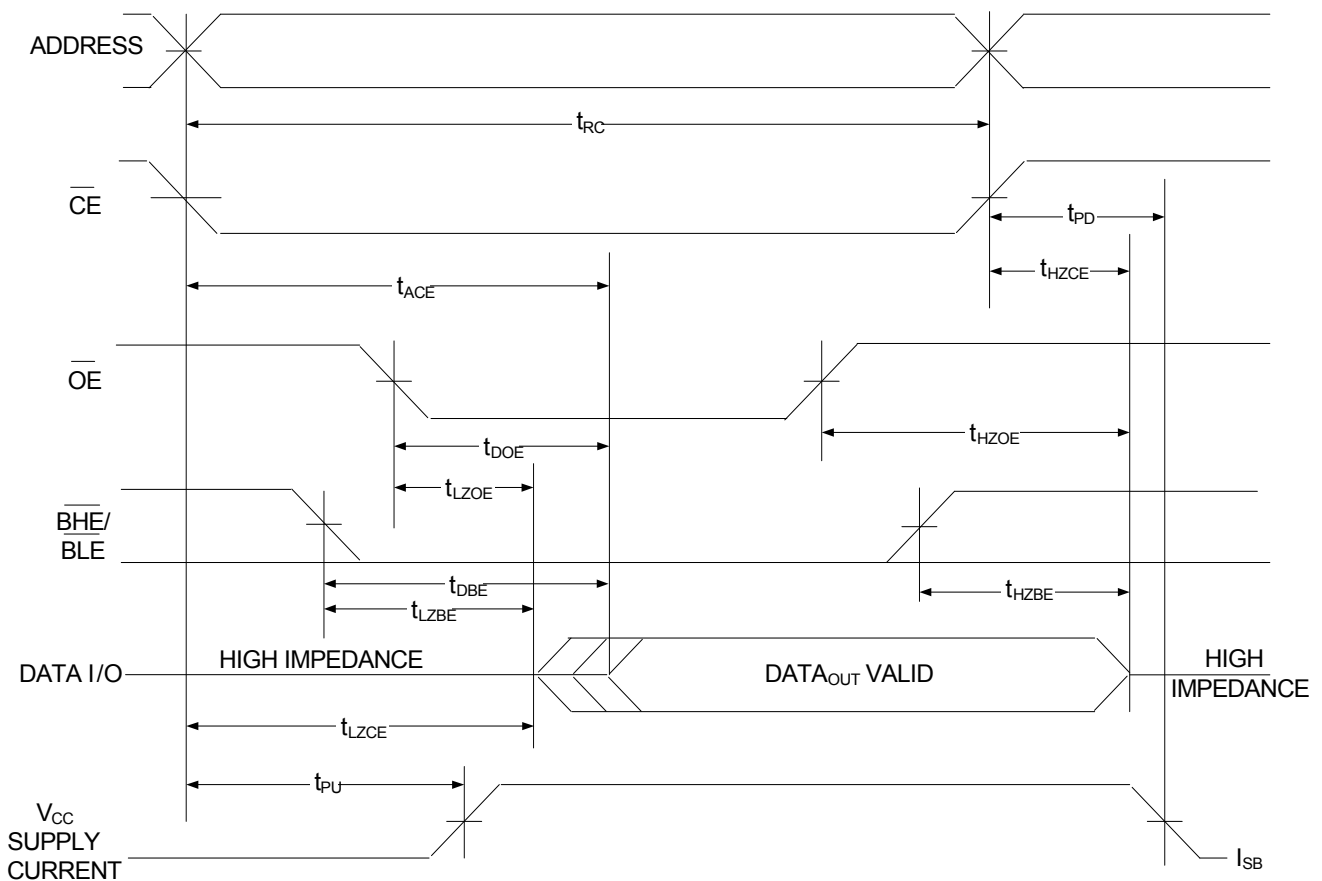


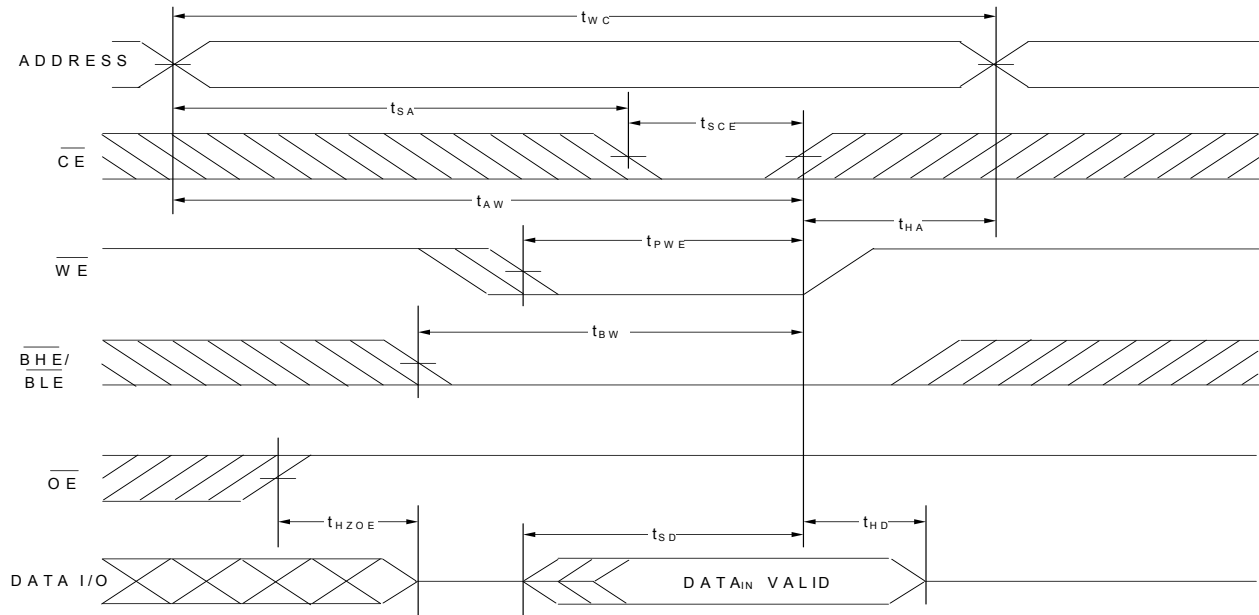
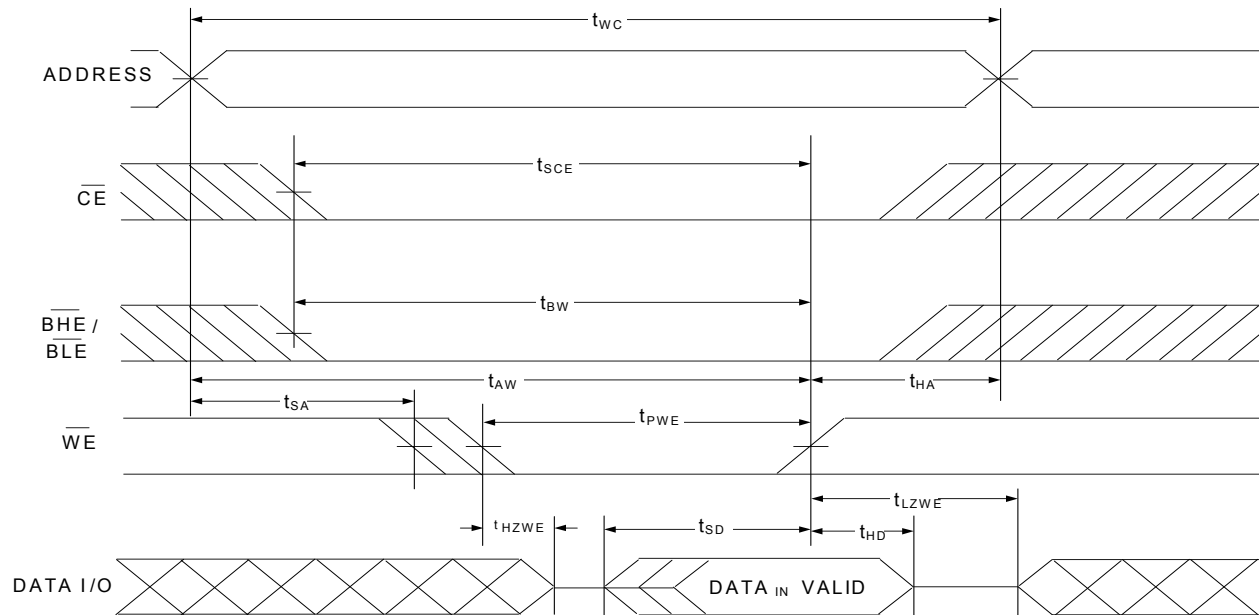
Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]



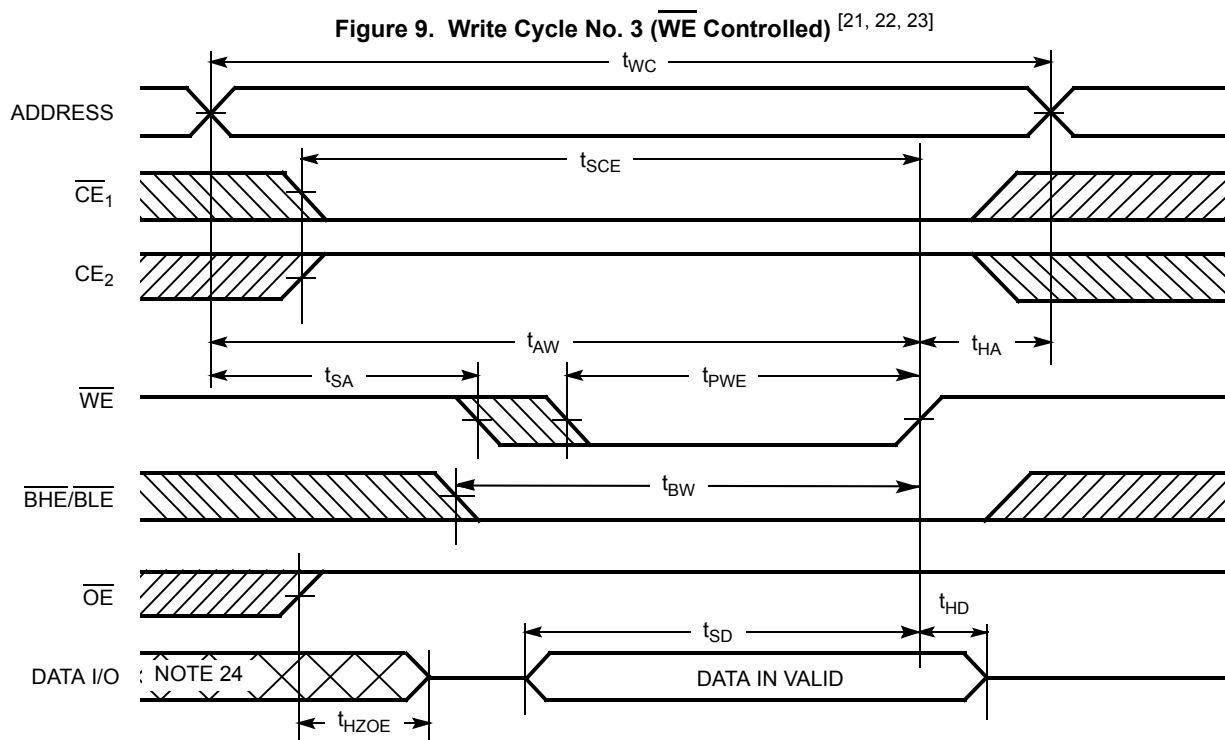
Notes

16. \overline{WE} is HIGH for the read cycle.

17. Address valid prior to or coincident with \overline{CE} LOW transition.

Switching Waveforms (continued)
Figure 7. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18, 19]

Figure 8. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [18, 19, 20]

Notes

18. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$.
20. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms (continued)

Notes

21. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ –I/O ₇	Mode	Power
H	X ^[25]	X ^[25]	HI-Z	Power down	Standby (I _{SB})
L	L	H	Data out	Read all bits	Active (I _{CC})
L	X	L	Data in	Write all bits	Active (I _{CC})
L	H	H	HI-Z	Selected, outputs disabled	Active (I _{CC})

Note

25. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1049GN30-10ZSXI	51-85087	44-pin TSOP II	Industrial
		CY7C1049GN30-10VXI	51-85090	36-pin Molded SOJ	
	4.5 V–5.5 V	CY7C1049GN-10VXI	51-85090	36-pin Molded SOJ	

Ordering Code Definitions

CY	7	C	1	04	9	GN	XX	-	XX	XX	X	I	
													Temperature Range: I = Industrial
													Pb-free
													Package Type: XX = V or ZS V = 36-pin Molded SOJ; ZS = 44-pin TSOP II
													Speed: XX = 10 ns
													Voltage Range: XX = 30 or blank 30 = 2.2 V–3.6 V; no character = 4.5 V–5.5 V
													Process Technology: GN = 65 nm
													Data width: 9 = × 8-bits
													Density: 04 = 4-Mbit
													Family Code: 1 = Fast Asynchronous SRAM family
													Technology Code: C = CMOS
													Marketing Code: 7 = SRAM
													Company ID: CY = Cypress

Package Diagrams

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087

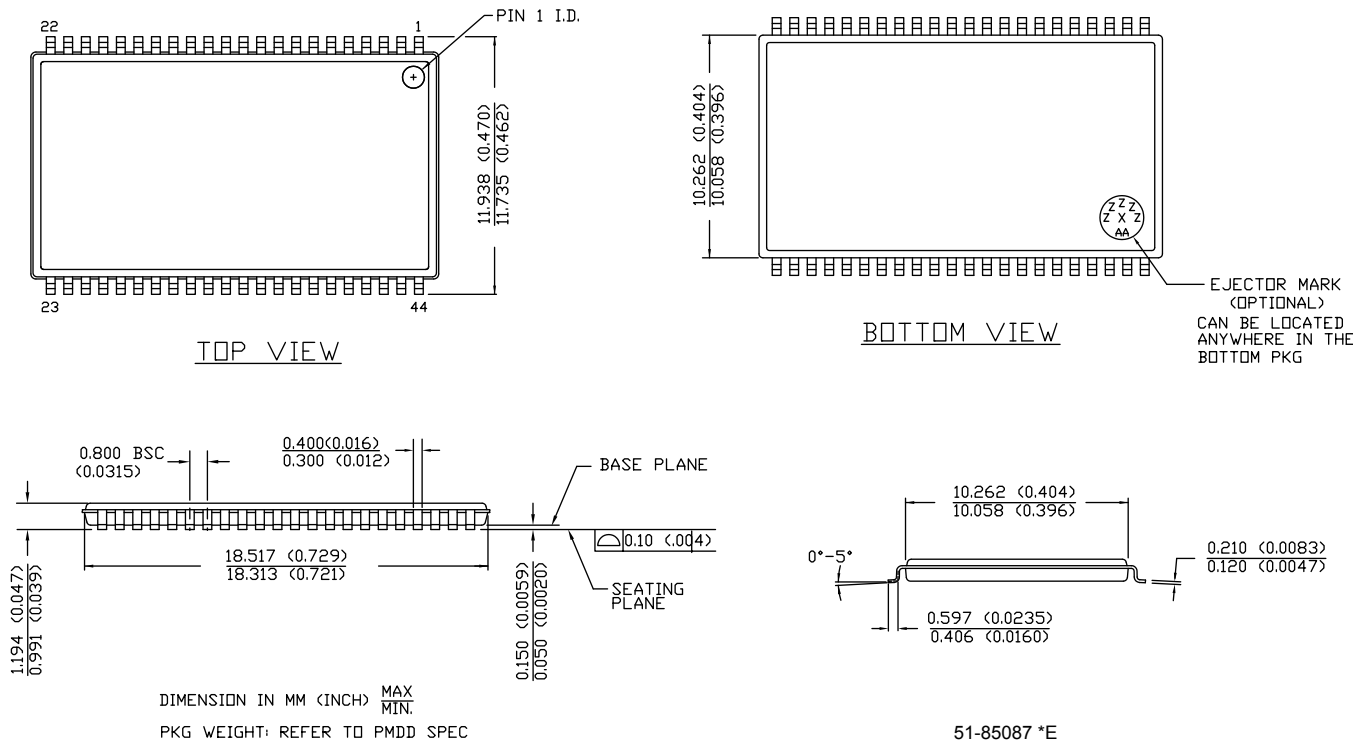
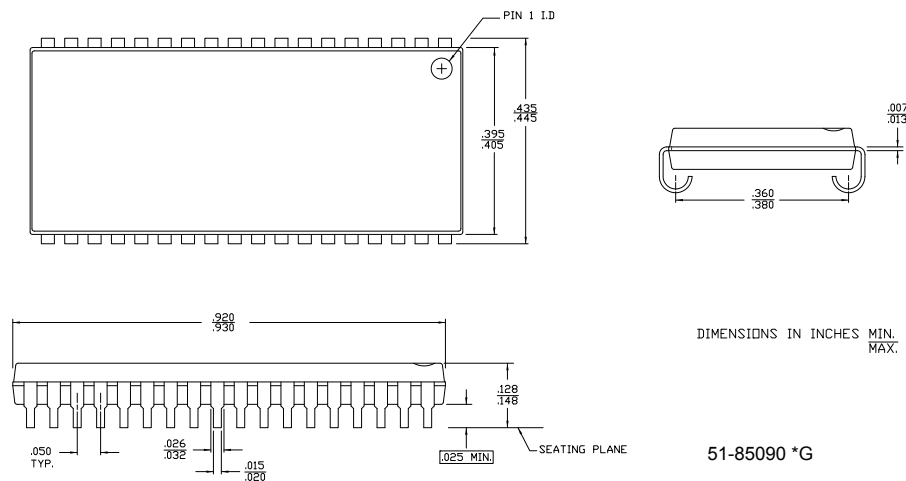


Figure 11. 36L SOJ V36.4 (Molded) Package Outline, 51-85090

36 Lead (400 MIL) Molded SOJ V36



Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeter
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY7C1049GN, 4-Mbit (512K words × 8 bit) Static RAM
Document Number: 002-10613

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	5074703	NILE	01/06/2016	New data sheet.
*A	5082587	NILE	01/12/2016	Updated Logic Block Diagram – CY7C1049GN . Updated Ordering Information : Updated part numbers.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2016. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.