

Features

- Temperature ranges
 - Automotive-E: -40 °C to 125 °C
- Pin and function compatible with CY7C10212CV33
- High speed
 - $t_{AA} = 12$ ns (Automotive-E)
- CMOS for optimum speed and power
- Low active power: 325 mW (max)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free 48-ball FBGA package

Functional Description

The CY7C10212CV33 is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

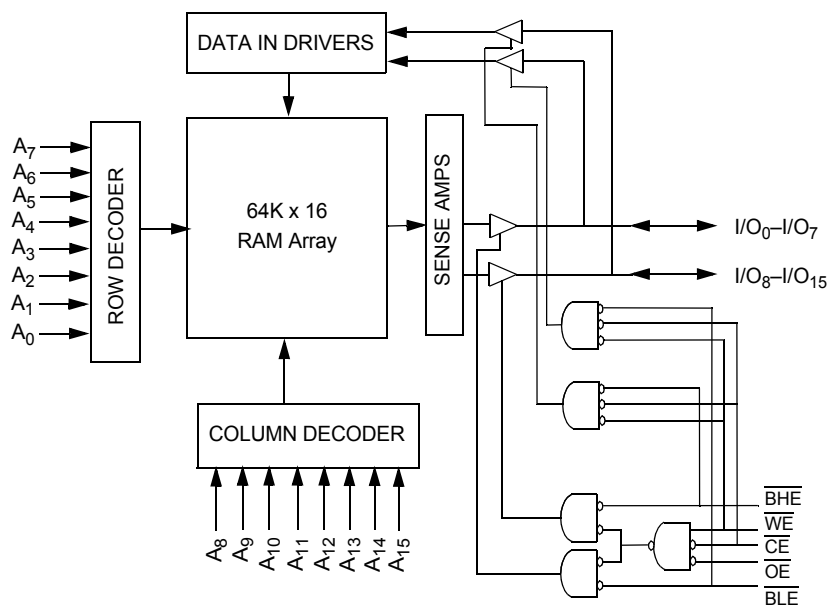
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. For more information, see the [Truth Table on page 9](#) for a complete description of Read and Write modes.

The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (\overline{CE} LOW and WE LOW).

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

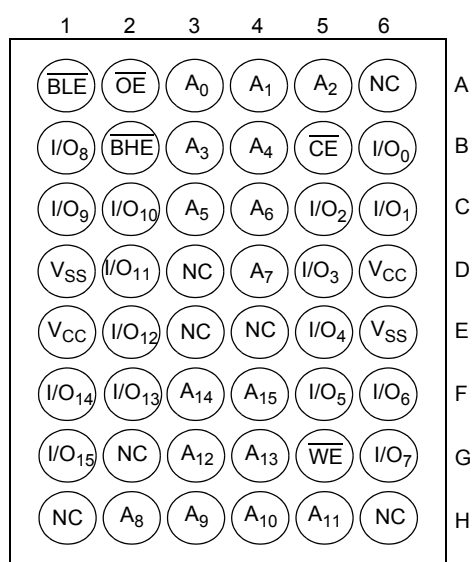
Selection Guide	3	Package Diagrams	11
Pin Configuration	3	Acronyms	12
Maximum Ratings	4	Document Conventions	12
Operating Range	4	Units of Measure	12
Electrical Characteristics	4	Document History Page	13
Capacitance	5	Sales, Solutions, and Legal Information	14
Thermal Resistance	5	Worldwide Sales and Design Support	14
AC Test Loads and Waveforms	5	Products	14
Switching Characteristics	6	PSoC® Solutions	14
Switching Waveforms	7	Cypress Developer Community	14
Truth Table	9	Technical Support	14
Ordering Information	10		
Ordering Code Definitions	10		

Selection Guide

Description	-12	Unit
Maximum Access Time	12	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Pin Configuration

Figure 1. 48-ball FBGA pinout ^[1]



Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage on
 V_{CC} Relative to GND ^[2] -0.3 V to +4.6 V

DC Voltage Applied to Outputs
in High Z State ^[2] -0.3 V to $V_{CC} + 0.3$ V

DC Input Voltage ^[2] -0.3 V to $V_{CC} + 0.3$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch Up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive-E	-40 °C to +125 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[2]		-0.3	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-12	+12	μA
I/O_Z	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output disabled	-12	+12	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	—	90	mA
I_{SB1}	Automatic CE Power Down Current — TTL Inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	—	20	mA
I_{SB2}	Automatic CE Power Down Current — CMOS Inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	—	10	mA

Note

2. $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 0.5 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

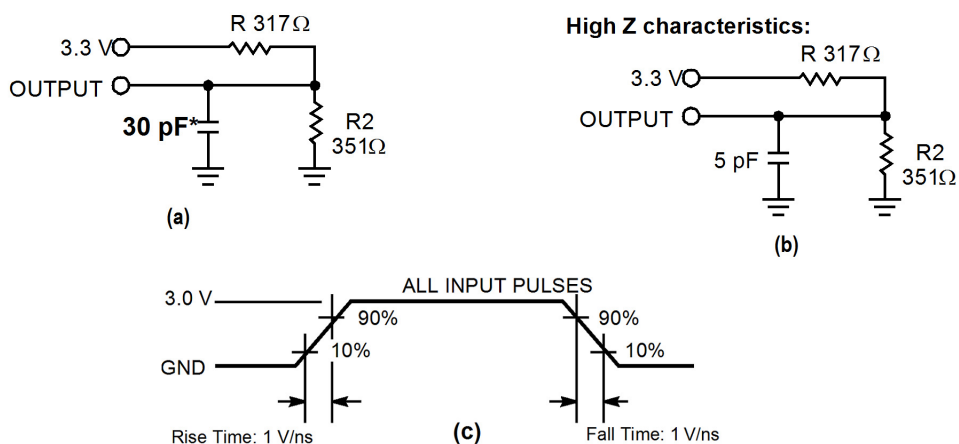
Parameter ^[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	95.32	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		10.68	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Speed is tested using the Thevenin load shown in Figure 2 (a). High Z characteristics are tested using the test load shown in Figure 2 (b).

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description	-12		Unit
		Min	Max	
Read Cycle				
t _{power} ^[6]	V _{CC} (Typical) to the First Access	100	–	μs
t _{RC}	Read Cycle Time	12	–	ns
t _{AA}	Address to Data Valid	–	12	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid	–	12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	–	6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[7]	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[7, 8]	–	6	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[7, 8]	–	6	ns
t _{PU} ^[9]	$\overline{\text{CE}}$ LOW to Power Up	0	–	ns
t _{PD} ^[9]	$\overline{\text{CE}}$ HIGH to Power Down	–	12	ns
t _{DBE}	Byte Enable to Data Valid	–	6	ns
t _{LZBE}	Byte Enable to Low Z	0	–	ns
t _{HZBE}	Byte Disable to High Z	–	6	ns
Write Cycle ^[10, 11]				
t _{WC}	Write Cycle Time	12	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	9	–	ns
t _{AW}	Address Setup to Write End	9	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Setup to Write Start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	8	–	ns
t _{SD}	Data Setup to Write End	6	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[7, 8]	–	6	ns
t _{BW}	Byte Enable to End of Write	8	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of [Figure 2 on page 5](#). Transition is measured ± 500 mV from steady state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, $\overline{\text{WE}}$ LOW, and $\overline{\text{BHE/BLE}}$ LOW. $\overline{\text{CE}}$, $\overline{\text{WE}}$, and $\overline{\text{BHE/BLE}}$ is LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle pulse width for write cycle 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [12, 13]

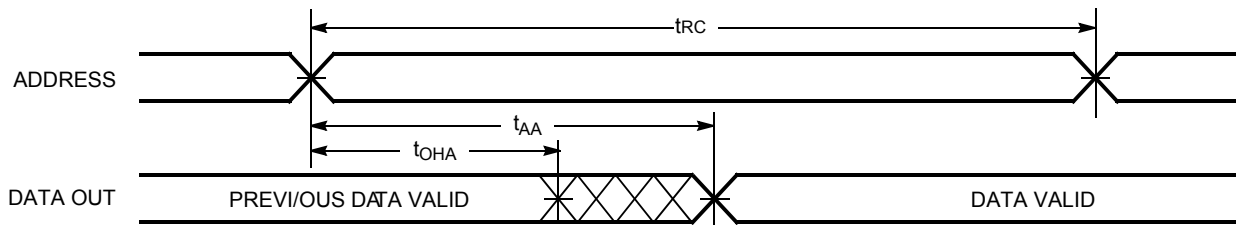
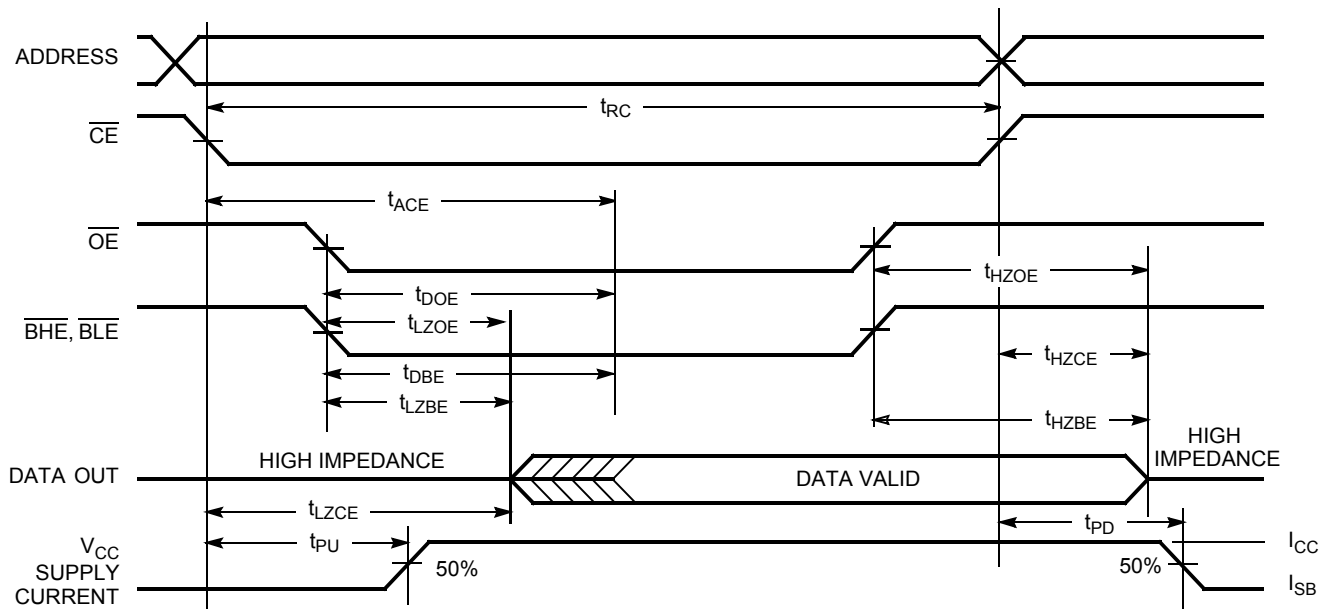


Figure 4. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [13, 14]



Notes

12. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IL}}$.
13. $\overline{\text{WE}}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [15, 16]

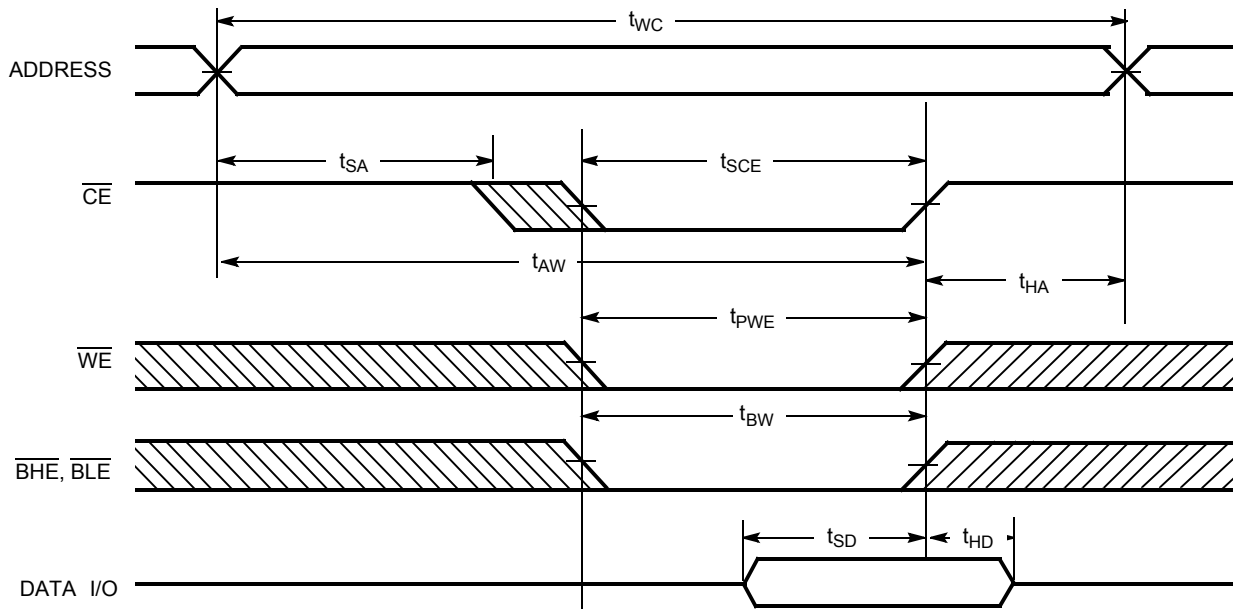
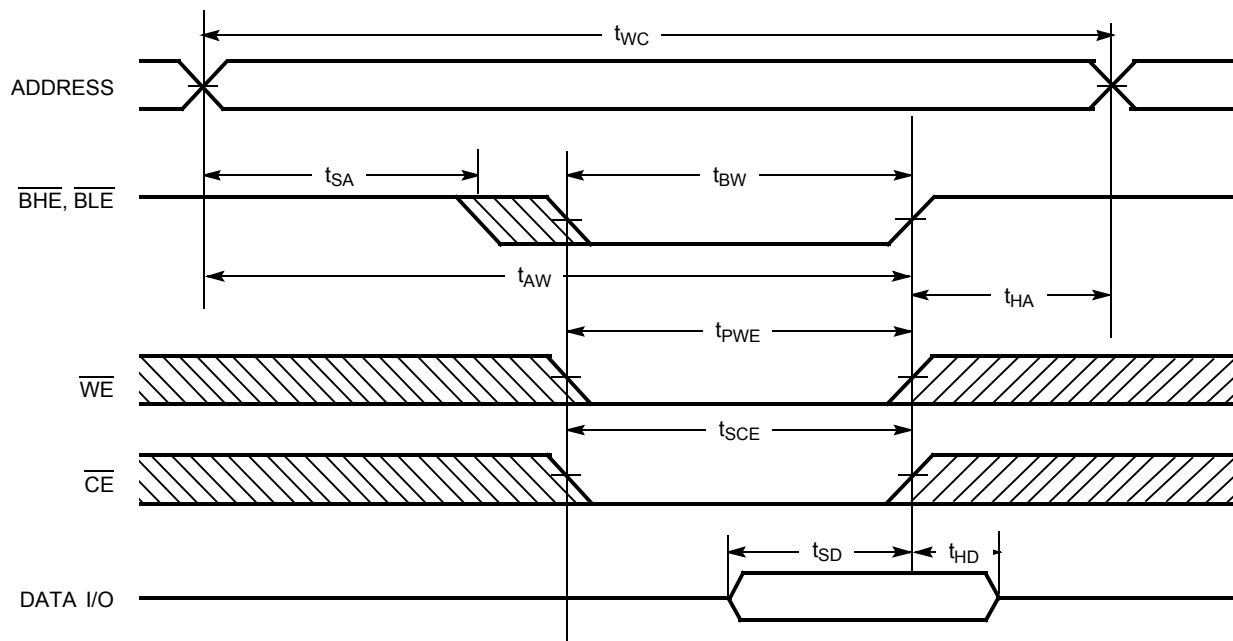


Figure 6. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

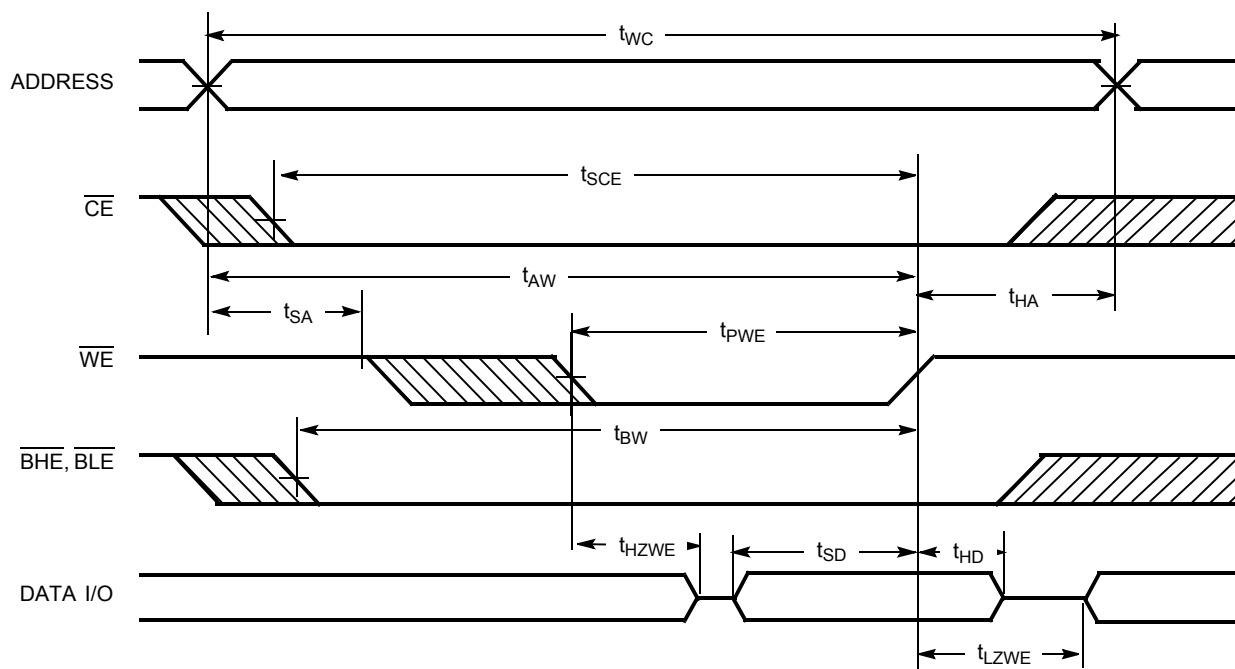


Notes

15. Data I/O is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}}$ = V_{IH} .

16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

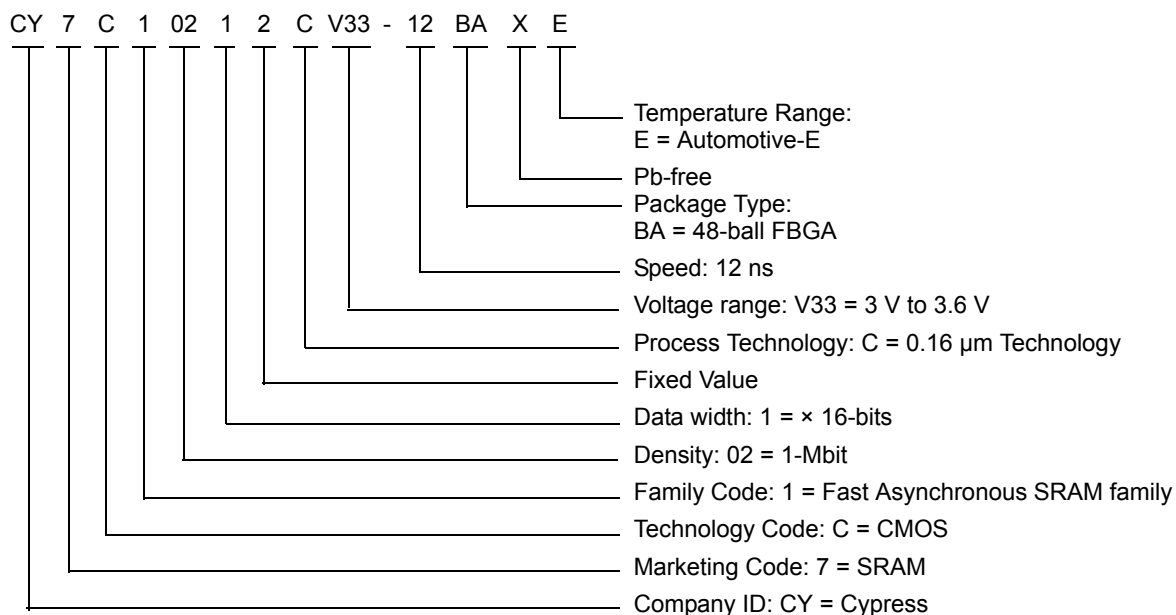
Figure 7. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ – I/O ₇	I/O ₈ – I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

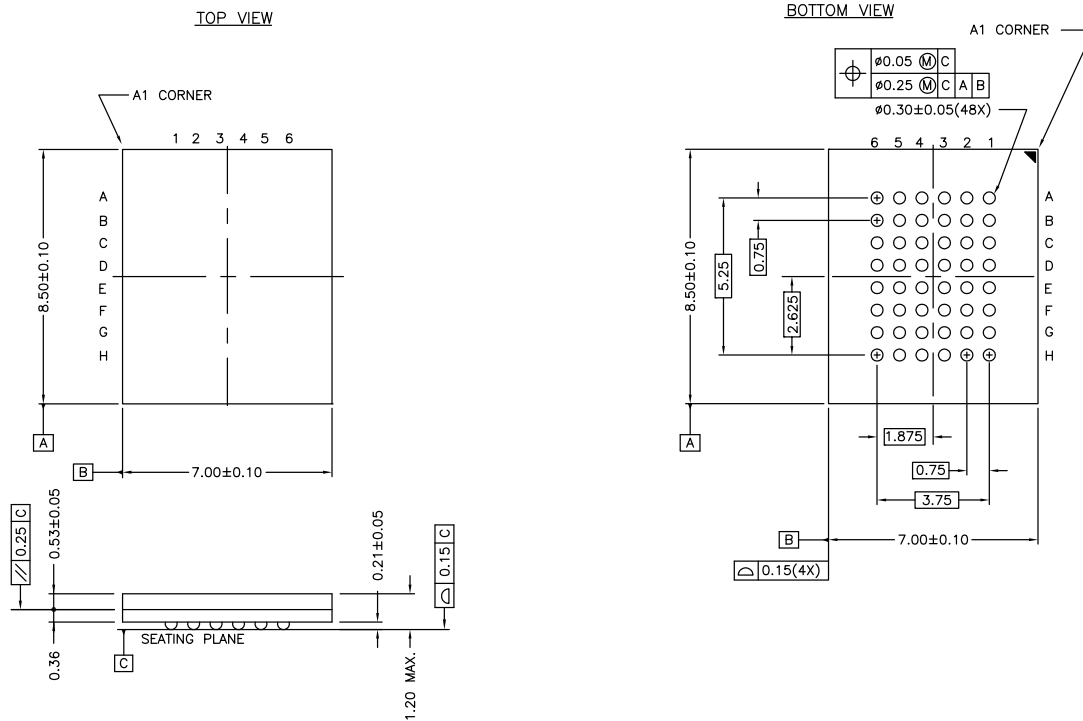
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C10212CV33-12BAXE	51-85106	48-ball FBGA (Pb-free)	Automotive-E

Ordering Code Definitions



Package Diagrams

Figure 8. 48-ball FBGA (7 × 8.5 × 1.2 mm) BA48A Package Outline, 51-85106



51-85106 *G

Acronyms

Acronym	Description
BGA	Ball Grid Array
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
MHz	megahertz
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C10212CV33, 1-Mbit (64 K × 16) Static RAM Document Number: 001-82303				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	3723052	10/29/2012	TAVA	New data sheet.
*A	4178071	10/30/2013	VINI	Updated in new template. Completing Sunset Review.
*B	4571877	11/18/2014	VINI	Added related documentation hyperlink in page 1. Added Note 11 in Switching Characteristics . Added note reference 11 in the Switching Characteristics table. Updatd Figure 7 title.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2012-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.