CY62256EV18 MoBL®

256-Kbit (32 K × 8) Static RAM

Features

- Very high speed: 70 ns
- Temperature ranges:
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 1.65 V to 2.25 V
- Pin compatible with CY62256N
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 28-pin Narrow SOIC package

Functional Description

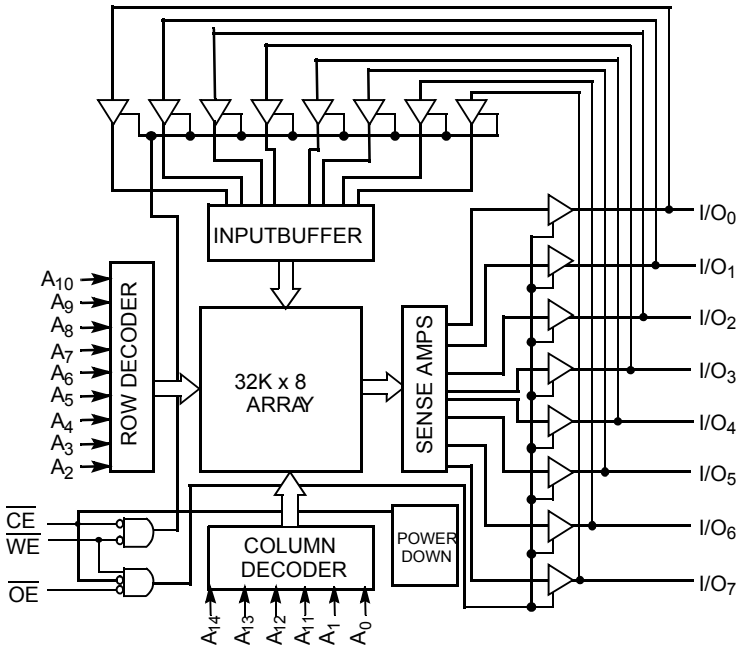
The CY62256EV18 is a high performance CMOS static RAM module organized as 32 K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take chip enable ($\overline{CE}$) LOW and write enable ($\overline{WE}$) LOW. Data on the eight I/O pins is then written into the location specified on the address pin (A_0 through A_{14}).

To read from the device, take chip enable ($\overline{CE}$ LOW) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, click here.

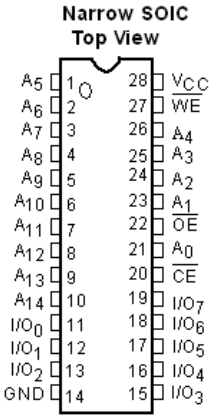
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 28-pin Narrow SOIC pinout



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62256EV18LL	Industrial	1.65	1.8	2.25	70	1.3	2.0	11	16	1	4

Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.2 V to 2.45 V

DC voltage applied to outputs in high Z State [2, 3] .....–0.2 V to 2.45 V

DC input voltage [2, 3] .....–0.2 V to 2.45 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[4]
CY62256EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		70 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		1.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.2	V
V_{IH}	Input HIGH voltage	V_{CC} = 1.65 V to 2.25 V		1.4	–	V_{CC} + 0.2 V	V
V_{IL}	Input LOW voltage	V_{CC} = 1.65 V to 2.25 V		–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = 2.25 V, I_{OUT} = 0 mA, CMOS levels	–	11	16	mA
		f = 1 MHz		–	1.3	2.0	mA
I_{SB1}	Automatic CE power-down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 2.25 V		–	1	4	µA
I_{SB2} [6]	Automatic CE power-down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} < 0.2 V, f = 0, V_{CC} = 2.25 V		–	1	4	µA

Notes

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.5 V for pulse durations less than 20 ns.
4. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. Chip enables ($\overline{CE}$) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

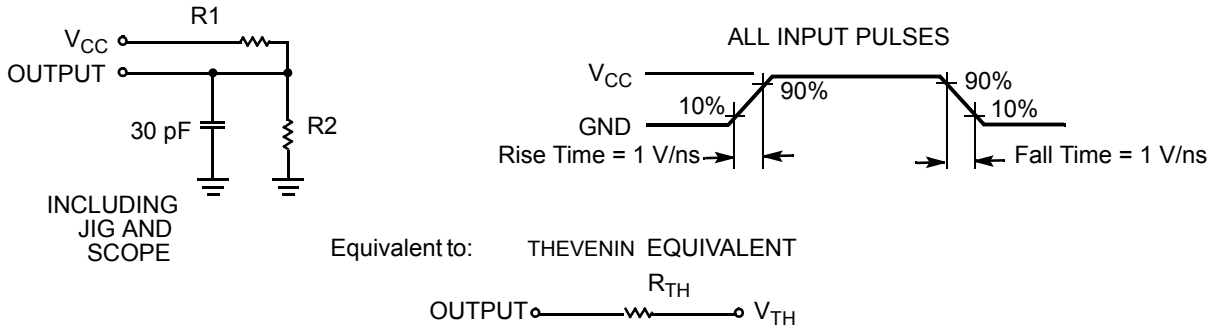
Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	28-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	76.56	°C/W
Θ_{JC}	Thermal resistance (junction to case)		36.07	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	1.8 V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.8	V

Note
7. Tested initially and after any design or process changes that may affect these parameters.

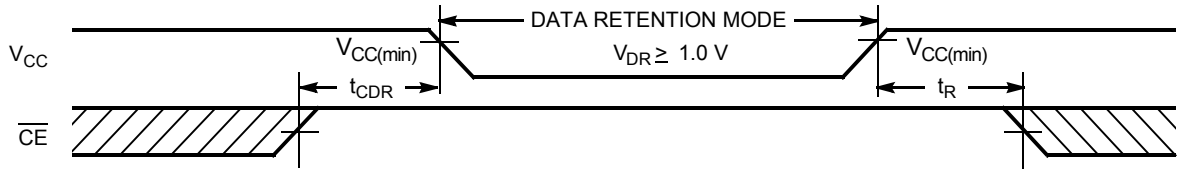
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [8]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [9]	Data retention current	V_{CC} = 1.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	3	µA
t_{CDR} [10]	Chip deselect to data retention time		0	–	–	ns
t_R [11]	Operation recovery time		70	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [12]



Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
9. Chip enables ($\overline{CE}$) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

Switching Characteristics

Over the Operating Range

Parameter [13]	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	70	–	ns
t_{AA}	Address to data valid	–	70	ns
t_{OHA}	Data hold from address change	5	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	70	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	35	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [14]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [14, 15]	–	25	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [14]	5	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [14, 15]	–	25	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	70	ns
Write Cycle [16, 17]				
t_{WC}	Write cycle time	70	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	60	–	ns
t_{AW}	Address setup to write end	60	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	50	–	ns
t_{SD}	Data setup to write end	30	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [14, 15]	–	25	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [14]	5	–	ns

Notes

13. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
17. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ low) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [18, 19]

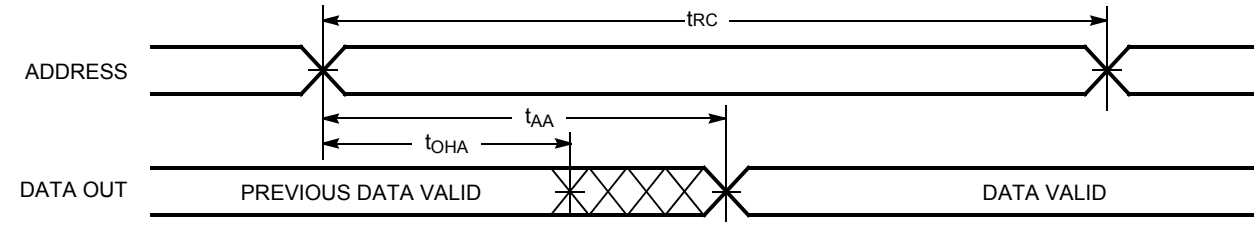


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [19, 20]

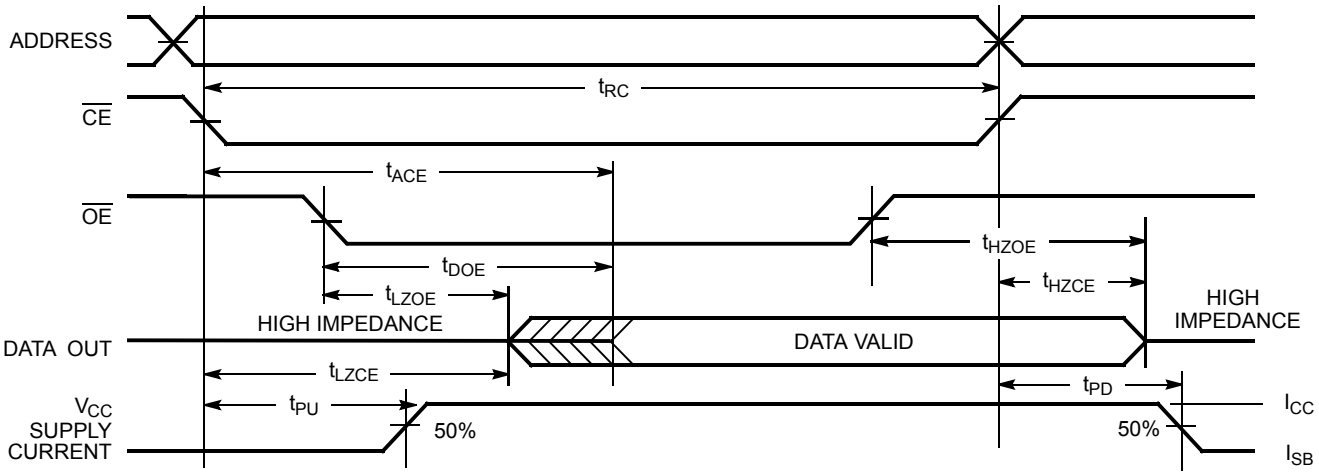
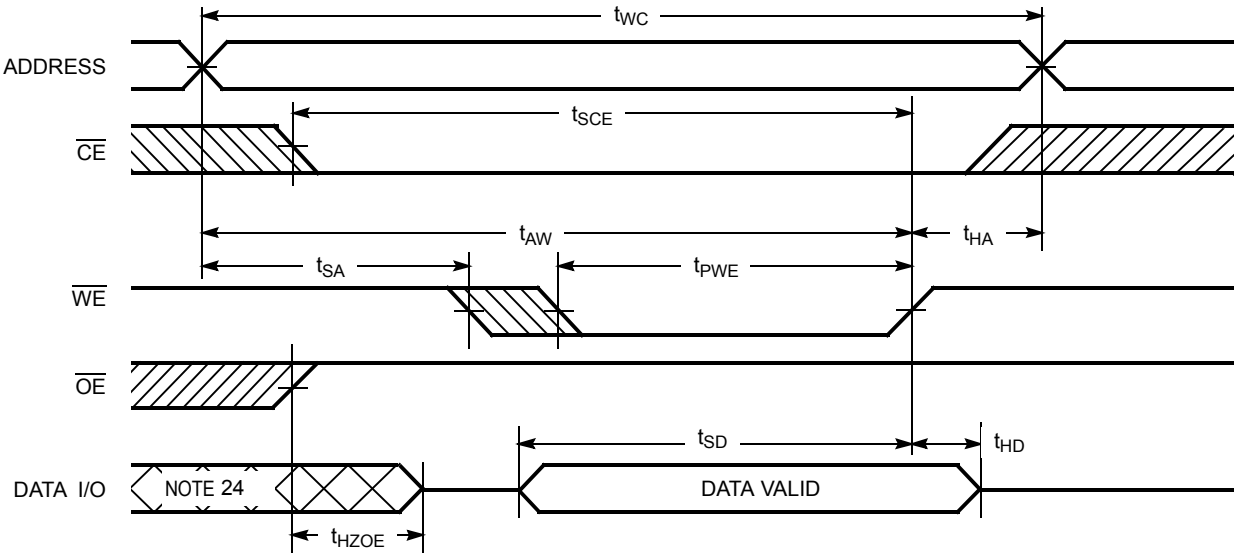


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [21, 22, 23]



Notes

18. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid before or similar to $\overline{CE}$ transition LOW.
21. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [25, 26, 27]

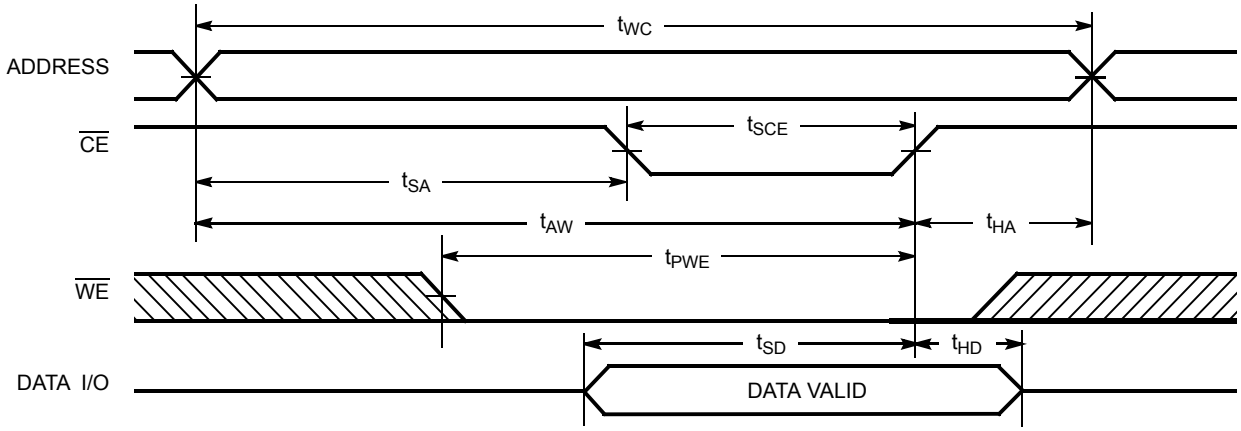
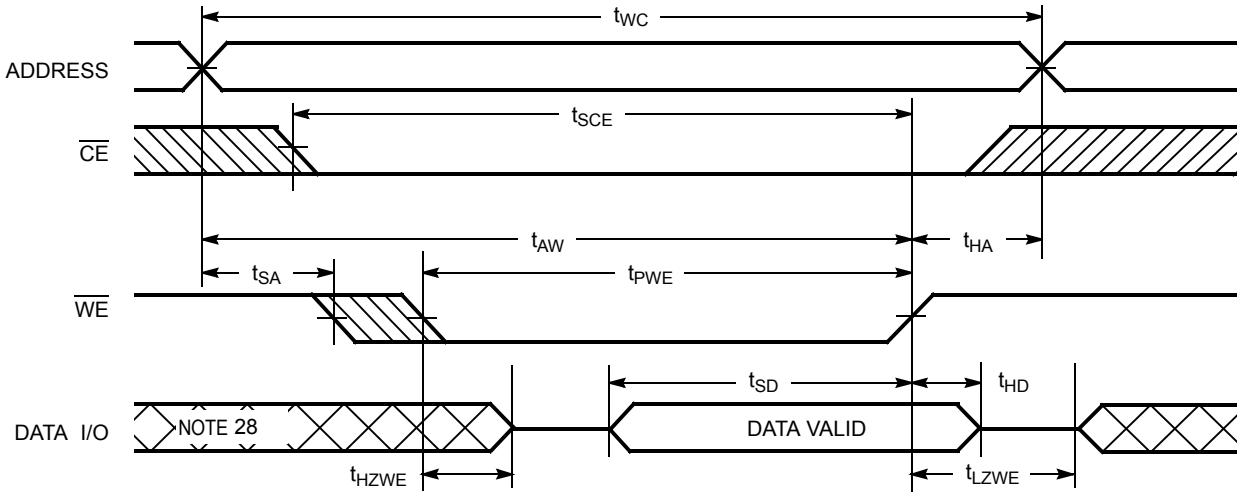


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27]



Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X [29]	X [29]	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X [29]	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

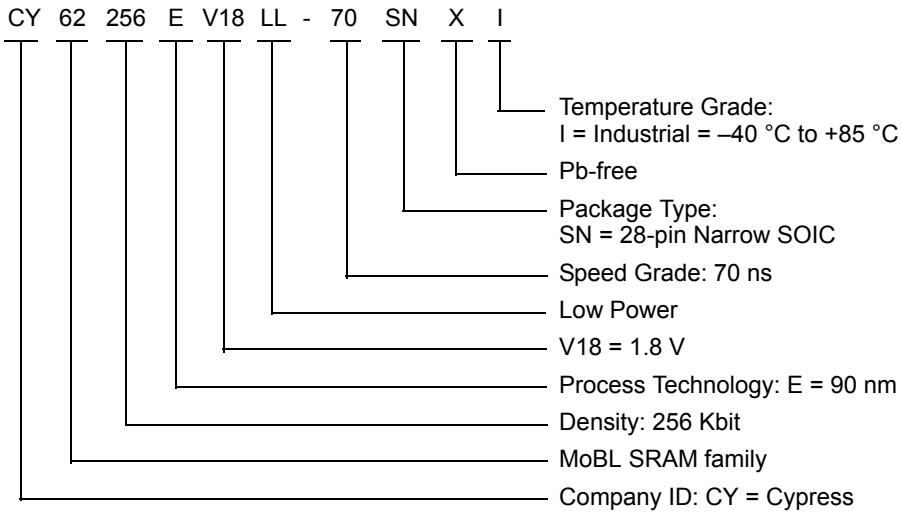
Note
29. The 'X' (Don't care) state for the $\overline{CE}$ / $\overline{OE}$ / $\overline{WE}$ in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256EV18LL-70SNXI	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	Industrial

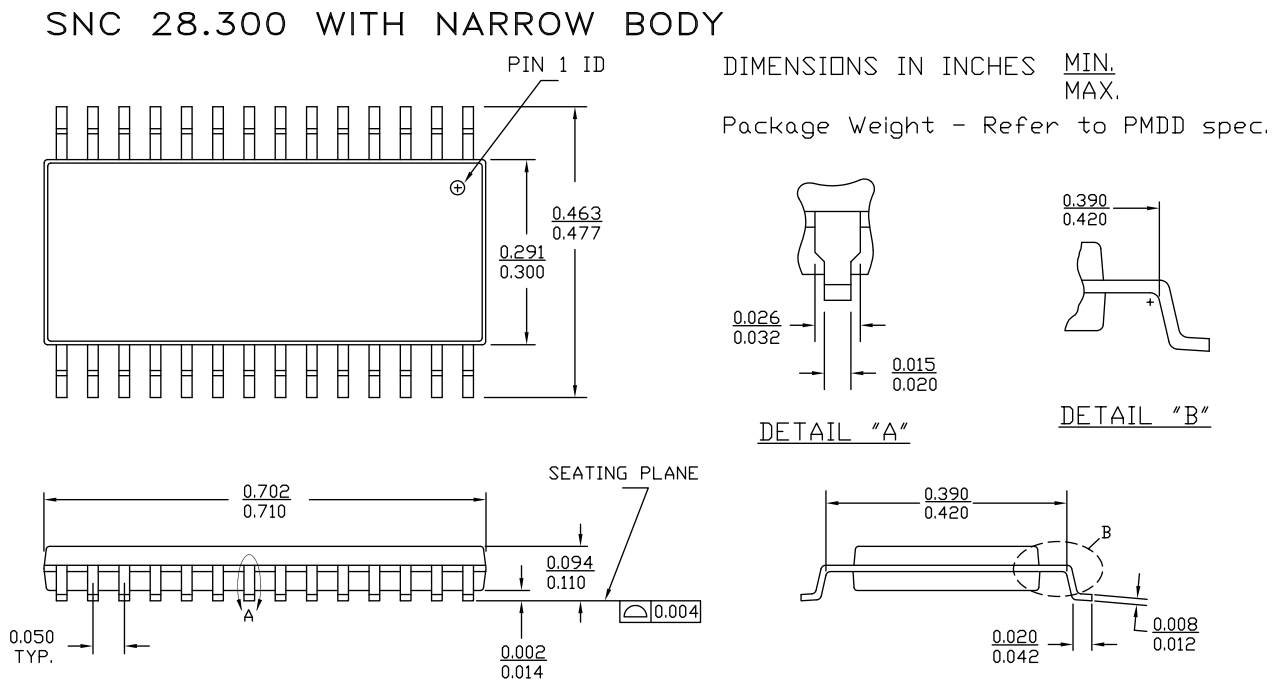
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 9. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092



51-85092 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOIC	Small Outline Integrated Circuit
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62256EV18 MoBL®, 256-Kbit (32 K × 8) Static RAM Document Number: 001-69650				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3334904	09/07/2011	RAME	New data sheet.
*A	3413173	10/18/2011	RAME	Changed status from Preliminary to Final.
*B	3733339	09/04/2012	JISH	Fixed typo errors. Completing Sunset Review.
*C	4573121	11/18/2014	JISH	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*D	4928585	09/21/2015	VINI	Updated Switching Characteristics: Added Note 17 and referred the same note in “Write Cycle”. Updated to new template. Completing Sunset Review.

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