

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 3.5 μ A
 - Maximum standby current: 8.7 μ A
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC) packages

Functional Description

The CY62148GN is a high-performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable

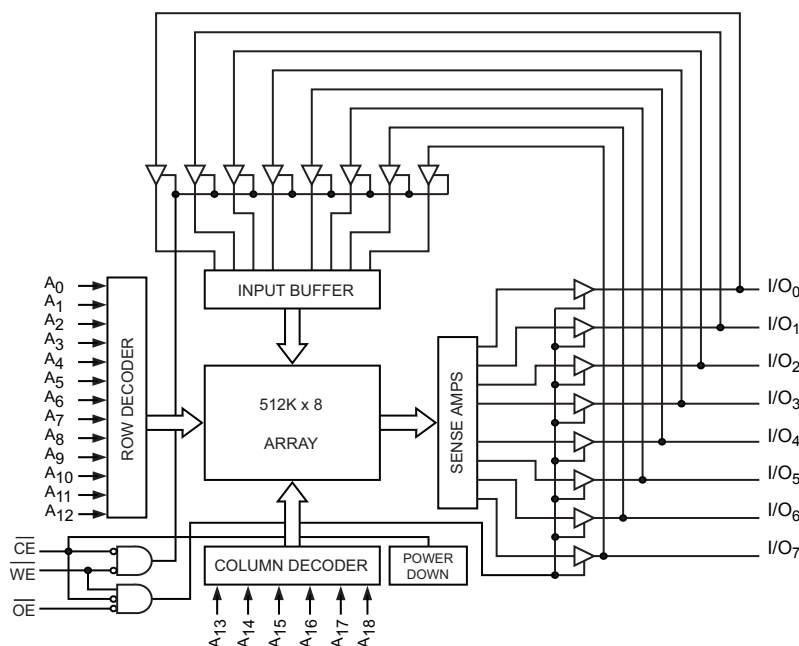
applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH). The eight input and output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), Outputs are disabled ($\overline{\text{OE}}$ HIGH), or during an active Write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

To write to the device, take Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

To read from the device, take Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

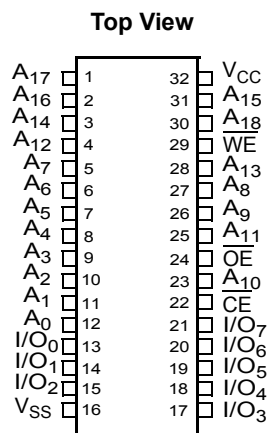


Contents

Pin Configurations	3	Ordering Information	11
Product Portfolio	3	Ordering Code Definitions	11
Maximum Ratings	4	Package Diagrams	12
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	16
Data Retention Characteristics	6	Worldwide Sales and Design Support	16
Data Retention Waveform	6	Products	16
Switching Characteristics	7	PSoC® Solutions	16
Switching Waveforms	8	Cypress Developer Community	16
Truth Table	10	Technical Support	16

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II Pinout



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation					
				Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
				f = 1 MHz		f = f _{max}			
				Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62148GN30	Industrial	2.2 V–3.6 V	45	–	6	–	20	3.5	8.7
CY62148GN		4.5 V–5.5 V							

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.5 V to $V_{CC} + 0.5$ V

DC voltage applied to outputs
in high Z state ^[2, 3] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[2, 3] -0.5 V to $V_{CC} + 0.5$ V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[4]
CY62148GN	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V, 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	2	—	—	V
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.2	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5$ ^[6]	—	—	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	—	—	0.4	V
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$	—	—	0.4	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$	—	—	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V —	2	—	$V_{CC} + 0.3$ ^[3]	V
		2.7 V to 3.6 V —	2	—	$V_{CC} + 0.3$ ^[3]	
		4.5 V to 5.5 V —	2.2	—	$V_{CC} + 0.5$	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V —	-0.3 ^[2]	—	0.6	V
		2.7 V to 3.6 V —	-0.3 ^[2]	—	0.8	
		4.5 V to 5.5 V —	-0.5	—	0.8	
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, output disabled	-1	—	+1	μA
I_{CC}	V_{CC} operating supply current	$f = f_{\text{max}} = 1/t_{RC}$ $V_{CC} = V_{CC(\text{max})}$, $I_{OUT} = 0 \text{ mA}$	—	—	20	mA
		$f = 1 \text{ MHz}$ CMOS levels	—	—	6	
I_{SB1} ^[7]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = f_{\text{max}}$ (address and data only), $f = 0$ (\overline{OE} and \overline{WE}) $V_{CC} = V_{CC(\text{max})}$	—	3.5	8.7	μA
I_{SB2} ^[7]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC(\text{max})}$	—	3.5	8.7	μA

Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$ for pulse durations less than 20 ns for $I \leq 30 \text{ mA}$.
- $V_{IH(\text{max})} = V_{CC} + 0.75 \text{ V}$ for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to $V_{CC(\text{min})}$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25^\circ\text{C}$.
- This parameter is guaranteed by design and not tested.
- Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

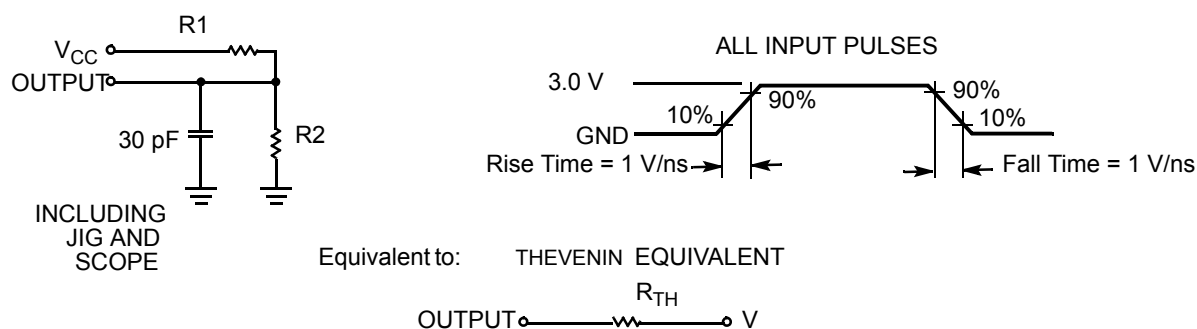
Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(Typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	°C/W
Θ _{JC}	Thermal resistance (junction to case)		25.12	17.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[9]



Parameter ^[8]	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 μs or stable at V_{CC(min)} > 100 μs.

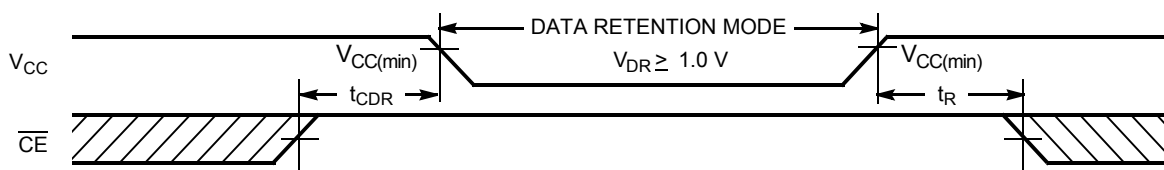
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
$I_{CCDR}^{[11, 12]}$	Data retention current	$V_{CC} = 1.2V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	–	13	μA
$t_{CDR}^{[13]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[13, 14]}$	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ C$.
11. Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
13. These parameters are guaranteed by design.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 μs or stable at $V_{CC(min)}$ > 100 μs .

Switching Characteristics

Over the operating range

Parameter ^[15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45	–	ns
t _{AA}	Address to data valid	–	45	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	\overline{CE} LOW to data valid	–	45	ns
t _{DOE}	\overline{OE} LOW to data valid	–	22	ns
t _{LZOE}	\overline{OE} LOW to low Z ^[16]	5	–	ns
t _{HZOE}	\overline{OE} HIGH to high Z ^[16, 17]	–	18	ns
t _{LZCE}	\overline{CE} LOW to low Z ^[16]	10	–	ns
t _{HZCE}	\overline{CE} HIGH to high Z ^[16, 17]	–	18	ns
t _{PU}	\overline{CE} LOW to power-up	0	–	ns
t _{PD}	\overline{CE} HIGH to power-down	–	45	ns
Write Cycle ^[18, 19]				
t _{WC}	Write cycle time	45	–	ns
t _{SCE}	\overline{CE} LOW to write end	35	–	ns
t _{AW}	Address setup to write end	35	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	\overline{WE} pulse width	35	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	\overline{WE} LOW to high Z ^[16, 17]	–	18	ns
t _{LZWE}	\overline{WE} HIGH to low Z ^[16]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

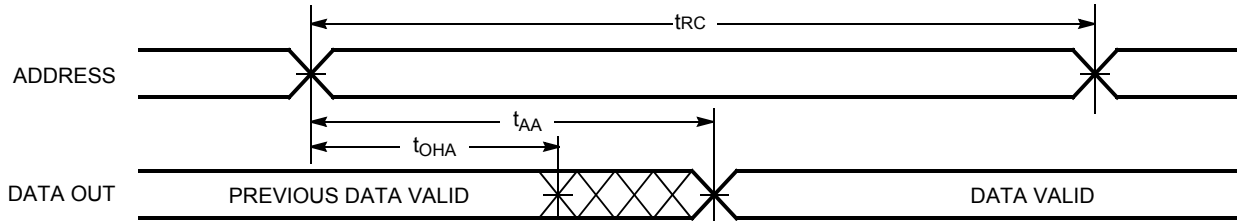


Figure 5. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [21, 22]

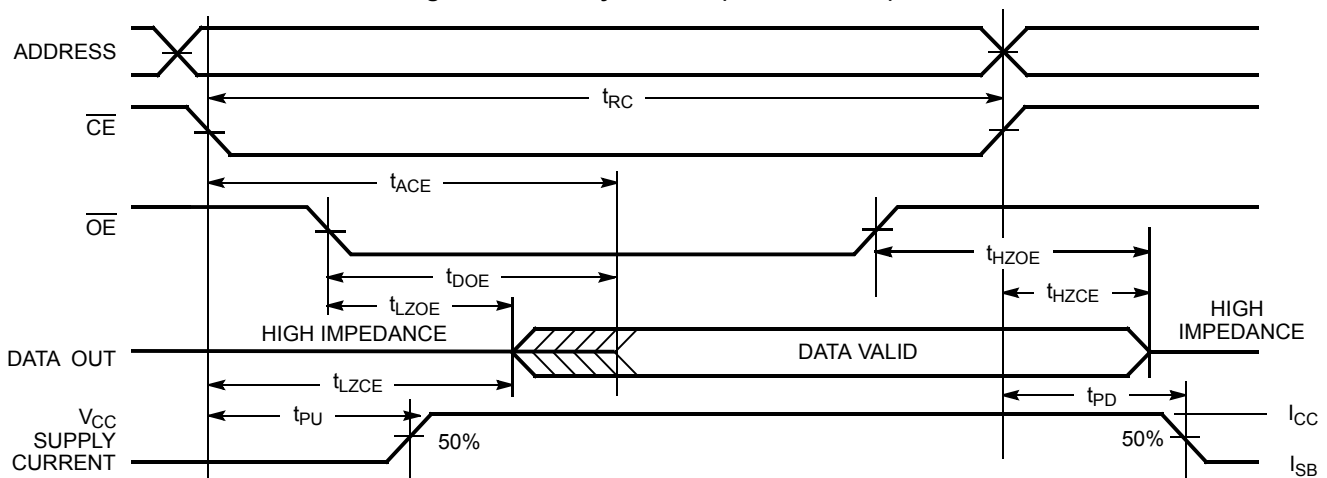
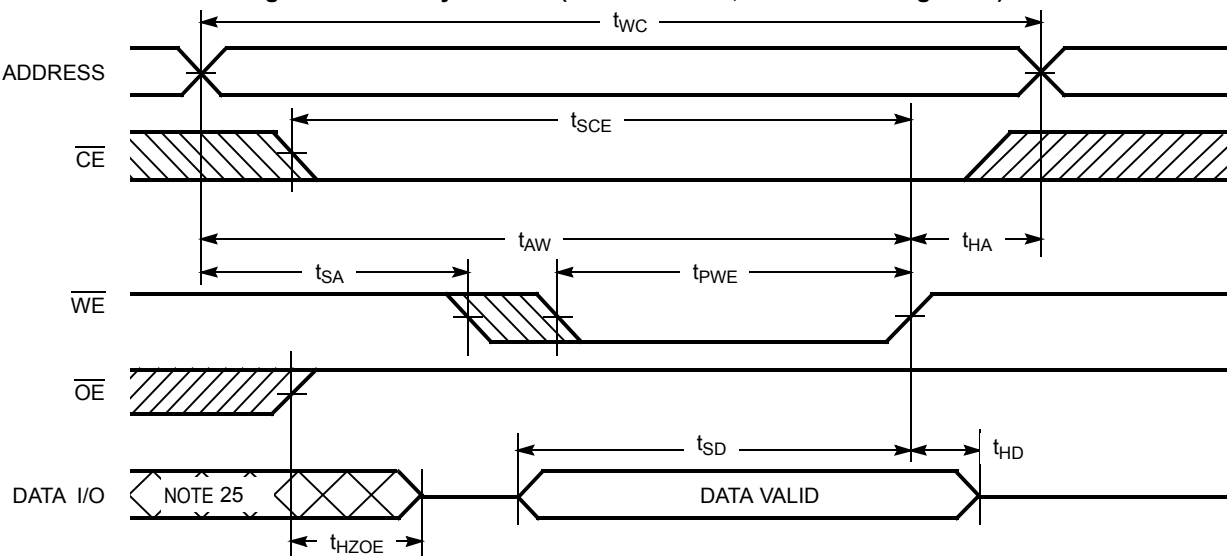


Figure 6. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write) [23, 24]



Notes

20. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$.
21. $\overline{\text{WE}}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{\text{CE}}$ transition LOW.
23. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
24. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [26, 27]

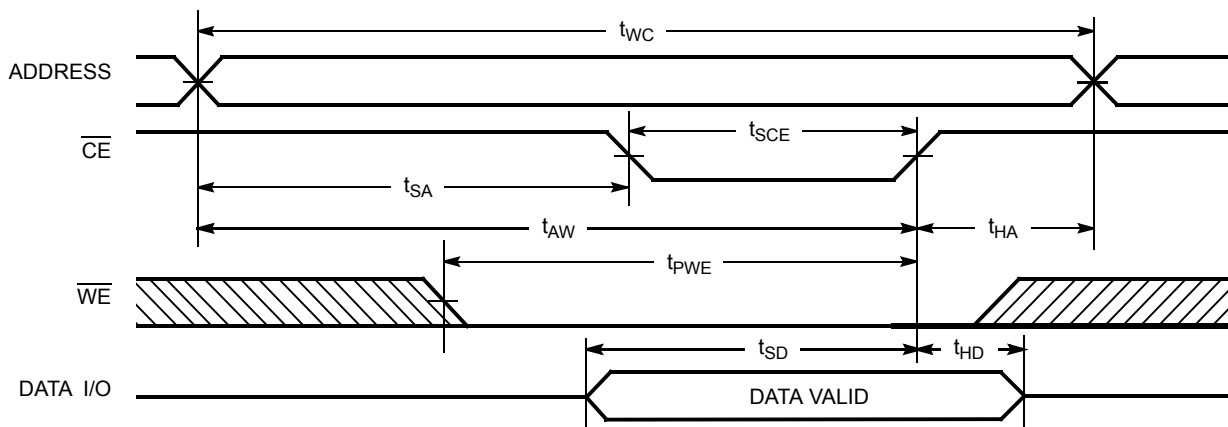
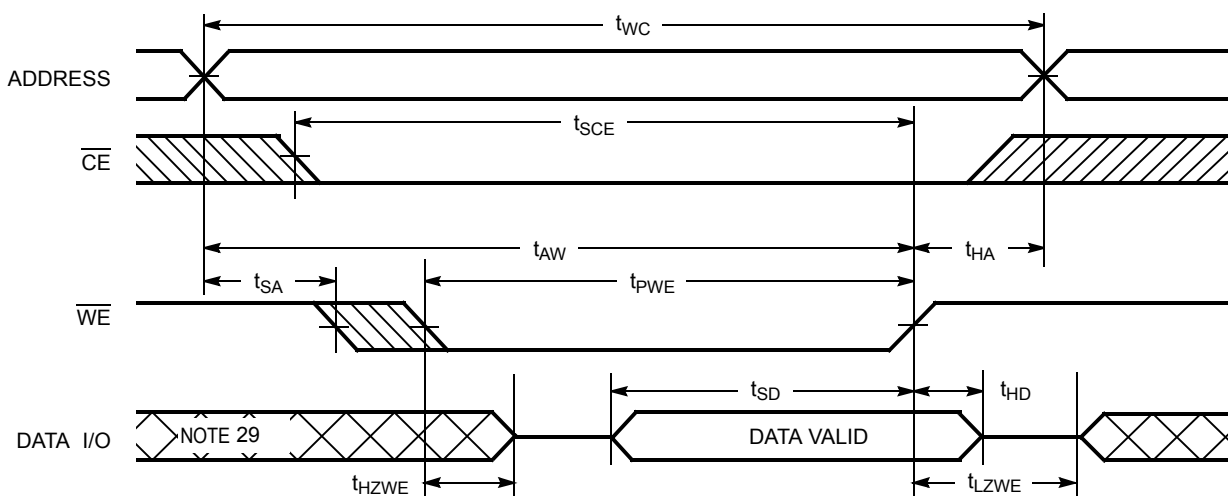


Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [27, 28]



Notes

26. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.

27. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.

28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	I/O	Mode	Power
H ^[30]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note

30. Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



Table 1 lists the CY62148GN MoBL[®] key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>.

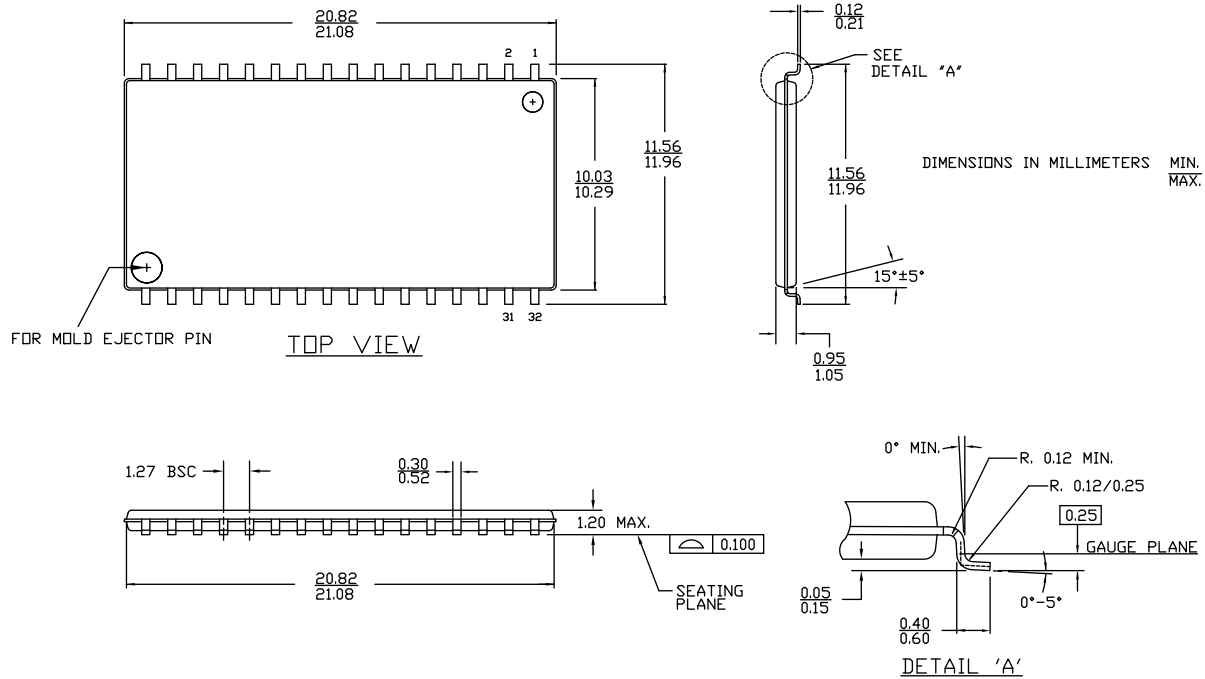
Speed (ns)	Voltage Range (V)	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148GN30-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
		CY62148GN30-45SXI	51-85081	32-pin SOIC (Pb-free)	
	4.5 V–5.5 V	CY62148GN-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
		CY62148GN-45SXI	51-85081	32-pin SOIC (Pb-free)	

The diagram illustrates the pinout and naming convention for MoBL SRAM devices. It shows two rows of pins: Pin 1 through Pin 8 on the left, and Pin 9 through Pin 16 on the right. The pins are numbered 1 through 16. Below the pin numbers, the corresponding pin names are listed: CY, 621, 4, 8, GN, XX, -, XX, XX, X, X. Lines connect each pin name to its respective pin number. To the right of the pin names, there are labels explaining the naming convention:

- Temperature Grade: X = I
I = Industrial
- Pb-free
- Package Type: XX = ZS or S
ZS = 32-pin TSOP II
S = 32-pin SOIC
- Speed Grade: XX = 45 ns
- Voltage Range: 30 = 3 V typ; no character = 5 V typ
- Process Technology: GN = 65 nm
- Bus width: 8 = × 8
- Density: 4 = 4-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

Package Diagrams

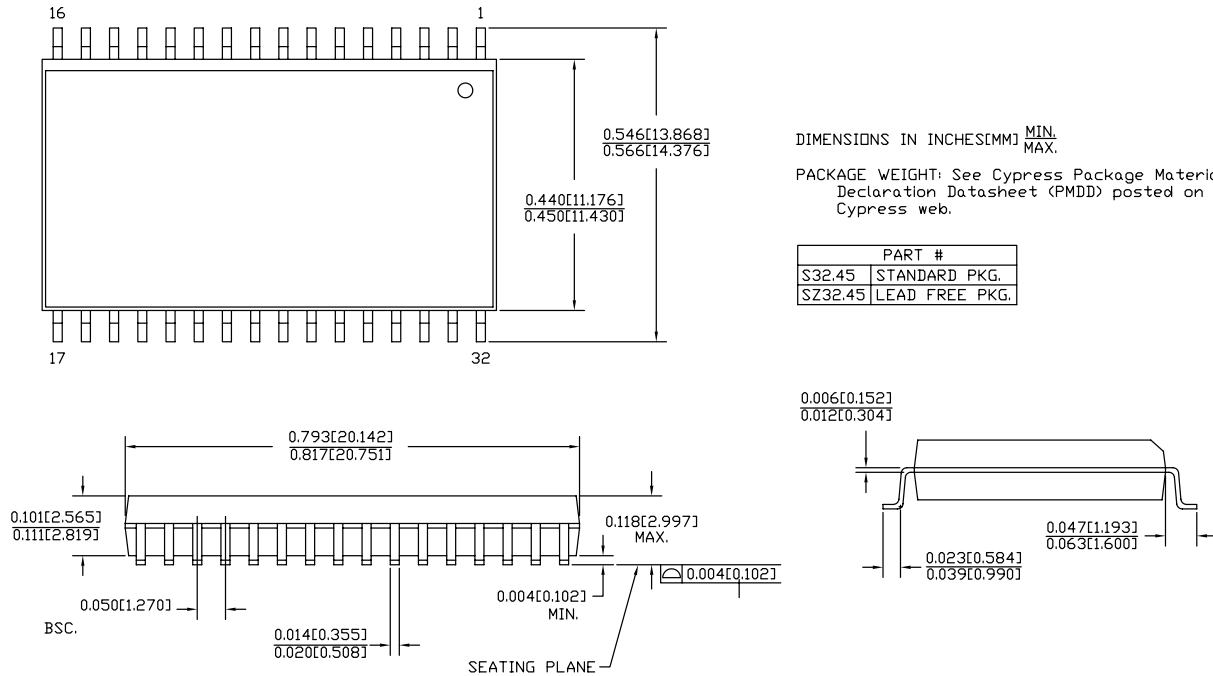
Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 *D

Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



DIMENSIONS IN INCHES [MM] MIN. MAX.

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

PART #	
S32.45	STANDARD PKG.
SZ32.45	LEAD FREE PKG.

51-85081 *E

Acronyms

Acronym	Description
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
MoBL	More Battery Life
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62148GN MoBL [®] , 4-Mbit (512K × 8) Static RAM Document Number: 001-95418				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5056496	NILE	12/29/2015	New data sheet.
*A	5092456	NILE	01/19/2016	Added "2.2 V to 3.6 V" range related information in all instances across the document. Updated Ordering Information : Updated part numbers.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2015-2016. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.