

# 4-Mbit (512K × 8) Static RAM

## Features

- Very high speed: 45 ns
- Voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62148B
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A (Industrial)
- Ultra low active power
  - Typical active current: 2.0 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC)<sup>[1]</sup> packages

## Functional Description

The CY62148E is a high performance CMOS static RAM organized as 512K words by 8-bits. This device features

advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), Outputs are disabled ( $\overline{OE}$  HIGH), or during an active Write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

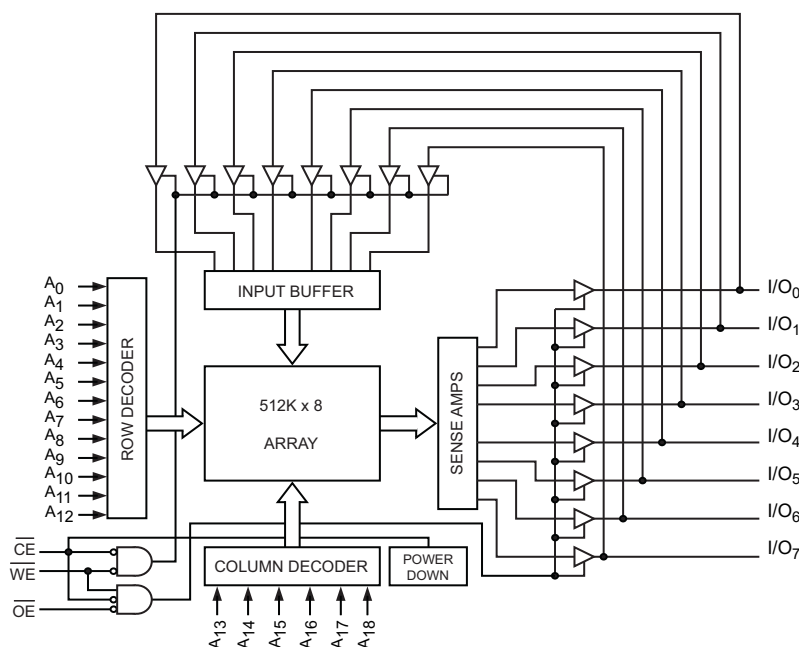
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

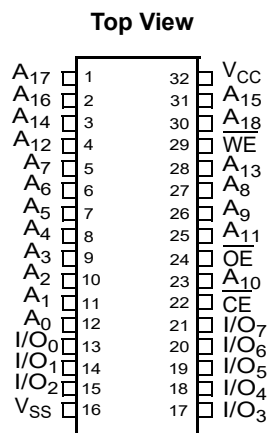
1. SOIC package is available only in 55 ns speed bin.

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## Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout [2]



## Product Portfolio

Product		Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
							Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
							f = 1 MHz		f = f <sub>max</sub>			
			Min	Typ <sup>[3]</sup>	Max		Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62148ELL	TSOP II	Industrial	4.5	5.0	5.5	45	2	2.5	15	20	1	7
CY62148ELL	SOIC	Industrial / Automotive-A	4.5	5.0	5.5	55	2	2.5	15	20	1	7

### Notes

- SOIC package is available only in 55 ns speed bin.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
to ground potential ..... -0.5 V to 6.0 V ( $V_{CCmax} + 0.5$  V)

DC voltage applied to outputs  
in high Z state <sup>[4, 5]</sup> ..... -0.5 V to 6.0 V ( $V_{CCmax} + 0.5$  V)

DC input voltage <sup>[4, 5]</sup> ..... -0.5 V to 6.0 V ( $V_{CCmax} + 0.5$  V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}^{[6]}$
CY62148E	Industrial / Automotive-A	-40 °C to +85 °C	4.5 V to 5.5 V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			55 ns <sup>[7]</sup>			Unit
			Min	Typ <sup>[8]</sup>	Max	Min	Typ <sup>[8]</sup>	Max	
$V_{OH}^{[9]}$	Output HIGH voltage	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.4	–	–	2.4	–	–	V
		$V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA	–	–	3.4 <sup>[8]</sup>	–	–	3.4 <sup>[8]</sup>	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 2.1$ mA	–	–	0.4	–	–	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 4.5$ V to 5.5 V	2.2	–	$V_{CC} + 0.5$	2.2	–	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 4.5$ V to 5.5 V For TSOPII package	-0.5	–	0.8	–	–	–	V
		For SOIC package	–	–	–	-0.5	–	0.6 <sup>[10]</sup>	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	–	+1	-1	–	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , output disabled	-1	–	+1	-1	–	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$ , $I_{OUT} = 0$ mA CMOS levels	–	15	20	–	15	20	mA
		$f = 1$ MHz	–	2	2.5	–	2	2.5	
$I_{SB2}^{[11]}$	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = V_{CC(max)}$	–	1	7	–	1	7	μA

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns for  $I \leq 30$  mA.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- SOIC package is available only in 55 ns speed bin.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Please note that the maximum  $V_{OH}$  limit for this device does not exceed minimum CMOS  $V_{IH}$  of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum  $V_{IH}$  of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.
- Under DC conditions the device meets a  $V_{IL}$  of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.6 V. This is applicable to SOIC package only.
- Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

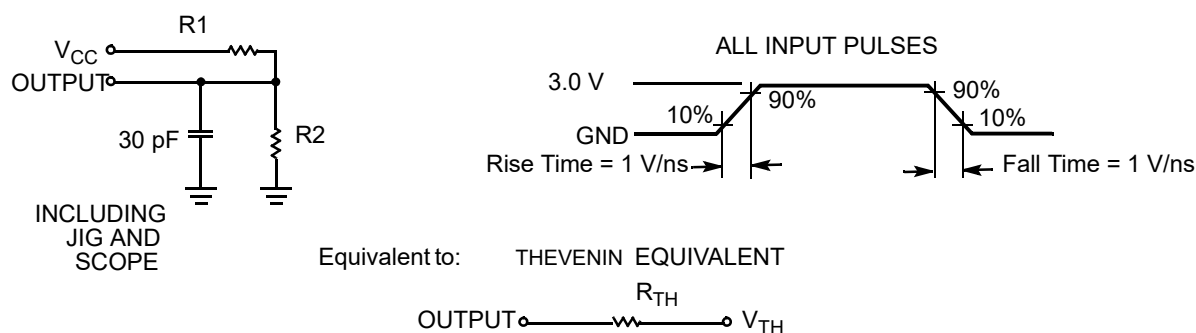
Parameter <sup>[12]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(Typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.57	59.10	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		25.01	12.19	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter <sup>[12]</sup>	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

### Note

12. Tested initially and after any design or process changes that may affect these parameters.

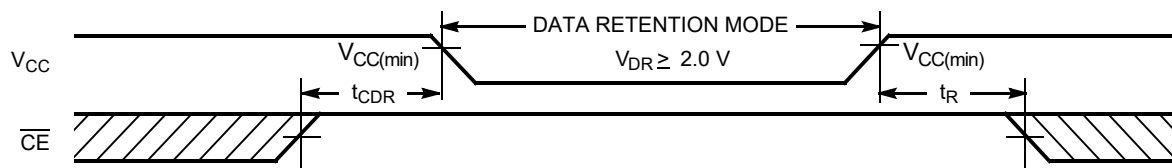
## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ <sup>[13]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	—	—	V
$I_{CCDR}^{[14]}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	—	1	7	$\mu\text{A}$
$t_{CDR}$	Chip deselect to data retention time		0	—	—	ns
$t_R^{[15]}$	Operation recovery time		45/55	—	—	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

13. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .
14. Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} > 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} > 100\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the operating range

Parameter <sup>[16, 17]</sup>	Description	45 ns		55 ns <sup>[18]</sup>		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>RC</sub>	Read cycle time	45	–	55	–	ns
t <sub>AA</sub>	Address to data valid	–	45	–	55	ns
t <sub>OHA</sub>	Data hold from address change	10	–	10	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[19]</sup>	5	–	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[19, 20]</sup>	–	18	–	20	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[19]</sup>	10	–	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[19, 20]</sup>	–	18	–	20	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle <sup>[21, 22]</sup>						
t <sub>WC</sub>	Write cycle time	45	–	55	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	40	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	40	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[19, 20]</sup>	–	18	–	20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[19]</sup>	10	–	10	–	ns

### Notes

16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note [AN66311](#). However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).

18. SOIC package is available only in 55 ns speed bin.

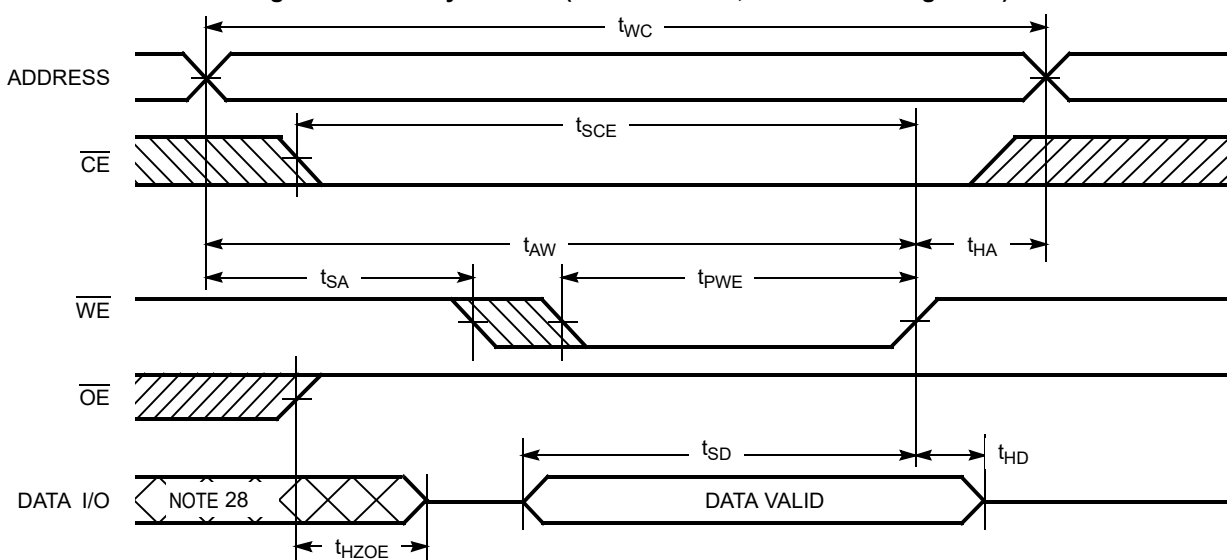
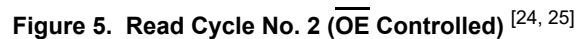
19. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

20.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

21. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

22. The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Figure 4. Read Cycle No. 1 (Address Transition Controlled) [23, 24]**

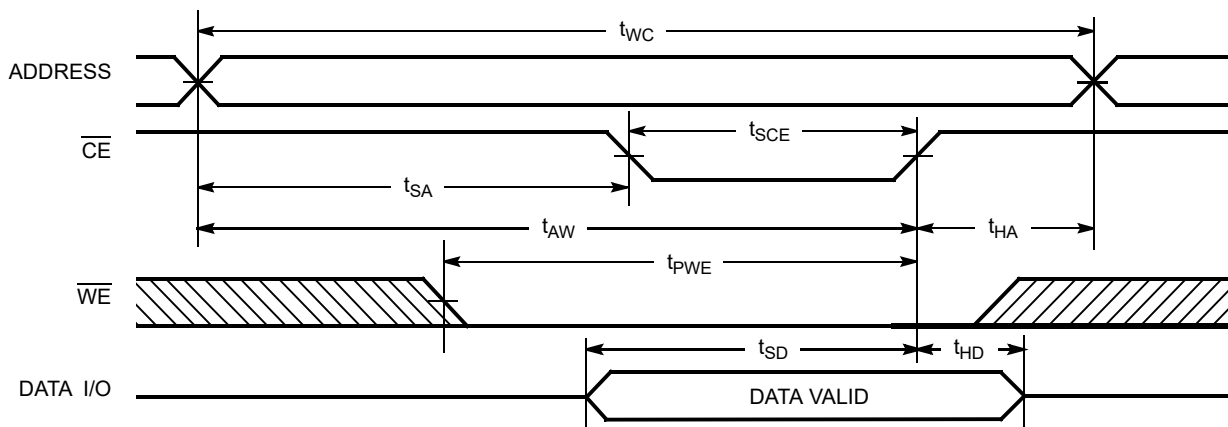


28. During this period, the I/Os are in output state and input signals must not be applied.

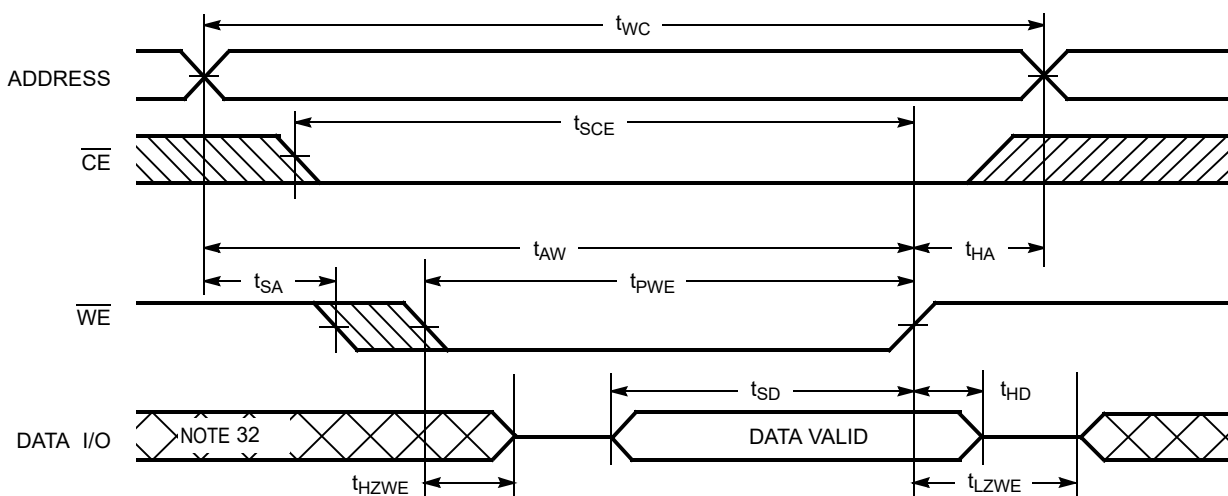


## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [29, 30]



**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [30, 31]



### Notes

29. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .

30. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.

31. The minimum write cycle pulse width should be equal to the sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

32. During this period, the I/Os are in output state and input signals must not be applied.

## Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Mode	Power
H <sup>[33]</sup>	X	X	High Z	Deselect/power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data in	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )

### Note

33. Chip enable ( $\overline{\text{CE}}$ ) must be HIGH at CMOS level to meet the  $I_{\text{SB2}}$  /  $I_{\text{CCDR}}$  spec. Other inputs can be left floating.

**Table 1** lists the CY62148E MoBL<sup>®</sup> key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>.

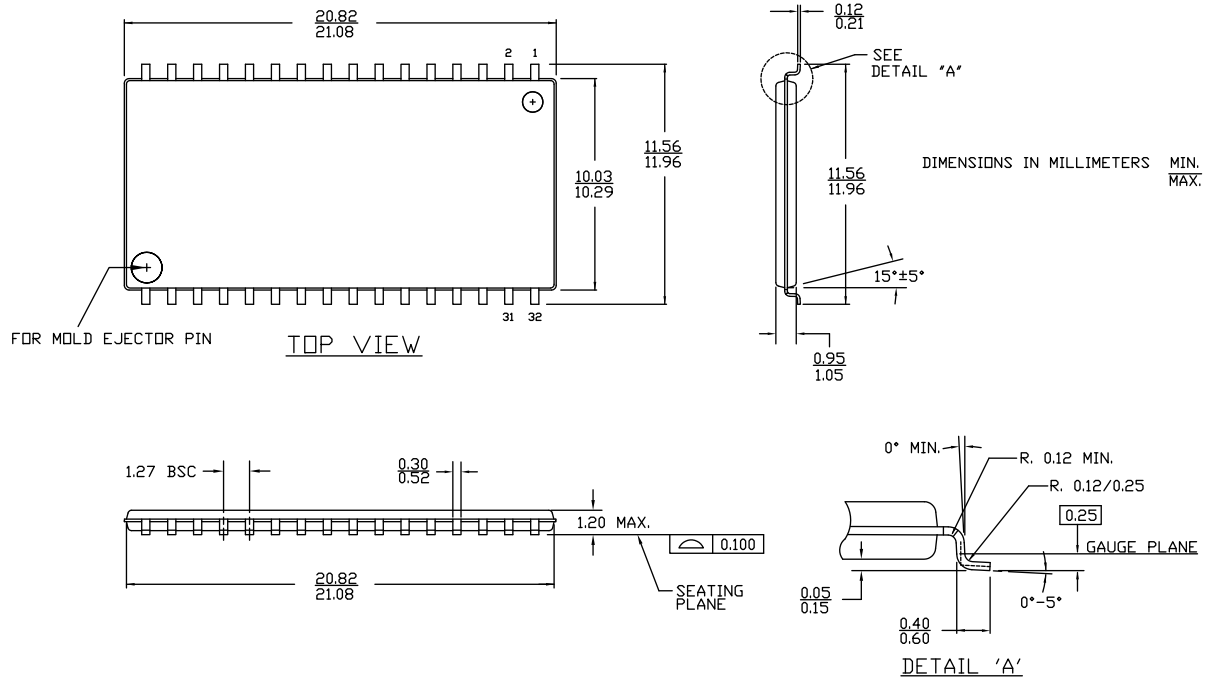
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
55	CY62148ELL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

Diagram illustrating the structure of the MoBL SRAM part number, showing the relationship between the part number fields and their corresponding specifications:

- Temperature Grade: X = I  
I = Industrial
- Pb-free
- Package Type: XX = ZS or S  
ZS = 32-pin TSOP II  
S = 32-pin SOIC
- Speed Grade: XX = 45 ns or 55 ns
- LL = Low Power
- Process Technology: E = 90 nm
- Bus Width: 8 = × 8
- Density: 4 = 4-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

## Package Diagrams

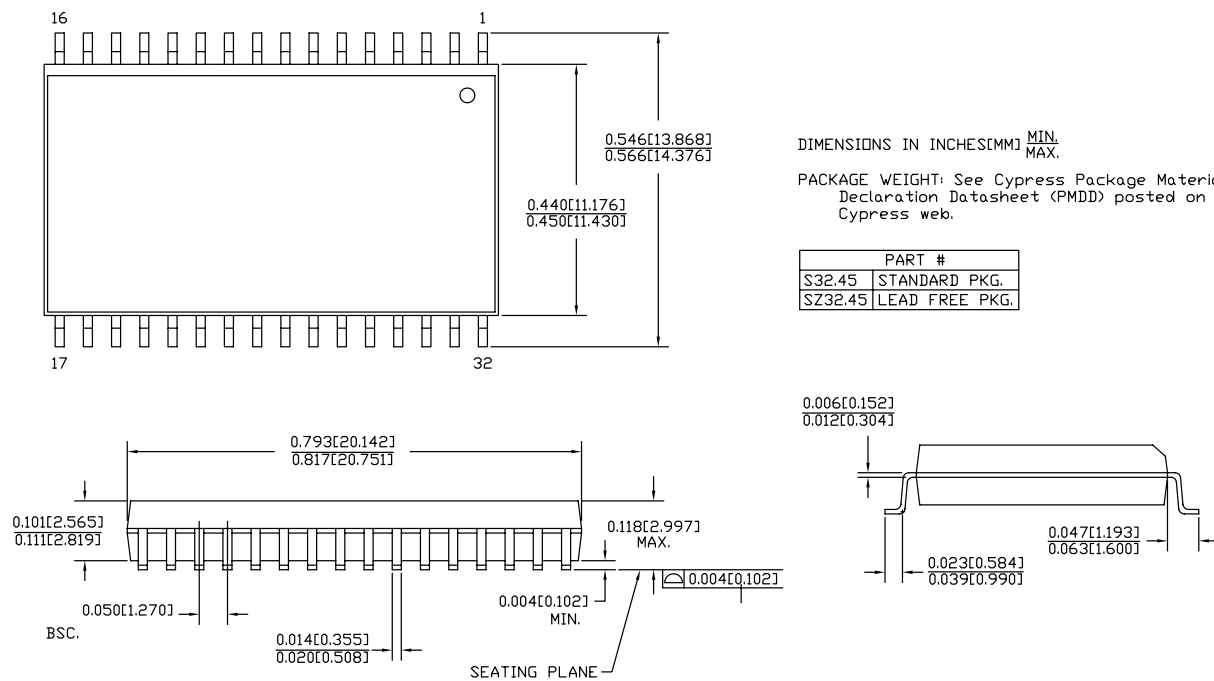
Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



51-85095 \*D

## Package Diagrams (continued)

**Figure 10. 32-pin SOIC (450 Mils) Package Outline, 51-85081**



51-85081 \*E

## Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
MoBL	More Battery Life
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62148E MoBL <sup>®</sup> , 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201580	AJU	01/08/2004	New data sheet.
*A	249276	SYT	08/03/2004	<p>Changed status from Advance Information to Preliminary.</p> <p>Updated <a href="#">Features</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Functional Description</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Pin Configurations</a> (Added RTSOP II and removed FBGA Package).</p> <p>Updated <a href="#">Operating Range</a> (Updated Note 6 (Changed V<sub>CC</sub> stabilization time from 100 μs to 200 μs)).</p> <p>Updated <a href="#">Data Retention Characteristics</a> (Changed maximum value of I<sub>CCDR</sub> parameter from 2.0 μA to 2.5 μA; changed minimum value of t<sub>R</sub> parameter from 100 μs to t<sub>RC</sub> ns).</p> <p>Updated <a href="#">Switching Characteristics</a> (Changed minimum value of t<sub>OHA</sub> parameter from 6 ns to 10 ns for both 35 ns and 45 ns speed bin; changed maximum value of t<sub>DOE</sub> parameter from 15 ns to 18 ns for 35 ns speed bin; changed maximum value of t<sub>HZOE</sub>, t<sub>HZWE</sub> parameters from 12 ns to 15 ns for 35 ns speed bin and 15 ns to 18 ns for 45 ns speed bin; changed minimum value of t<sub>SCE</sub> parameter from 25 ns to 30 ns for 35 ns speed bin and 40 ns to 35 ns for 45 ns speed bin; changed maximum value of t<sub>HZCE</sub> parameter from 12 ns to 18 ns for 35 ns speed bin and 15 ns to 22 ns for 45 ns speed bin; changed minimum value of t<sub>SD</sub> parameter from 15 ns to 18 ns for 35 ns speed bin and 20 ns to 22 ns for 45 ns speed bin).</p> <p>Updated <a href="#">Ordering Information</a> (Corrected typo in Package Name column; also updated part numbers).</p>
*B	414820	ZSD	12/16/2005	<p>Changed status from Preliminary to Final.</p> <p>Changed the address of Cypress Semiconductor Corporation on Page 1 from "3901 North First Street" to "198 Champion Court".</p> <p>Updated <a href="#">Features</a> (Removed 35 ns speed bin).</p> <p>Updated <a href="#">Pin Configurations</a> (Removed the Note "DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application." and its reference).</p> <p>Updated <a href="#">Product Portfolio</a> (Removed 35 ns speed bin).</p> <p>Updated <a href="#">Maximum Ratings</a> (Updated Note 4 (to include current limit)).</p> <p>Updated <a href="#">Electrical Characteristics</a> (Removed "L" version of CY62148E; changed typical value of I<sub>CC</sub> parameter from 1.5 mA to 2 mA at f = 1 MHz; changed maximum value of I<sub>CC</sub> parameter from 2 mA to 2.5 mA at f = 1 MHz; changed typical value of I<sub>CC</sub> parameter from 12 mA to 15 mA at f = f<sub>max</sub>; removed I<sub>SB1</sub> parameter and its details; changed typical value of I<sub>SB2</sub> parameter from 0.7 μA to 1 μA and maximum value of I<sub>SB2</sub> parameter from 2.5 μA to 7 μA).</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a> (Changed the AC test load capacitance from 100 pF to 30 pF in <a href="#">Figure 2</a>; changed test load parameters R<sub>1</sub>, R<sub>2</sub>, R<sub>TH</sub> and V<sub>TH</sub> from 1838 Ω, 994 Ω, 645 Ω and 1.75 V to 1800 Ω, 990 Ω, 639 Ω and 1.77 V).</p> <p>Updated <a href="#">Data Retention Characteristics</a> (Changed maximum value of I<sub>CCDR</sub> parameter from 2.5 μA to 7 μA; added typical value for I<sub>CCDR</sub> parameter).</p> <p>Updated <a href="#">Switching Characteristics</a> (Removed 35 ns speed bin; changed minimum value of t<sub>LZOE</sub> parameter from 3 ns to 5 ns; changed minimum value of t<sub>LZCE</sub> and t<sub>LZWE</sub> parameters from 6 ns to 10 ns; changed maximum value of t<sub>HZCE</sub> parameter from 22 ns to 18 ns; changed minimum value of t<sub>PWE</sub> parameter from 30 ns to 35 ns; changed minimum value of t<sub>SD</sub> parameter from 22 ns to 25 ns).</p> <p>Updated <a href="#">Ordering Information</a> (Updated part numbers; also removed "Package Name" column and added "Package Diagram" column).</p>

**Document History Page** (continued)

Document Title: CY62148E MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C	464503	NXR	05/25/2006	Updated <a href="#">Product Portfolio</a> (Included Automotive Range). Updated <a href="#">Operating Range</a> (Included Automotive Range). Updated <a href="#">Electrical Characteristics</a> (Included Automotive Range). Updated <a href="#">Data Retention Characteristics</a> (Included Automotive Range). Updated <a href="#">Switching Characteristics</a> (Included Automotive Range). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*D	485639	VKN	07/21/2006	Updated <a href="#">Operating Range</a> (Replaced "2.2 V to 3.6 V" with "4.5 V to 5.5 V" in "V <sub>CC</sub> " column).
*E	833080	VKN	03/09/2007	Updated <a href="#">Electrical Characteristics</a> : Added SOIC package in "Test Conditions" of V <sub>IL</sub> parameter and also added corresponding values. Added Note 10 and referred the same note in maximum value of V <sub>IL</sub> parameter corresponding to SOIC package.
*F	890962	VKN	03/09/2007	Updated <a href="#">Pin Configurations</a> (Added Note 2 and referred the same note in <a href="#">Figure 1</a> ). Updated <a href="#">Product Portfolio</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Operating Range</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Electrical Characteristics</a> (Included Automotive-A range and removed Automotive-E range; added Note 11 (related to I <sub>SB2</sub> ) and referred the same note in I <sub>SB2</sub> parameter). Updated <a href="#">Data Retention Characteristics</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Switching Characteristics</a> (Included Automotive-A range and removed Automotive-E range). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*G	2947039	VKN	06/10/2010	Updated <a href="#">Truth Table</a> (Added Note 33 and referred the same note in "CE" column). Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagrams</a> : spec 51-85095 – Changed revision from ** to *A. spec 51-85081 – Changed revision from *B to *C. Updated to new template.
*H	3006318	AJU	08/23/2010	Updated <a href="#">Data Retention Characteristics</a> (Added Note 14 and referred the same note in I <sub>CCDR</sub> parameter). Updated <a href="#">Ordering Information</a> : No change in part numbers. Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*I	3235744	RAME	04/20/2011	Updated <a href="#">Functional Description</a> (Removed the line "For best practice recommendations, refer to the Cypress application note <a href="#">AN1064</a> , <a href="#">SRAM System Guidelines</a> ."). Updated <a href="#">Package Diagrams</a> : spec 51-85095 – Changed revision from *A to *B. Completing Sunset Review.
*J	3302815	RAME	07/14/2011	Updated to new template.
*K	3539544	TAVA	03/01/2012	Updated <a href="#">Electrical Characteristics</a> (Updated Note 10). Updated <a href="#">Package Diagrams</a> : spec 51-85081 – Changed revision from *C to *D. Completing Sunset Review.



**Document History Page** (continued)

Document Title: CY62148E MoBL <sup>®</sup> , 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*L	3992135	MEMJ	05/06/2013	Updated <a href="#">Functional Description</a> : Updated description. Updated <a href="#">Electrical Characteristics</a> (Added one more Test Condition "V <sub>CC</sub> = 5.5 V, I <sub>OH</sub> = -0.1 mA" for V <sub>OH</sub> parameter and also added corresponding values). Updated <a href="#">Package Diagrams</a> : spec 51-85081 – Changed revision from *D to *E. Completing Sunset Review.
*M	4099045	VINI	08/19/2013	Updated <a href="#">Switching Characteristics</a> : Added Note 16 and referred the same note in "Parameter" column. Updated to new template.
*N	4576526	VINI	11/21/2014	Updated <a href="#">Features</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end. Updated <a href="#">Switching Characteristics</a> : Added Note 22 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 31 and referred the same note in <a href="#">Figure 8</a> .
*O	4794169	NILE	06/11/2015	Updated <a href="#">Package Diagrams</a> : spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*P	5285890	VINI	06/01/2016	Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated all values in "32-pin SOIC Package" and "32-pin TSOP II Package" columns. Updated <a href="#">Data Retention Characteristics</a> : Removed details in "Conditions" column corresponding to t <sub>R</sub> parameter (To match the speed grade). Updated to new template. Completing Sunset Review.
*Q	6072272	VINI	02/15/2018	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*R	6533264	VINI	04/04/2019	Updated to new template. Completing Sunset Review.

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