

# FailSafe™ PacketClock Global Communications Clock Generator

## Features

- Fully Integrated Phase-Locked Loop (PLL)
- FailSafe™ Output
- 8 kHz Reference Clock
- PLL Driven by a Crystal Oscillator that is Phase Aligned with External Reference
- Selectable Standard Communication Output Frequencies
- Low Jitter, High Accuracy Outputs
- 3.3 V Operation
- 16-pin TSSOP Package
- Commercial and Industrial Temperature Ranges

## Functional Description

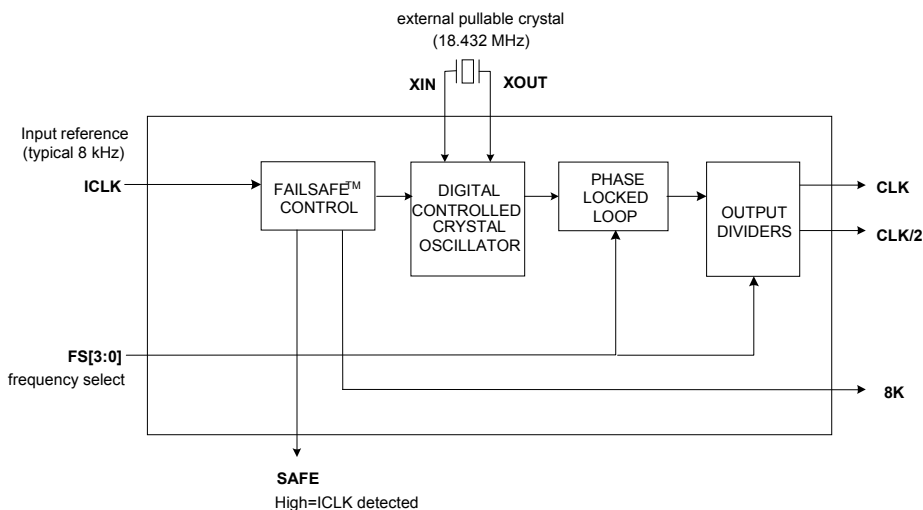
CY26049 is a FailSafe frequency synthesizer with a reference clock input and three clock outputs. The device provides an optimum solution for applications which require continuous operation in case of primary clock failure. The continuous, glitch-free operation is achieved by using a DCXO which serves as a primary clock source. The FailSafe control circuit synchronizes the DCXO with the reference as long as the reference is within the pull range of the crystal.

In the event of a reference clock failure the DCXO maintains the last frequency and phase information of the reference clock. The unique feature of the CY26049-36 is that the DCXO is, in fact, the primary clocking source. When the reference clock is restored, the DCXO automatically resynchronizes to the reference. The status of the reference clock input, as detected by the CY26049-36, is reported by the SAFE pin.

In the buffer mode (FS3:FS0 = 1110 or 1111), the CY26049-36 can be used as a jitter attenuator. In this mode, extensive jitter on the input clock is 'filtered', resulting in a low jitter output clock.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

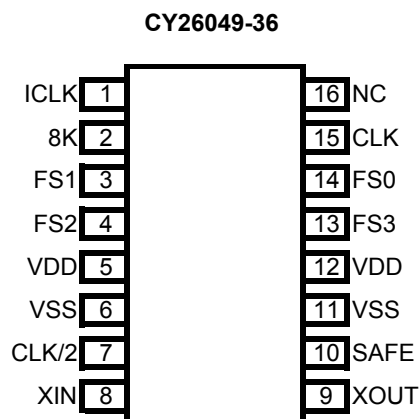


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## Pin Configuration

Figure 1. 16-pin TSSOP pinout (Top View)



## Pin Definitions

| Pin Name | Pin Number | Pin Description   |
|----------|------------|---|
| ICLK     | 1          | <b>Reference Input Clock</b> ; 8 kHz or 10 to 60 MHz.   |
| 8K       | 2          | <b>Clock Output</b> ; 8 kHz or high impedance in buffer mode.                                       |
| FS1      | 3          | <b>Frequency Select 1</b> ; Determines CLK outputs according to <a href="#">Table 1 on page 4</a> . |
| FS2      | 4          | <b>Frequency Select 2</b> ; Determines CLK outputs according to <a href="#">Table 1 on page 4</a> . |
| VDD      | 5          | <b>Voltage Supply</b> ; 3.3 V.  |
| VSS      | 6          | <b>Ground</b>   |
| CLK/2    | 7          | <b>Clock Output</b> ; Frequency according to <a href="#">Table 1 on page 4</a> .                    |
| XIN      | 8          | <b>Pullable Crystal Input</b> ; 18.432 MHz.   |
| XOUT     | 9          | <b>Pullable Crystal Output</b> ; 18.432 MHz.  |
| SAFE     | 10         | <b>High = reference ICLK within range, Low = reference ICLK out of range.</b>                       |
| VSS      | 11         | <b>Ground</b>   |
| VDD      | 12         | <b>Voltage Supply</b> ; 3.3 V.  |
| FS3      | 13         | <b>Frequency Select 3</b> ; Determines CLK outputs according to <a href="#">Table 1 on page 4</a> . |
| FS0      | 14         | <b>Frequency Select 0</b> ; Determines CLK outputs according to <a href="#">Table 1 on page 4</a> . |
| CLK      | 15         | <b>Clock Output</b> ; Frequency according to <a href="#">Table 1 on page 4</a> .                    |
| NC       | 16         | <b>No Connect</b>   |

## Frequency Select Tables

**Table 1. CY26049-36 Frequency Select–Output Decoding Table–External Mode (MHz except as noted)**

| ICLK  | FS3 | FS2 | FS1 | FS0 | CLK/2                 | CLK                   | 8K                    | Crystal |
|-------|-----|-----|-----|-----|-----------------------|-----------------------|-----------------------|---------|
| 8 kHz | 0   | 0   | 0   | 0   | 1.544                 | 3.088                 | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 0   | 0   | 1   | 2.048                 | 4.096                 | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 0   | 1   | 0   | 22.368                | 44.736                | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 0   | 1   | 1   | 17.184                | 34.368                | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 1   | 0   | 0   | 77.76                 | 155.52                | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 1   | 0   | 1   | 16.384                | 32.768                | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 1   | 1   | 0   | 14.352                | 28.704                | 8 kHz                 | 18.432  |
| 8 kHz | 0   | 1   | 1   | 1   | High Z <sup>[1]</sup> | High Z <sup>[1]</sup> | High Z <sup>[1]</sup> | 18.432  |
| 8 kHz | 1   | 0   | 0   | 0   | 18.528                | 37.056                | 8 kHz                 | 18.432  |
| 8 kHz | 1   | 0   | 0   | 1   | 12.352                | 24.704                | 8 kHz                 | 18.432  |
| 8 kHz | 1   | 0   | 1   | 0   | 7.68                  | 15.36                 | 8 kHz                 | 18.432  |
| 8 kHz | 1   | 0   | 1   | 1   | High Z <sup>[1]</sup> | High Z <sup>[1]</sup> | High Z <sup>[1]</sup> | 18.432  |
| 8 kHz | 1   | 1   | 0   | 0   | 12.288                | 24.576                | 8 kHz                 | 18.432  |
| 8 kHz | 1   | 1   | 0   | 1   | 16.384                | 32.768                | 8 kHz                 | 18.432  |

**Table 2. CY26049-36 Frequency Select–Output Decoding Table–Buffer Mode**

| ICLK         | FS3 | FS2 | FS1 | FS0 | CLK/2    | CLK      | 8K                    | Crystal |
|--------------|-----|-----|-----|-----|----------|----------|-----------------------|---------|
| 20 to 60 MHz | 1   | 1   | 1   | 0   | ICLK/2   | ICLK     | High Z <sup>[1]</sup> | ICLK/2  |
| 10 to 30 MHz | 1   | 1   | 1   | 1   | 2 × ICLK | 4 × ICLK | High Z <sup>[1]</sup> | ICLK    |

**Note**

1. High Z = high impedance.

## Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply Voltage ( $V_{DD}$ ) ..... -0.5 to +7.0 V

DC Input Voltage ..... -0.5 V to  $V_{DD} + 0.5$  V

Storage Temperature

(Non-Condensing) ..... -55 °C to +125 °C

Junction Temperature ..... -40 °C to +125 °C

Data Retention at  $T_J = 125$  °C ..... > 10 years

Package Power Dissipation ..... 350 mW

ESD (Human Body Model) MIL-STD-883 ..... 2000 V

## Recommended Pullable Crystal Specifications

| Parameter <sup>[2]</sup> | Description  | Comments  | Min  | Typ    | Max  | Units    |
|--------------------------|--|---|------|--------|------|----------|
| $F_{NOM}$                | Nominal crystal frequency                                | Parallel resonance, fundamental mode, AT cut                                | –    | 18.432 | –    | MHz      |
| $C_{LNOM}$               | Nominal load capacitance                                 |   | –    | 14     | –    | pF       |
| $R_1$                    | Equivalent series resistance (ESR)                       | Fundamental mode  | –    | –      | 25   | $\Omega$ |
| $R_3/R_1$                | Ratio of third overtone mode ESR to fundamental mode ESR | Ratio used because typical $R_1$ values are much less than the maximum spec | 3    | –      | –    |          |
| DL                       | Crystal drive level                                      | No external series resistor assumed   | –    | 0.5    | 2    | mW       |
| $F_{3SEPHI}$             | Third overtone separation from $3 \times F_{NOM}$        | High side   | 400  | –      | –    | ppm      |
| $F_{3SEPLO}$             | Third overtone separation from $3 \times F_{NOM}$        | Low side  | –    | –      | –200 | ppm      |
| $C_0$                    | Crystal shunt capacitance                                |   | –    | –      | 7    | pF       |
| $C_0/C_1$                | Ratio of shunt to motional capacitance                   |   | 180  | –      | 250  |          |
| $C_1$                    | Crystal motional capacitance                             |   | 14.4 | 18     | 21.6 | fF       |

## Recommended Operating Conditions

| Parameter   | Description   | Min  | Typ | Max  | Unit |
|-------------|---|------|-----|------|------|
| $V_{DD}$    | Operating Voltage   | 3.15 | 3.3 | 3.45 | V    |
| $T_{AC}$    | Ambient Temperature (Commercial Temperature)  | 0    | –   | 70   | °C   |
| $T_{AI}$    | Ambient Temperature (Industrial Temperature)  | –40  | –   | 85   | °C   |
| $C_{LOAD}$  | Max Output Load Capacitance   | –    | –   | 15   | pF   |
| $t_{PU}$    | Power up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | –   | 500  | ms   |
| $t_{ER(I)}$ | 8 kHz Input Edge Rate, 20% to 80% of $V_{DD} = 3.3$ V   | 0.07 | –   | –    | V/ns |

### Note

2. Ecliptek crystals ECX-5761-18.432 M and ECX-5762-18.432 M meet these specifications.

## DC Electrical Specifications

Commercial Temperature: 0 °C to 70 °C

| Parameter | Description            | Test Conditions   | Min | Typ     | Max | Unit          |
|-----------|------------------------|---|-----|---------|-----|---------------|
| $I_{OH}$  | Output High Current    | $V_{OH} = V_{DD} - 0.5 \text{ V}$ ,<br>$V_{DD} = 3.3 \text{ V}$ (source)    | 12  | 24      | –   | mA            |
| $I_{OL}$  | Output Low Current     | $V_{OL} = 0.5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}$ (sink)                  | 12  | 24      | –   | mA            |
| $V_{IH}$  | Input High Voltage     | CMOS Levels   | 0.7 | –       | –   | $V_{DD}$      |
| $V_{IL}$  | Input High Voltage     | CMOS Levels   | –   | –       | 0.3 | $V_{DD}$      |
| $I_{IH}$  | Input High Current     | $V_{IH} = V_{DD}$   | –   | 5       | 10  | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current      | $V_{IL} = 0 \text{ V}$  | –   | 5       | 10  | $\mu\text{A}$ |
| $C_{IN}$  | Input Capacitance      |   | –   | –       | 7   | pF            |
| $I_{OZ}$  | Output Leakage Current | High Z <sup>[3]</sup> output  | –   | $\pm 5$ | –   | $\mu\text{A}$ |
| $I_{DD}$  | Supply Current         | $C_{LOAD} = 15 \text{ pF}$ , $V_{DD} = 3.45 \text{ V}$ ,<br>FS [3:0] = 0100 | –   | –       | 45  | mA            |
|           |                        | $C_{LOAD} = 15 \text{ pF}$ , $V_{DD} = 3.45 \text{ V}$ ,<br>FS [3:0] = 1101 | –   | –       | 30  | mA            |

## DC Electrical Specifications

Industrial Temperature: –40 °C to 85 °C

| Parameter | Description            | Test Conditions   | Min | Typ     | Max | Unit          |
|-----------|------------------------|---|-----|---------|-----|---------------|
| $I_{OH}$  | Output High Current    | $V_{OH} = V_{DD} - 0.5 \text{ V}$ ,<br>$V_{DD} = 3.3 \text{ V}$ (source)    | 10  | 20      | –   | mA            |
| $I_{OL}$  | Output Low Current     | $V_{OL} = 0.5 \text{ V}$ , $V_{DD} = 3.3 \text{ V}$ (sink)                  | 10  | 20      | –   | mA            |
| $V_{IH}$  | Input High Voltage     | CMOS Levels   | 0.7 | –       | –   | $V_{DD}$      |
| $V_{IL}$  | Input High Voltage     | CMOS Levels   | –   | –       | 0.3 | $V_{DD}$      |
| $I_{IH}$  | Input High Current     | $V_{IH} = V_{DD}$   | –   | 5       | 10  | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current      | $V_{IL} = 0 \text{ V}$  | –   | 5       | 10  | $\mu\text{A}$ |
| $C_{IN}$  | Input Capacitance      |   | –   | –       | 7   | pF            |
| $I_{OZ}$  | Output Leakage Current | High Z <sup>[3]</sup> output  | –   | $\pm 5$ | –   | $\mu\text{A}$ |
| $I_{DD}$  | Supply Current         | $C_{LOAD} = 15 \text{ pF}$ , $V_{DD} = 3.45 \text{ V}$ ,<br>FS [3:0] = 0100 | –   | –       | 50  | mA            |
|           |                        | $C_{LOAD} = 15 \text{ pF}$ , $V_{DD} = 3.45 \text{ V}$ ,<br>FS [3:0] = 1101 | –   | –       | 35  | mA            |

## Thermal Resistance

| Parameter <sup>[4]</sup> | Description                                 | Test Conditions   | 16-pin TSSOP | Unit |
|--------------------------|---|---|--------------|------|
| $\theta_{JA}$            | Thermal resistance<br>(junction to ambient) | Test conditions follow standard test methods and<br>procedures for measuring thermal impedance, in<br>accordance with EIA/JESD51. | 89           | °C/W |
| $\theta_{JC}$            | Thermal resistance<br>(junction to case)    |   | 12           | °C/W |

### Notes

3. High Z = high impedance.

4. These parameters are guaranteed by design and are not tested.

## AC Electrical Specifications

Commercial Temperature: 0 °C to 70 °C and Industrial Temperature: –40 °C to 85 °C

| Parameter                 | Description                        | Test Conditions  | Min  | Typ  | Max  | Unit |
|---------------------------|------------------------------------|--|------|------|------|------|
| $f_{\text{ICLK-E}}$       | Frequency, Input Clock             | Input Clock Frequency, External Mode   | –    | 8.00 | –    | kHz  |
| $f_{\text{ICLK-B}}$       | Frequency, Input Clock             | Input Clock Frequency, Buffer Mode   | 10   | –    | 60   | MHz  |
| LR                        | FailSafe Lock Range <sup>[5]</sup> | Range of reference ICLK for Safe = High  | –250 | –    | +250 | ppm  |
| $t_{\text{DC}} = t_2/t_1$ | Output Duty Cycle                  | Duty Cycle defined in Figure 2, measured at 50% of $V_{\text{DD}}$   | 45   | 50   | 55   | %    |
| $t_{\text{PJIT1}}$        | Clock Jitter; output > 5 MHz       | Period Jitter, Peak to Peak, 10,000 periods  | –    | –    | 250  | ps   |
|                           |                                    | RMS Period Jitter, RMS   | –    | –    | 50   | ps   |
| $t_{\text{PJIT2}}$        | Clock Jitter; output < 5 MHz       | Period Jitter, Peak to Peak, 10,000 periods  | –    | –    | 500  | ps   |
|                           |                                    | RMS Period Jitter, RMS   | –    | –    | 100  | ps   |
| $t_{\text{P\_LOCK}}$      | PLL Lock Time <sup>[6]</sup>       | Time for PLL to lock within $\pm 150$ ppm of target frequency  | –    | –    | 3    | ms   |
| $t_{\text{FS\_LOCK}}$     | Failsafe Lock Time <sup>[6]</sup>  | Time for PLL to lock to ICKL (outputs phase aligned with ICKL and Safe = High)                                 | –    | –    | 7    | s    |
| $f_{\text{ERROR}}$        | Frequency Synthesis Error          | Actual mean frequency error versus target  | –    | 0    | –    | ppm  |
| ER                        | Rising Edge Rate                   | Output Clock Edge Rate, Measured from 20% to 80% of $V_{\text{DD}}$ , $C_{\text{LOAD}} = 15$ pF. See Figure 3. | 0.8  | 1.4  | 2    | V/ns |
| EF                        | Falling Edge Rate                  | Output Clock Edge Rate, Measured from 20% to 80% of $V_{\text{DD}}$ , $C_{\text{LOAD}} = 15$ pF. See Figure 3. | 0.8  | 1.4  | 2    | V/ns |

## Voltage and Timing Definitions

Figure 2. Duty Cycle Definition;  $\text{DC} = t_2/t_1$

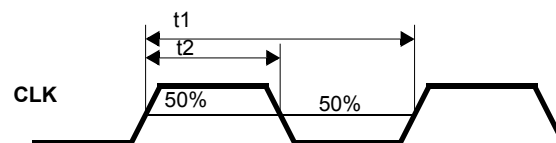
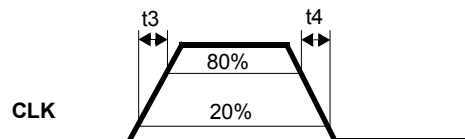


Figure 3. Rise and Fall Time Definitions:  $\text{ER} = 0.6 \times V_{\text{DD}} / t_3$ ,  $\text{EF} = 0.6 \times V_{\text{DD}} / t_4$

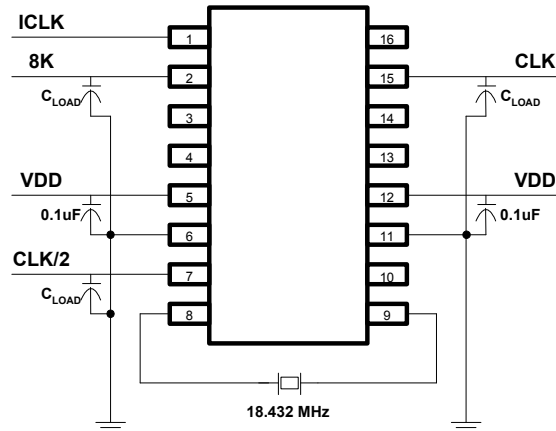


### Notes

5. Dependent on crystals chosen and crystal specs.
6. Lock times are measured beginning when  $V_{\text{DD}}$  has reached its minimum specified value and ICLK is stable.

## Test Circuit

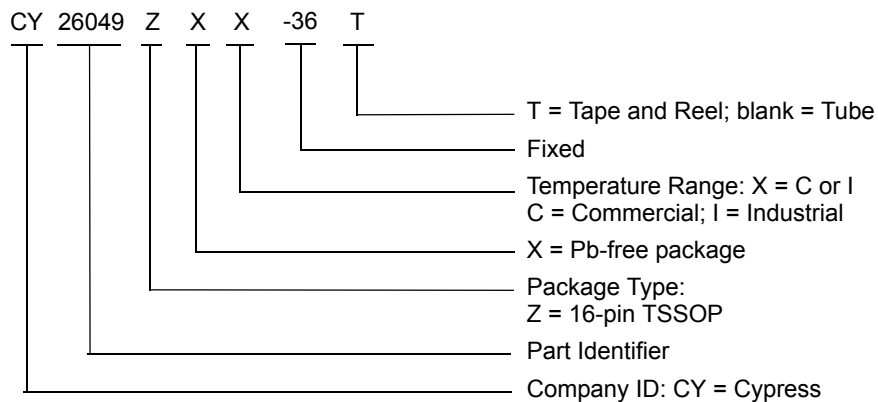
Figure 4. Test Circuit



## Ordering Information

| Ordering Code  | Package Type               | Operating Temperature Range |
|----------------|----------------------------|-----------------------------|
| <b>Pb-free</b> |                            |                             |
| CY26049ZXC-36  | 16-pin TSSOP               | Commercial, 0 °C to 70 °C   |
| CY26049ZXC-36T | 16-pin TSSOP–Tape and Reel | Commercial, 0 °C to 70 °C   |
| CY26049ZXI-36  | 16-pin TSSOP               | Industrial, –40 °C to 85 °C |
| CY26049ZXI-36T | 16-pin TSSOP–Tape and Reel | Industrial, –40 °C to 85 °C |

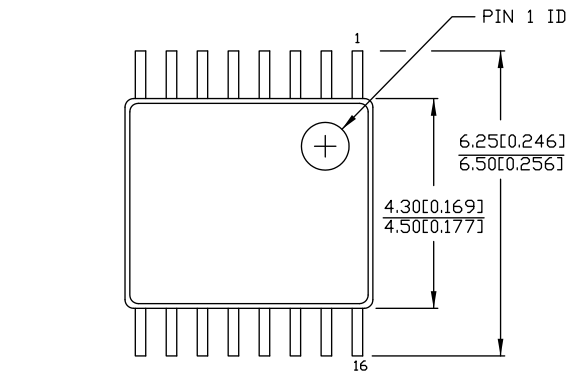
## Ordering Code Definitions





## Package Diagram

**Figure 5. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091**

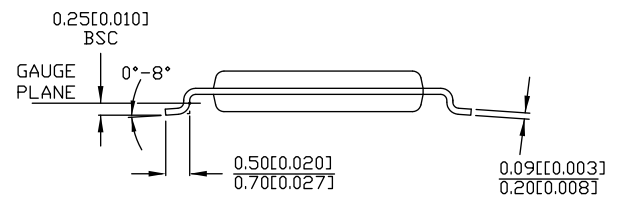
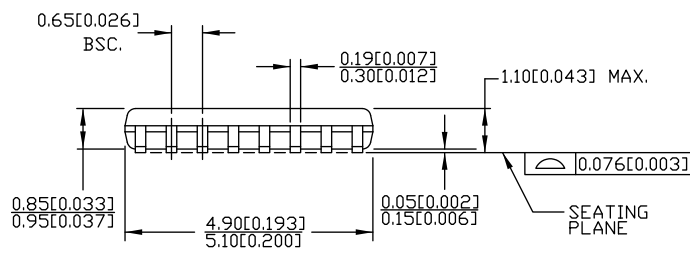


DIMENSIONS IN MM[INCHES] MIN.  
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

| PART #   |                |
|----------|----------------|
| Z16.173  | STANDARD PKG.  |
| ZZ16.173 | LEAD FREE PKG. |



51-85091 \*E

## Acronyms

| Acronym | Description                                |
|---------|--|
| CMOS    | Complementary Metal Oxide Semiconductor    |
| DCXO    | Digital Controlled Crystal Oscillator      |
| ESD     | Electrostatic Discharge                    |
| ESR     | Equivalent Series Resistance               |
| JEDEC   | Joint Electron Devices Engineering Council |
| PLL     | Phase Locked Loop                          |
| TSSOP   | Thin Shrunk Small Outline Package          |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure   |
|--------|-------------------|
| °C     | degree Celsius    |
| fF     | femtofarad        |
| kHz    | kilohertz         |
| MHz    | megahertz         |
| μA     | microampere       |
| mA     | milliampere       |
| mm     | millimeter        |
| ms     | millisecond       |
| mW     | milliwatt         |
| ns     | nanosecond        |
| Ω      | ohm               |
| %      | percent           |
| pF     | picofarad         |
| ppm    | parts per million |
| ps     | picosecond        |
| s      | second            |
| V      | volt              |

## Document History Page

| Document Title: CY26049-36, FailSafe™ PacketClock Global Communications Clock Generator<br>Document Number: 38-07415 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Rev.   | ECN No. | Submission Date | Orig. of Change | Description of Change   |
| **   | 114749  | 08/08/02        | CKN             | New data sheet  |
| *A   | 120067  | 01/06/03        | CKN             | Changed "FailSafe is a trademark of Silicon Graphics, Inc." to read "FailSafe is a trademark of Cypress Semiconductor"  |
| *B   | 128000  | 07/15/03        | IJA             | Changed Benefits to read "When reference is in range, SAFE pin is driven high"<br>Changed first sentence to "CY26049 is a FailSafe frequency synthesizer with a reference clock input and three clock outputs"<br>Changed title from "Failsafe™ PacketClock™ Global Communications Clocks" to "FailSafe™ PacketClock™ Global Communications Clock Generator"<br>Changed definitions in Pin Description Table<br>Replaced format for Absolute Maximum Conditions<br>Replaced Recommended Pullable Crystal Specifications table<br>Added $t_{pu}$ to Recommended Operating Conditions<br>Added $I_{IH}$ and $I_{IL}$ to DC Electrical Specifications<br>Replaced AC Electrical Specifications from CY26049-16 data sheet<br>Changed Voltage and Timing Definitions to match CY2410 data sheet<br>Moved Package Diagram to end of data sheet |
| *C   | 244412  | See ECN         | RGL             | Spec. ( $t_{ER(I)}$ ) Input Edge Rate in the Recommended Operating Conditions Table<br>Added Lead Free Devices  |
| *D   | 2865396 | 01/25/2010      | TSAI / KVM      | Added 8 kHz ref clock to p. 1 Features<br>Moved Functional Description to p. 1, replacing Benefits section<br>Removed Selector Guide table<br>Added units (MHz) to ICLK column of <a href="#">Table 2</a><br>Standardized parameter name capitalization in AC Electrical table<br>Changed timing parameter name $t_6$ to $t_{P\_LOCK}$<br>Added footnote for $t_{P\_LOCK}$ and $t_{FS\_LOCK}$<br>Remove part numbers CY26049ZC-36, CY26049ZC-36T, CY26049ZI-36 and CY26049ZI-36T<br>Updated to new template.<br>Post to external web.   |
| *E   | 2925613 | 04/30/10        | KVM             | Posting to external web.  |
| *F   | 3377436 | 09/20/2011      | PURU            | Added <a href="#">Ordering Code Definitions</a> .<br>Updated <a href="#">Package Diagram</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template.   |
| *G   | 4545891 | 10/20/2014      | TAVA            | Updated <a href="#">Package Diagram</a> :<br>spec 51-85091 – Changed revision from *C to *E.<br>Updated to new template.<br>Completing Sunset Review.   |
| *H   | 4587350 | 12/05/2014      | TAVA            | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end.  |
| *I   | 5281528 | 05/23/2016      | PSR             | Added <a href="#">Thermal Resistance</a> .<br>Updated to new template.  |

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| Touch Sensing                 | <a href="http://cypress.com/touch">cypress.com/touch</a>           |
| USB Controllers               | <a href="http://cypress.com/usb">cypress.com/usb</a>               |
| Wireless/Rf                   | <a href="http://cypress.com/wireless">cypress.com/wireless</a>     |

#### PSoC® Solutions

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#### Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

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