PRELIMINARY

CY22701

1 PLL In-System Programmable Clock Generator

Features

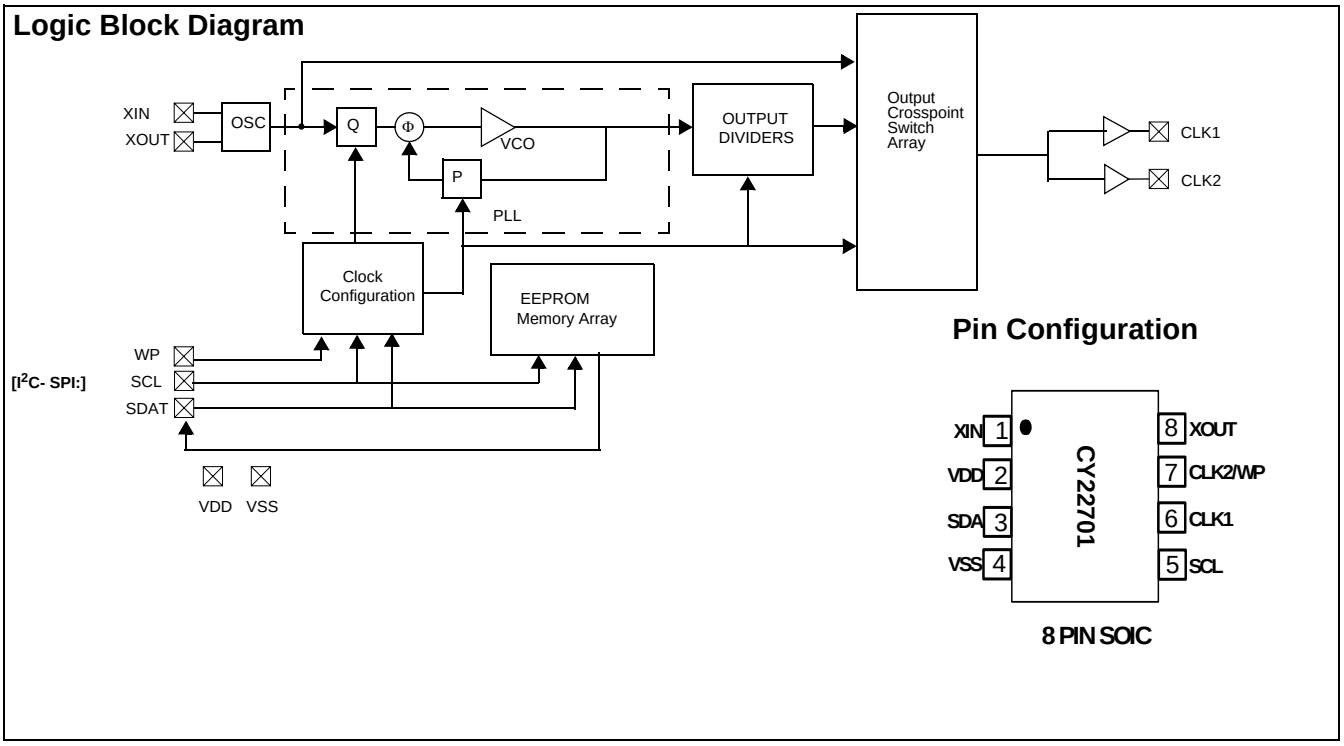
- In-system programmable through I^2C Serial Programming Interface (SPI)
- Programmable SRAM and non-volatile EEPROM memory bits with 3.3V supply
- Integrated, phase-locked loop with programmable P and Q counters, output dividers
- Low-jitter, high-accuracy outputs
- 3.3V Operation
- 8-lead SOIC

Benefits

- Custom timing solutions for designs not suitable for factory custom silicon, Xtals, or ASICs for production
- Program and optimize designs while chip is on system board
- Programming voltages contained in chip
- High-performance PLL enables control of output frequencies that are customizable to support a wide range of applications
- Meets critical timing requirements in complex system designs
- Meets industry-standard voltage platforms
- Industry standard packaging saves on board space

Part Number	No. of Outputs	Input Frequency Range	Output Frequency Range
CY22701	2	1 – 167 MHz (Driven Clock Input) {Commercial} 1 –150 MHz (Driven Clock Input) {Industrial} 8 – 30 MHz (Crystal Reference) {Comm. or Ind.}	80 kHz – 200 MHz (3.3V) {Commercial} 80 kHz –167 MHz (3.3V) {Industrial}

Logic Block Diagram



Pin Configuration

8 PIN SOIC

Pin Description

Name	Pin Number	Description
XIN	1	Reference crystal input
VDD	2	3.3V voltage supply
SDAT	3	Data input for serial programming
VSS	4	Ground
SCL	5	Clock signal input for serial programming
CLK1	6	Clock output 1 (Default to reference frequency)
CLK2/WP	7	Clock output 2/Write Protect (Default Write Protect)
XOUT[1]	8	Reference crystal output

Functional Description

The CY22701 uses an EEPROM array along with on-chip programming voltages to program the device for development, or in production on the circuit board. An industry standard I^2C serial programming interface (SPI) is used to program the scratchpad and clock core.

Clock Features

The programmable clock core is configured with the following features:

- **Crystal Oscillator**: Programmable drive and load, support for external references up to 167 MHz. See Reference Frequency (REF) on page 4
- **PLL**: Programmable P, Q, offset, and loop filter parameters.
- **Outputs**: 2 outputs and two programmable linear dividers. The output swing of CLK1 and 2 is set by VDD (3.3V).

Clock configuration is stored in a dedicated 2-kbit block of nonvolatile EEPROM and a 2-kbit block of volatile SRAM. The SPI is used to write new configuration data to the on-chip programmable registers that are defined within the clock configuration memory blocks.

Serial Programming Interface (SPI)

The SPI uses industry-standard signaling in both standard and fast modes to program the 2-kbit EEPROM dedicated to clock configuration, and the 2-kbit SRAM block. See sections beginning with Using the Serial Programming Interface on page 2 for more information.

Default Start-up Condition for CY22701

The default clock configuration is:

- The crystal oscillator circuit is active.
- CLK1 outputs REF frequency.
- Pin 7 is configured as Write Protect (see “Write Protect (WP) Registers” section on page 5 to configure as CLK2)

This default clock configuration is typically customized to meet the needs of a specific application. It provides a clock signal upon power-on, to facilitate in-system programming. Alternatively, the CY22701 may be programmed with a different clock configuration prior to placement of the CY22701 in systems. While you can develop your own subroutine to program any or all of the individual registers described in the following pages, it may be easier to use CyberClocks™ to produce the required register setting file.

Using the Serial Programming Interface

The CY22701 provides an industry-standard serial programming interface for volatile and nonvolatile, in-system programming of unique frequencies and options. Serial programming and reprogramming allows for quick design changes and product enhancements, eliminates inventory of old design parts, and simplifies manufacturing.

The CY22701 is a group of two slave devices with addresses as shown in *Figure 1*. The serial programming interface address of the CY22701 clock configuration 2-kbit EEPROM block is 68H. The serial programming interface address of the CY22701 clock configuration 2-kbit SRAM block is 69H. Should there be a conflict with any other devices in your system, both device addresses can also be changed using CyberClocks. Registers in the clock configuration 2-kbit SRAM memory block are written, when the user wants to update the clock configuration for on-the-fly changes. Registers in the clock configuration EEPROM block are written, if the user wants to update the clock configuration so that it is saved and used again after power-up or reset.

All programmable registers in the CY22701 are addressed with eight bits and contain eight bits of data. *Table 1* lists the specific register definitions and their allowable values. See section Serial Programming Interface Timing on page 10, for a detailed description.

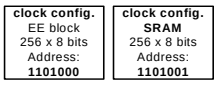


Figure 1. Device Addresses for EEPROM and SRAM Clock Configuration Blocks

Note:
1. Float XOUT if XIN is externally driven.

Table 1. Summary Table – CY22701 Programmable Registers

Register	Description	D7	D6	D5	D4	D3	D2	D1	D0
09H	CLKOE control	0	0	0	CLK2	CLK1	0	0	0
OCH	DIV1SRC mux and DIV1N divider	DIV1SRC	DIV1N(6)	DIV1N(5)	DIV1N(4)	DIV1N(3)	DIV1N(2)	DIV1N(1)	DIV1N(0)
11H	Write Protect registers	0	0	0	0	WPSrc Default=0	1	0	0
12H	Input crystal oscillator drive control	0	0	XCapSrc default=1	XDRV(1)	XDRV(0)	0	0	0
13H	Input load capacitor control	CapLoad (7)	CapLoad (6)	CapLoad (5)	CapLoad (4)	CapLoad (3)	CapLoad (2)	CapLoad (1)	CapLoad (0)
40H	Charge Pump and PB counter	1	1	0	Pump(2)	Pump(1)	Pump(0)	PB(9)	PB(8)
41H		PB(7)	PB(6)	PB(5)	PB(4)	PB(3)	PB(2)	PB(1)	PB(0)
42H	PO counter, Q counter	PO	Q(6)	Q(5)	Q(4)	Q(3)	Q(2)	Q(1)	Q(0)
45H	Crosspoint switch matrix control	1	CLKSRC2 for CLK1	CLKSRC1 for CLK1	CLKSRC0 for CLK1	CLKSRC2 for CLK2	CLKSRC1 for CLK2	CLKSRC0 for CLK2	1
47H	DIV2SRC mux and DIV2N divider	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV1N(1)	DIV2N(0)

CY22701 Frequency Calculation and Register Definitions

The CY22701 is an extremely flexible clock generator with three basic variables that can be used to determine the final output frequency:

1. Input reference frequency (REF)
2. the internally calculated P and Q dividers
3. Post divider, which can be a fixed or calculated value.

There are three basic formulas for determining the final output frequency of a CY22701-based design. Any one of these three formulas may be used:

CLK = ((REF * Ptotal)/Qtotal)/Post Divider

CLK = REF/Post Divider

CLK = REF

The basic PLL block diagram is shown in *Figure 2*. Each of the two clock outputs on the CY22701 has a total of seven output options available to it. There are six post divider options available: /2 (two of these), /3, /4, /DIV1N and /DIV2N. DIV1N and DIV2N are independently calculated and are applied to individual output groups. The post divider options can be applied to the calculated VCO frequency ((REF*P)/Q) or to the reference frequency directly.

In addition to the six post divider output options, the seventh option bypasses the PLL and passes the reference frequency directly to the crosspoint switch matrix.

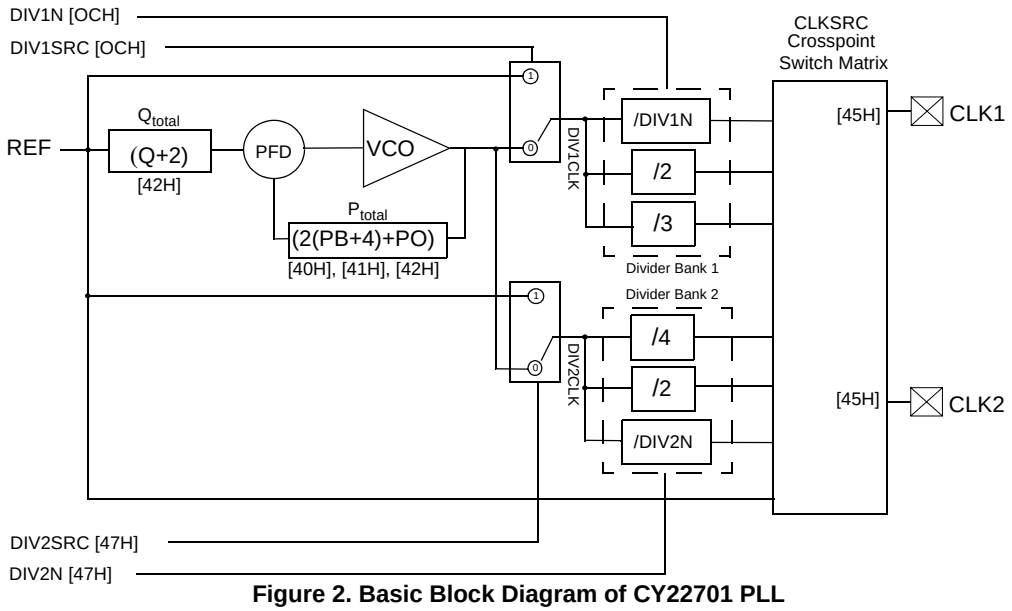


Figure 2. Basic Block Diagram of CY22701 PLL

Reference Frequency (REF)

The reference frequency can be a crystal or a driven frequency. For crystals, the frequency range must be between 8 MHz and 30 MHz. For a driven frequency, the frequency range must be between 1 MHz and 167 MHz (Commercial Temp.) or 150 MHz (Industrial Temp.).

Using a Crystal as the Reference Input

The input crystal oscillator of the CY22701 is an important feature because of the flexibility it allows the user in selecting a crystal as a reference frequency source. The input oscillator has programmable gain, allowing for maximum compatibility with a reference crystal, regardless of manufacturer, process, performance and quality.

Programmable Crystal Input Oscillator Gain Settings

The Input crystal oscillator gain (XDRV) is controlled by two bits in register 12H, and are set according to *Table 2*. The parameters controlling the gain are the crystal frequency, the internal crystal parasitic resistance (ESR, available from the manufacturer), and the CapLoad setting during crystal start-up.

Bits 3 and 4 of register 12H control the input crystal oscillator gain setting. Bit 4 is the MSB of the setting, and bit 3 is the LSB. The setting is programmed according to *Table 2*.

All other bits in the register are reserved and should be programmed LOW. See *Table 3* for bit locations and values.

Using an External Clock as the Reference Input

The CY22701 can also accept an external clock as reference, with speeds up to 167 MHz (or 150 MHz at Industrial Temp.). With an external clock, the XDRV (register 12H) bits must be set according to *Table 4*.

Input Load Capacitors

Input load capacitors allow the user to set the load capacitance of the CY22701 to match the input load capacitance from a crystal. The value of the input load capacitors is determined by 8 bits in a programmable register [13H]. The proper CapLoad register setting is determined by the formula:

CapLoad = (C_L – C_{BRD} – C_{CHIP})/0.09375 pF

where:

- C_L = specified load capacitance of your crystal.
- C_{BRD} = the total board capacitance, due to external capacitors and board trace capacitance. In CyberClocks, this value defaults to 2 pF.
- C_{CHIP} = 6 pF.
- 0.09375 pF = the step resolution available due to the 8-bit register.

In CyberClocks, only the crystal capacitance (C_L) is specified. C_{CHIP} is set to 6 pF, and C_{BRD} defaults to 2 pF. If your board capacitance is higher or lower than 2 pF, the formula above can be used to calculate a new CapLoad value and programmed into register 13H.

In CyberClocks, enter the crystal capacitance (C_L). The value of CapLoad will be determined automatically and programmed into the CY22701. Through the SDAT and SCLK pins, the value can be adjusted up or down if your board capacitance is greater or less than 2 pF. For an external clock source, CapLoad defaults to 1. See *Table 5* for CapLoad bit locations and values.

The input load capacitors are placed on the CY22701 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when non-linear load capacitance is affected by load, bias, supply and temperature changes.

Table 2. Programmable Crystal Input Oscillator Gain Settings

	Calculated CapLoad Value	00H – 20H		20H – 30H		30H – 40H	
	Crystal ESR	30Ω	60Ω	30Ω	60Ω	30Ω	60Ω
Crystal Input Frequency	8 – 15 MHz	00	01	01	10	01	10
	15 – 20 MHz	01	10	01	10	10	10
	20 – 25 MHz	01	10	10	10	10	11
	25 – 30 MHz	10	10	10	11	11	N/A

Table 3. Register Map for Input Crystal Oscillator Gain Setting

Address	D7	D6	D5	D4	D3	D2	D1	D0
12H	0	0	XCapSrc, default=1	XDRV(1)	XDRV(0)	0	0	0

Table 4. Programmable External Reference Input Oscillator Drive Settings

Reference Frequency	1–25 MHz	25–50 MHz	50–90 MHz	90–167 MHz
Drive Setting	00	01	10	11

Table 5. Input Load Capacitor Register Bit Setting

Address	D7	D6	D5	D4	D3	D2	D1	D0
13H	CapLoad(7)	CapLoad(6)	CapLoad(5)	CapLoad(4)	CapLoad(3)	CapLoad(2)	CapLoad(1)	CapLoad(0)

DCXO

The default clock configuration of the CY22701 has 256 stored values that are used to adjust the frequency of the crystal oscillator, by changing the load capacitance. In order to use these stored values, the clock configuration must be reprogrammed to enable the DCXO feature.

To Configure for DCXO Operation

- XCapSrc, Register 12H[5] = 0
- XDRV[1:0], Register 12H[4:3] = (see *Table 2*)

Once the clock configuration block is programmed for DCXO operation, the SPI may be used to dynamically change the capacitor load value on the crystal. A change in crystal load capacitance corresponds with a change in the reference frequency. Thus, the crystal oscillator frequency can be adjusted from –150 ppm of the nominal frequency value to +150 ppm of the nominal frequency value. “Nominal frequency – 150 ppm” is achieved by writing 00000000 into the CapLoad register, and “nominal frequency + 150 ppm” is achieved by writing 11111111 into the CapLoad register

Write Protect (WP) Registers

To reconfigure pin 7 as WP, to control enable/disable of write protection, use the SPI to write the following:

WPSrc, Register 11H[3] = 0

CLK2, Register 09H[4] = 0

CLKSRC 2,1,0, Register 45H[3:1] = 111

When active (WP = 1), WP prevents the control logic for the EE from initiating a erase/program cycle for the EEPROM blocks. All serial shifting works as normal.

To reconfigure pin 7 as CLK2, use the SPI to write the following:

WPSrc, Register 11H[3] = 1

CLK2, Register 09H[4] = 1

CLKSRC 2,1,0, Registers 45H[3:1] = see *Table 11*

PLL Frequency, Q Counter

The first counter is known as the Q counter. The Q counter divides REF by its calculated value. Q is a 7-bit variable with a maximum value of 127 and minimum value of 0. The primary value of Q is determined by 7 bits in register 42H (6..0), but 2 is added to this register value to achieve the total Q, or Q_{total}. Q_{total} is defined by the formula:

$Q_{total} = Q + 2$.

The minimum value of Q_{total} is 2. The maximum value of Q_{total} is 129. Register 42H is defined in *Table 6*.

Stable operation of the CY22701 cannot be guaranteed if REF/Q_{total} falls below 250 kHz. Q_{total} bit locations and values are defined in *Table 6*.

PLL Frequency, P Counter

The next counter definition is the P (product) counter. The P counter is multiplied with the (REF/Q_{total}) value to achieve the VCO frequency. The product counter, defined as P_{total}, is made up of two internal variables, PB and PO. The formula for calculating P_{total} is:

$P_{total} = (2(PB + 4) + PO)$

PB is a 10-bit variable, defined by registers 40H(1:0) and 41H(7:0). The 2 LSBs of register 40H are the two MSBs of variable PB. Bits 4..2 of register 40H are used to determine the charge pump settings (see section, Charge Pump Settings [40H(2..0)] on page 6”). The 3 MSBs of register 40H are preset and reserved and cannot be changed.

PO is a single bit variable, defined in register 42H(7). This allows for odd numbers in P_{total}.

The remaining 7 bits of 42H are used to define the Q counter, as shown in *Table 6*.

The minimum value of P_{total} is 8. The maximum value of P_{total} is 2055. To achieve the minimum value of P_{total}, PB and PO should both be programmed to 0. To achieve the maximum value of P_{total}, PB should be programmed to 1023, and PO should be programmed to 1.

Stable operation of the CY22701 cannot be guaranteed if the value of $(P_{total}*(REF/Q_{total}))$ is above 400 MHz or below 100 MHz. Registers 40H, 41H and 42H are defined in *Table 7*.

Table 6. Q Counter Register Definition

Register	D7	D6	D5	D4	D3	D2	D1	D0
42H	PO	**Q(6)**	**Q(5)**	**Q(4)**	**Q(3)**	**Q(2)**	**Q(1)**	**Q(0)**

Table 7. P Counter Register Definition

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	**PB(9)**	**PB(8)**
41H	**PB(7)**	**PB(6)**	**PB(5)**	**PB(4)**	**PB(3)**	**PB(2)**	**PB(1)**	**PB(0)**
42H	**PO**	Q(6)	Q(5)	Q(4)	Q(3)	Q(2)	Q(1)	Q(0)

Table 8. PLL Post Divider Options

Address	D7	D6	D5	D4	D3	D2	D1	D0
OCH	DIV1SRC	DIV1N(6)	DIV1N(5)	DIV1N(4)	DIV1N(3)	DIV1N(2)	DIV1N(1)	DIV1N(0)
47H	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV2N(1)	DIV2N(0)

PLL Post Divider Options

The output of the VCO is routed through two independent muxes, then to two divider banks to determine the final clock output frequency. The mux determines if the clock signal feeding into the divider banks is the calculated VCO frequency or REF. There are 2 select muxes (DIV1SRC and DIV2SRC) and 2 divider banks (Divider Bank 1 and Divider Bank 2) used to determine this clock signal. The clock signals passing through DIV1SRC and DIV2SRC are referred to as DIV1CLK and DIV2CLK, respectively.

The divider banks have 4 unique divider options available: /2, /3, /4, and /DIVxN. DIVxN is a variable that can be independently programmed (DIV1N and DIV2N) for each of the 2 divider banks. The minimum value of DIVxN is 4. The maximum value of DIVxN is 127. A value of DIVxN below 4 is not guaranteed to work properly.

DIV1SRC is a single bit variable, controlled by register OCH. The remaining 7 bits of register OCH determine the value of post divider DIV1N.

DIV2SRC is a single bit variable, controlled by register 47H. The remaining 7 bits of register 47H determine the value of post divider DIV2N.

Register OCH and 47H are defined in *Table 8*.

Charge Pump Settings [40H(2..0)]

The correct pump setting is important for PLL stability. Charge pump settings are controlled by bits (4..2) of register 40H, and are dependent on internal variable PB (see section [00H to 08H] – Reserved [0AH to 0BH] – Reserved [0DH to 10H] –Reserved [14H to 3FH] –Reserved [43H to 44H] –Reserved [48H to FFH] –Reserved [46H] –Reserved on page 7). *Table 9* summarizes the proper charge pump settings, based on P_{total}. See *Table 10*, Register 40H Change Pump Bit Settings on page 6, for register 40H bit locations.

Although using *Table 10* will guarantee stability, it is recommended to use the Print Preview function in CyberClocks™ to determine the ideal charge pump settings for optimal jitter performance.

PLL stability cannot be guaranteed for P_{total} values below 16 and above 1023. If P_{total} values above 1023 are needed, use CyberClocks to determine the best charge pump setting.

Table 9. Charge Pump Settings

Charge Pump Setting – Pump(2..0)	Calculated P_{total}
000	16–44
001	45–479
010	480–639
011	640–799
100	800–1023
101, 110, 111	Do Not Use – device will be unstable

Table 10.Register 40H Change Pump Bit Settings

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	PB(9)	PB(8)

Clock Output Settings

CLKSRC - Clock Output Crosspoint Switch Matrix [45H(7..0)]

Both clock output can be defined to come from one of seven unique frequency sources. The CLKSRC(2..0) crosspoint switch matrix defines which source is attached to each individual clock output. CLKSRC(2..0) is set in Registers 45H.

When DIV1N is divisible by 4, then CLKSRC(0,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1). When DIV1N is 6, then CLKSRC(0,1,1) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1).

When DIV2N is divisible by 4, then CLKSRC(1,0,1) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0). When DIV2N is divisible by 8, then CLKSRC(1,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0).

CLKOE - Clock Output Enable Control [09H(7..0)]

Each clock output has its own output enable, CLKOE, controlled by register 09H(7..0). To enable an output, set the corresponding CLKOE bit to 1. CLKOE settings are in *Table 13*.

Test, Reserved, and Blank Registers

Writing to any of the following registers will cause the part to exhibit abnormal behavior:

[00H to 08H] – Reserved
[0AH to 0BH] – Reserved
[0DH to 10H] –Reserved
[14H to 3FH] –Reserved
[43H to 44H] –Reserved
[48H to FFH] –Reserved
[46H] –Reserved

Table 11.Clock Output Settings – Clock Source CLKSRC[2:0]

CLKSRC2	CLKSRC1	CLKSRC0	Definition and Notes
0	0	0	Reference Input
0	0	1	DIV1CLK/DIV1N. DIV1N is defined by register [OCH]. Allowable values for DIV1N are 4 to 127. If Divider Bank 1 is not being used, set DIV1N to 8
0	1	0	DIV1CLK/2. Fixed /2 divider option. If this option is used, DIV1N must be divisible by 4.
0	1	1	DIV1CLK/3. Fixed /3 divider option. If this option is used, set DIV1N to 6.
1	0	0	DIV2CLK/DIV2N. DIV2N is defined by Register [47H]. Allowable values for DIV2N are 4 to 127. If Divider Bank 2 is not being used, set DIV2N to 8.
1	0	1	DIV2CLK/2. Fixed /2 divider option. If this option is used, DIV2N must be divisible by 4.
1	1	0	DIV2CLK/4. Fixed /4 divider option. If this option is used, DIV2N must be divisible by 8.
1	1	1	Reserved – Do not use

Table 12.CLKSRC Registers

Address	D7	D6	D5	D4	D3	D2	D1	D0
45H	1	CLKSRC2 for CLK1	CLKSRC1 for CLK1	CLKSRC0 for CLK1	CLKSRC2 for CLK2	CLKSRC1 for CLK2	CLKSRC0 for CLK2	1

Table 13.CLKOE Bit Setting

Address	D7	D6	D5	D4	D3	D2	D1	
09H	0	0	0	CLKOE for CLK2	CLKOE for CLK1	0	0	0

Serial Programming Interface (SPI) Protocol and Timing

The CY22701 utilizes a 2-serial-wire interface SDAT and SCLK that operates up to 400 kbits/sec in Read or Write mode. The basic Write serial format is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in *Figure 4*.

Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is LOW as illustrated in *Figure 5*.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in *Figure 6*.

Start Sequence – Start Frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (7 bits) and a R/$\overline{W}$ bit, followed by register address (8 bits) and register data (8 bits).

Stop Sequence – Stop Frame is indicated by SDAT going HIGH when SCLK is HIGH. A Stop Frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During Write Mode the CY22701 will respond with an Acknowledge pulse after every 8 bits. This is accomplished by pulling the SDAT line LOW during the N*9th clock cycle as illustrated in *Figure 7*. (N = the number of bytes transmitted). During Read Mode the acknowledge pulse after the data packet is sent is generated by the master.

Device Addressing

The first seven bits of the device address word for the clock configuration EEPROM block are 1101000. The first seven bits of the device address word for the clock configuration SRAM block are 1101001. The final bit of the address specifies the operation (HIGH/1 = Read, LOW/0 = Write)

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit word address after the device address word, which is followed by an acknowledgment bit from the EEPROM (ack = 0/LOW). The next 8 bits must contain the data word intended for storage. After the data word is received, the EEPROM responds with another acknowledge bit (ack = 0/LOW), and the device that is addressing the EEPROM must end the write sequence with a stop condition. The EEPROM now enters an internal write process transferring the data received to nonvolatile memory. During, and until completion of, this internal write process, the EEPROM will not respond to other commands.

Writing Multiple Bytes

The CY22701 is capable of receiving up to 16 consecutive written bytes. In order to write more than one byte at a time, the device addressing the EEPROM does not end the write sequence with a stop condition. Instead, the device can send up to fifteen more bytes of data to be stored. After each byte, the EEPROM responds with an acknowledge bit, just like after the first byte. The EEPROM will accept data until the acknowledge bit is responded to by the stop condition, at which time it enters the internal write process as described in the section above. When receiving multiple bytes, the CY22701 internally increments the address of the last 4 bits in the address word. After 16 bytes are written, that incrementing brings it back to the first word that was written. If more than 16 bytes are written, the CY22701 will overwrite the first bytes written.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY22701 has an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word 'n,' then a current address read operation would return the value stored in location 'n+1'. When the CY22701 receives the slave address with the R/W bit set to a '1,' the CY22701 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY22701 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is accomplished by sending the address to the CY22701 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next the master reissues the control byte with the R/W byte set to '1.' The CY22701 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition which causes the CY22701 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the memory blocks. Similarly, sequential reads within either the EEPROM or SRAM clock configuration blocks will wrap within the block to the first word of the same block after reaching the end of either block.

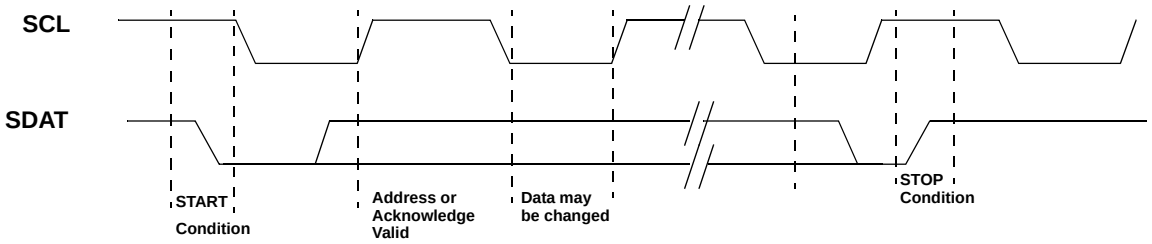


Figure 3. Data Transfer Sequence on the Serial Bus

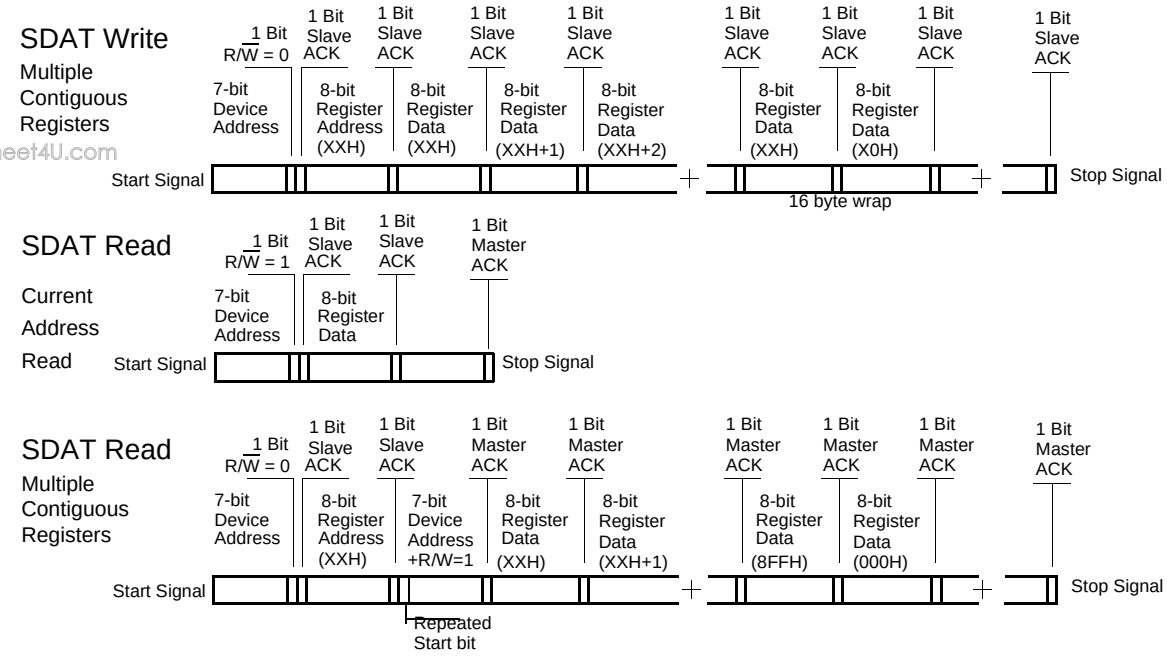


Figure 4. Data Frame Architecture

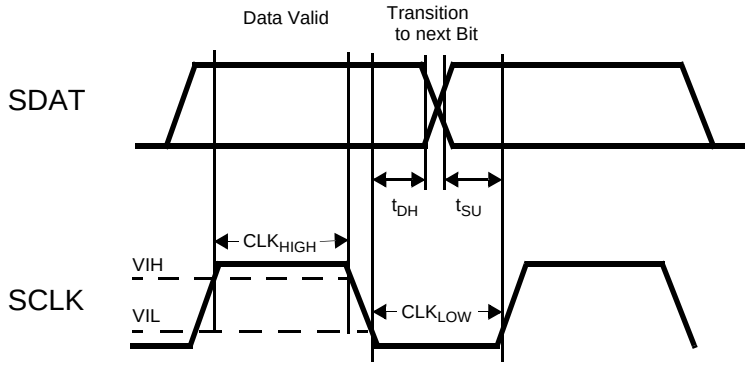


Figure 5. Data Valid and Data Transition Periods

Serial Programming Interface Timing

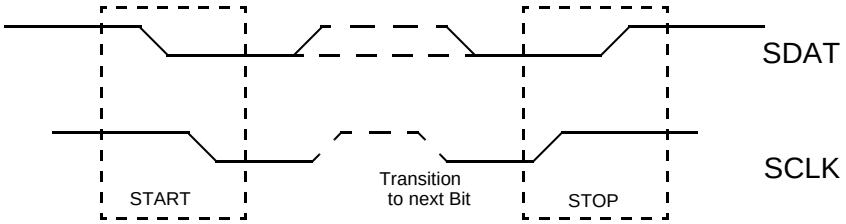


Figure 6. Start and Stop Frame

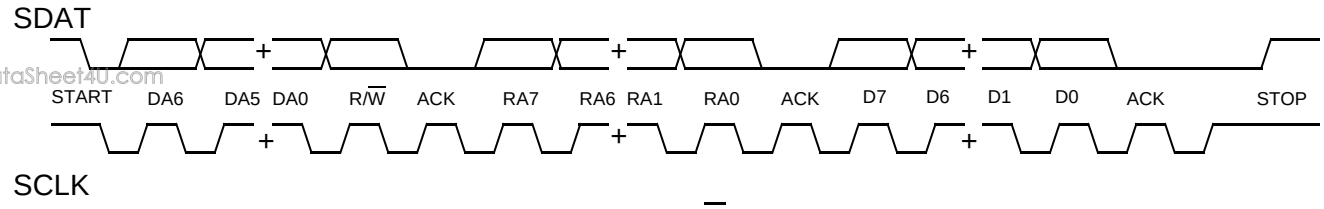


Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)

Table 14.Recommended Pullable Crystal Specifications

Parameter	Description	Comments	Min.	Typ.	Max.	Units
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPHI}	Third overtone separation from 3*F_{NOM}	High side	400	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3*F_{NOM}	Low side	–	–	–200	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature	–65	125	°C
T_J	Junction Temperature	–40	100	°C
	Logic Inputs	V_{SS} – 0.5	V_{DD} + 0.5	V
	I^2C interface (SDAT and SCL)	–0.5	5.5	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.5	V_{DD} + 0.5	V
	Electro-Static Discharge		2000	V
	Endurance (@ 25°C)		1,000,000 (100k/page)	writes
	Data retention	10		yrs

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature, Industrial grade	–40	–	85	°C
T_A	Ambient Temperature, Commercial grade	0	–	70	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current[2]	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	–	24	mA
I_{OL}	Output Low Current[2]	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	–	24	mA
V_{IH}	Input High Voltage	CMOS levels	0.7 * V_{DD}	–	–	V
V_{IL}	Input Low Voltage	CMOS levels	–	–	0.3 * V_{DD}	V
C_{IN}	Input Capacitance[2, 3]		–	–	7	pF
I_{IZ}	Input Leakage Current	Except XTAL pins	–	–	10	µA
$f_{\Delta XO}$	VCXO Pullability Range[3]		±150	–	–	ppm
I_{VDD}	Supply Current		–	45	–	mA
I_{SB}	Supply Current - Power Down Mode Enabled	Current drawn while part is in standby.	–	5	40	µA

DC Electrical Specifications – 2.5V Outputs

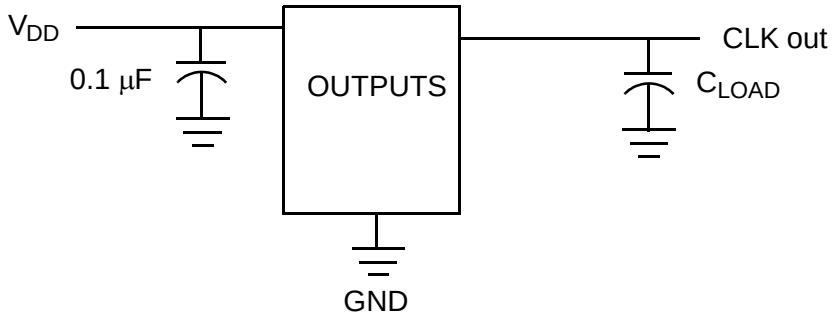
Parameter	Name	Description	Min.	Typ.	Max.	Unit
$I_{OH2.5}$	Output High Current[2, 4]	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	–	24	mA
$I_{OL2.5}$	Output Low Current[2, 4]	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	–	24	mA

Notes:
2. Guaranteed by design, not 100% tested.
3. Crystal must meet *Table 14* specifications.
4. V_{DD} is only specified and characterized at 3.3V ± 5%. V_{DDL} may be powered at any value between 3.465 and 2.375.

AC Electrical Specifications (VDD = 3.3V)

Parameter[5]	Name	Description	Min.	Typ.	Max.	Unit
DC	Clock Output Duty Cycle	f_{OUT} < 150 MHz f_{OUT} > 150 MHz, or $f_{OUT} = f_{REF}$ See *Figure 8*	45 40	50 50	55 60	%
ER_O	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF See *Figure 9*.	0.8	1.4	–	V/ns
EF_O	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF See *Figure 9*.	0.8	1.4	–	V/ns
t_5	Output to Output Skew	For related clock outputs	–	–	250	ps
t_9	Clock Jitter	Maximum absolute jitter (EEPROM quiet) (during EEPROM reads) (during EEPROM writes)	–	250 300 350	–	ps
t_{10}	PLL Lock Time		–	–	60	ms
$t_{VDDramp}$	Power Supply Ramp	Ramp time from 1.5V to 2.5V[6]		–	15	ms
$t_{VDDpowerdown}$	Power Supply Power Down after Write	Wait time after a write to EEPROM is initiated by the stop bit until V_{DD} fails below 2.5V	20	–	–	ms
Memory Section Specifications						
F_{SCL}	SCL input frequency		–		400	kHz
t_L	Clock Pulse Low	CLK_{LOW}, 20–80% of V_{DD}	1.3	–	–	µs
t_H	Clock Pulse High	CLK_{HIGH}, 80–20% of V_{DD}	0.6	–	–	µs
t_{SP}	Noise Suppression Time	Square noise spike on input	–	–	50	ns
t_{AA}	Clock Low to Data Out Valid		0.1	–	0.9	µs
t_{BUFF}	Time the bus must be free before a new transmission may start		1.2	–	–	µs
$t_{HDSTART}$	Start Hold Time		0.6	–	–	µs
$t_{SUSTART}$	Start Set-up Time		0.6	–	–	µs
t_{DH}	Data in Hold Time		0	–	–	ms
t_{SU}	Data in Set-up time		100	–	–	ns
t_{RI}	Inputs rise time		–	–	300	ns
t_{FI}	Inputs fall time		–	–	300	ns
t_{SUSTOP}	Stop Set-up Time		0.6	–	–	µs
t_{DH}	Data Out Hold Time		50	–	–	ns
t_{WR}	Write Cycle Time		–	–	20	ms

Test and Measurement Set-up



Notes:
5. Not 100% tested.
6. The power supply voltage must increase monotonically from 0 to 2.5V; once V_{DD} reaches 1.5V, it must ramp to 2.5V within 15 ms.

Voltage and Timing Definitions

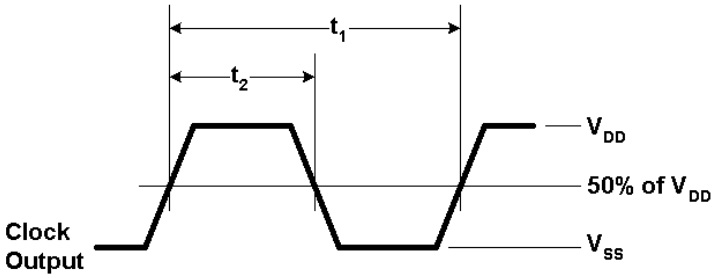


Figure 8. Duty Cycle Definition; DC = t_2/t_1

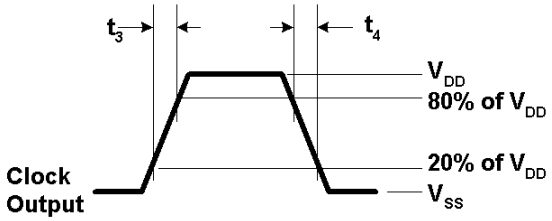


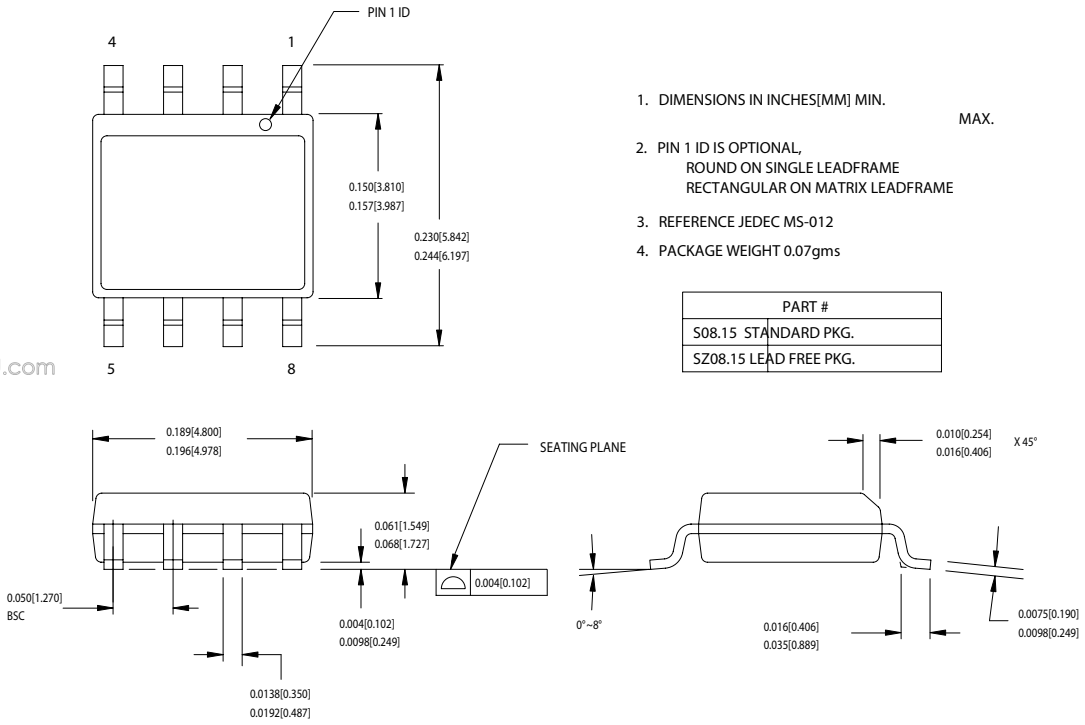
Figure 9. Rise and Fall Time Definitions: ER = 0.6 x V_{DD} / t_3, EF = 0.6 x V_{DD} / t_4

Ordering Information

Ordering Code	Feature	Package Name	Package Type	Operating Range	Operating Voltage
CY22701FSXC	Field Programmable	Lead Free SOIC	8 Pin SOIC	Commercial	3.3V
CY22701FSXCT	Field Programmable	Lead Free SOIC - Tape and Reel	8 Pin SOIC	Commercial	3.3V
CY22701FSXI	Field Programmable	Lead Free SOIC	8 Pin SOIC	Industrial	3.3V
CY22701FSXIT	Field Programmable	Lead Free SOIC - Tape and Reel	8 Pin SOIC	Industrial	3.3V

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

51-85066-*C

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Document History Page

Document Title: CY22701 1 PLL In-System Programmable Clock Generator Document Number: 38-07698				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	226712	See ECN	RGL	New data sheet
*A	318313	See ECN	RGL	swapped CLK2 to CLK1 in Summary and CLKOE Bit Setting Tables.
*B	320154	See ECN	LPG	Minor Change - Correct footer