SONY

CXP85452/85460

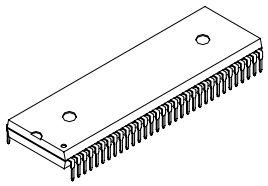
CMOS 8-bit Single Chip Microcomputer

Description

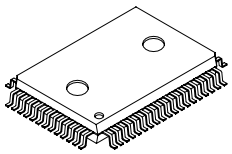
The CXP85452/85460 are a highly integrated microcomputers composed of a 8-bit CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I²C bus interface, PWM output, remote control reception circuit, HSYNC counter, and watchdog timer.

Futhermore, the CXP85452/85460 series provides power-on reset and sleep functions which enable to lower power consumption.

64 pin SDIP (Plastic)



64 pin QFP (Plastic)



Structure

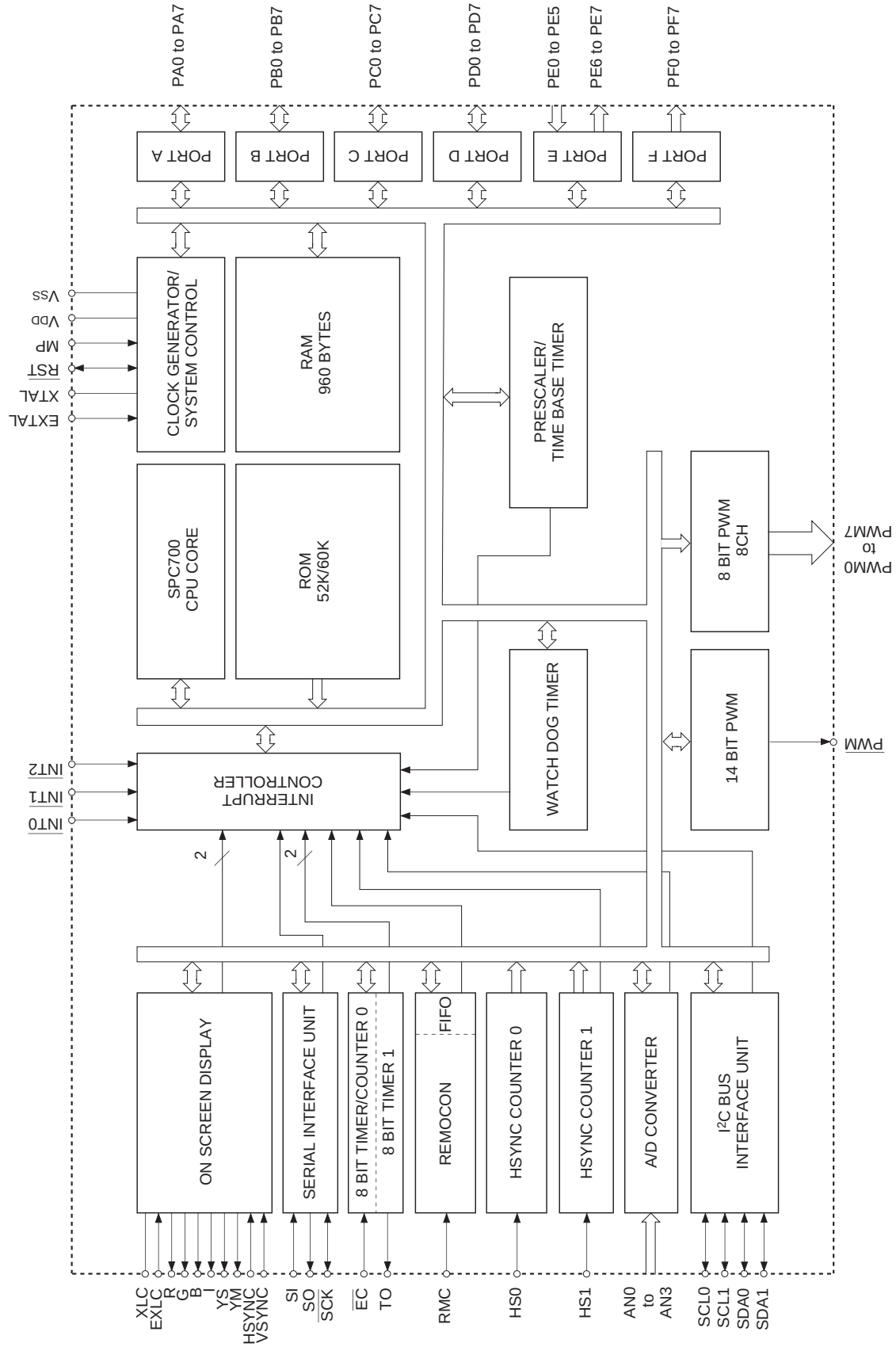
Silicon gate CMOS IC

Features

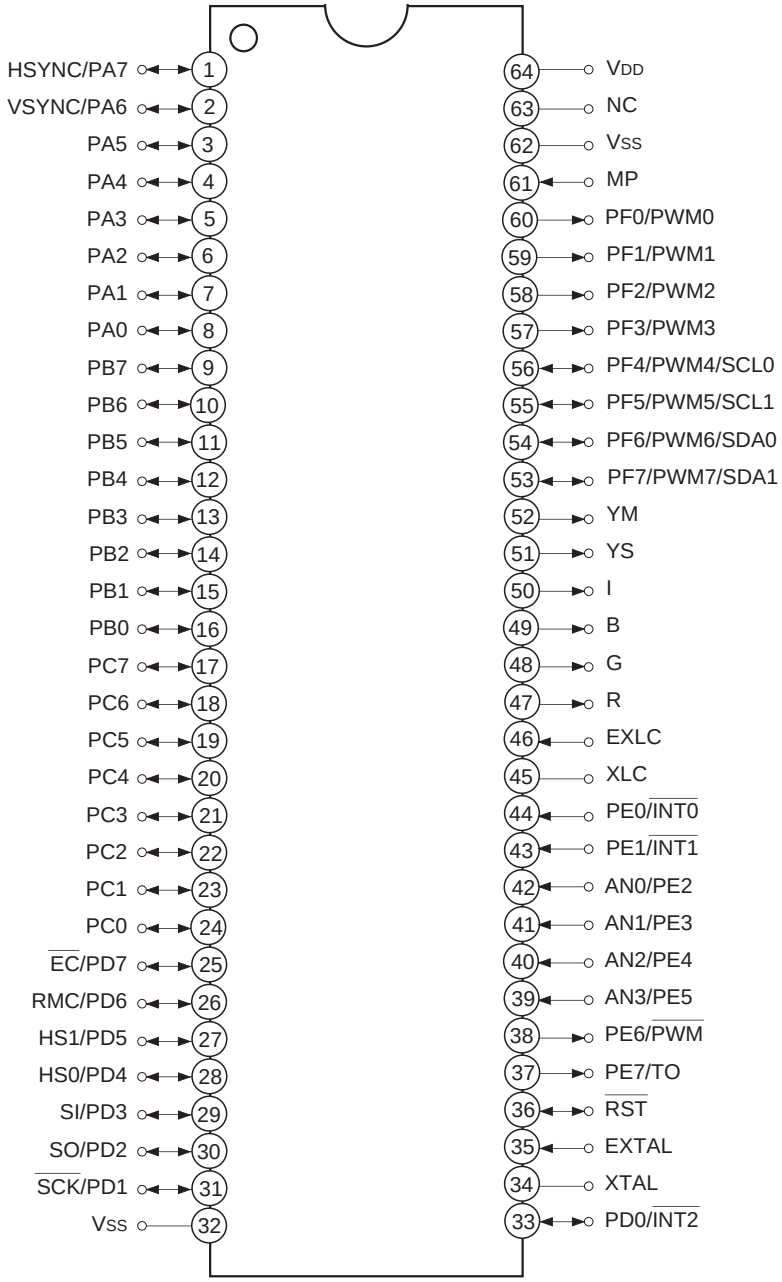
- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 0.5µs at 8MHz
- Incorporated ROM capacity 52K bytes (CXP85452)
  60K bytes (CXP85460)
- Incorporated RAM capacity 960 bytes
- Peripheral functions
  - A/D converter: 8-bit, 4-channel successive approximation method (Conversion time of 20µs at 8MHz)
  - Serial interface: 8-bit clock sync type, 1 channel
  - Timer: 8-bit timer
    8-bit timer/counter
    19-bit time-base timer
  - On screen display (OSD) function: 12 × 18 dots, 384 character types, 15 character colors, 12lines of 32 characters, black frame output/half blanking, shadow, background color on full screen/half blanking, double scanning, jitter elimination circuit
  - I²C bus interface
  - PWM output: 14 bits, 1 channel
    8 bits, 8 channels
  - Remote control reception circuit: 8-bit pulse measurement circuit, 6-state FIFO
  - HSYNC counter: 2 channels
  - Watchdog timer
- Interruption 13 factors, 13 vectors, multi-interruption possible
- Standby mode SLEEP
- Package 64-pin plastic SDIP/QFP
- Piggyback/evaluator CXP85400 64-pin ceramic PSDIP/PQFP
  CXP85490 64-pin ceramic PSDIP (accommodates custom font)

E94323B86

Block Diagram

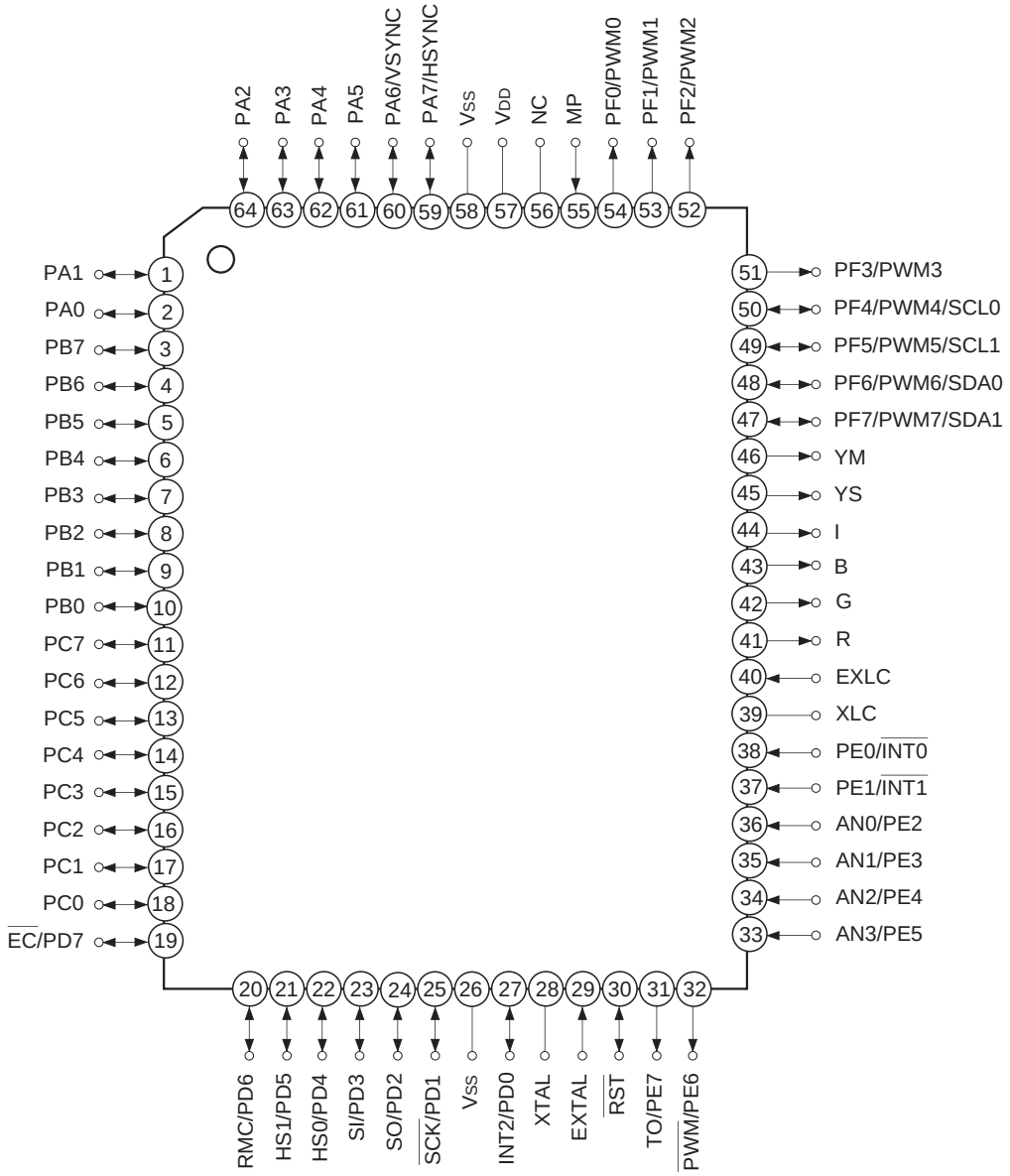


Pin Assignment (Top View) 64-pin SDIP



Note) 1. NC (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are both connected to GND.
3. MP (Pin 61) is always connected to GND.

Pin Assignment (Top View) 64-pin QFP



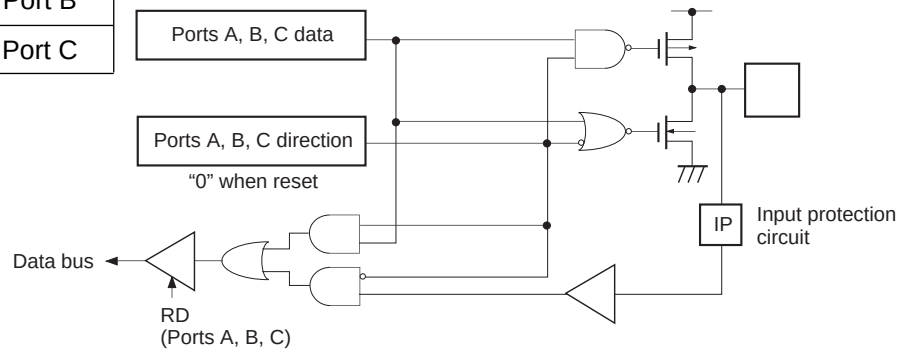
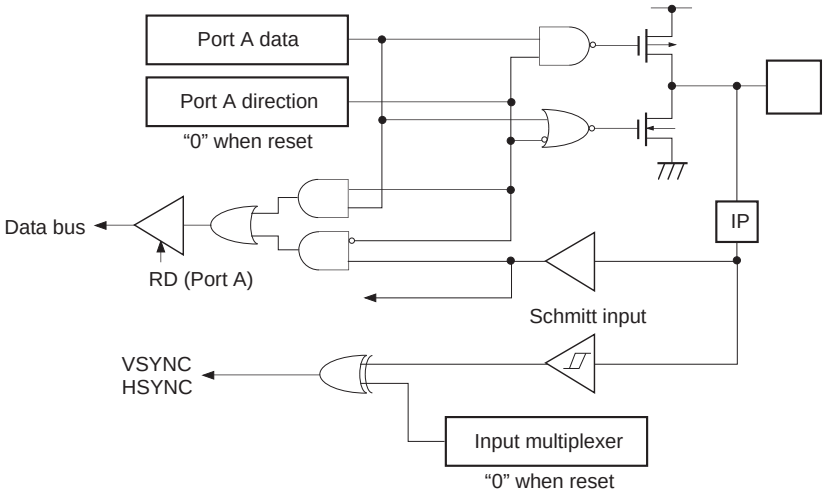
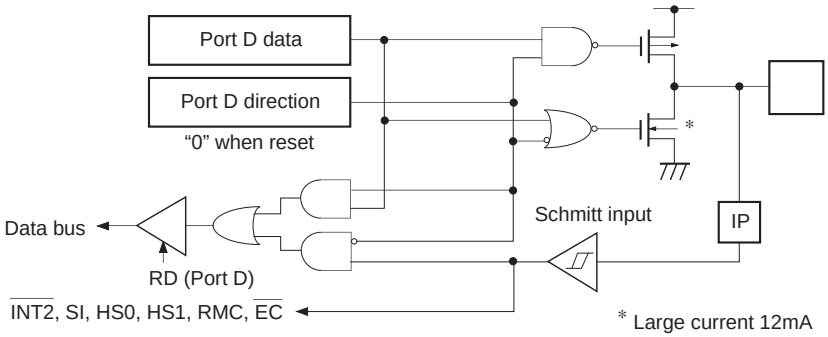
Note) 1. NC (Pin 56) is always connected to V_{DD}.
2. Vss (Pins 26 and 58) are both connected to GND.
3. MP (Pin 55) is always connected to GND.

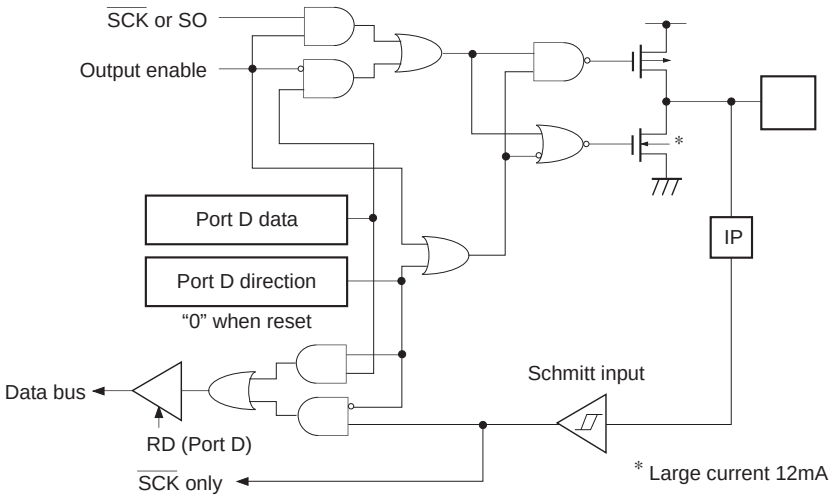
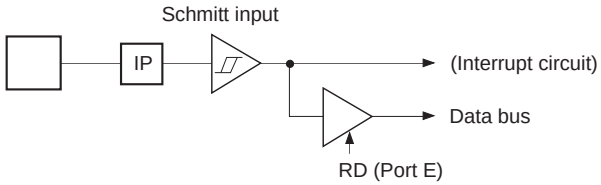
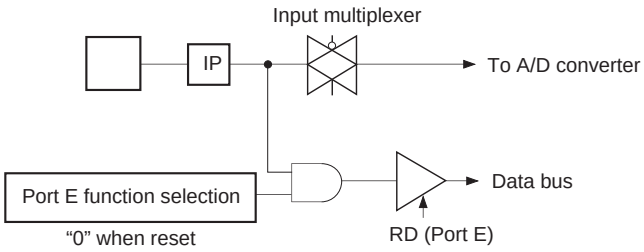
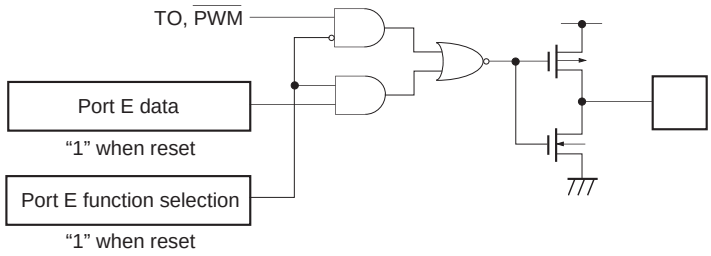
Pin Description

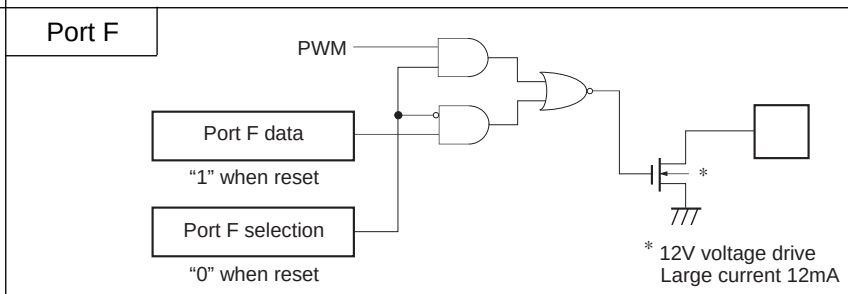
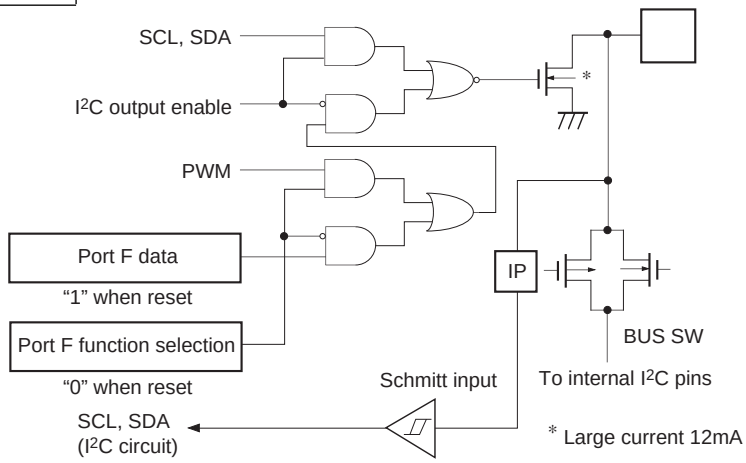
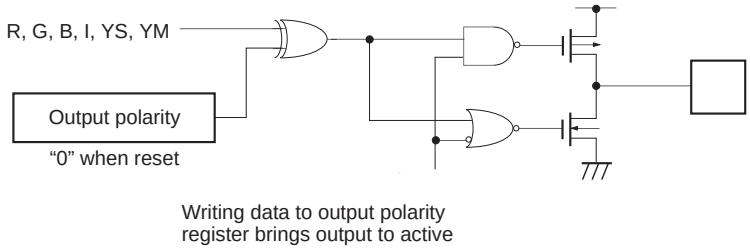
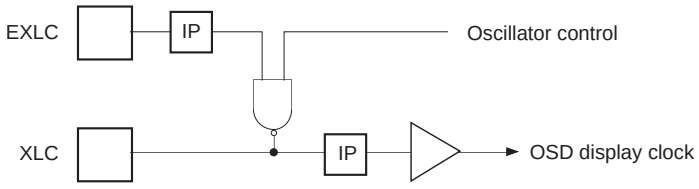
Symbol	I/O	Description	
PA0 to PA5	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PA6/VSYNC	I/O/Input		OSD display vertical synchronization signal input pin.
PA7/HSYNC	I/O/Input		OSD display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/$\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. 12mA sink current drive possible. (8 pins)	Input pin for external interruption request. Active when falling edge.
PD1/$\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O pin.
PD2/SO	I/O/Output		Serial data output pin.
PD3/SI	I/O/Input		Serial data input pin.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input pin.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input pin.
PD6/RMC	I/O/Input		Remote control reception circuit input pin.
PD7/$\overline{\text{EC}}$	I/O/Input		External event input pin for timer/counter.
PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Input pin for external interruption request. Active when falling edge. (2 pins)
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 pins)
PE6/$\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/TO	Output/Output		Timer/counter rectangular wave output pin.
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port. Large current (12mA) N-ch open drain output. Lower 4 bits are mid-voltage drive (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output pin. (8 pins)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		I^2C bus interface transfer clock I/O pin. (2 pins)
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		I^2C bus interface transfer data I/O pin. (2 pins)
R, G, B, I, YS, YM	Output	OSD display 6-bit output pin. (6 pins)	

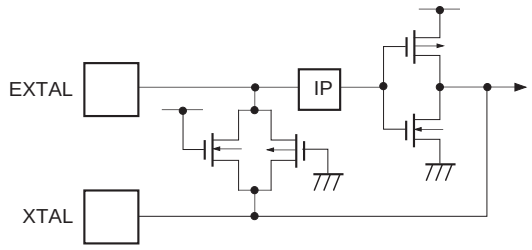
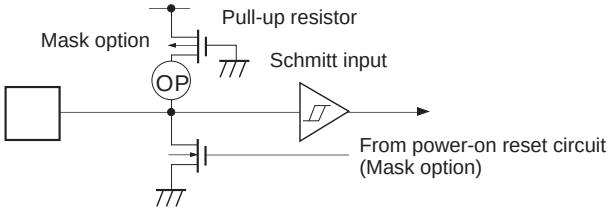
Symbol	I/O	Description
EXLC	Input	OSD display clock oscillation I/O pin. Oscillation frequency is determined by the external L and C.
XLC	Output	
EXTAL	Input	Crystal connection pin for system clock oscillation. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset pin for active at low level. This pin becomes I/O pin, and outputs low level at the power on with power-on reset function executed. (Mask option)
MP	Input	Test mode input pin. Always connect to GND.
NC		NC. Under normal operation, connect to V_{DD}.
V_{DD}		Positive supply voltage pin.
Vss		GND. Both Vss pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA5 PB0 to PB7 PC0 to PC7 22 pins	Port A Port B Port C 	Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins	Port A 	Hi-Z
PD0/$\overline{INT2}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{EC}$ 6 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PD1/$\overline{\text{SCK}}$ PD2/SO 2 pins	Port D 	Hi-Z
PE0/$\overline{\text{INT0}}$ PE1/INT1 2 pins	Port E 	Hi-Z
PE2/AN0 to PE5/AN3 4 pins	Port E 	Hi-Z
PE6/$\overline{\text{PWM}}$ PE7/TO 2 pins	Port E 	High level

Pin	Circuit format	When reset
PF0/PWM0 to PF3/PWM3 4 pins	Port F  	Hi-Z
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1 4 pins	Port F  	Hi-Z
R G B I YS YM 6 pins	 Writing data to output polarity register brings output to active	Hi-Z
EXLC XLC 2 pins	 	Oscillation halted

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during STOP. (This device does not enter the STOP mode.)	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Mid-voltage drive output voltage	V_{OUTP}	–0.3 to +15.0	V	PF0 to PF3 pins
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Ports excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current output port (value per pin)*2
Low level total output current	$\sum I_{OL}$	130	mA	Total of all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current output port is Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes.
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or SLEEP mode.
		2.5	5.5	V	Guaranteed data hold range for STOP mode.*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	*3
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4
Operating temperature	Topr	–20	+75	°C	

*1 This device does not enter the STOP mode.

*2 PA, PB, PC, PE2 to PE5, SCL0, SCL1, SDA0, SDA1 pins

*3 $\overline{INT2}$, $\overline{SCK}$, SI, HS0, HS1, RMC, $\overline{EC}$, $\overline{INT0}$, $\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$ pins

*4 Specifies only during external clock input.

DC Characteristics (Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, R, G, B, I, YS, YM	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, $\overline{RST}$*1	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM, $\overline{RST}$*2	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr off)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (Output Tr off)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current	I_{DD}	V_{DD}*3	1/2 frequency dividing operation mode V_{DD} = 5.5V, 8MHz crystal oscillation (C_1 = C_2 = 22pF)		18	30	mA
	I_{DDSL}		SLEEP mode V_{DD} = 5.5V, 8MHz crystal oscillation (C_1 = C_2 = 22pF)		0.9	3	mA
	I_{DDST}		STOP mode*4 V_{DD} = 5.5V, termination of 8MHz oscillation	—	—	—	µA
Input capacitance	C_{IN}	PA to PD, PE0 to PE5, SCL, SDA, EXLC, EXTAL, $\overline{RST}$	1MHz clock 0V for non-measurement pins		10	20	pF

*1 Specifies $\overline{RST}$ pin only when the power-on reset circuit is selected with mask option.

*2 For $\overline{RST}$ pin, specifies the input current when pull-up resistor is selected, and specifies the leakage current when non-resistor is selected.

*3 When all output pins open. Specifies only when the OSD oscillation is halted.

*4 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	3.5	9	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	50		ns
System clock rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*1		ns
Event count input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

*1 tsys indicates three values according to the contents of the clock control register (CLC: 00FE$_H$) upper 2 bits (CPU clock selection).
tsys (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

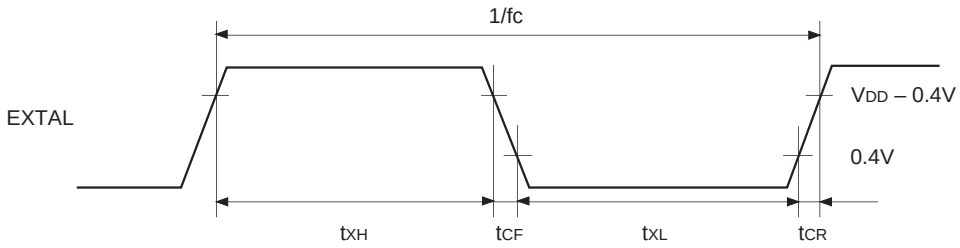


Fig. 2. Clock applied condition

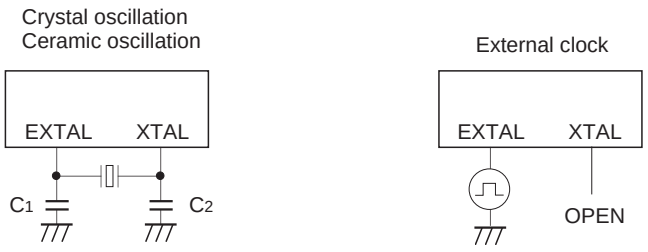
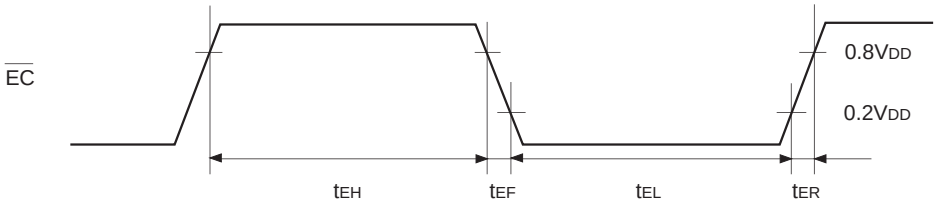


Fig. 3. Event count clock timing

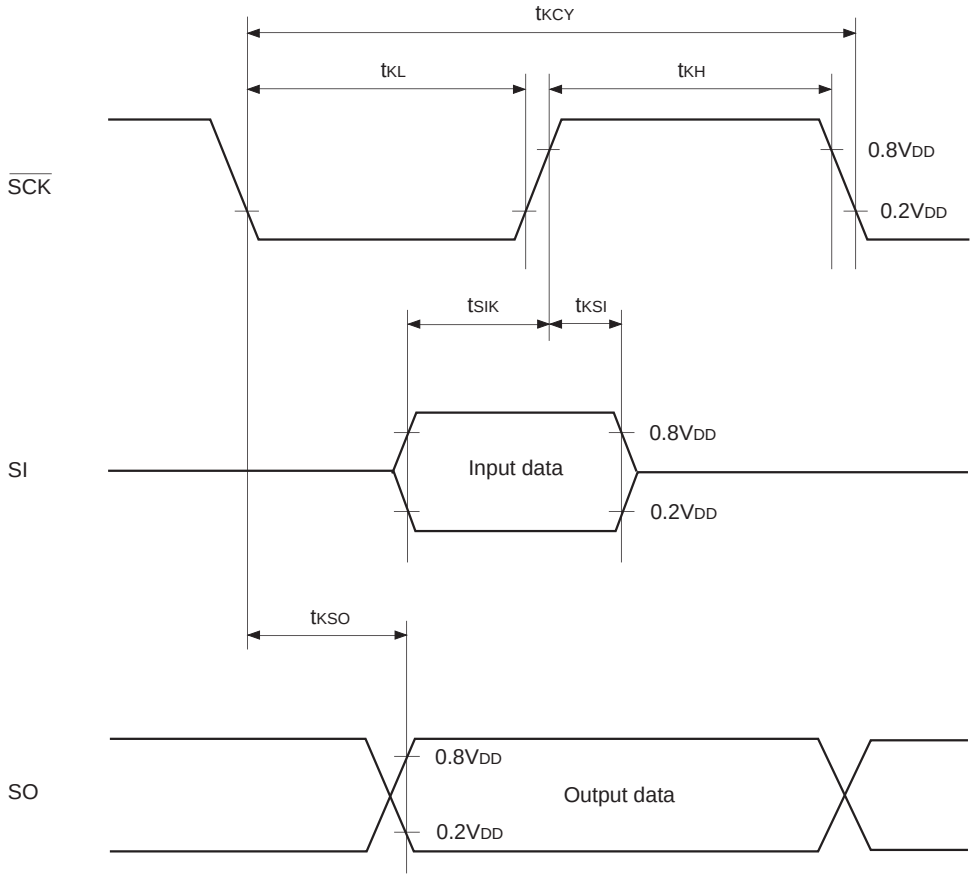


(2) Serial transfer (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc – 50		ns
SI input set-up time (for $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

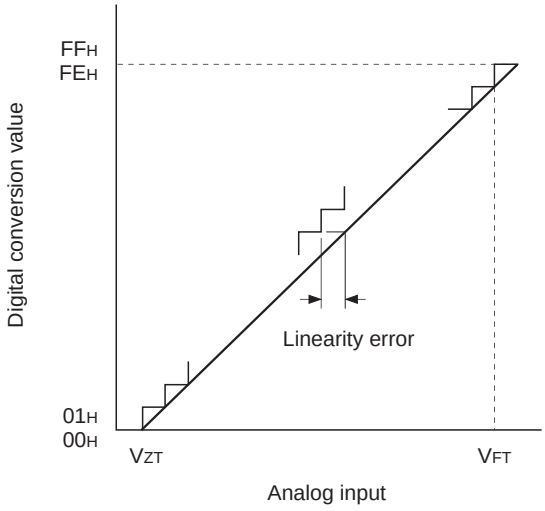
Fig. 4. Serial transfer timing



(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–50	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN3		0		V_{DD}	V

Fig. 5. Definitions for A/D converter terms



*1 V_{ZT}: Digital conversion values change between 00H⟷01H.

*2 V_{FT}: Digital conversion values change between 0EH⟷0FH.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control registor (ADC: 00F6H) and the bits 7 (PCK1) and 6 (PCK0) of the clock control registor (CLC: 00FEH)

PCK1, 0 \ CKS	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT2}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 6. Interruption input timing

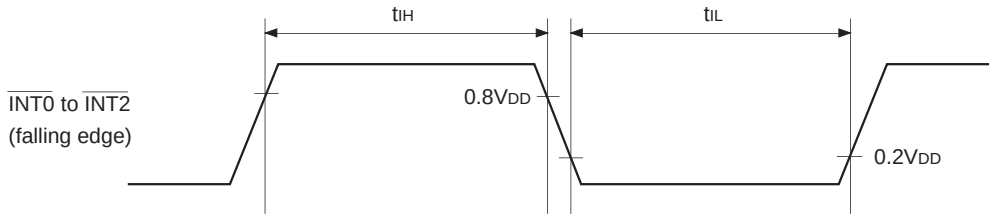
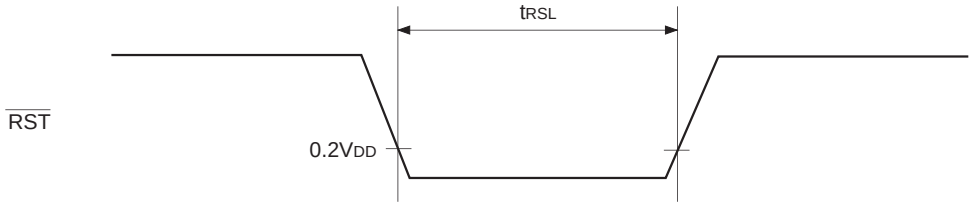


Fig. 7. $\overline{RST}$ input timing



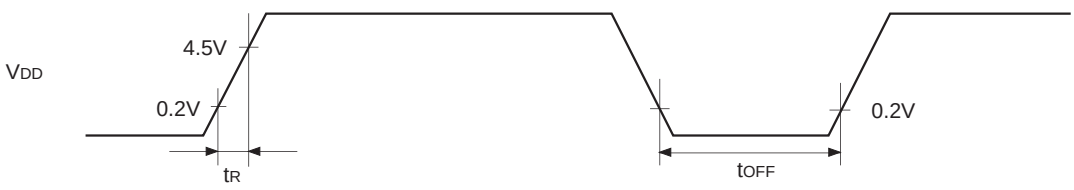
(5) Power-on reset

Power-on reset*1 (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cutt-off time	t_{OFF}		Repeated power-on reset	1		ms

*1 Specifies only when power-on reset function is selected.

Fig. 8. Power-on reset



Take care when turning on power.

(6) I²C bus timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		4.0		µs
Clock low level width	t_{LOW}	SCL		4.7		µs
Clock high level width	t_{HIGH}	SCL		4.0		µs
Set-up time for repeated transfers	$t_{SU; STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD; DAT}$	SDA, SCL		0*1		µs
Data set-up time	$t_{SU; DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Set-up time for transfer completion	$t_{SU; STO}$	SDA, SCL		4.7		µs

*1 For the data hold time, the SCL rise time (300ns Max.) is not considered so that 300ns should be exceeded.

Fig. 9. I²C bus transfer data timing

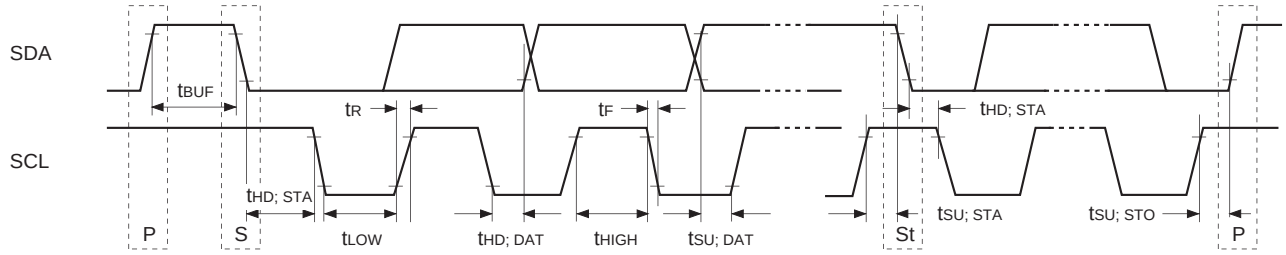
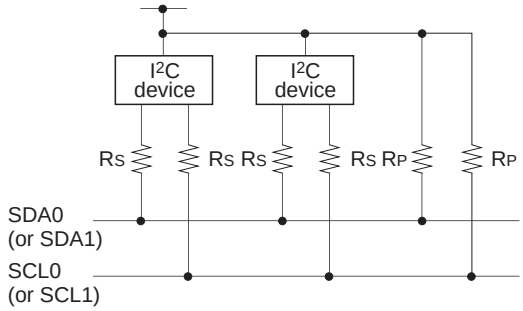


Fig. 10. I²C device recommended circuit



- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condiiton	Min.	Max.	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	7*1 14*2	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		µs
VSYNC pulse width	t_{VWD}	HSYNC	Fig. 11	1		H*3
HSYNC afterwrite rise and fall times	t_{HCG}	HSYNC	Fig. 11		200	ns
VSYNC beforewrite rise and fall times	t_{VCG}	VSYNC	Fig. 11		1.0	µs

*1 Oscillation clock at 4MHz operation

*2 Oscillation clock at 8MHz operation

*3 H indicates 1HSYNC period.

Fig. 11. OSD timing

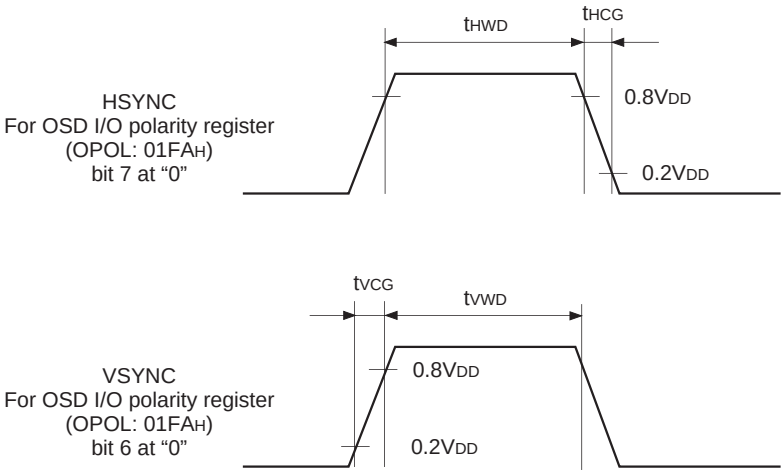
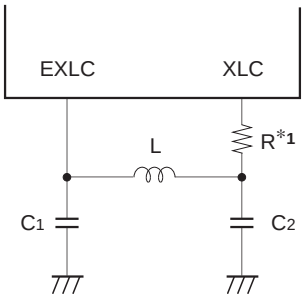


Fig. 12. LC oscillation circuit connection

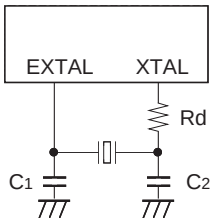


*1 The series resistor for XLC is used to reduce the frequency of occurrence of the undesired radiation.

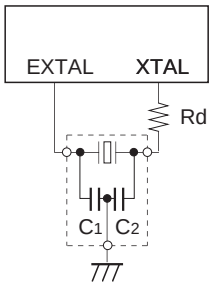
Appendix

Fig. 13. SPC700 Series recommended oscillation circuit

(i)



(ii)



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0*2	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*1	4.00				(ii)
	CST4.19MGW*1	4.19				
	CST8.00MTW*1	8.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	12	12	0*2	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0*2	(i)
		4.19				
		8.00				

*1 These models have the on-chip grounding capacitors (C_1 and C_2).

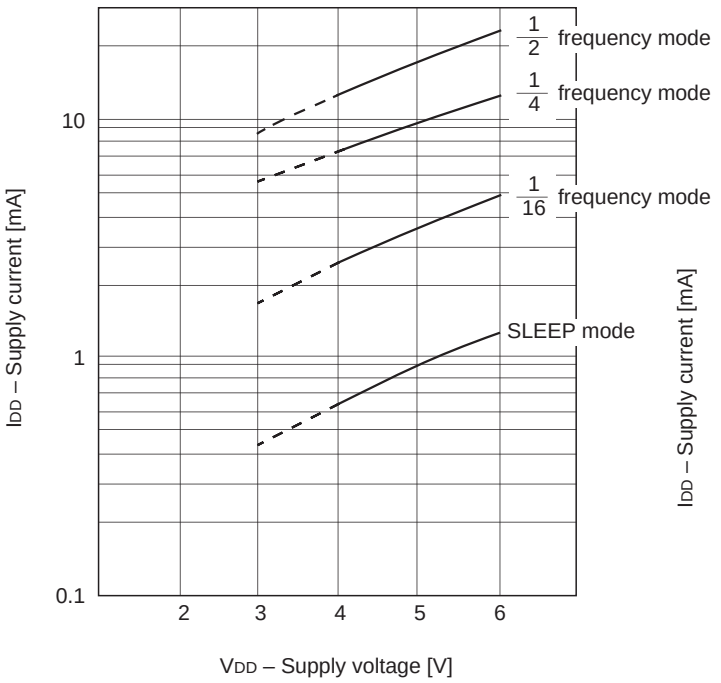
*2 The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.

Mask Option Table

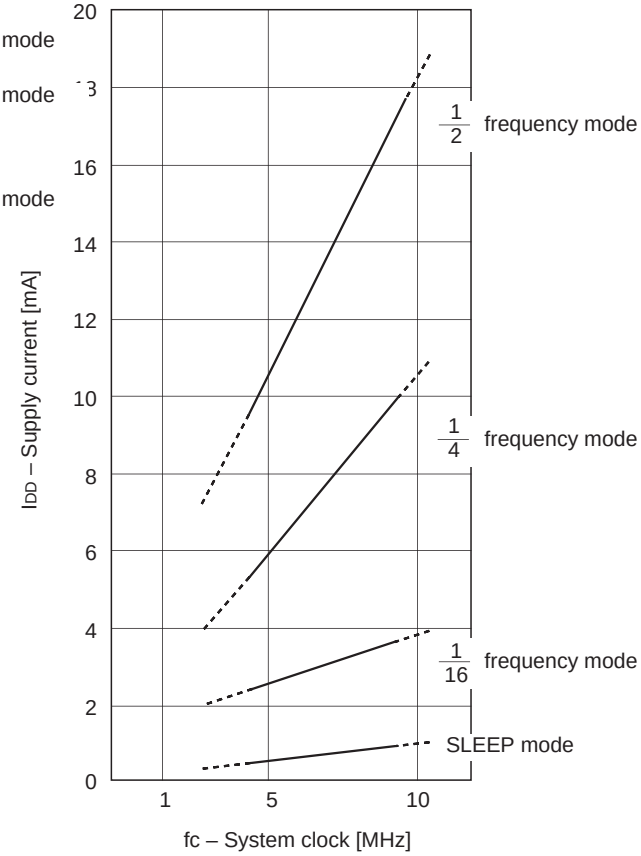
Item	Inclusion	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

Fig. 14. Characteristics curves

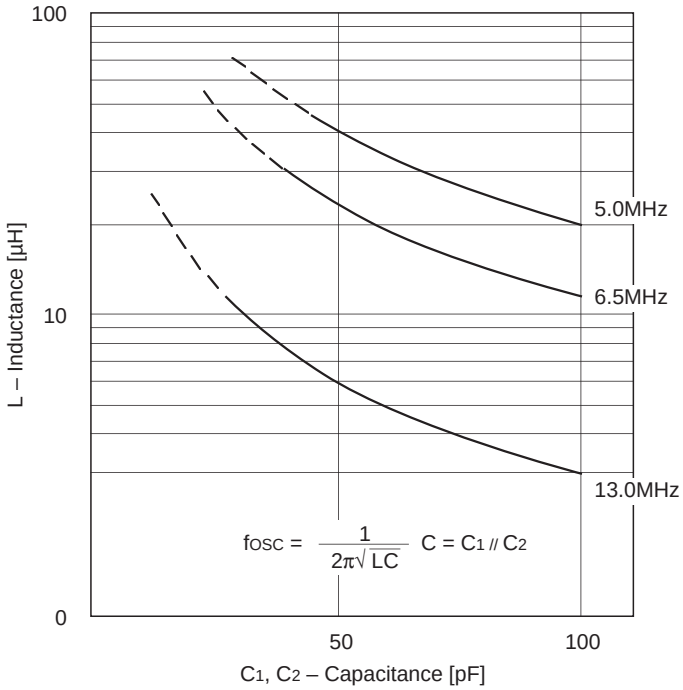
IDD vs. VDD (fc = 8MHz, Ta = 25°C, Typical)



IDD vs. fc (VDD = 5V, Ta = 25°C, Typical)

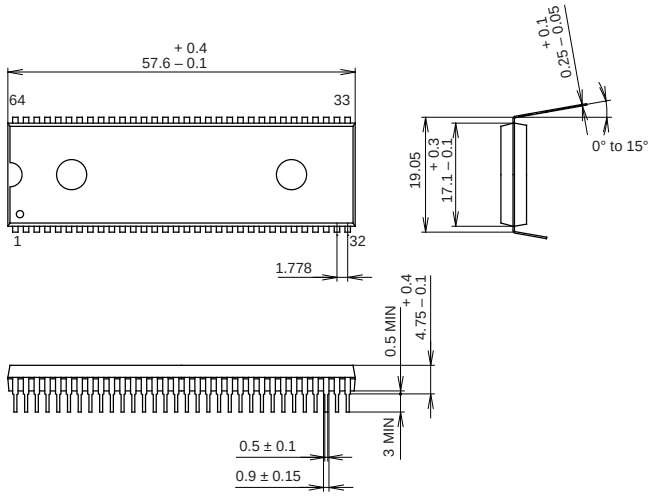


Parameter Curve for OSD Oscillator L vs. C
(Analytically calculated value)



Package Outline Unit: mm

64PIN SDIP (PLASTIC) 750mil

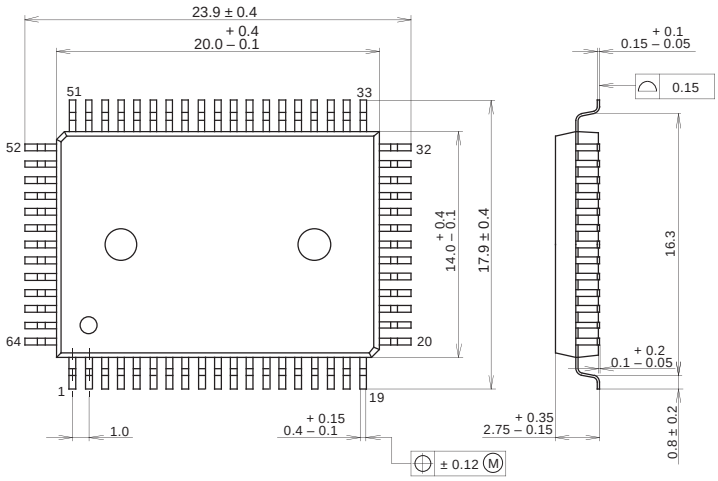


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750-A
JEDEC CODE	

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP–64P–L01
EIAJ CODE	*QFP064–P–1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g