SONY

CXP829P60

CMOS 8-bit Single Chip Microcomputer

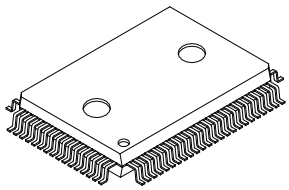
Description

The CXP829P60 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, fluorescent display panel controller/driver, I²C bus interface, remote control transmission circuit, remote control reception circuit, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

This LSI also provides sleep/stop functions which enable to lower power consumption.

The CXP829P60 is the PROM-incorporated version of the CXP82960 with built-in mask ROM, and it is able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

80 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

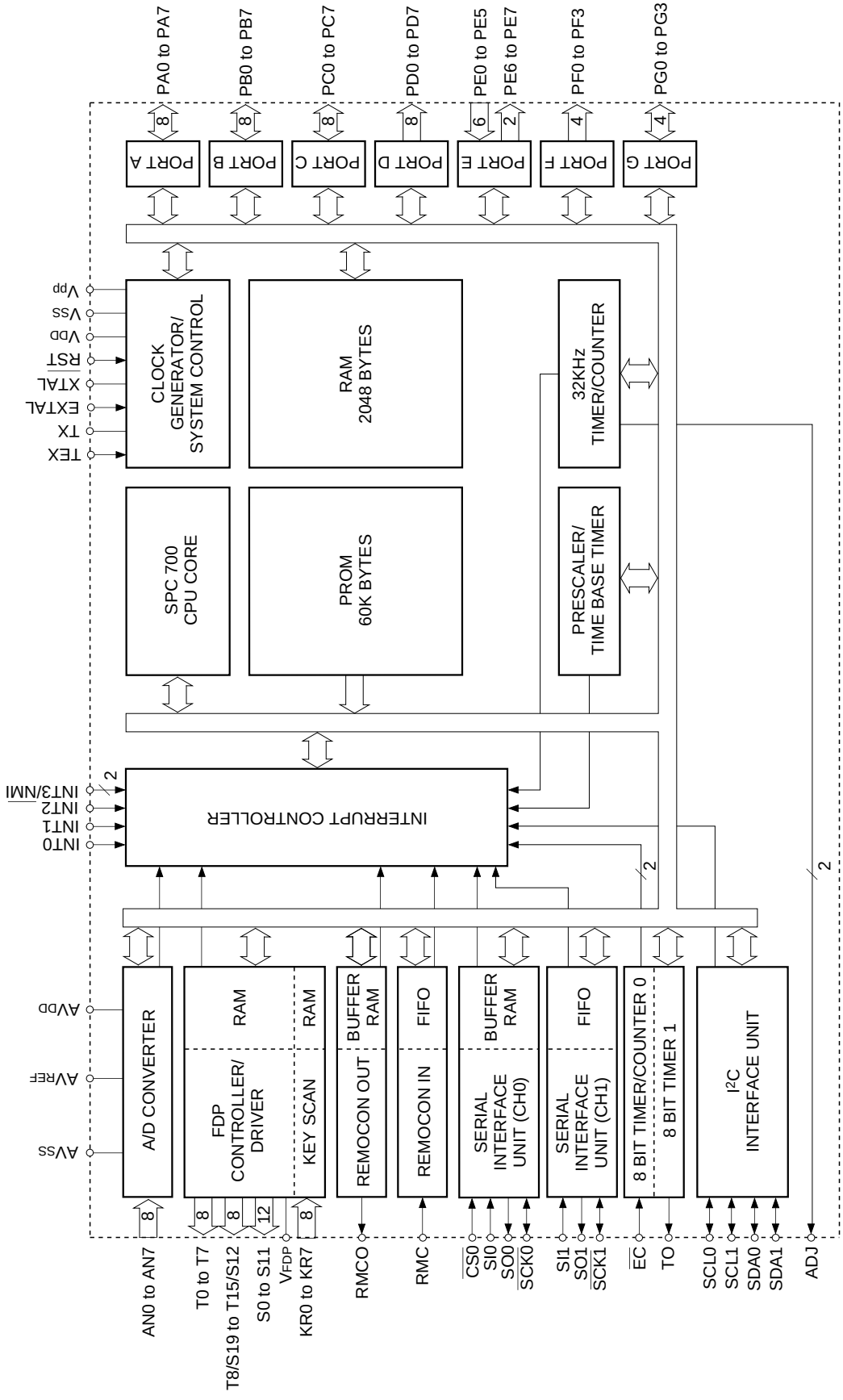
Features

- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 250ns at 16MHz operation (122µs at 32kHz operation)
- Incorporated PROM capacity — 60K bytes
- Incorporated RAM capacity — 2048 bytes (including fluorescent display area)
- Peripheral functions
  - — A/D converter — 8 bits, 8 channels, successive approximation method (Conversion time of 20µs/16MHz)
  - — Serial interface — Buffer RAM incorporated (Auto transfer for 1 to 32 bytes), 1 channel
    8-bit, 8-stage FIFO incorporated
    (Auto transfer for 1 to 8 bytes), 1 channel
  - — Timers — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
    32kHz timer/counter
  - — Fluorescent display panel controller/driver — High voltage drive output port of 28 pins (40V)
    Maximum of 196 segments display possible
    1 to 16-digit dynamic display
    Dimmer function
    On-chip incorporated pull-down resistor
    Hardware key scan function
    Maximum of 12 × 8 key matrix supportable
  - — I²C bus interface
  - — Remote control transmission circuit — Auto transmission for 1 to 32 bytes, restart function, carrier output function
  - — Remote control reception circuit — 8-bit pulse measurement counter, 6-stage FIFO
- Interruption — 16 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 80-pin plastic QFP

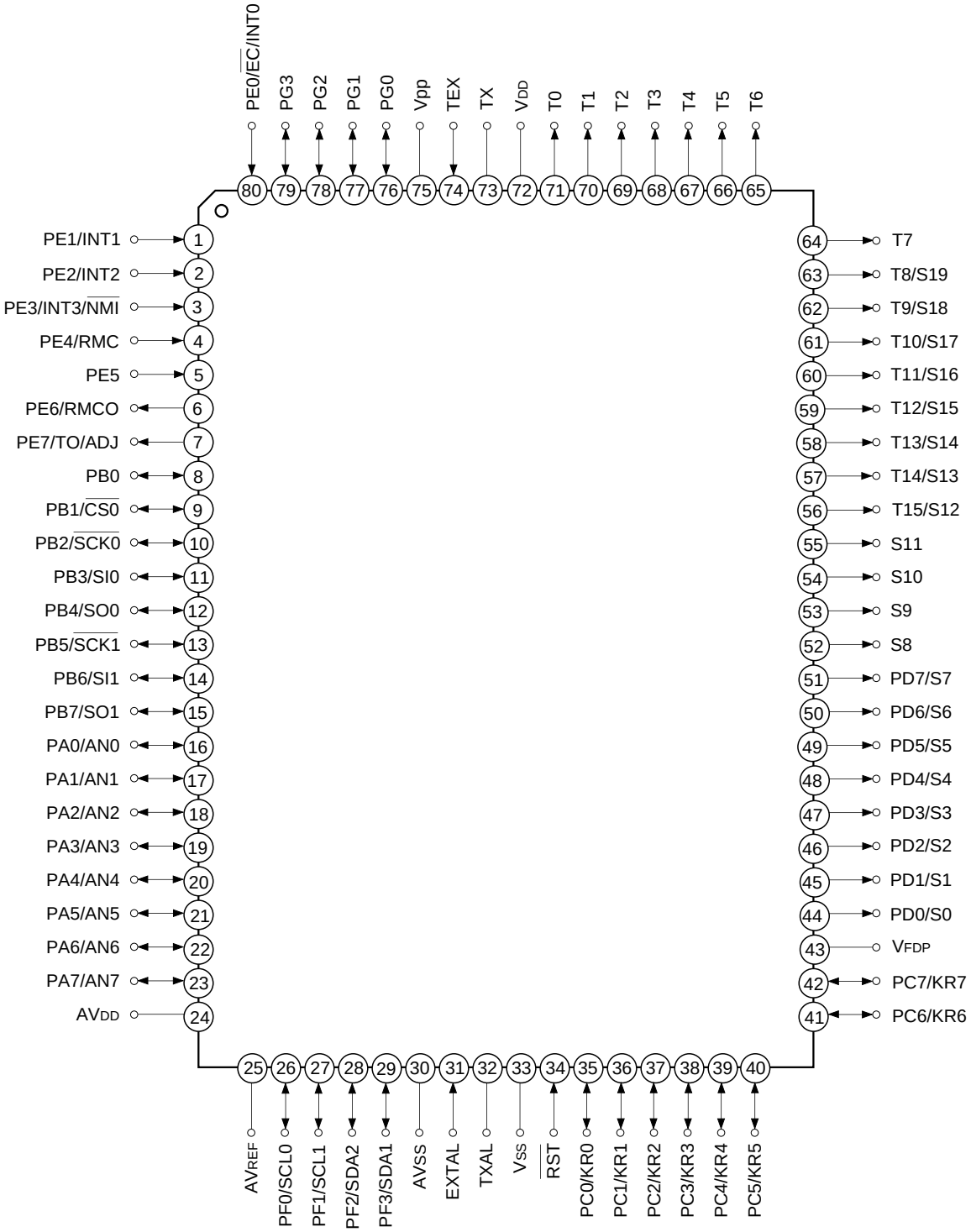
Perchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

E95326-PP

Block Diagram



Pin Assignment (Top View)



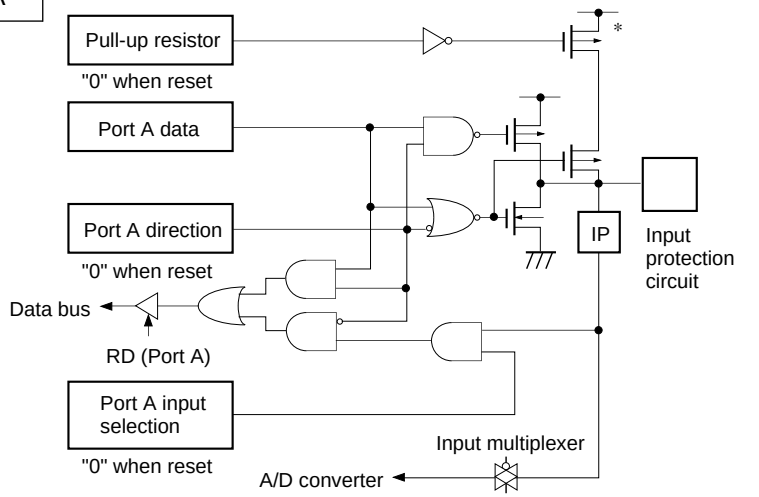
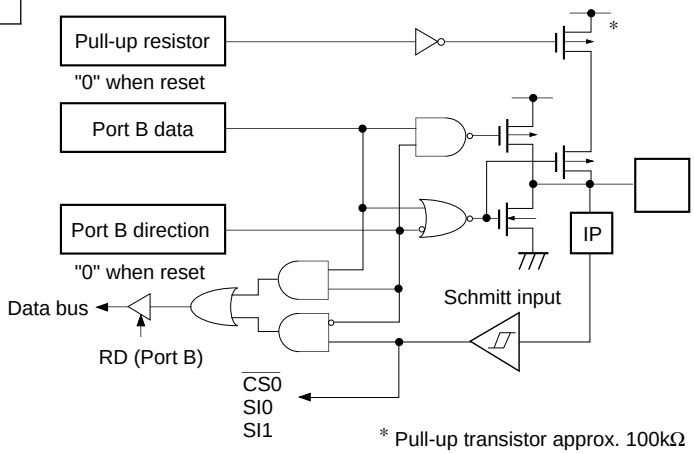
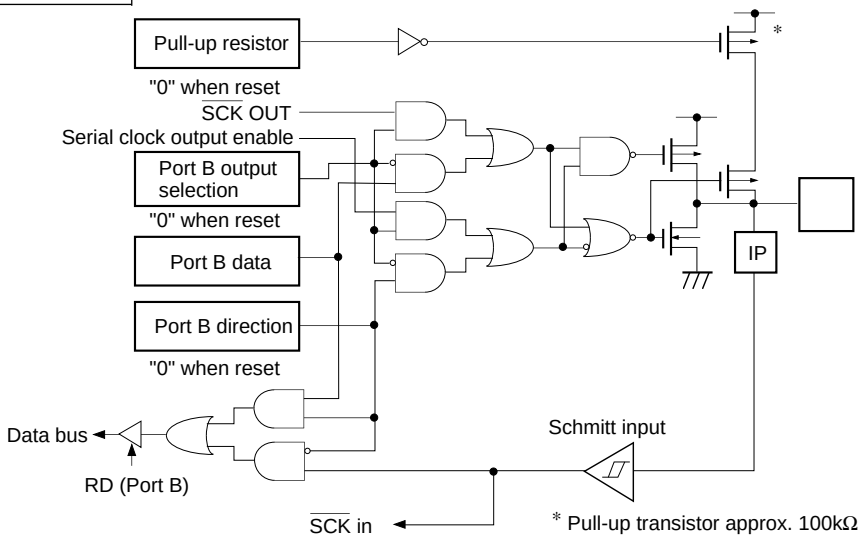
Note) Vpp (Pin 75) must be connected to V_{DD}.

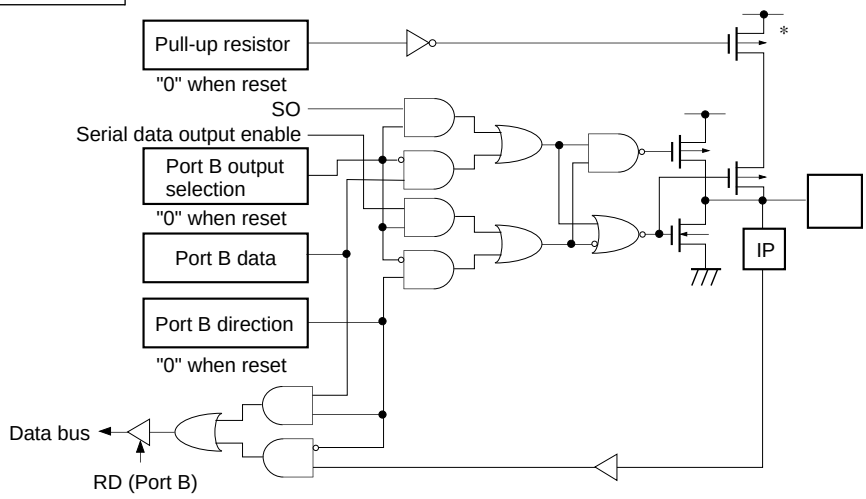
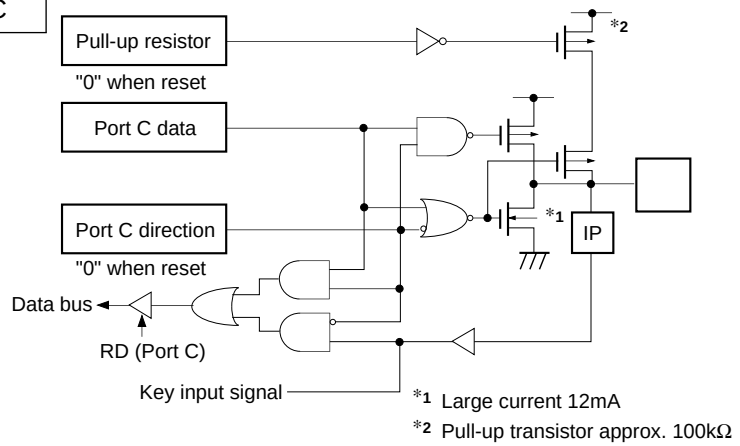
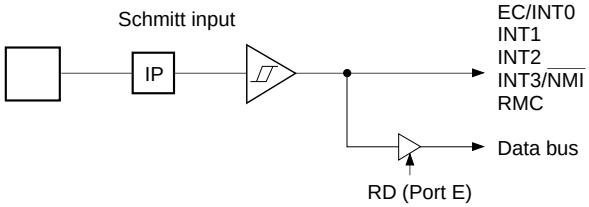
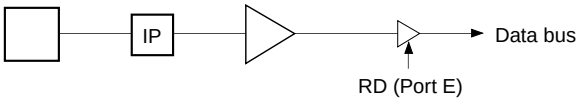
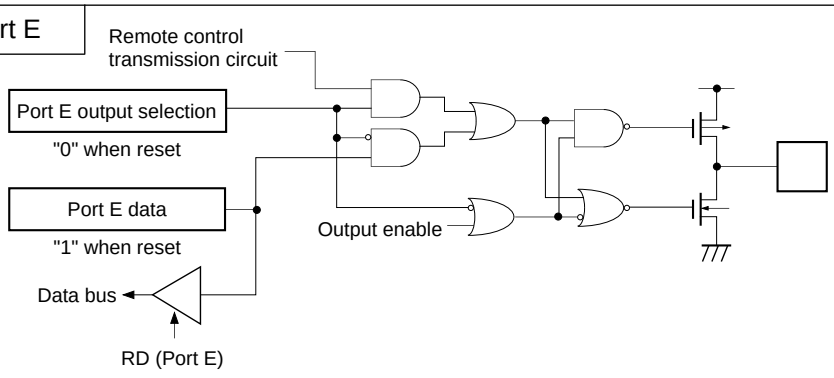
Pin Description

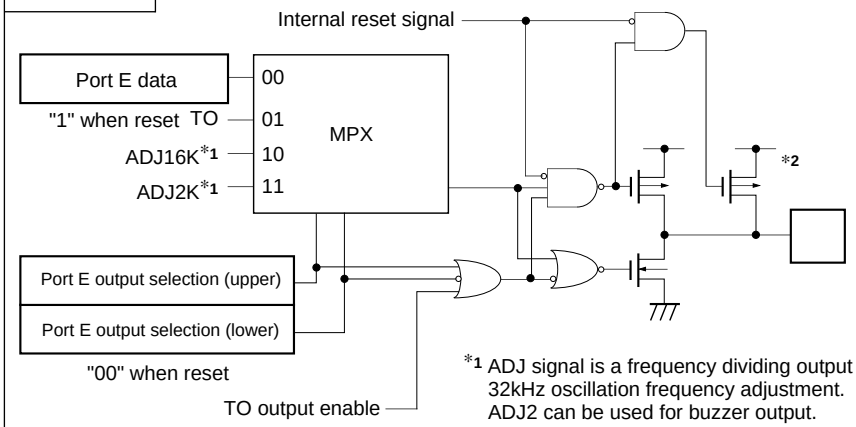
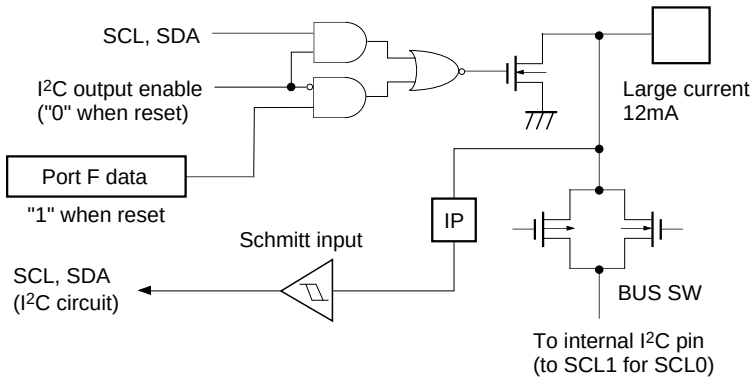
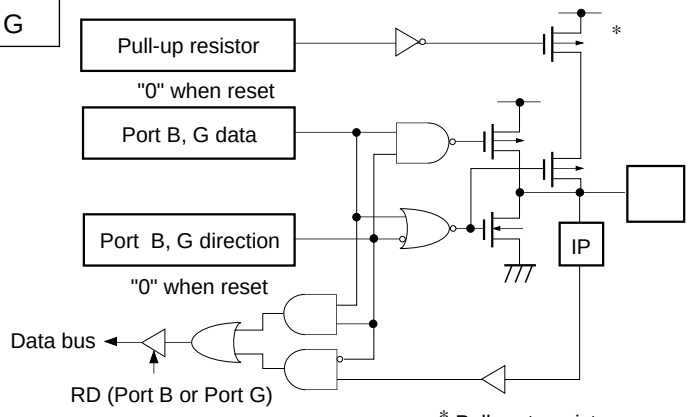
Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal (8 pins).
PE0/INT0/$\overline{EC}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins) — External event inputs for timer/counter.
PE1/INT1	Input/Input		
PE2/INT2	Input/Input		
PE3/INT3/ $\overline{NMI}$	Input/Input/Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Remote control reception circuit input.
PE5	Input		
PE6/RMCO	Output/Output		Carrier output of remote control transmission circuit.
PE7/TO/ADJ	Output/Output/ Output		Output for the timer/counter rectangular waves, and 32kHz oscillation dividing frequency.

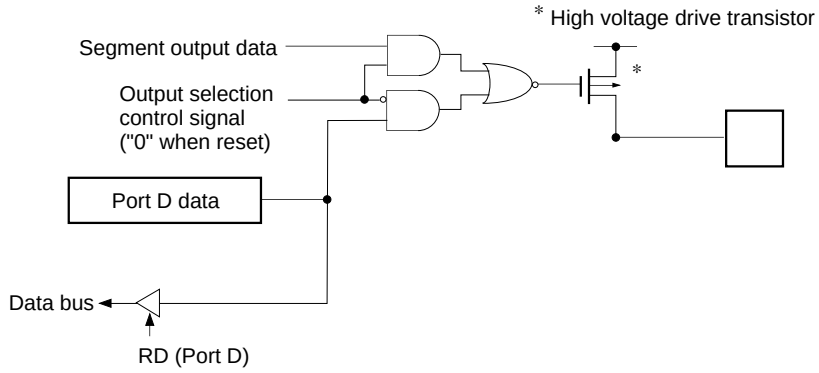
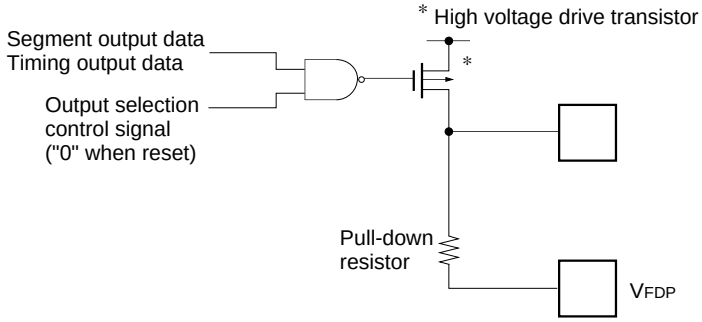
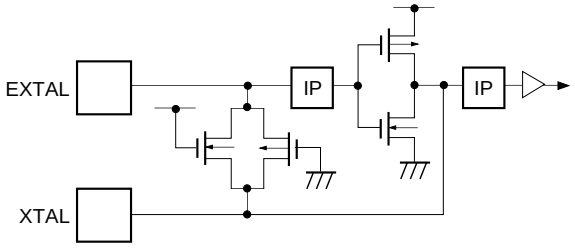
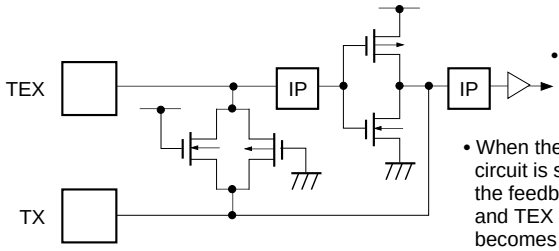
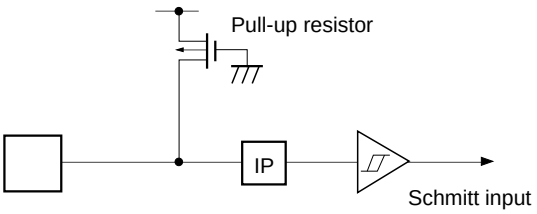
Pin code	I/O	Functions	
PF0/SCL0 PF1/SCL1	Output/I/O	(Port F) 4-bit output port, operating as N-ch open drain output for large current (12mA). (4 pins)	Transfer clock I/Os for I^2C bus interface. (2 pins)
PF2/SDA0 PF3/SDA1	Output/I/O		Transfer data I/Os for I^2C bus interface. (2 pins)
PG0 to PG3	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (4 pins)	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output ports. (8 pins)	FDP segment signal outputs. (8 pins)
S8 to S11	Output	FDP segment signal outputs. (4 pins)	
T8/S12 to T15/S19	Output/Output	Outputs for FDP timing signals/segment signals. (8 pins)	
T0 to T7	Output	FDP timing signal outputs.	
V_{FDP}		FDP voltage supply.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event counter, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
NC		NC. Under normal operation, connect to V_{DD}.	
AV_{DD}		Positive power supply for A/D converter.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		A/D converter GND.	
Vpp		Positive power supply for built-in PROM writing. Connect to V_{DD} for normal operation.	
V_{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A  	Hi-Z
PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 3 pins	Port B  Not Schmitt input for SI0 and SI1.	Hi-Z
PB2/$\overline{SCK0}$ PB5/SCK1 2 pins	Port B  	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B 	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC}$/INT0 PE1/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	Port E 	Hi-Z
PE5 1 pin	Port E 	Hi-Z
PE6/RMCO 1 pin	Port E 	High level

Pin	Circuit format	When reset
PE7/TO/ADJ 1 pin	Port E  *1 ADJ signal is a frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2 can be used for buzzer output. *2 Pull-up transistor approx. 150kΩ.	High level (with approx. 150kΩ resistor when reset)
PF0/SCL0 PF1/SCL1 PF2/SDA0 PF3/SDA1 4 pins	Port F  	Hi-Z
PB0 PG0 to PG3 5 pins	Port B Port G  * Pull-up transistor approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PD0/S0 to PD7/S7 8 pins	Port D 	Hi-Z
S8 to S11 T15/S12 to T8/S19 T0 to T7 20 pins		Low level
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes High.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX becomes Low level and TX becomes High level.	Oscillation
$\overline{\text{RST}}$ 1 pins		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Display output voltage	V_{OD}	V_{DD} – 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} is reference.
High level output current	I_{OH}	–5	mA	All pins excluding outputs*3 (value per pin)
	I_{ODH1}	–15	mA	Display outputs S0 to S11 (value per pin)
	I_{ODH2}	–35	mA	Display outputs T0 to T7, and T8/S19 to T15/S12 (value per pin)
High level total output current	$\sum I_{OH}$	–40	mA	Total for all pins excluding display outputs
	$\sum I_{ODH}$	–100	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	Port (value per pin)
	I_{OLC}	20	mA	Large current Port (value per pin)*4
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowabl power dissipation	P_D	600	mW	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 Specifies output current of general-purpose I/O ports.

*4 The large current drive transistor is the N-CH transistor of Port C (PC) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for high-speed mode (1/2, 1/4 frequency dividing clock)
		3.5	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock) or SLEEP mode
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
	Vpp	Vpp = V_{DD}		V	*4
Analog power supply	AV_{DD}	4.5	5.5	V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*3
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2
	V_{ILEX}	–0.3	0.4	°C	EXTAL*3
Operating temperature	Topr	–10	+75		

*1 Value for each pin of normal input port (PA, PB0, PB3, PB4, PB6, PB7, PC, PE5, PG).

*2 Value of the following pins: $\overline{RST}$, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, INT3/$\overline{NMI}$, RMC, SCL0, SCL1, SDA0, SDA1.

*3 Specifies only during external clock input.

*4 Vpp and V_{DD} should be set to the same voltage.

*5 AV_{DD} and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA, PB, PC, PE6, PE7, PG	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PC*1, PG*1				–50	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–3.3			µA
Display output current	I_{OH}	S0 to S11	V_{DD} = 4.5V V_{OH} = V_{DD} – 2.5V	–8			mA
		S12/T15 to S19/T8, T0 to T7		–20			mA
Open drain output leakage current (P-CH Tr off state)	I_{LOL}	S0 to S11, S12/T15 to S19/T8, T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} – 35V V_{FDP} = V_{DD} – 35V			–20	µA
Pull-down resistance	R_L	S8 to S11, S12/T15 to S19/T8, T0 to T7	V_{DD} = 5V V_{OD} – V_{FDP} = 30V	60	100	270	kΩ
I/O leakage current	I_{IZ}	PA to PC*1, PG*1	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr off state)	I_{LOH}	PF	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (Output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*2	I_{DD1}	V_{DD}	High speed mode operation (1/2 frequency dividing clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		36	55	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		46	120	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		2.6	10	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation			30	µA
Input capacity	C_{IN}	PA to PC, PE0 to PE5, PG, PF, EXTAL, XTAL, TX, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 PA to PC and PG specify the input current when pull-up resistance has been selected, leakage current when no resistance has been selected.

*2 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC}$	Fig. 3	4tsys*1			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			µs
Event count input rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock registor (address: $00FE_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

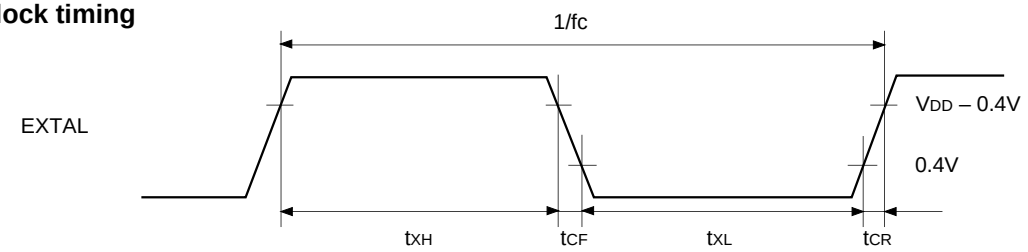


Fig. 2. Clock applied conditions

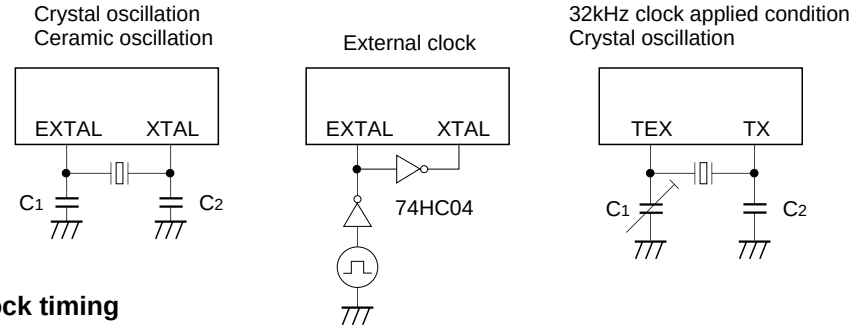
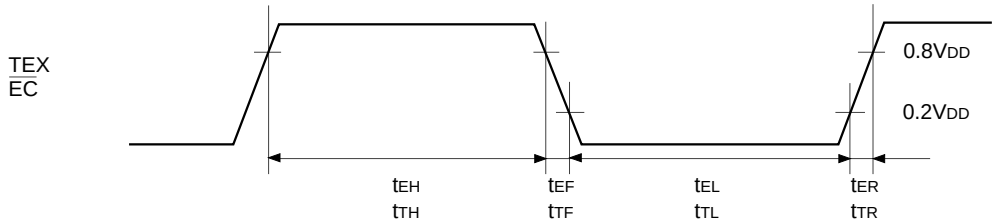


Fig. 3. Event count clock timing



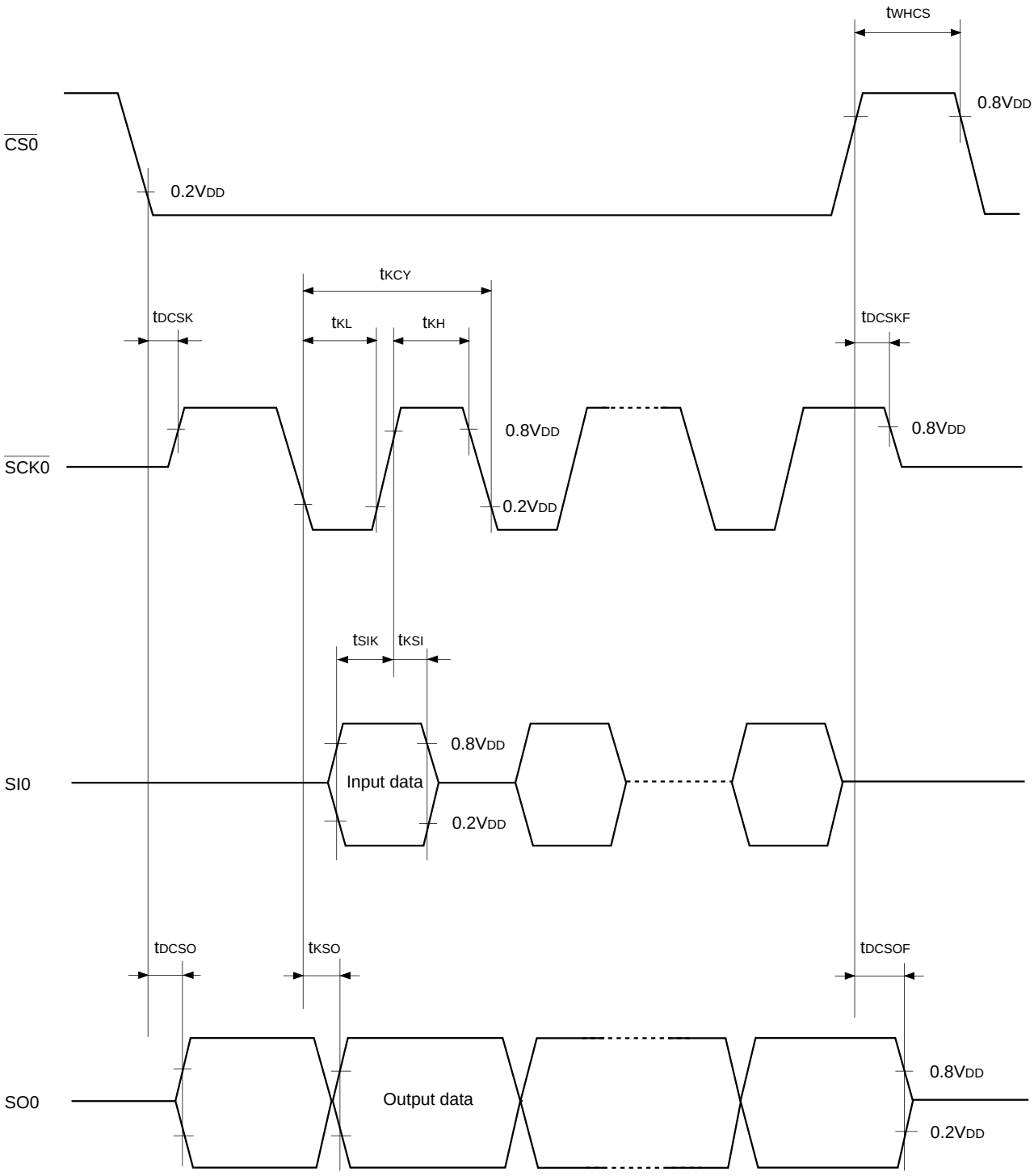
(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow\rightarrow\overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow\overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS0}\downarrow\rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI0 input setup time (for $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock registor (CLC: 00FE$_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing (CH0)



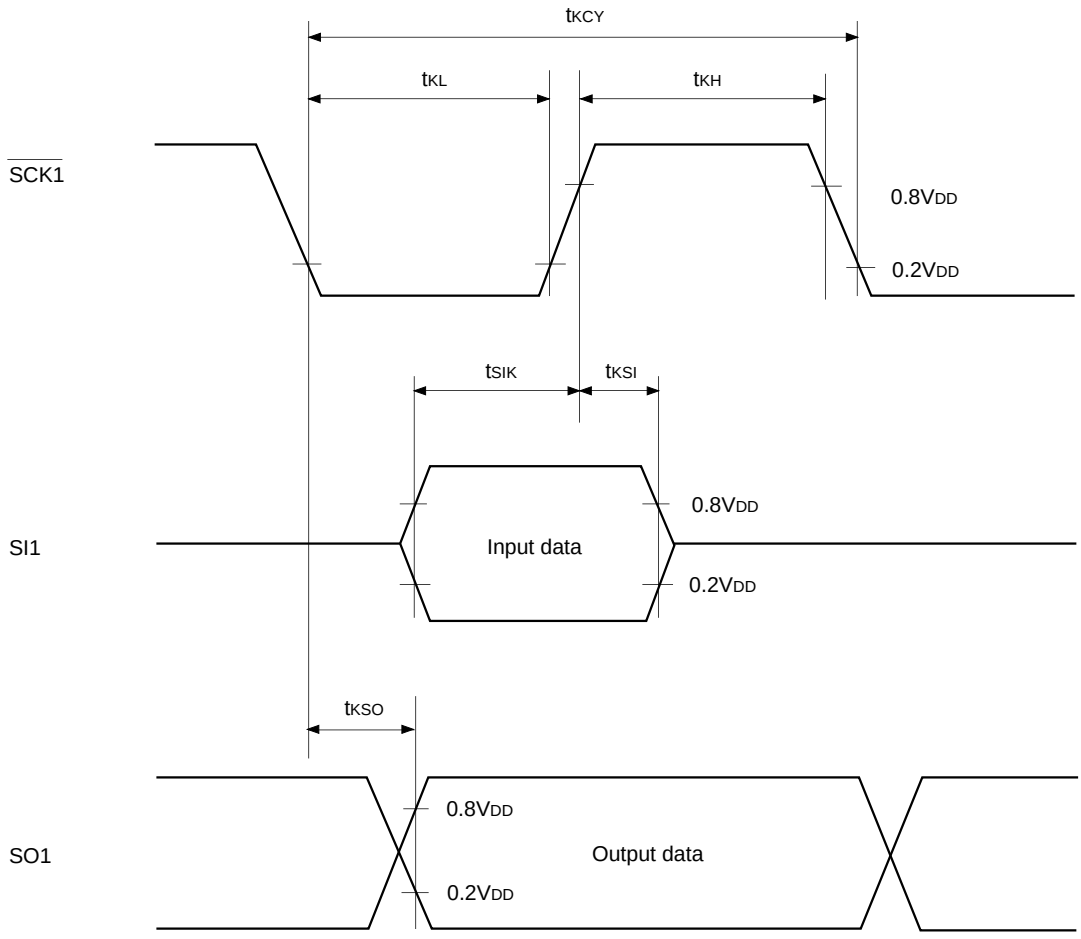
Serial transfer (CH1) (SIO mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys + 200		ns
			Ouput mode	16000/fc		ns
$\overline{SCK1}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys + 100		ns
			Ouput mode	8000/fc – 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ ouput mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ ouput mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 200	ns
			$\overline{SCK1}$ ouput mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock registor (CLC: $00FE_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK1}$output mode, SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing (SIO mode)



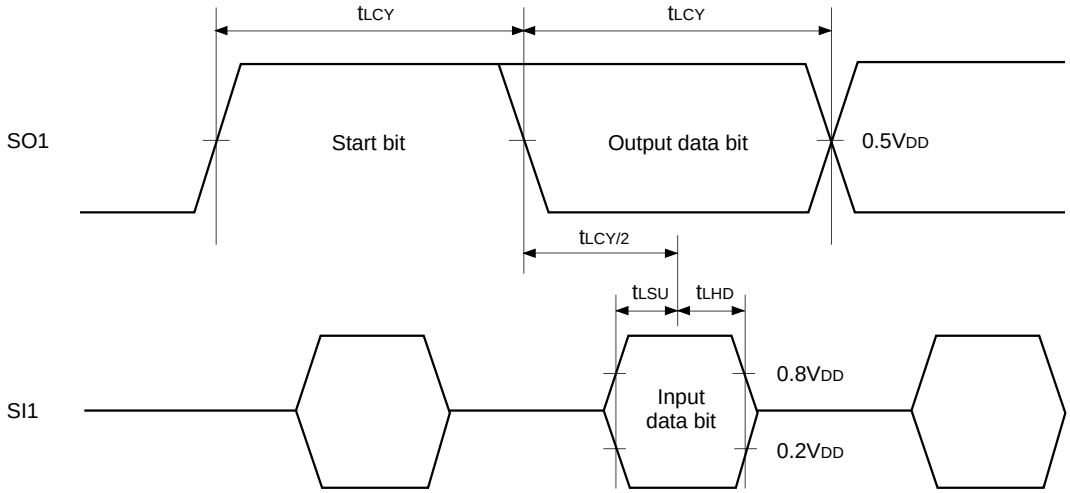
Serial transfer (CH1) (Special mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

*1 t_{LCY} is specified only when the lower two bits (SO1 clock selected) of the serial mode register (CH1) (SIOM1: $01E2_H$) is set to 104µs.

Note) The load condition for SO1 is 50pF + 1TTL.

Fig. 6. Serial transfer CH1 timing (Special mode)

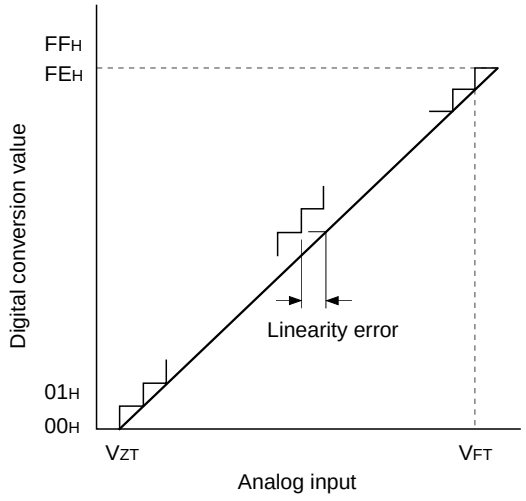


(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 7. Definition of A/D converter terms



*1 V_{ZT}: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

CKS / PCK1, PCK0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 8. Interruption input timing

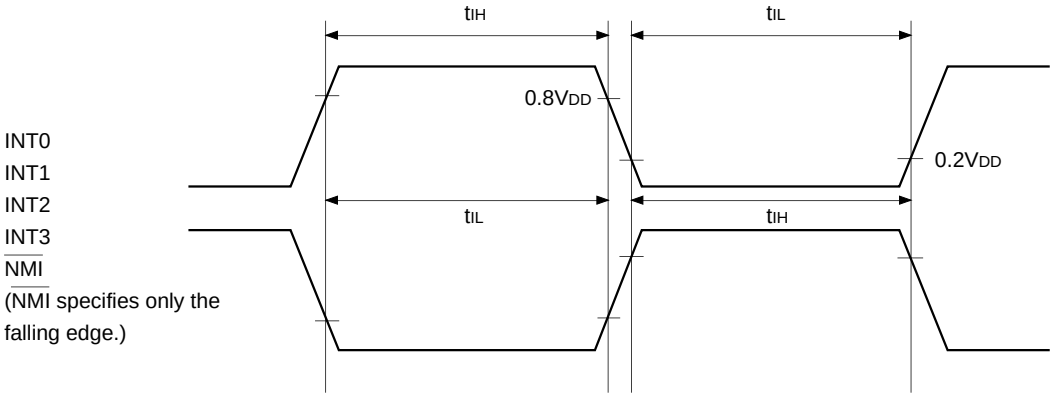
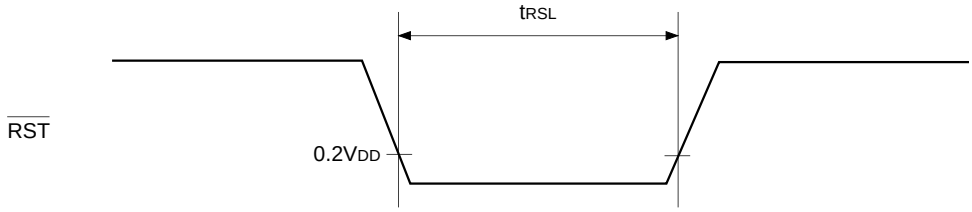


Fig. 9. $\overline{RST}$ input timing



(5) I²C bus timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repetitive transfers	$t_{SU; STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD; DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU; DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU; STO}$	SDA, SCL		4.7		µs

*1 The data hold time must exceed 300ns because the SCL rise time (300ns max.) is not taken into consideration.

Fig.10. I²C bus transfer timing

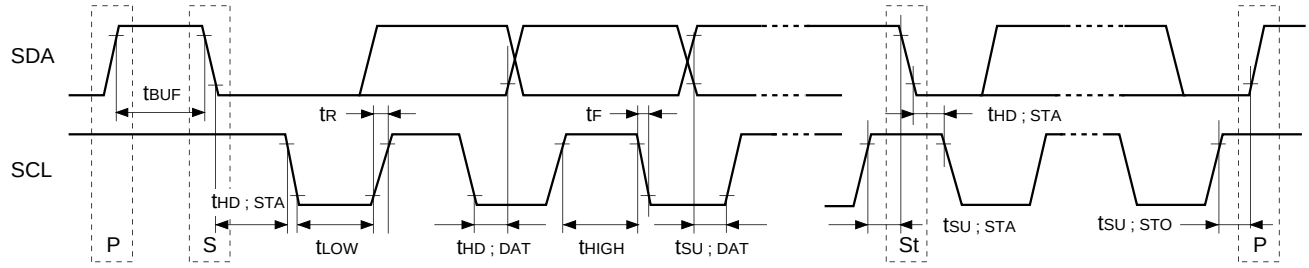
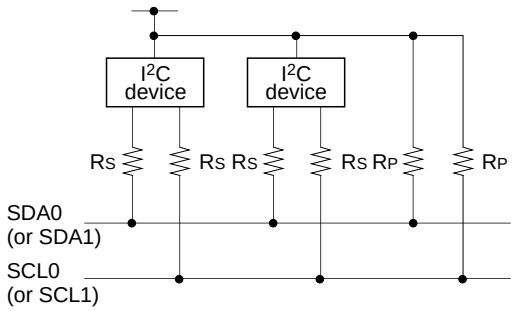


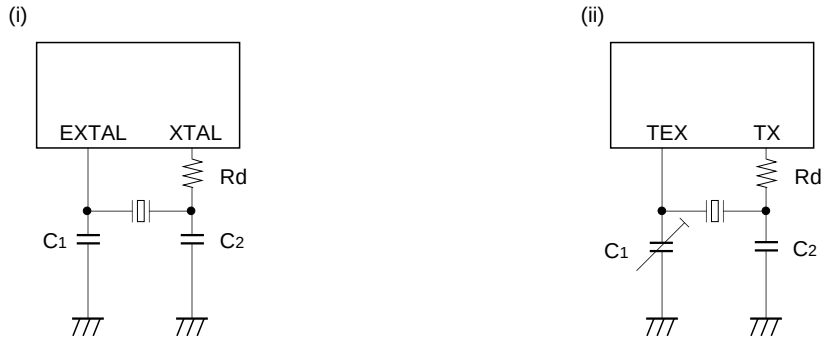
Fig.11. Recommended circuit example for I²C device



- Pull-up resistors (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (Rs = 300Ω or less) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flash-over.

Appendix

Fig. 12. Recommended oscillation circuit



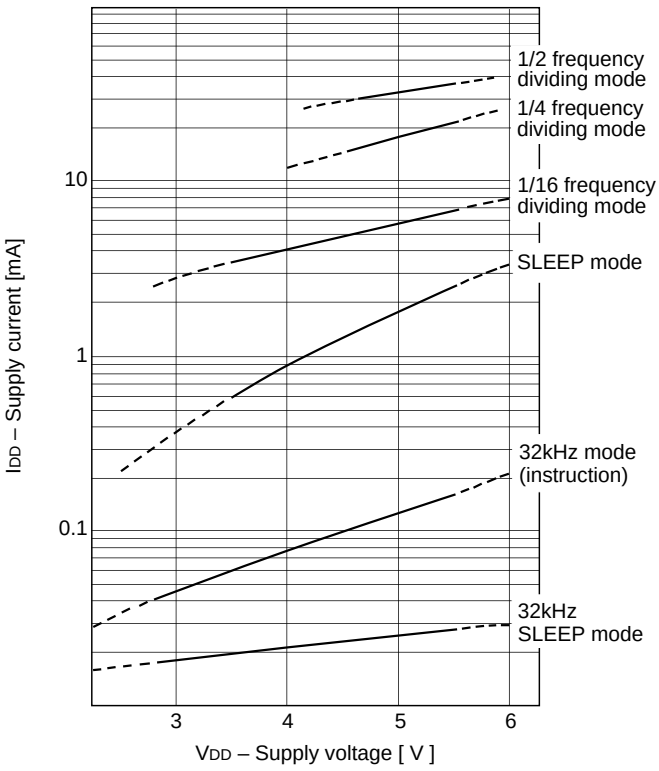
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Product List

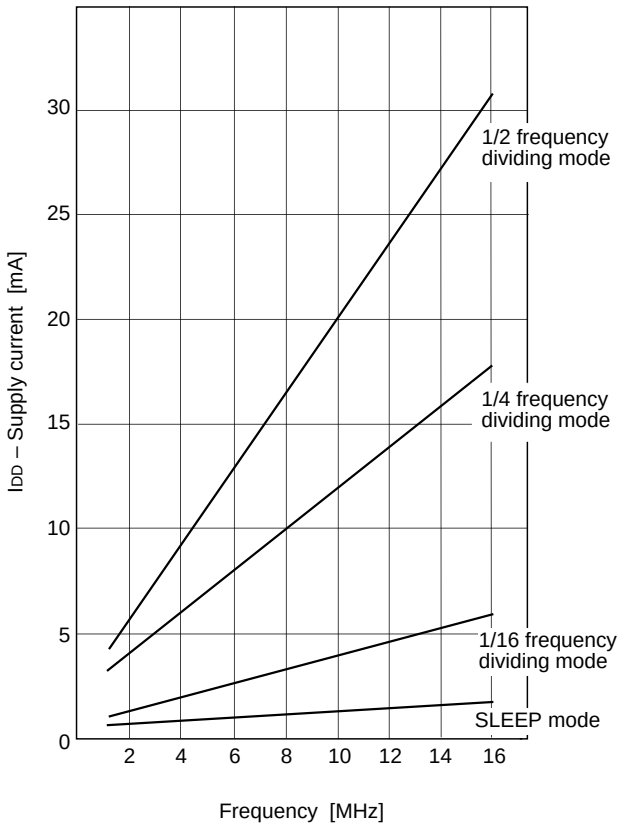
Option item	Mask product				PROM version
	CXP82940	CXP82948	CXP82952	CXP82960	CXP829P60Q-1-□□□
Package	80-pin plasitc QFP				80-pin plasitc QFP
ROM capacitance	40 Kbytes	48 Kbytes	52 Kbytes	60 Kbytes	PROM 60 Kbytes
Reset pull-up resistance	Existent/Non-existent				Existent
High voltage drive pin pull-down resistance	Existent/Non-existent				Non-existent (PD0/S0 to PD7/S7) Existent (T0 to T15, S8 to S11)

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

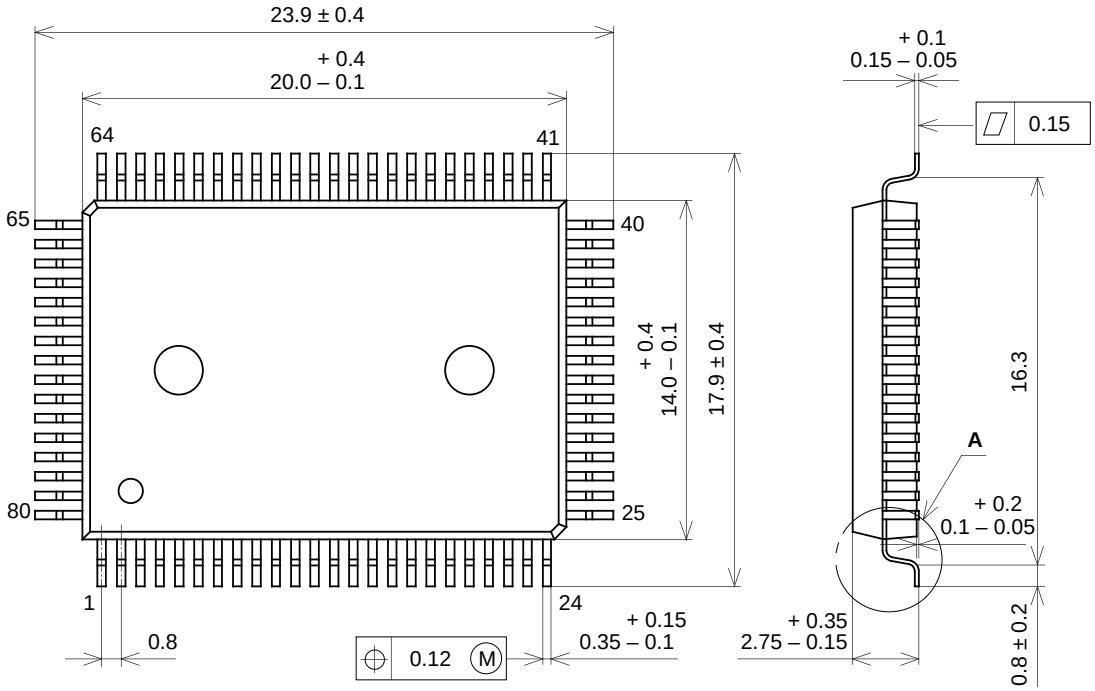


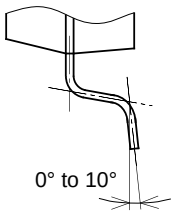
IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g