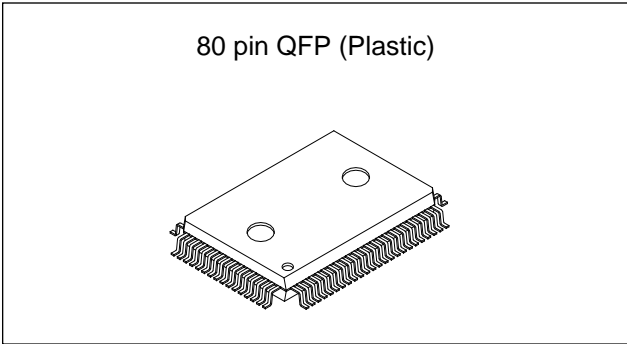# SONY

CXP82940/82948/82952/82960

CMOS 8-bit Single Chip Microcomputer

Description

The CXP82940/82948/82952/82960 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, fluorescent display panel controller/driver, I^{2}C bus interface, remote control transmission circuit, remote control reception circuit, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

80 pin QFP (Plastic)

Features1

- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
- Incorporated ROM capacity

- Incorporated RAM capacity
- Periphera; functions
  — A/D converter

  — Serial interface

  — Timers

  — Fluorescent display panel controller/driver

  — I^{2}C bus interface
  — Remote control transmission circuit

  — Remote control reception circuit
- Interruption
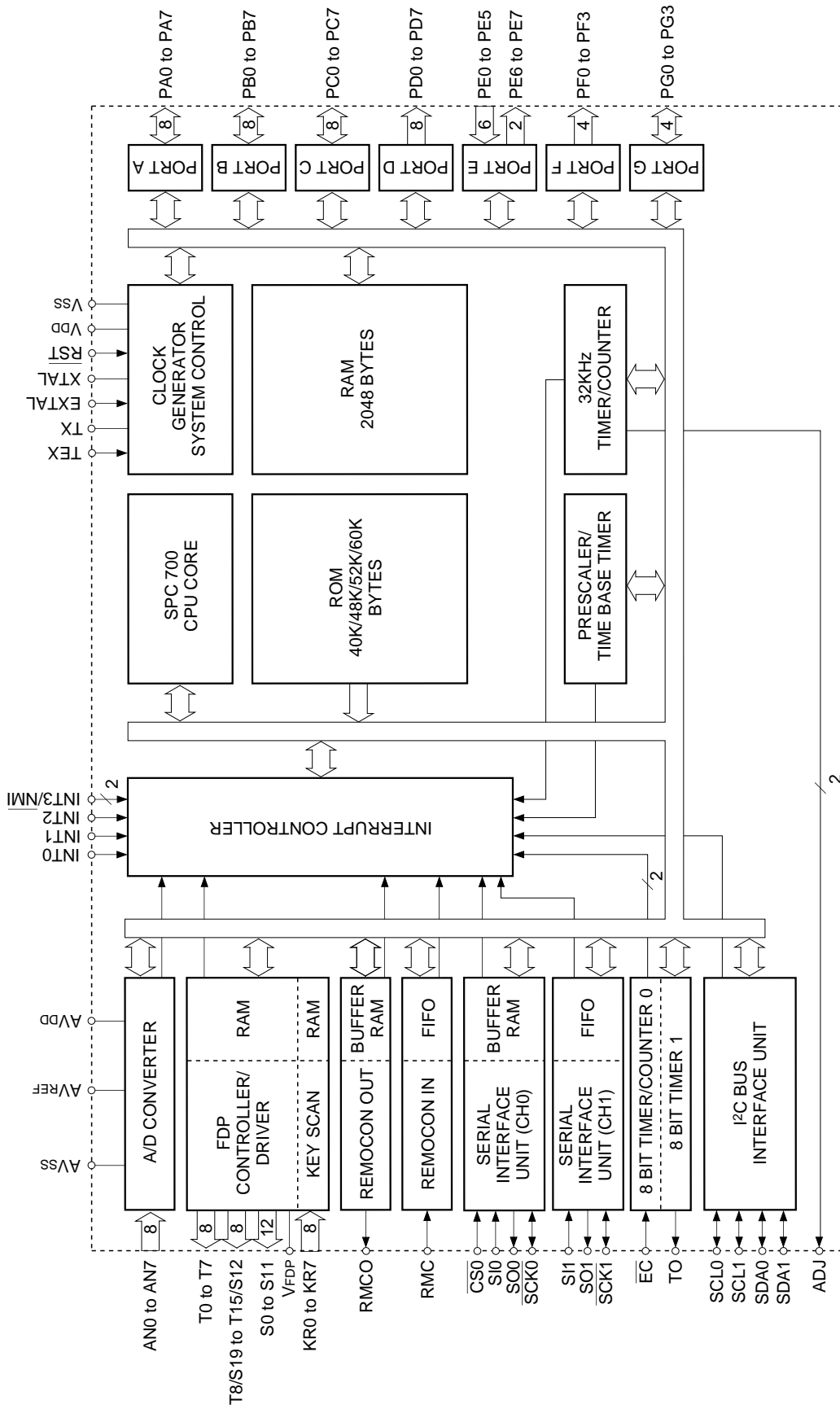- Standby mode
- Package
- Piggyback/evaluation chip

250ns at 16MHz operation
(122µs at 32kHz operation)
40K bytes (CXP82940)
48K bytes (CXP82948)
52K bytes (CXP82952)
60K bytes (CXP82960)
2048 bytes (including fluorescent display area)

8-bit, 8-channel, successive approximation method
(Conversion time of 20µs/16MHz)
Buffer RAM incorporated (Auto transfer for 1 to 32 bytes), 1 channel
8-bit, 8-stage FIFO incorporated
(Auto transfer for 1 to 8 bytes), 1 channel
8-bit timer, 8-bit timer/counter, 19-bit time base timer
32kHz timer/counter
Maximum of 196 segments display possible
1 to 16-digit dynamic display
Dimmer function
High voltage drive output (40V)
Incorporated pull-down resistor (Mask option)
Hardware key scan function
Maximum of 12 × 8 key matrix supportable

Auto transmission for 1 to 32 bytes,
restart function, carrier output function
8-bit pulse measurement counter, 6-stage FIFO
16 factors, 15 vectors, multi-interruption possible
SLEEP/STOP
80-pin plastic QFP
CXP82900 80-pin ceramic QFP

Structure
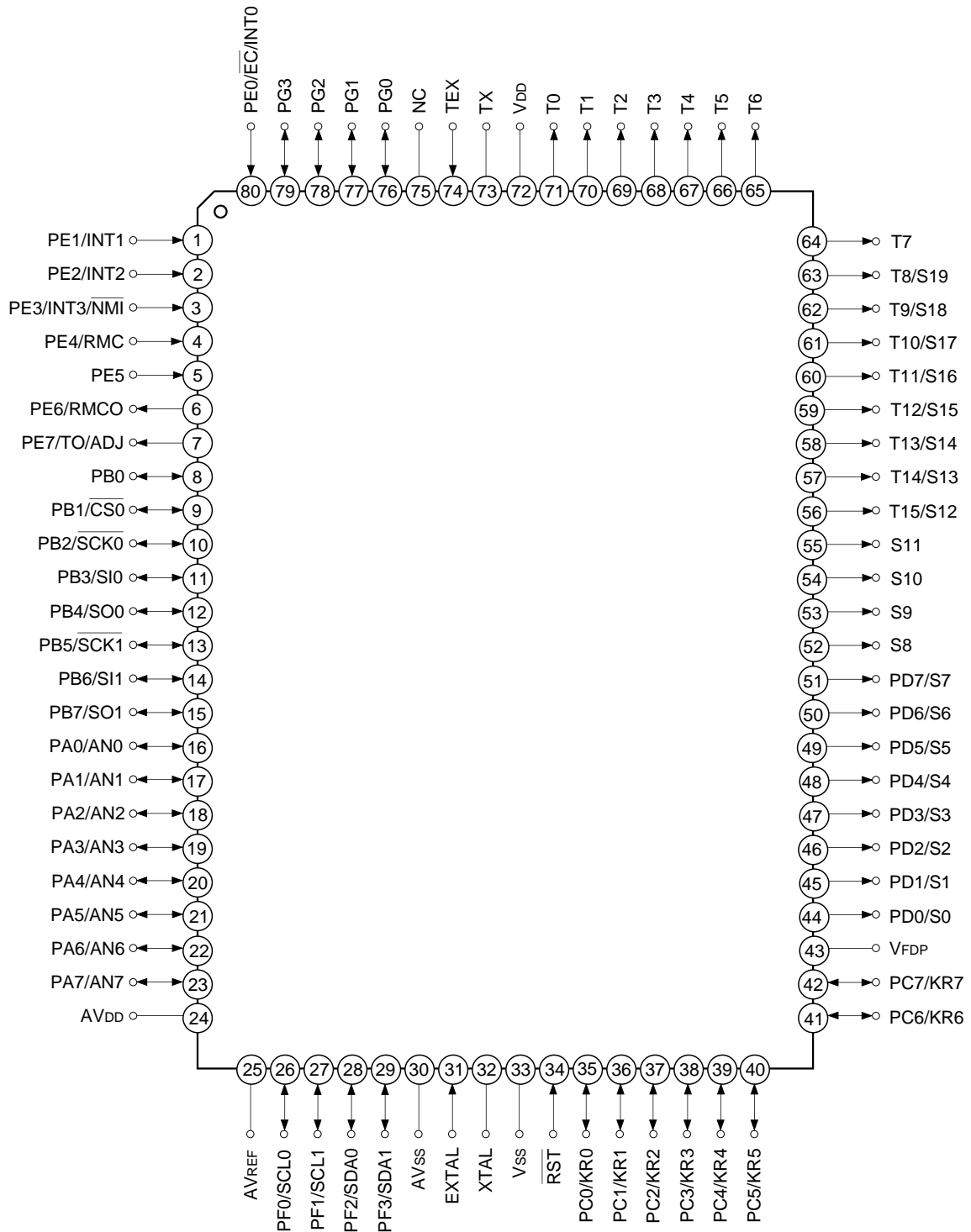
Silicon gate CMOS IC

E95130-PK

Block Diagram

PA0 to PA7 — PORT A — 8

PB0 to PB7 — PORT B — 8

PC0 to PC7 — PORT C — 8

PD0 to PD7 — PORT D — 8

PE0 to PE5 — PORT E — 6
PE6 to PE7 — 2

PF0 to PF3 — PORT F — 4

PG0 to PG3 — PORT G — 4

CLOCK GENERATOR SYSTEM CONTROL

VSS
VDD
RST
XTAL
EXTAL
TX
TEX

RAM 2048 BYTES

32KHz TIMER/COUNTER

SPC 700 CPU CORE

ROM 40K/48K/52K/60K BYTES

PRESCALER/ TIME BASE TIMER

INTERRUPT CONTROLLER

INT3/NMI — 2
INT2
INT1
INT0

2

A/D CONVERTER

FDP CONTROLLER/ DRIVER — RAM

KEY SCAN — RAM

REMOCON OUT — BUFFER RAM

REMOCON IN — FIFO

SERIAL INTERFACE UNIT (CH0) — BUFFER RAM

SERIAL INTERFACE UNIT (CH1) — FIFO

8 BIT TIMER/COUNTER 0
8 BIT TIMER 1

I²C BUS INTERFACE UNIT

AVDD
AVREF
AVSS

AN0 to AN7 — 8

T0 to T7 — 8
T8/S19 to T15/S12 — 8
S0 to S11 — 12
VFDP
KR0 to KR7 — 8

RMCO

RMC

CS0
SI0
SO0
SCK0

SI1
SO1
SCK1

EC
TO

SCL0
SCL1
SDA0
SDA1

ADJ

2

Pin Assignment (Top View)

Top pins (80–65): PE0/$\overline{EC}$/INT0 (80), PG3 (79), PG2 (78), PG1 (77), PG0 (76), NC (75), TEX (74), TX (73), V$_{DD}$ (72), T0 (71), T1 (70), T2 (69), T3 (68), T4 (67), T5 (66), T6 (65)

Left pins (1–24):
- PE1/INT1 (1)
- PE2/INT2 (2)
- PE3/INT3/$\overline{NMI}$ (3)
- PE4/RMC (4)
- PE5 (5)
- PE6/RMCO (6)
- PE7/TO/ADJ (7)
- PB0 (8)
- PB1/$\overline{CS0}$ (9)
- PB2/$\overline{SCK0}$ (10)
- PB3/SI0 (11)
- PB4/SO0 (12)
- PB5/$\overline{SCK1}$ (13)
- PB6/SI1 (14)
- PB7/SO1 (15)
- PA0/AN0 (16)
- PA1/AN1 (17)
- PA2/AN2 (18)
- PA3/AN3 (19)
- PA4/AN4 (20)
- PA5/AN5 (21)
- PA6/AN6 (22)
- PA7/AN7 (23)
- AV$_{DD}$ (24)

Right pins (64–41):
- T7 (64)
- T8/S19 (63)
- T9/S18 (62)
- T10/S17 (61)
- T11/S16 (60)
- T12/S15 (59)
- T13/S14 (58)
- T14/S13 (57)
- T15/S12 (56)
- S11 (55)
- S10 (54)
- S9 (53)
- S8 (52)
- PD7/S7 (51)
- PD6/S6 (50)
- PD5/S5 (49)
- PD4/S4 (48)
- PD3/S3 (47)
- PD2/S2 (46)
- PD1/S1 (45)
- PD0/S0 (44)
- V$_{FDP}$ (43)
- PC7/KR7 (42)
- PC6/KR6 (41)

Bottom pins (25–40): AV$_{REF}$ (25), PF0/SCL0 (26), PF1/SCL1 (27), PF2/SDA0 (28), PF3/SDA1 (29), AV$_{SS}$ (30), EXTAL (31), XTAL (32), V$_{SS}$ (33), $\overline{RST}$ (34), PC0/KR0 (35), PC1/KR1 (36), PC2/KR2 (37), PC3/KR3 (38), PC4/KR4 (39), PC5/KR5 (40)

Note) NC (Pin 75) must be connected to V$_{DD}$.

Pin Description

Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal (8 pins).
PE0/INT0/$\overline{EC}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins) / External event inputs for timer/counter.
PE1/INT1	Input/Input		
PE2/INT2	Input/Input		
PE3/INT3/ $\overline{NMI}$	Input/Input/Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Remote control reception circuit input.
PE5	Input		
PE6/RMCO	Output/Output		Carrier output of remote control transmission circuit.
PE7/TO/ADJ	Output/Output/ Output		Output for the timer/counter rectangular waves, and 32kHz oscillation dividing frequency.
PF0/SCL0 PF1/SCL1	Output/I/O	(Port F) 4-bit output port, operating as N-ch open drain output for large current (12mA). (4 pins)	Transfer clock I/Os for I2C bus interface.
PF2/SDA0 PF3/SDA1	Output/I/O		Transfer data I/Os for I2C bus interface.

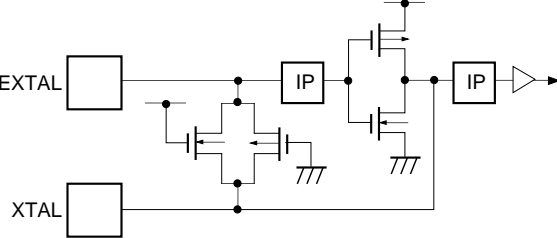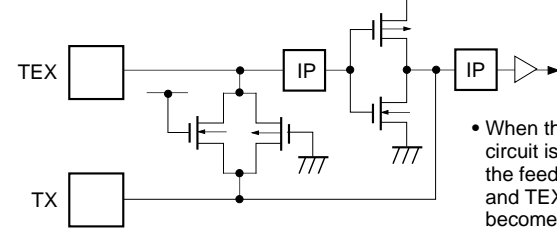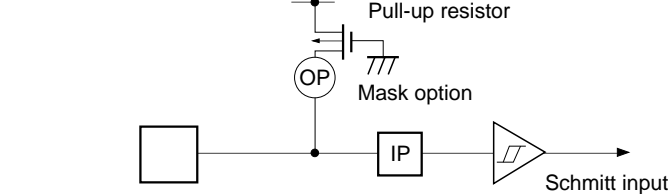| Pin code	I/O	Functions	
PG0 to PG3	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (4 pins)	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output ports. (8 pins)	FDP segment signal outputs. (8 pins)
S8 to S11	Output	FDP segment signal outputs. (4 pins)	
T8/S12 to T15/S19	Output/Output	Outputs for FDP timing signals/segment signals. (8 pins)	
T0 to T7	Output	FDP timing signal outputs.	
V_{FDP}		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
NC		NC. Under normal operation, connect to V_{DD}.	
AV_{DD}		Positive power supply for A/D converter.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		A/D converter GND.	
V_{DD}		Positive power supply.	
V_{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	**Port A** Pull-up resistor — "0" when reset Port A data Port A direction — "0" when reset Data bus ◄ RD (Port A) Port A input selection — "0" when reset A/D converter ◄ Input multiplexer IP — Input protection circuit * Pull-up transistor approx. 100kΩ	Hi-Z
PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 3 pins	**Port B** Pull-up resistor — "0" when reset Port B data Port B direction — "0" when reset Data bus ◄ RD (Port B) $\overline{CS0}$ SI0 SI1 Schmitt input IP * Pull-up transistor approx. 100kΩ Not Schmitt input for SI0 and SI1.	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	**Port B** Pull-up resistor — "0" when reset $\overline{SCK}$ OUT Output enable Port B output selection — "0" when reset Port B data Port B direction — "0" when reset Data bus ◄ RD (Port B) IP Schmitt input $\overline{SCK}$ in ◄ * Pull-up transistor approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	**Port B** Pull-up resistor — "0" when reset SO Output enable Port B output selection — "0" when reset Port B data Port B direction — "0" when reset Data bus ◄ — RD (Port B) IP * Pull-up transistor approx. 100kΩ	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	**Port C** Pull-up resistor — "0" when reset — *2 Port C data Port C direction — "0" when reset — *1 Data bus ◄ — RD (Port C) IP Key input signal *1 Large current 12mA *2 Pull-up transistor approx. 100kΩ	Hi-Z
PE0/EC/INT0 PE1/INT1 PE2/INT2 PE3/INT3/NMI PE4/RMC 5 pins	**Port E** Schmitt input IP EC/INT0 INT1 INT2 INT3/NMI RMC Data bus RD (Port E)	Hi-Z
PE5 1 pin	**Port E** IP — Data bus RD (Port E)	Hi-Z
PE6/RMCO 1 pin	**Port E** Remote control transmission circuit Port E output selection — "0" when reset Reset E data — "1" when reset Output enable Data bus ◄ — RD (Port E)	High level

– 7 –

Pin	Circuit format	When reset
PE7/TO/ADJ 1 pin	**Port E** Internal reset signal Port E data — 00 "1" when reset TO — 01 MPX ADJ16K[*1] — 10 ADJ2K[*1] — 11 Port E output selection (upper) Port E output selection (lower) "00" when reset TO output enable *1 ADJ signal is a frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2 can be used for buzzer output. *2 Pull-up transistor approx. 150kΩ.	High level (with approx. 150kΩ resistor when reset)
PF0/SCL0 PF1/SCL1 PF2/SDA0 PF3/SDA1 4 pins	**Port F** SCL, SDA I2C output enable ("0" when reset) Large current 12mA Port F data "1" when reset Schmitt input IP SCL, SDA (I2C circuit) BUS SW To internal I2C pin (to SCL1 for SCL0)	Hi-Z
PB0 PG0 to PG3 5 pins	**Port B** **Port G** Pull-up resistor * "0" when reset Port B data or Port G data Port B direction or Port G direction "0" when reset IP Data bus RD (Port B or Port G) * Pull-up transistor approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PD0/S0 to PD7/S7 8 pins	**Port D** * High voltage drive transistor Segment output data Output selection control signal ("0" when reset) Port D data OP Mask option Pull-down transistor VFDP Data bus RD (Port D)	Hi-Z or Low level (when PD resistor is connected)
S8 to S11 T15/S12 to T8/S19 T0 to T7 20 pins	* High voltage drive transistor Segment output data Timing output data Output selection control signal ("0" when reset) OP Mask option Pull-down resistor VFDP	Hi-Z or Low level (when PD resistor is connected)
EXTAL XTAL 2 pins	EXTAL IP IP XTAL • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes High.	Oscillation
TEX TX 2 pins	TEX IP IP TX • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX becomes Low level and TX becomes High level.	Oscillation
$\overline{RST}$ 1 pin	Pull-up resistor OP Mask option IP Schmitt input	Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
Input voltage	V_{IN}	−0.3 to +7.0[*1]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*1]	V	
Display output voltage	V_{OD}	$V_{DD} − 40$ to $V_{DD} + 0.3$	V	As P channel transistor is open drain, V_{DD} is reference.
High level output current	I_{OH}	−5	mA	All pins excluding outputs[*2] (value per pin)
	I_{ODH1}	−15	mA	Display outputs S0 to S11 (value per pin)
	I_{ODH2}	−35	mA	Display outputs T0 to T7, and T8/S19 to T15/S12 (value per pin)
High level total output current	ΣI_{OH}	−40	mA	Total for all pins excluding display outputs
	ΣI_{ODH}	−100	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	Port (value per pin)
	I_{OLC}	20	mA	Large current Port (value per pin)[*3]
Low level total output current	ΣI_{OL}	100	mA	Total for all output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

[*1] V_{IN} and V_{OUT} must not exceed $V_{DD} + 0.3$V.

[*2] Specifies output current of general-purpose I/O ports.

[*3] The large current drive transistor is the N-CH transistor of Port C (PC) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for high-speed mode (1/2, 1/4 frequency dividing clock)
		3.5	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock) or SLEEP mode
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[1]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input[2]
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL[3]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[1]
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input[2]
	V_{ILEX}	−0.3	0.4	V	EXTAL[3]
Operating temperature	T_{opr}	−20	+75	°C	

[1] Value for each pin of normal input port (PA, PB0, PB3, PB4, PB6, PB7, PC, PE5, PG).

[2] Value of the following pins: $\overline{RST}$, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, INT3/$\overline{NMI}$, RMC, SCL0, SCL1, SDA0, SDA1.

[3] Specifies only during external clock input.

Electrical Characteristics

DC Characteristics
(Ta = −20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA, PB, PC, PE6, PE7, PG	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
Low level output current	V_{OL}		$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
		PC, PF	$V_{DD} = 4.5V$, $I_{OL} = 12.0mA$			1.5	V
		PF (SCL0, SCL1, SDA0, SDA1)	$V_{DD} = 4.5V$, $I_{OL} = 3.0mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 4.0mA$			0.6	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	µA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	−0.5		−40	µA
	I_{IHT}	TEX	$V_{DD} = 5.5V$, $V_{IL} = 5.5V$	0.1		10	µA
	I_{ILT}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	−0.1		−10	µA
	I_{ILR}	$\overline{RST}$[1]	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	−1.5		−400	µA
	I_{IL}	PA to PC[2], PG[2]				−50	µA
			$V_{DD} = 4.5V$, $V_{IL} = 4.0V$	−3.3			µA
Display output current	I_{OH}	S0 to S11	$V_{DD} = 4.5V$ $V_{OH} = V_{DD} - 2.5V$	−8			mA
		S12/T15 to S19/T8, T0 to T7		−20			mA
Open drain output leakage current (P-CH Tr off state)	I_{LOL}	S0 to S11, S12/T15 to S19/T8, T0 to T7	$V_{DD} = 5.5V$ $V_{OL} = V_{DD} - 35V$ $V_{FDP} = V_{DD} - 35V$			−20	µA
Pull-down resistance[3]	R_L	S0 to S11, S12/T15 to S19/T8, T0 to T7	$V_{DD} = 5V$ $V_{OD} - V_{FDP} = 30V$	60	100	270	kΩ
I/O leakage current	I_{IZ}	PA to PC[2], PG[2], $\overline{RST}$[1]	$V_{DD} = 5.5V$ $V_I = 0, 5.5V$			±10	µA
Open drain output leakage current (N-ch Tr off state)	I_{LOH}	PF	$V_{DD} = 5.5V$, $V_{OH} = 5.5V$			10	µA
I²C bus switch connection impedance (Output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	$V_{DD} = 4.5V$ $V_{SCL0} = V_{SCL1} = 2.25V$ $V_{SDA0} = V_{SDA1} = 2.25V$			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current[4]	I_{DD1}	V_{DD}	High speed mode operation (1/2 frequency dividing clock)		31	50	mA
			V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)				
	I_{DD2}		V_{DD} = 3V, 32MHz crystal oscillation (C_1 = C_2 = 47pF)		40	100	µA
	I_{DDS1}		SLEEP mode		2.5	10	mA
			V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)				
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		8	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation			10	µA
Input capacity	C_{IN}	PA to PC, PE0 to PE5, PF, PG, EXTAL, XTAL, TEX, TX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

[1] $\overline{RST}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

[2] PA to PC and PG specify the input current when pull-up resistance has been selected, leakage current when no resistance has been selected.

[3] When incorporated pull-down resistance has been selected through mask option.

[4] When all pins are open.

AC Characteristics

(1) Clock timing (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC}$	Fig. 3	4tsys*			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			μs
Event count input rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

＊tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEн).

tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")
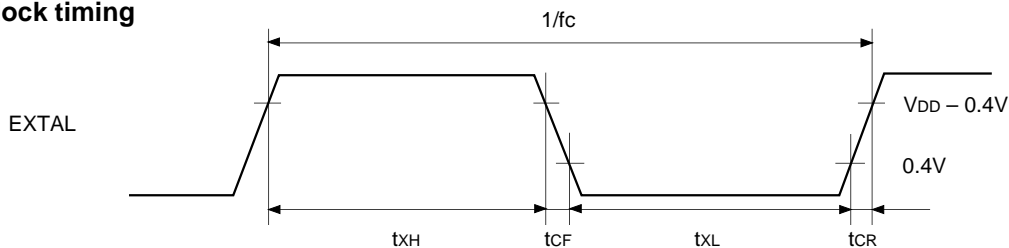
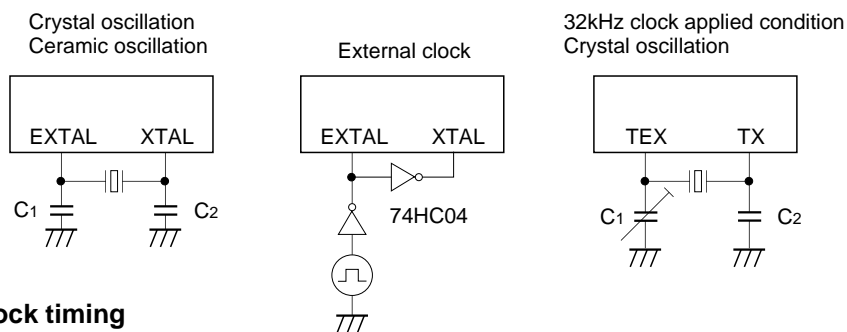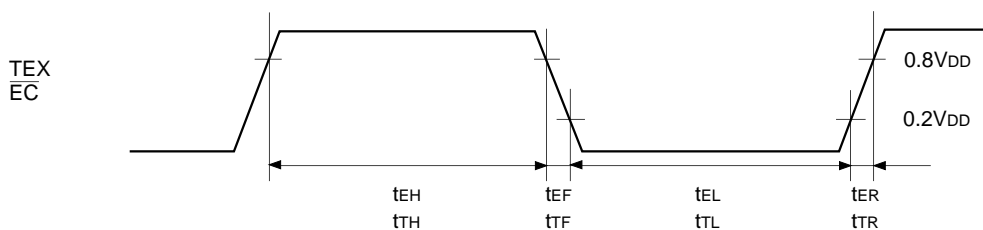**Fig. 1. Clock timing**

Fig. 2. Clock applied conditions

Fig. 3. Event count clock timing

(2) Serial transfer (CH0) $\quad$ (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

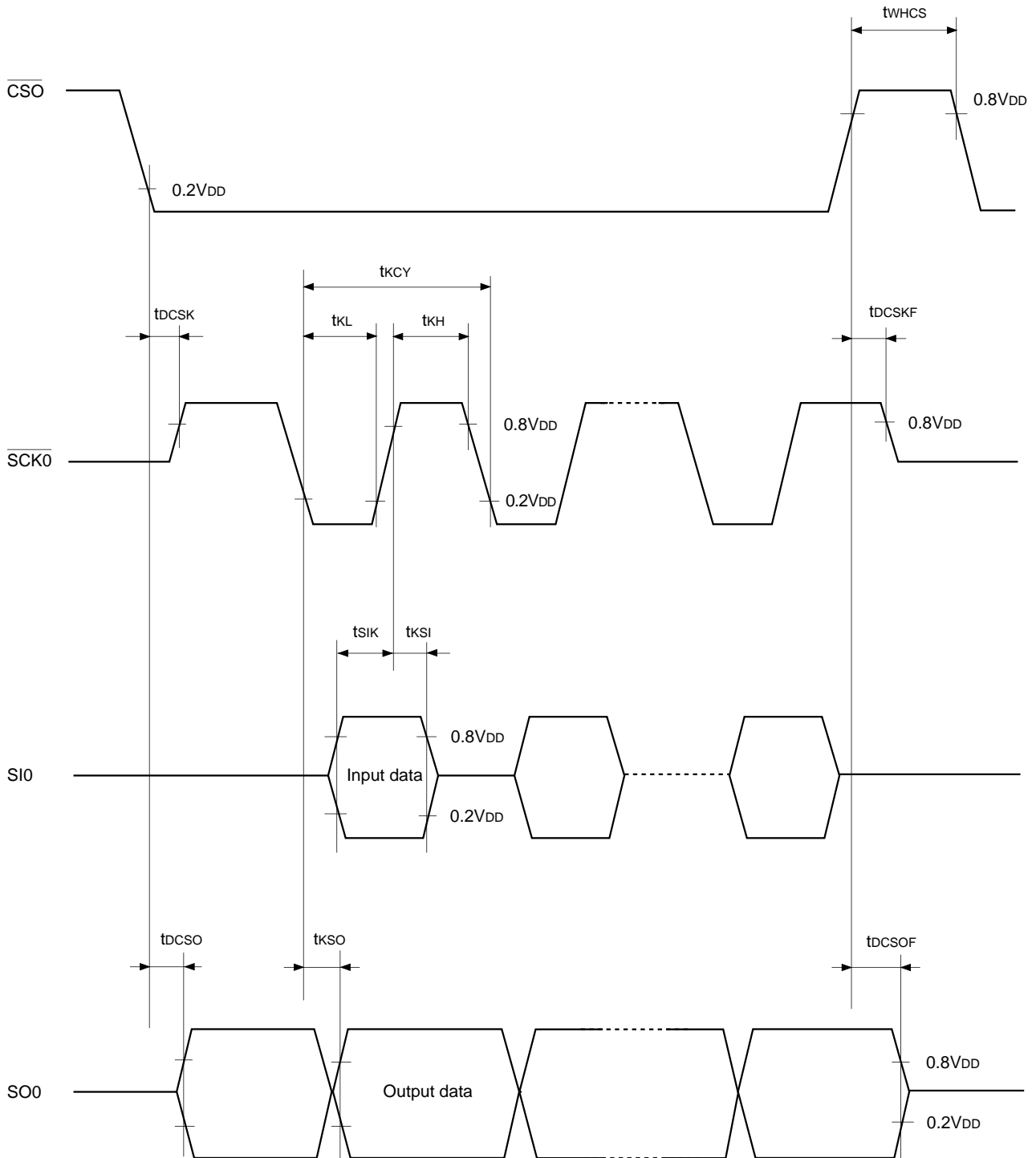| Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$1.5t_{SYS} + 200$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$1.5t_{SYS} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$1.5t_{SYS} + 200$	ns
$\overline{CS} \uparrow \rightarrow SO$ float delay time	t_{DCSOF}	SO0	Chip select transfer mode		$1.5t_{SYS} + 200$	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{SYS} + 200$		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{SYS} + 200$		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{SYS} + 100$		ns
			Output mode	8000/fc − 100		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	$-t_{SYS} + 100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	$2t_{SYS} + 100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		$2t_{SYS} + 200$	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{SYS} indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FE$_H$).

t_{SYS} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO correspond to each pin of $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0.

Note 3) The load condition for the $\overline{SCK}$ output mode, SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing (CH0)

Serial transfer (CH1) (SIO mode)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2t_{sys} + 200		ns
			Ouput mode	16000/fc		ns
$\overline{SCK1}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	t_{sys} + 100		ns
			Ouput mode	8000/fc − 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ ouput mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	t_{sys} + 200		ns
			$\overline{SCK1}$ ouput mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		t_{sys} + 200	ns
			$\overline{SCK1}$ ouput mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the control clock registor (address: 00FE$_H$).

t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing (SIO mode)
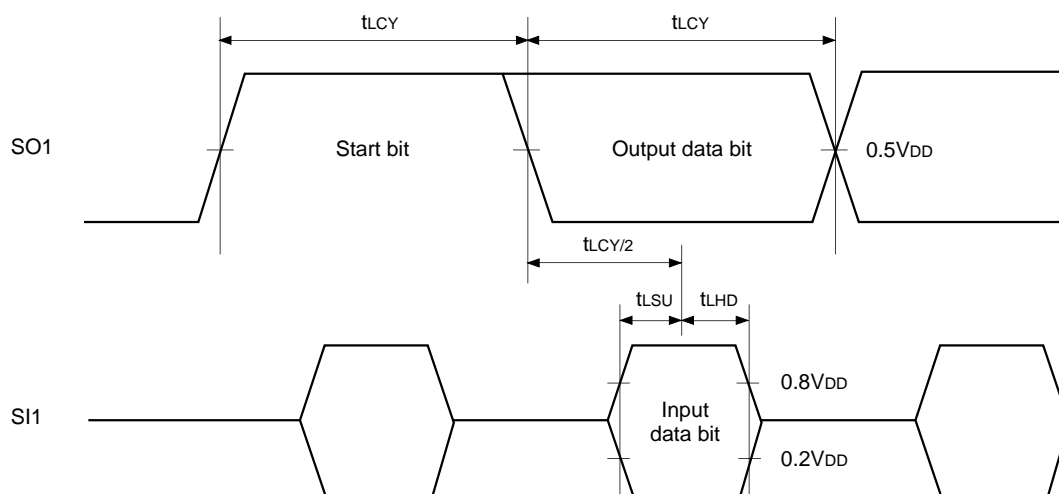
Serial transfer (CH1) (Special mode)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}*	SO1 SI1			104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

* t_{LCY} is specified only when the lower two bits (SO1 clock selected) of the serial mode register (CH1) (SIOM1: address 01E2$_H$) is set to 104μs.

Note) The load condition for SO1 is 50pF + 1TTL.
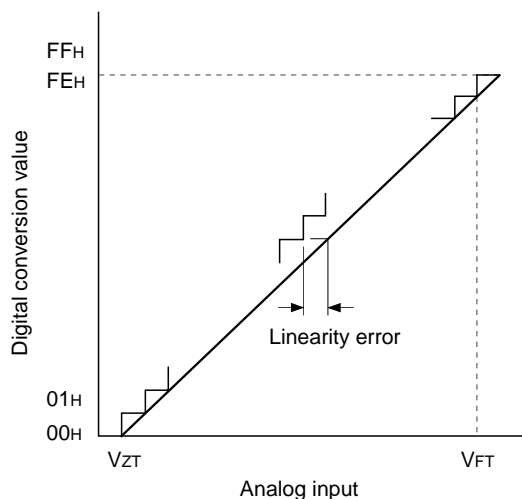
Fig. 6. Serial transfer CH1 timing (Special mode)

(3) A/D converter characteristics

(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V_{ZT}*1		Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V	−10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			μs
Sampling time	t_{SAMP}			12/f_{ADC}*3			μs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} − 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV$_{REF}$ current	I_{REF}	AV$_{REF}$	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 7. Definition of A/D converter terms

*1 V_{ZT}: Value at which the digital conversion value change from 00H to 01H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (address: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (address: 00FEH).

PCK1, PCK0 〳 CKS	0 (φ/2 selection)	1 (φ selection)
00 (φ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (φ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (φ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 8. Interruption input timing

INT0
INT1
INT2
INT3
$\overline{NMI}$
($\overline{NMI}$ specifies only the falling edge.)

Fig. 9. $\overline{RST}$ input timing

$\overline{RST}$

(5) I²C bus timing (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repetitive transfers	$t_{SU; STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD; DAT}$	SDA, SCL		0*		µs
Data setup time	$t_{SU; DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU; STO}$	SDA, SCL		4.7		µs

* The data hold time must exceed 300ns because the SCL rise time (300ns max.) is not taken into consideration.
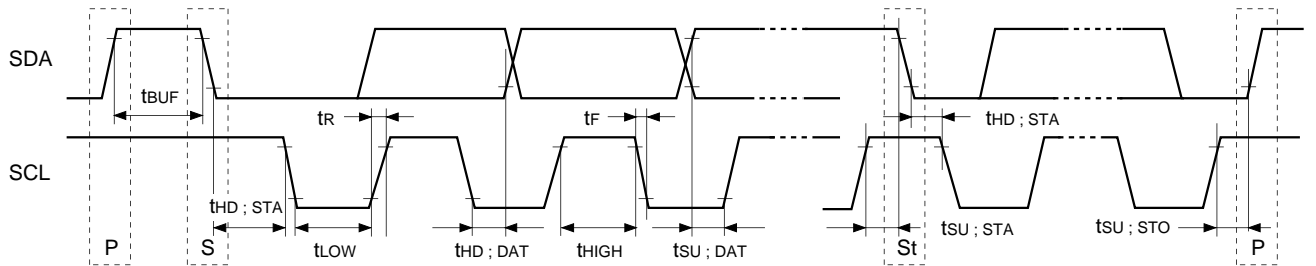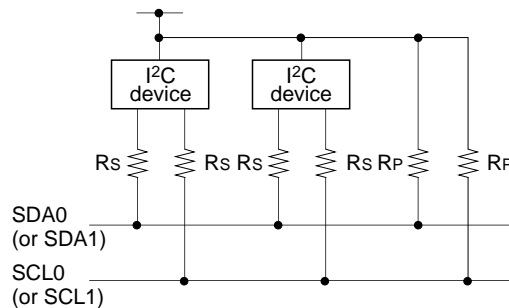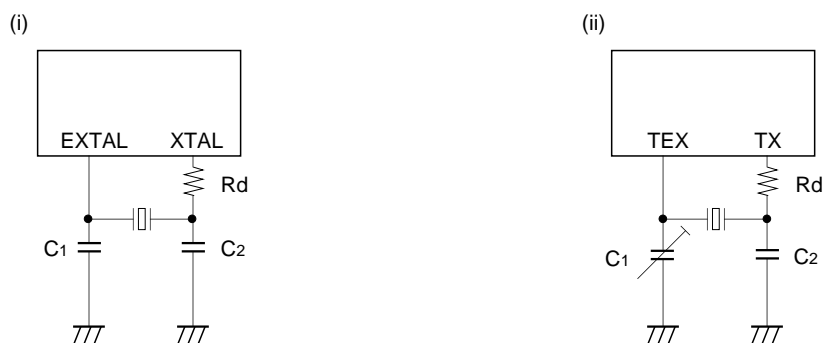
Fig.10. I²C bus transfer timing

Fig.11. Recommended circuit example for I²C device

• Pull-up resistors (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).

• Serial resistance (R_S = 300Ω or less) of SDA0 (or SDA1) and SCL0 (SCL1) reduces spike noise caused by CRT flash-over.

Appendix

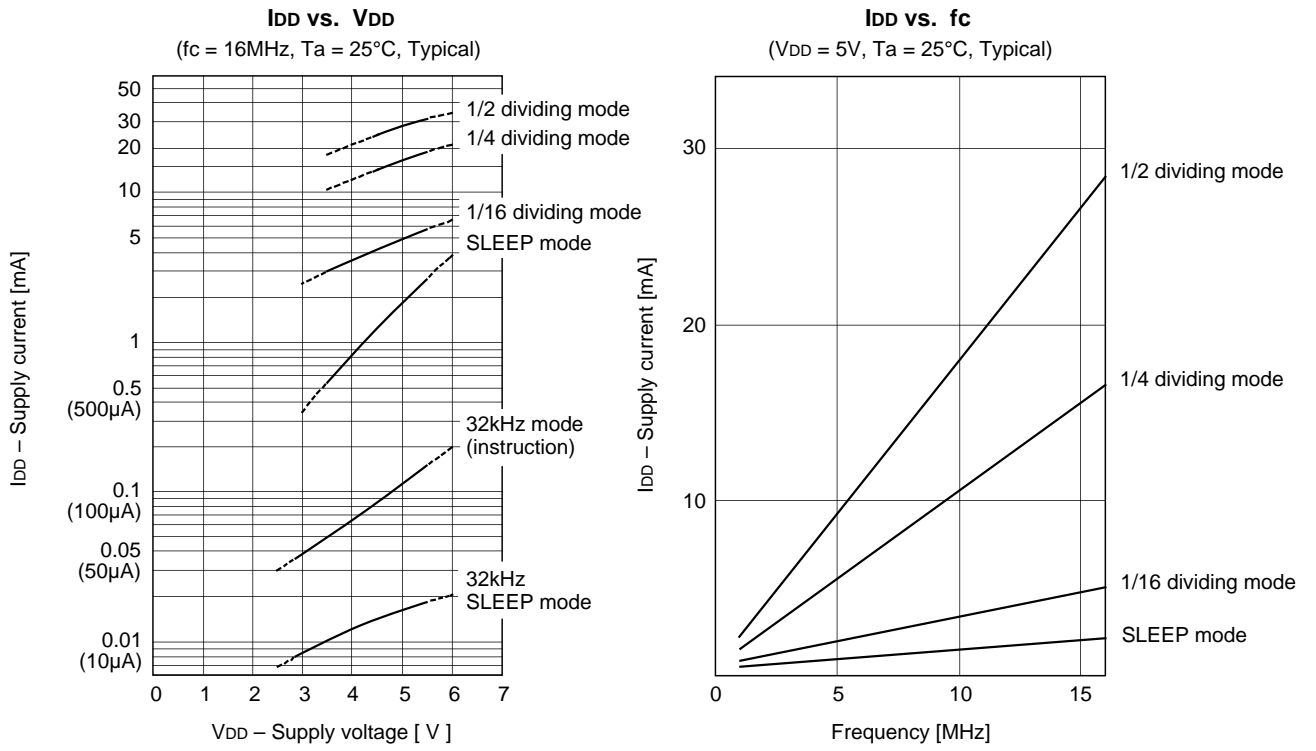**Fig. 12. Recommended oscillation circuit**

(i)   (ii)

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

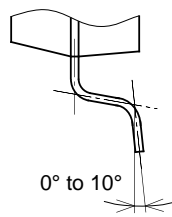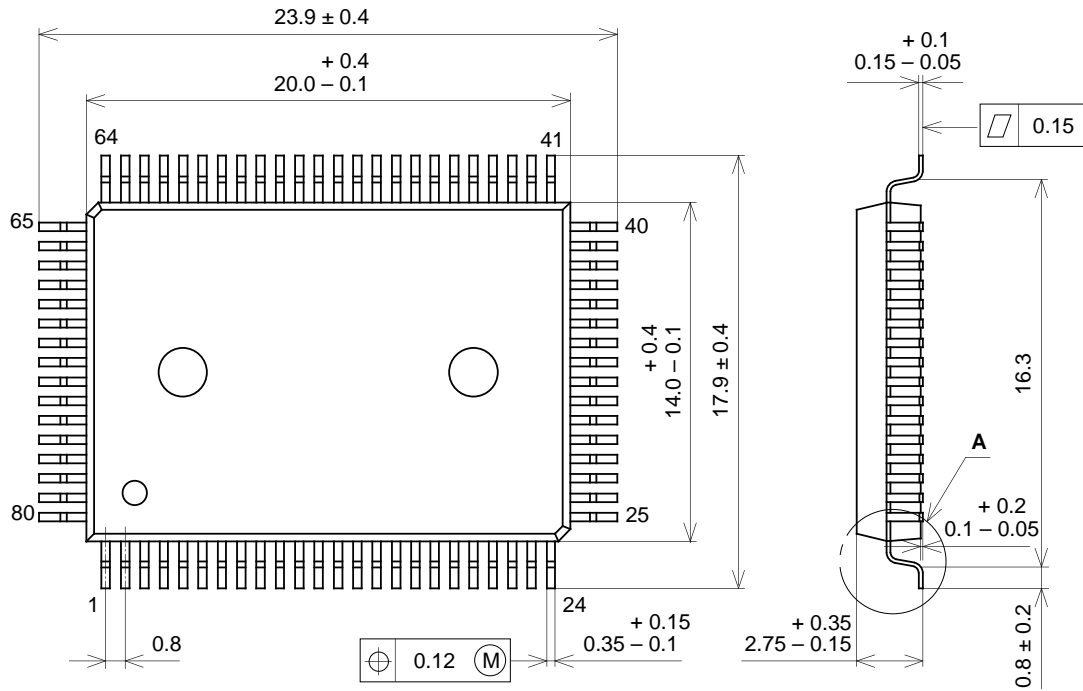**Mask Option Table**

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent
High voltage drive output port pull-down resistance	Non-existent	Existent (Selectable for each pin)

Characteristics Curve

I$_{DD}$ vs. V$_{DD}$
(fc = 16MHz, Ta = 25°C, Typical)

I$_{DD}$ – Supply current [mA]

50
30
20
10
5

1
0.5
(500μA)

0.1
(100μA)
0.05
(50μA)

0.01
(10μA)

1/2 dividing mode
1/4 dividing mode
1/16 dividing mode
SLEEP mode

32kHz mode
(instruction)

32kHz
SLEEP mode

0 1 2 3 4 5 6 7

V$_{DD}$ – Supply voltage [V]

I$_{DD}$ vs. fc
(V$_{DD}$ = 5V, Ta = 25°C, Typical)

I$_{DD}$ – Supply current [mA]

30

20

10

1/2 dividing mode

1/4 dividing mode

1/16 dividing mode

SLEEP mode

0 5 10 15

Frequency [MHz]

Package Outline   Unit: mm

80PIN QFP (PLASTIC)

DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g