

CMOS 8-bit Single Chip Microcomputer

Description

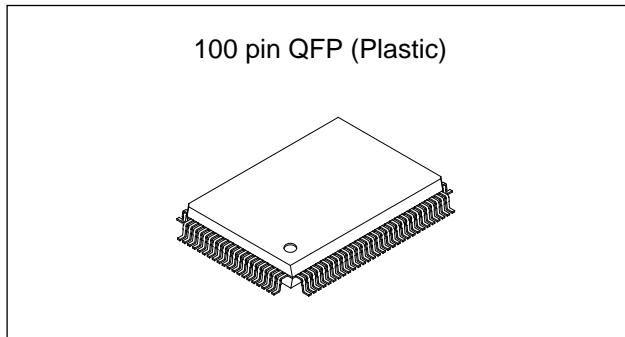
The CXP822P24 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer counter, fluorescent display tube controller/driver, remote control reception circuit, CTL duty detection circuit, 14-bit PWM output and high-speed output circuit besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP822P24 also provides sleep/stop function that enables lower power consumption.

CXP822P24 is the PROM-incorporated version of the CXP82224 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

Features

- Wide-range instruction system (213 instructions) to cover various types of data.
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
 122μs at 32kHz operation
- Incorporated PROM capacity 24K bytes
- Incorporated RAM capacity 704 bytes (including fluorescent display area)
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive approximation method
(Conversion time of 32μs/10MHz)
 - Serial interface SIO with 8-bit, 8-stage FIFO incorporated for data use
(Auto transfer for 1 to 8 bytes), 1 channel
 - Timer 8-bit standard SIO, 1 channel
 - Fluorescent display tube controller/driver 8-bit timer, 8-bit timer/counter, 19-bit time base timer
16-bit capture timer/counter, 32kHz timer/counter
 - Remote control reception circuit Maximum of 384 segment display possible
1 to 16-digit dynamic display
Dimmer function
High voltage drive output (40V)
 - PWM output circuit Incorporated pull-down resistor
 - CTL duty detection circuit Hardware key scan function
 - High-speed output circuit Maximum of 16 × 8 key matrix compatible
Incorporated noise elimination circuit
- Interruption Incorporated 8-bit, 6-stage FIFO for measurement data
- Standby mode 14 bits, 1 channel
- Package Precision of 800ns at 10MHz, 4 outputs.
19 factors, 15 vectors, multi-interruption possible
Sleep/stop
100-pin plastic QFP

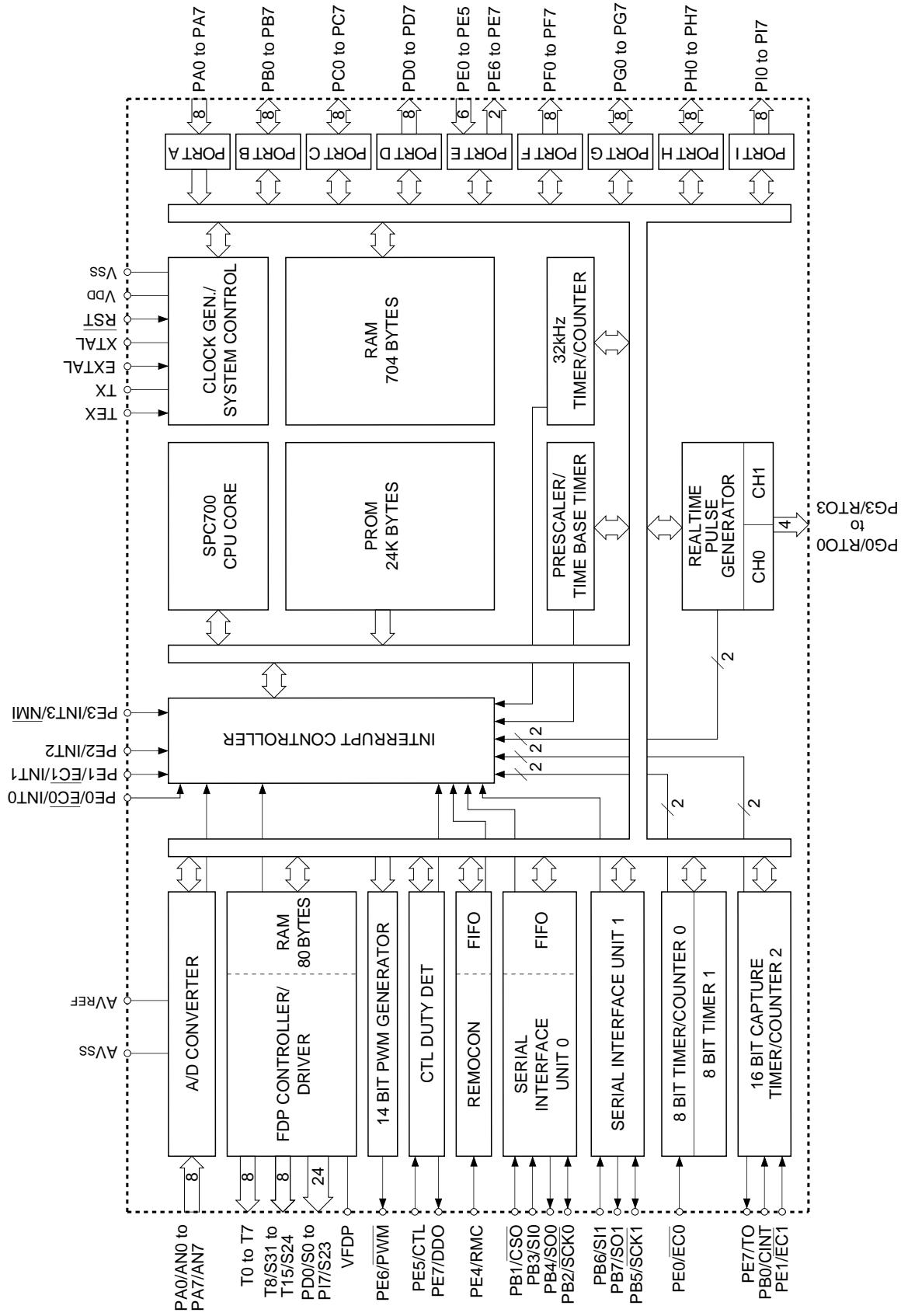


Structure

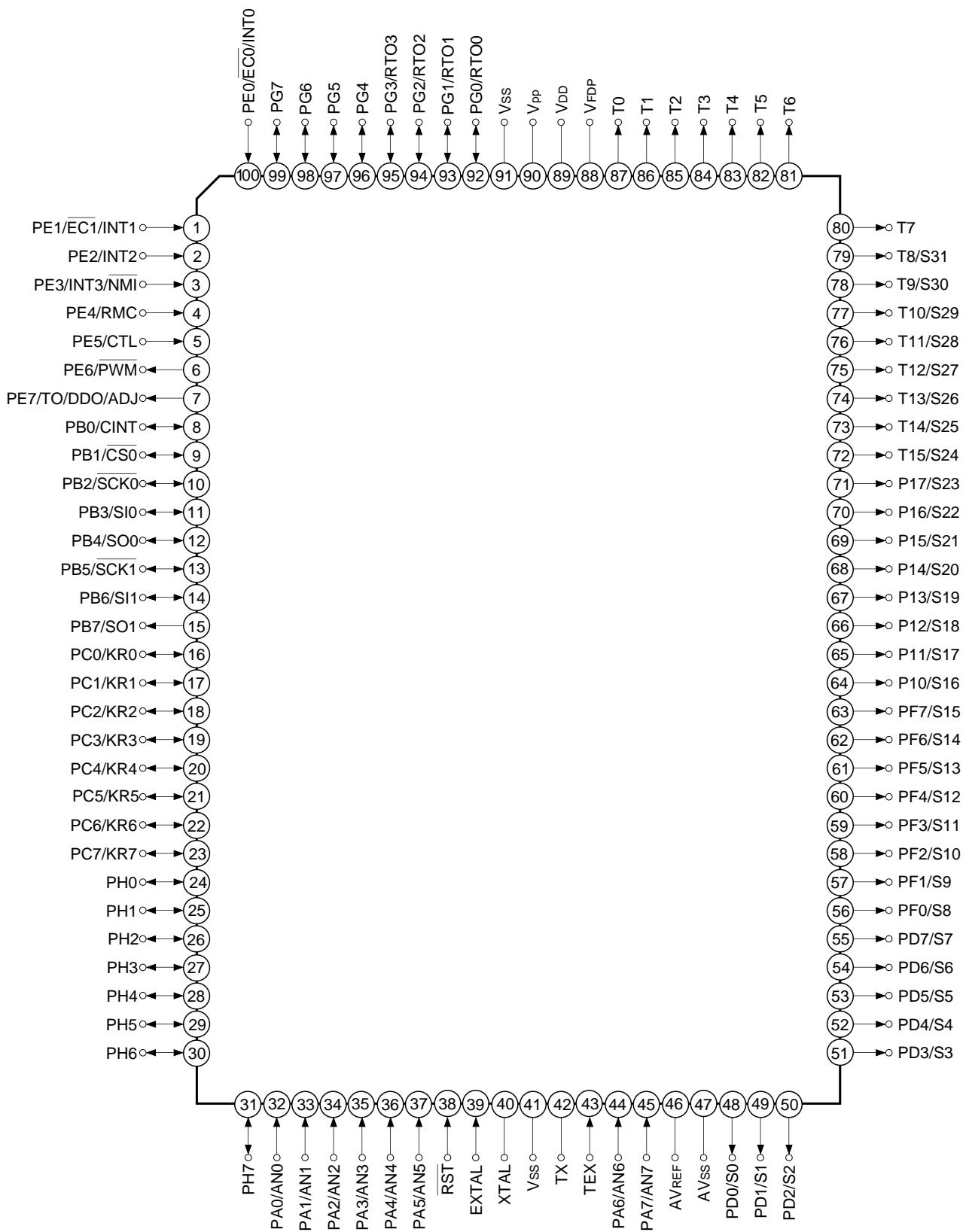
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



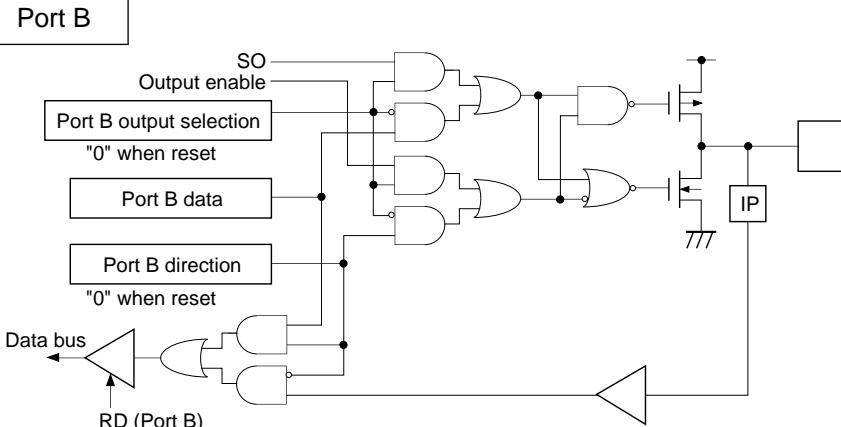
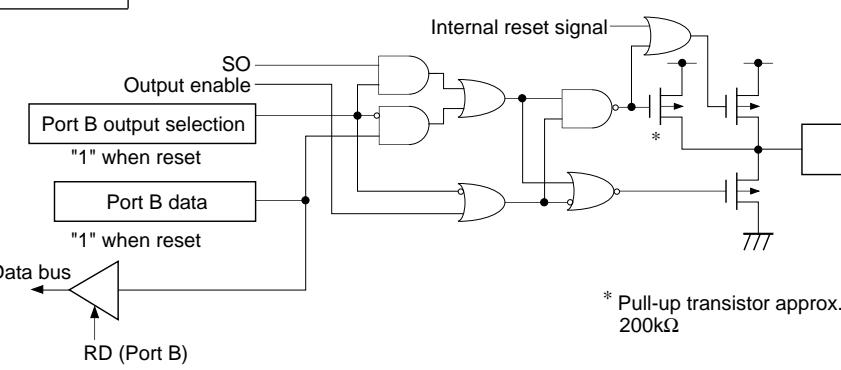
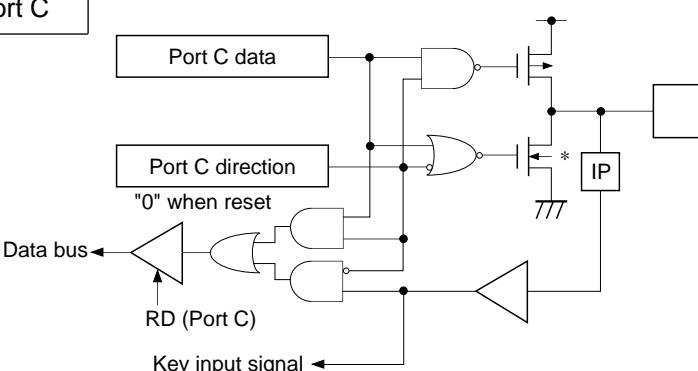
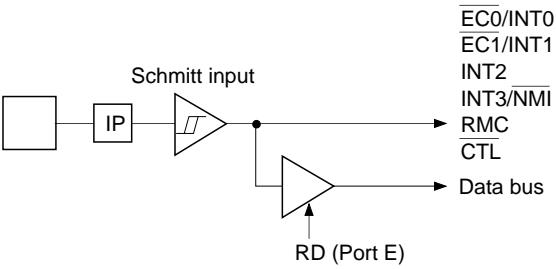
Pin Description

Symbol	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bit . (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O for lower 7bits can be set in a unit of single bits. Uppermost bit (PB7) is for output only. (8 pins)	Capture input to 16-bit timer/counter.	
PB1/CS0	I/O/Input		Chip select input for serial interface (CH0).	
PB2/SCK0	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/SCK1	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	Output/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current.	Serves as key return inputs when operating key scan with FDP segment signal.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PE0/INT0/EC0	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
PE1/INT1/EC1	Input/Input/Input			
PE2/INT2	Input/Input		Non-maskable interruption request input.	
PE3/INT3/NMI	Input/Input/Input			
PE4/RMC	Input/Input		Remote control reception circuit input.	
PE5/CTL	Input/Input		Input for CTL duty direction circuit.	
PE6/PWM	Output/Output		14-bit PWM output.	
PE7/TO/DDO/ ADJ	Output/Output/ Output/Output		Output for the 16-bit timer/counter rectangular waves, CTU duty detection, and 32kHz oscillation frequency demultiplication.	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PG0/PTO0 to PG3/RTO3	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Data for the lower 4 bits are gated with the contents of RTO or OR-gate output. (8 pins)	Outputs for real-time pulse generator (RTG). Functions as high-precision, real-time pulse output port. (4 pins)	
PG4 to PG7	I/O			

Symbol	I/O	Functions	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PI0/S16 to PI7/S23	Output/Output	(Port I) 8-bit output ports. (8 bits)	FDP segment signal outputs.
T8/S31 to T15/S24	Output/Output	Outputs for FDP timing (digit) signals/segment signals.	
T0 to T7	Output	FDP timing signal outputs.	
V _{FDP}		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
RST	Input	Low-level active, system reset.	
A _{VREF}	Input	Reference voltage input for A/D converter.	
A _{Vss}		A/D converter GND.	
V _{DD}		Vcc supply.	
V _{pp}		Vcc supply for incorporated PROM writing. Connect to V _{DD} during normal operation.	
V _{ss}		GND.	

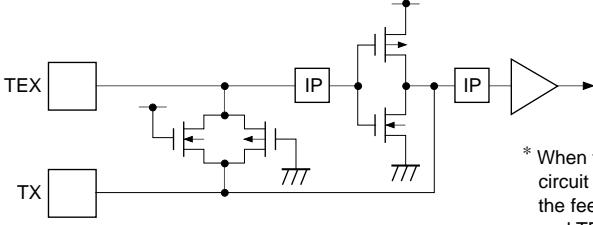
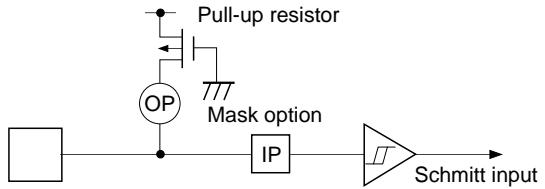
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	<p>Port A</p>	Hi-Z
PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1 4 pins	<p>Port B</p>	Hi-Z
PB2/SCK0 PB5/SCK1 2 pins	<p>Port B</p>	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	 <p>Port B</p> <p>SO Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p>	Hi-Z
PB7/SO1 1 pin	 <p>Port B</p> <p>SO Output enable</p> <p>Port B output selection "1" when reset</p> <p>Port B data "1" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Internal reset signal</p> <p>* Pull-up transistor approx. 200kΩ</p>	High level
PC0/KR0 to PC7/KR7 8 pins	 <p>Port C</p> <p>Port C data</p> <p>Port C direction "0" when reset</p> <p>Data bus</p> <p>RD (Port C)</p> <p>Key input signal</p> <p>* High current drive of 12mA possible</p>	Hi-Z
PE0/ <u>EC0</u> /INT0 PE1/ <u>EC1</u> /INT1 PE2/INT2 PE3/INT3/ <u>NMI</u> PE4/RMC PE5/CTL 6 pins	 <p>Port E</p> <p>Schmitt input</p> <p>EC0/INT0 <u>EC1</u>/INT1 INT2 INT3/NMI RMC CTL</p> <p>Data bus</p> <p>RD (Port E)</p>	Hi-Z

Pin	Circuit format	When reset
PE6/PWM 1 pin	<p>Port E</p> <p>PE6/PWM</p> <p>Port E output selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>PWM</p> <p>74HC14</p>	High level
PE7/TO/ DDO/ADJ 1 pin	<p>Port E</p> <p>PE7/TO/ DDO/ADJ</p> <p>Output enable</p> <p>TO → 0 DDO → 1 ADJ16K* → 2 ADJ2K* → 3</p> <p>MPX</p> <p>Port E output selection "00" when reset</p> <p>Port E output selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>74HC14</p> <p>74HC04</p> <p>* ADJ signal is a frequency demultiplication output for 32kHz oscillation frequency adjustment. ADJ2 can be used for buzzer output.</p>	High level
PG0/RTO0 to PG3/RTO3 4 pins	<p>Port G</p> <p>PG0/RTO0 to PG3/RTO3</p> <p>RTO data "0" when reset</p> <p>Port G data</p> <p>Port G direction "0" when reset</p> <p>Data bus</p> <p>RD (Port G)</p> <p>74HC14</p> <p>74HC04</p> <p>IP</p>	Hi-Z

Pin	Circuit format	When reset
PG4 to PG7 PH0 to PH7 12 pins	<p>Port G Port H</p> <p>Port G or Port H data</p> <p>Port G or Port H direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port G or Port H)</p> <p>IP</p>	Hi-Z
PD0/S0 to PD7/S7 PF0/S8 to PF7/S15 PI0/S16 to PI7/S23 24 pins	<p>Port D Port F Port I</p> <p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>Port D, F, or I data</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port D, F, or I)</p> <p>* High voltage drive transistor</p> <p>Pull-down resistor</p> <p>OP</p> <p>Mask option</p> <p>V_{FDP}</p>	Hi-Z or Low level (when PD resistance is added)
T15/S24 to T8/S31 T0 to T7 16 pins	<p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>* High voltage drive transistor</p> <p>Pull-down resistor</p> <p>OP</p> <p>Mask option</p> <p>V_{FDP}</p>	Hi-Z or Low level (when PD resistance is added)
EXTAL XTAL 2 pins	<p>EXTAL</p> <p>XTAL</p> <p>* Diagram shows circuit composition during oscillation.</p> <p>* Feedback resistor is removed during stop.</p>	Oscillation

Pin	Circuit format	When reset
TEX TX 2 pins	 <p>The diagram illustrates the internal circuitry for the TEX and TX pins. It features two square input boxes labeled 'TEX' and 'TX'. These inputs feed into a complex logic network consisting of several inverter symbols (IP) and a central multi-input AND-like gate. The output of this network is connected to a final inverter stage, which is followed by an open arrowhead indicating the signal path.</p> <p>* Diagram shows circuit composition during oscillation. * When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.</p>	Oscillation
$\overline{\text{RST}}$ 1 pin	 <p>The diagram shows the internal circuit for the $\overline{\text{RST}}$ pin. It consists of a single square input box. The signal passes through a 'Pull-up resistor' (represented by a vertical line with a dot at the top) and then enters an operational amplifier (op-amp) symbol labeled 'OP'. The output of the op-amp is connected to an 'IP' inverter stage. Finally, the signal is processed by a Schmitt input stage, indicated by a triangle with a hysteresis loop symbol.</p>	Low level

Absolute Maximum Ratings(V_{ss} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	V _{pp}	−0.3 to +13.0	V	Incorporated PROM
	V _{ss}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ¹	V	
Display output voltage	V _{OD}	V _{DD} − 40 to V _{DD} + 0.3	V	As P channel transistor is open drain, V _{DD} is reference.
High level output current	I _{OH}	−5	mA	All pins excluding display outputs* ² (value per pin)
	I _{ODH1}	−15	mA	Display outputs S0 to S23 (value per pin)
	I _{ODH2}	−35	mA	Display outputs T0 to T7, and T8/S31 to T15/S24 (value per pin)
High level total output current	ΣI _{OH}	−40	mA	Total for all pins excluding display outputs
	ΣI _{ODH}	−100	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	Port 1
	I _{OLC}	20	mA	High current Port 1 * ³
Low level total output current	ΣI _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	−10 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.*² Specifies output current of general-purpose I/O ports.*³ The high current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode Guaranteed operation range
		3.5	5.5		Low-speed mode Guaranteed operation range
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	V _{PP}	V _{PP} = V _{DD}		V	*4
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} – 0.4	V _{DD} + 0.3	V	EXTAL*3
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*2
	V _{ILEX}	-0.3	0.4	V	EXTAL*3
Operating temperature	T _{OPR}	-10	+75	°C	

*1 Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PG, PH).

*2 Value of the following pins: $\overline{\text{RST}}$, CINT, $\overline{\text{CS0}}$, SCK0, SCK1, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, INT2, INT3/ $\overline{\text{MT1}}$, RMC, CTL.

*3 Specifies only during external clock input.

*4 V_{PP} and V_{DD} should be set to the same voltage.

Electrical Characteristics**DC Characteristics**

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA, PB, PC, PE6, PE7, PG, PH	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}	PC	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	µA
	I _{IIE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	µA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	µA
	I _{ILT}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.1		-10	µA
	I _{ILR}	RST		-1.5		-400	µA
Display output current	I _{OH}	S0 to S23	V _{DD} = 4.5V, V _{OH} = V _{DD} - 2.5V	-8			mA
		S24/T15 to S31/T8 T0 to T7		-20			mA
Open drain output leakage current (P-CH Tr in off state)	I _{OL}	S24/T15 to S31/T8 T0 to T7	V _{DD} = 5.5V V _{OL} = V _{DD} - 35V V _{FDP} = V _{DD} - 35V			-20	µA
Pull-down resistance	R _L	S24/T15 to S31/T8 T0 to T7	V _{DD} = 5V V _{FDP} = V _{DD} - 35V	60	100	270	kΩ
I/O leakage current	I _{Iz}	PA to PC, PE, PG, PH	V _{DD} = 5.5V V _I = 0, 5.5V			±10	µA
Power supply current*	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency demultiplier clock) V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		20	40	mA
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		400	1000	µA
	I _{DDS1}		Sleep mode V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.2	8	mA
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	µA
	I _{DDS3}		Stop mode V _{DD} = 5.5V, Termination of 10MHz and 32kHz crystal oscillation			30	µA
Input capacity	C _{IN}	Pins other than S0 to S31, T0 to T7, PB7, PE6, AV _{REF} , AV _{SS} , V _{FDP} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

* When all pins are open.

AC Characteristics**(1) Clock timing**

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t _{CR} t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} t _{EL}	EC0, EC1	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	t _{ER} t _{EF}	EC0, EC1	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input pulse width	t _{TL} t _{TH}	TEX	Fig. 3	10			μs
Event count input rise time, fall time	t _{TR} t _{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

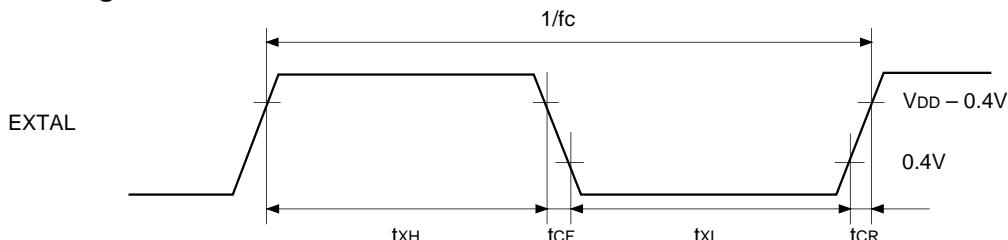
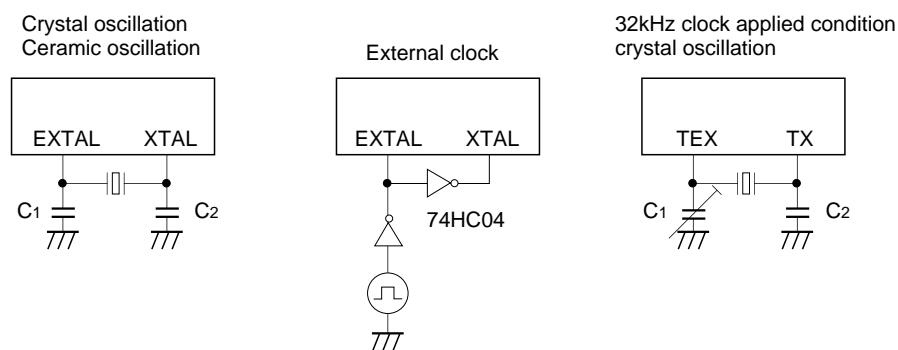
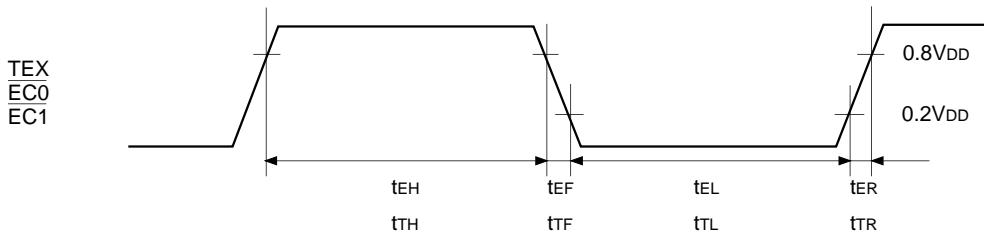
Fig. 1. Clock timing**Fig. 2. Clock applied conditions**

Fig. 3. Event count clock timing**(2) Serial transfer (CH0)**

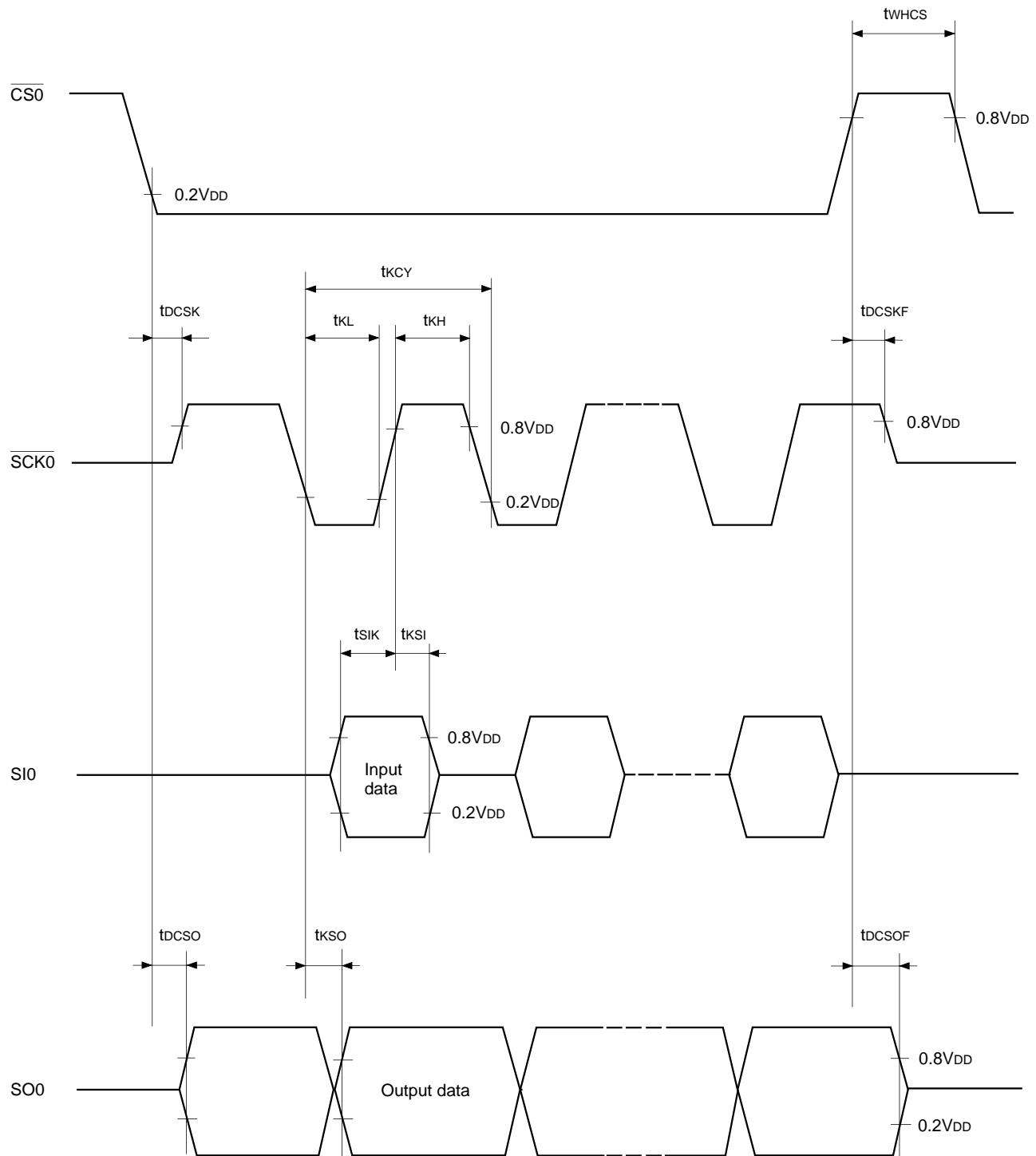
(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss=0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 input set-up time (for $SCK0 \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $SCK0 \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	$t_{sys} + 200$		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		$t_{sys} + 200$	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

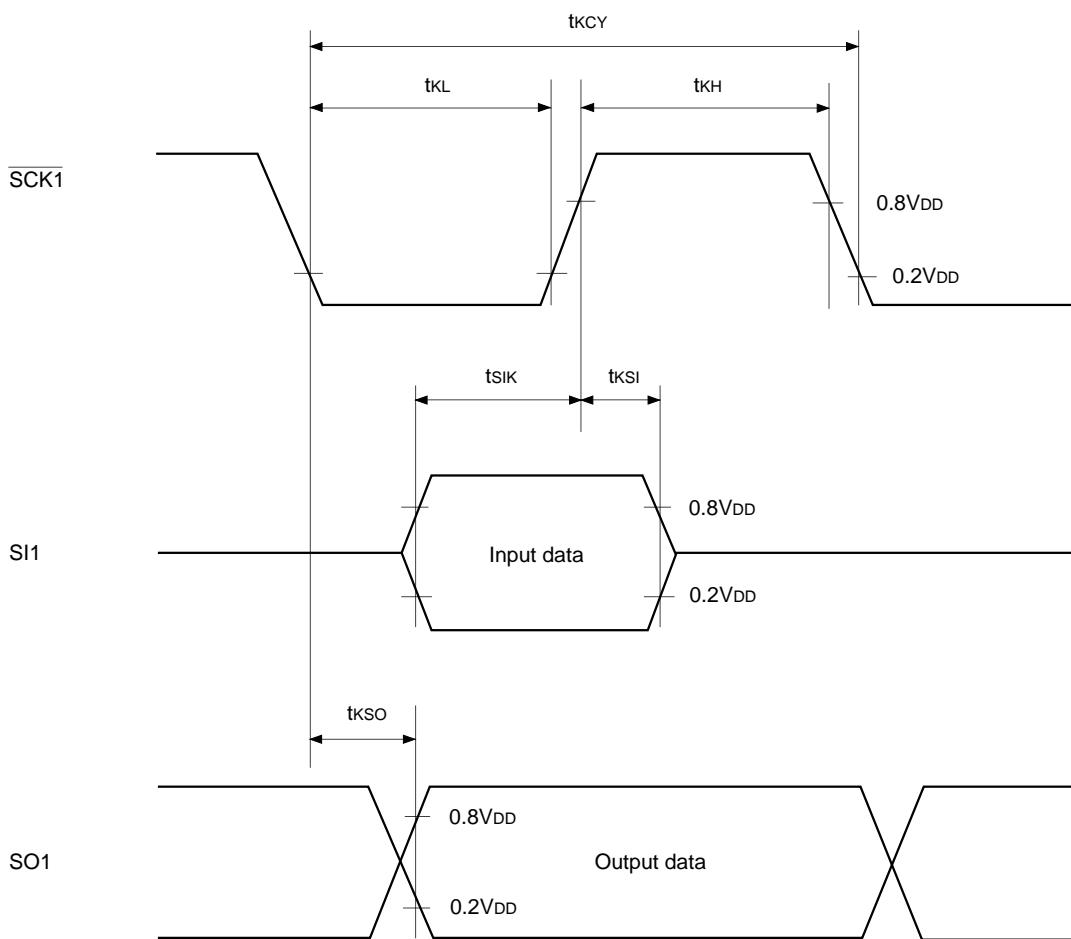
Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCK1 cycle time	t _{KCY}	SCK1	Input mode	1000		ns
			Output mode	16000/fc		ns
SCK1 High, Low level width	t _{KL} t _{KH}	SCK1	Input mode	400		ns
			Output mode	8000/fc - 50		ns
SI1 input set-up time (for SCK1 ↑)	t _{SIK}	SI1	SCK1 input mode	100		ns
			SCK1 output mode	200		ns
SI1 input hold time (for SCK1 ↑)	t _{KSI}	SI1	SCK1 input mode	200		ns
			SCK1 output mode	100		ns
SCK1 ↓ → SO1 delay time	t _{KSO}	SO1	SCK1 input mode		200	ns
			SCK1 output mode		100	ns

Note) The load condition for the SCK1 output mode, SO1 output delay time is 50pF + 1TTL.

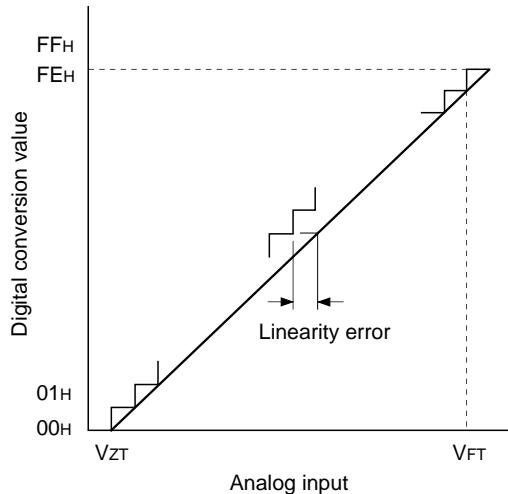
Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V _{ZT} *1		Ta = 25°C V _{DD} = AV _{DD} = 5.0V V _{DD} = AV _{SS} = 0V	-10	70	150	mV
Full-scale transition voltage	V _{FT} *2			4930	5050	5120	mV
Conversion time	t _{CONV}			160/f _{ADC} *3			μs
Sampling time	t _{SAMP}			12/f _{ADC} *3			μs
Reference input voltage	V _{REF}	AV _{REF}		V _{DD} - 0.5		V _{DD}	V
Analog input voltage	V _{IAN}	AN0 to AN7		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode		0.6	1.0	mA
	I _{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA

Fig. 6. Definitions of A/D converter terms



*1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to ADC operation clock selection (ADCS: Bit 6 of address 00F9H).

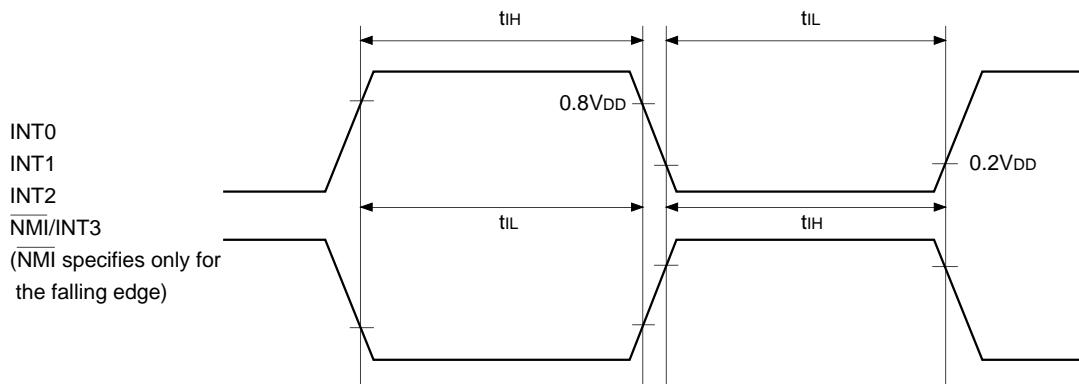
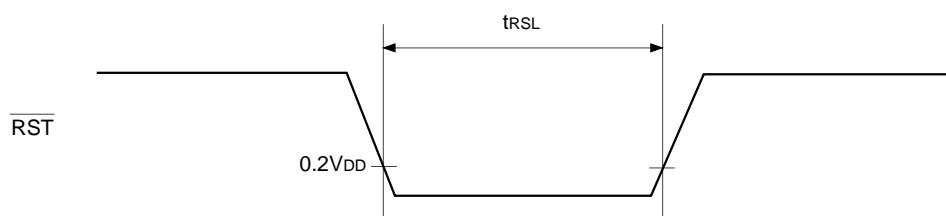
During PS2 selection, f_{ADC} = fc/2

During PS1 selection, f_{ADC} = fc

(4) Interruption, reset input (Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t _{IH} t _{IL}	INT0 INT1 INT2 NMI/INT3		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		8/fc		μs

Fig. 7. Interruption input timing

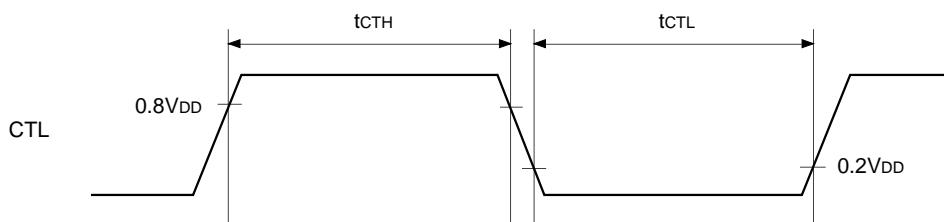
Fig. 8. $\overline{\text{RST}}$ input timing

(5) Others

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.0V, V_{SS} = 0V reference)

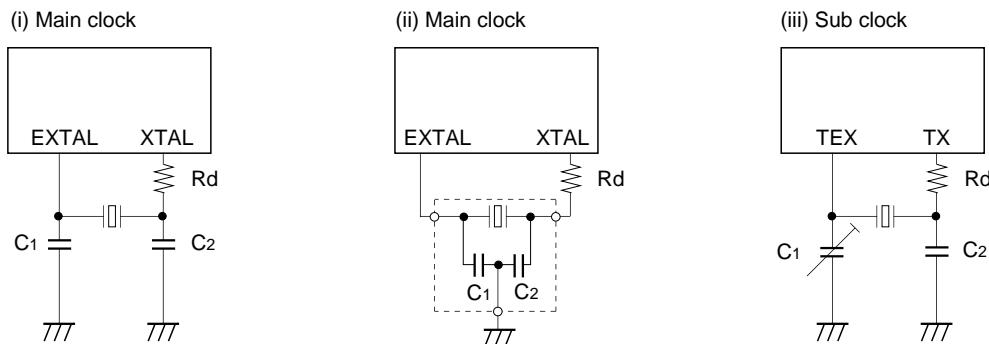
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CLK input High, Low level width	t _{CTH} t _{CTL}	CTL	t _{sys} = 2000/fc	t _{sys} + 200		ns

Fig. 9. Other timing



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				
	CST8.00MTW*	8.00				(ii)
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	15	15	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	(i)
		8.00				
		10.00				
	P3	32.768kHz	30	39	330k	(iii)

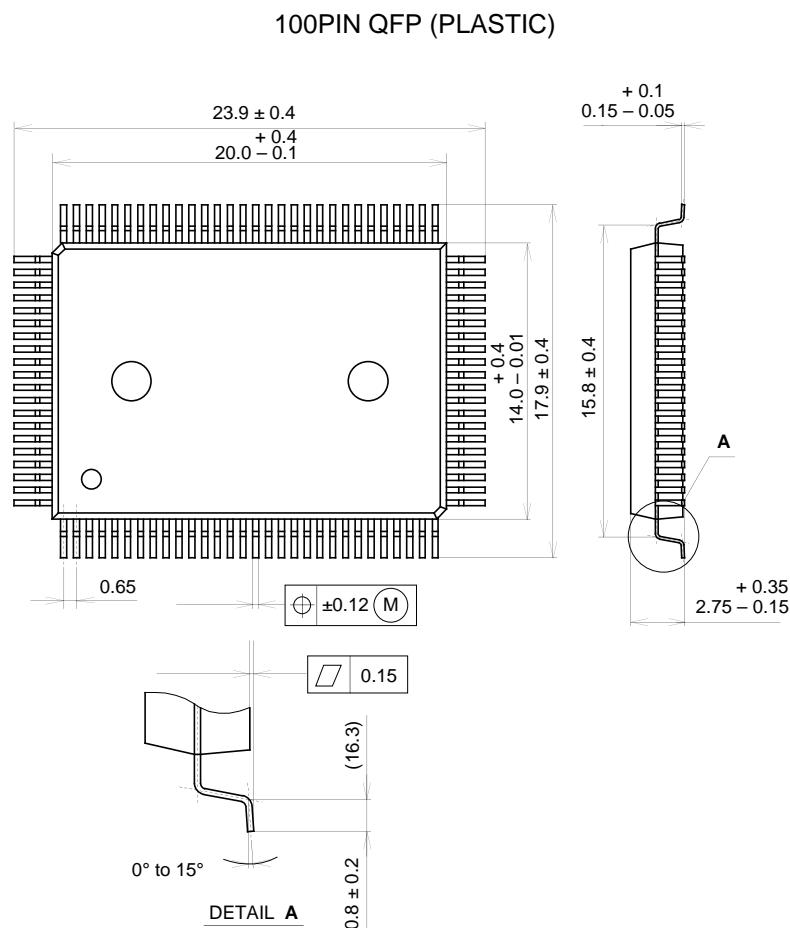
Those marked with an asterisk (*) signify types with built-in ground capacitance (C₁, C₂).

Selection Guide

Optional item	Mask product	CXP822P24Q-1- □□□
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	20K bytes/24K bytes	PROM 24K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existant
High voltage drive pin pull-up resistor	Existent/Non-existent	Non existent (S0/PD0 to S23/PF7) Existent (T0 to T15/S24)

Package Outline

Unit: mm



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g