SONY

CXG1115ER

Dual-band Low Noise Amplifier/Mixer

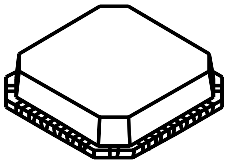
Description

The CXG1115ER is a dual-band (CDMA/GPS) low noise amplifier/mixer MMIC for the Japan CDMA cellular phones (J-CDMA). This IC is designed using the Sony's GaAs J-FET process.

Features

- High gain:
  - CDMA LNA High current mode Gp = 14.5dB (Typ.)
  - CDMA MIX Gc = 12dB (Typ.)
  - GPS LNA Gp = 18dB (Typ.)
  - GPS MIX Gc = 9.5dB (Typ.)
- Low noise figure:
  - CDMA LNA High current mode NF = 1.5dB (Typ.)
  - CDMA MIX NF = 4.5dB (Typ.)
  - GPS LNA NF = 1.7dB (Typ.)
  - GPS MIX NF = 5dB (Typ.)
- Low distortion
  - CDMA LNA High current mode Input IP3 = +3.5dBm (Typ.)
  - CDMA MIX Input IP3 = +2dBm (Typ.)
  - GPS LNA Input IP3 = –5.5dBm (Typ.)
  - GPS MIX Input IP3 = +2dBm (Typ.)
- Low noise amplifier with by-pass switch
- J-CDMA/GPS supported dual band
- Sharing the two-system LO signal source by the doubler system
- 24-pin VQFN small package

24 pin VQFN (Plastic)



Applications

J-CDMA

Structure

GaAs J-FET MMIC

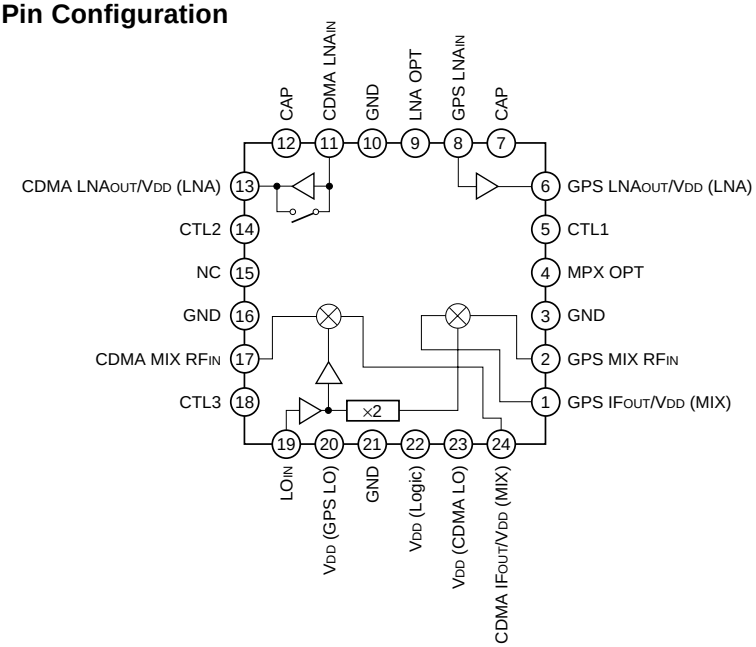
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+5	dBm
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.3	V

Block Diagram and Pin Configuration



GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E01851A26-PS

Electrical Characteristics

Conditions: V_{DD} = 2.7V, V_{CTL} (H) = 2.7V, V_{CTL} (L) = 0V, (Ta = 25°C)

Logic Block

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Control pin current	I_{CTL} (H)	—	35	50	µA	When no signal
Logic power current consumption	I_{DD}	—	0.3	0.6	mA	

CDMA-LNA Block Conditions: f_{RF} = 850MHz

Item	Control pin condition			Symbol	Min.	Typ.	Max.	Unit	Condition
	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$						
Current consumption	L	L	L	I_{DDSW}	—	0.1	0.3	mA	When no signal
	L	L	H	I_{DDM}	—	5	7		
	L	H	L	I_{DDL}	—	3.2	5		
	L	H	H	I_{DDH}	—	5.3	7.5		
Power gain	L	L	L	G_{PSW}	–4.3	–3.8	–3.3	dB	When a small signal
	L	L	H	G_{PM}	6	7	8		
	L	H	L	G_{PL}	12	13.5	15		
	L	H	H	G_{PH}	13	14.5	16		
	H	—	—	G_{POFF}	—	–13	–8		
Noise figure	L	L	H	NF_M	—	8	10	dB	
	L	H	L	NF_L	—	1.5	2		
	L	H	H	NF_H	—	1.5	2		
Input IP3	L	L	L	$IIP3_{SW}$	20	28	—	dBm	*1
	L	L	H	$IIP3_M$	6	8.5	—		
	L	H	L	$IIP3_L$	–1.5	1	—		
	L	H	H	$IIP3_H$	1.5	3.5	—		
Isolation	L	L	H	I_{SOM}	21	26	—	dB	When a small signal
	L	H	L	I_{SOL}	13	18	—		
	L	H	H	I_{SOH}	13	18	—		

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF} = 850MHz/850.9MHz, P_{RF} = 0dBm (G_{PSW} mode), P_{RF} = –20dBm (G_{PM} mode), P_{RF} = –25dBm (G_{PL}/G_{PH} mode).

CDMA-MIX Block Conditions: f_{RF} = 850MHz, $f_{LO} = f_{RF} - f_{IF}$, f_{IF} = 110MHz, P_{LO} = –10dBm

Item	Control pin condition			Symbol	Min.	Typ.	Max.	Unit	Condition
	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$						
Current consumption	L	—	—	I_{DD}	—	8	11	mA	When no signal
Conversion gain	L	—	—	G_C	10.5	12	13.5	dB	When a small signal
	H	—	—	G_{COFF}	—	–55	–45		
Noise figure	L	—	—	NF	—	4.5	6	dB	
Input IP3	L	—	—	IIP3	0	2	—	dBm	*2
LO – RF leak	L	—	—	P_{LK}	—	–23	–18	dBm	—

*2 Conversion from the IM3 suppression ratio for two-wave input: f_{RF} = 850MHz/850.9MHz, P_{RF} = –25dBm.

GPS-LNA Block Conditions: f_{RF} = 1575MHz

Item	Control pin condition			Symbol	Min.	Typ.	Max.	Unit	Condition
	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$						
Current consumption	H	—	—	I_{DD}	—	5.5	7.5	mA	When no signal
Conversion gain	H	—	—	G_P	16.5	18	19.5	dB	When a small signal
	L	—	—	G_{POFF}	—	–22	–17		
Noise figure	H	—	—	NF	—	1.7	2.2	dB	
Input IP3	H	—	—	IIP3	–8	–5.5	—	dBm	*3
Isolation	H	—	—	I_{SO}	23	28	—	dB	When a small signal

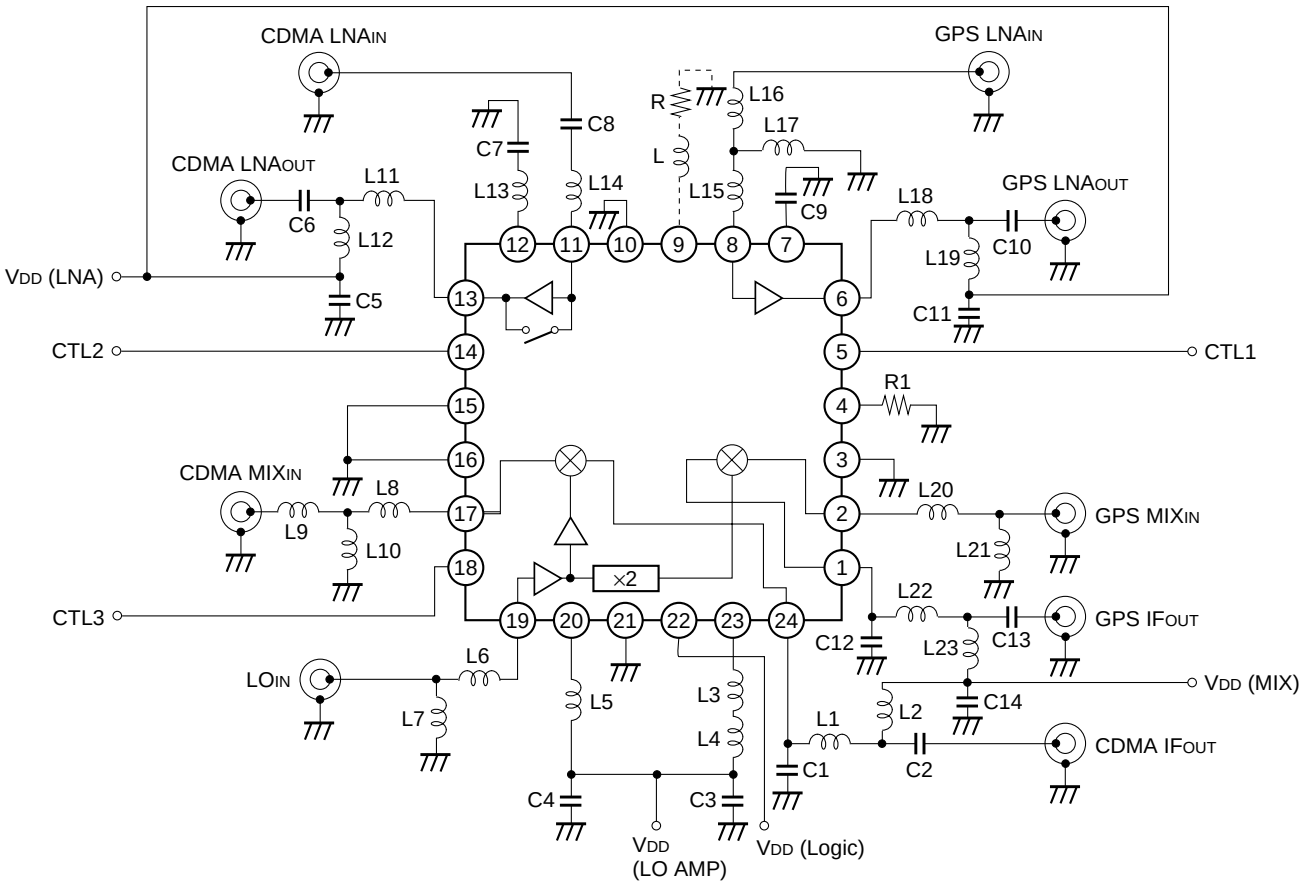
*3 Conversion from the IM3 suppression ratio for two-wave input: f_{RF} = 1574.5MHz/1575.5MHz, P_{RF} = –30dBm.

GPS-MIX Block Conditions: f_{RF} = 1575MHz, $f_{LO} = (f_{RF} - f_{IF})/2$, f_{IF} = 110MHz, P_{LO} = –10dBm

Item	Control pin condition			Symbol	Min.	Typ.	Max.	Unit	Condition
	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$						
Current consumption	H	—	—	I_{DD}	—	8	11	mA	When no signal
Conversion gain	H	—	—	G_C	8	9.5	11	dB	When a small signal
	L	—	—	G_{COFF}	—	–50	–40		
Noise figure	H	—	—	NF	—	5	6.5	dB	
Input IP3	H	—	—	IIP3	–1.5	2	—	dBm	*4
LO – RF leak	H	—	—	P_{LK}	—	–15	–10	dBm	@f_{LO} = $f_{RF} - f_{IF}$

*4 Conversion from the IM3 suppression ratio for two-wave input: f_{RF} = 1574.5MHz/1575.5MHz, P_{RF} = –25dBm.

Recommended Evaluation Circuit



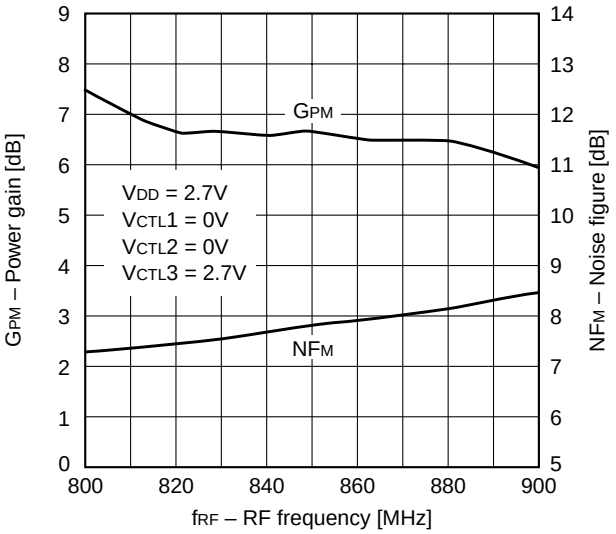
L1	220nH	L16	3.3nH	C8	100pF
L2	220nH	L17	8.2nH	C9	18pF
L3	27nH	L18	6.8nH	C10	100pF
L4	5.6nH	L19	3.9nH	C11	1000pF
L5	6.8nH	L20	10nH	C12	8pF
L6	33mH	L21	2.7nH	C13	1000pF
L7	12nH	L22	220nH	C14	1000pF
L8	27nH	L23	220nH	R1	100Ω
L9	18nH	C1	8pF	L*1	33nH
L10	22nH	C2	1000pF	R*1	—
L11	22nH	C3	1000pF		
L12	27nH	C4	100pF		
L13	2.2nH	C5	100pF		
L14	22nH	C6	1000pF		
L15	5.6nH	C7	1000pF		

*1 L and R of Pin 9 are used when the optional resistor is added in the low noise amplifier block.

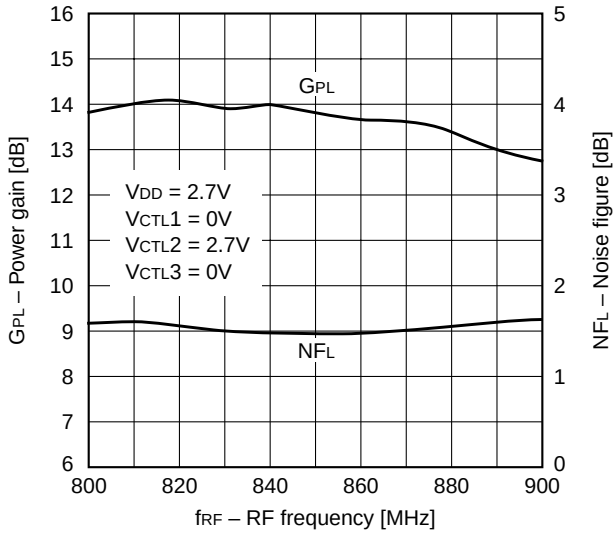
Example of Representative Characteristics (Ta = 25°C)

Low Noise Amplifier Block

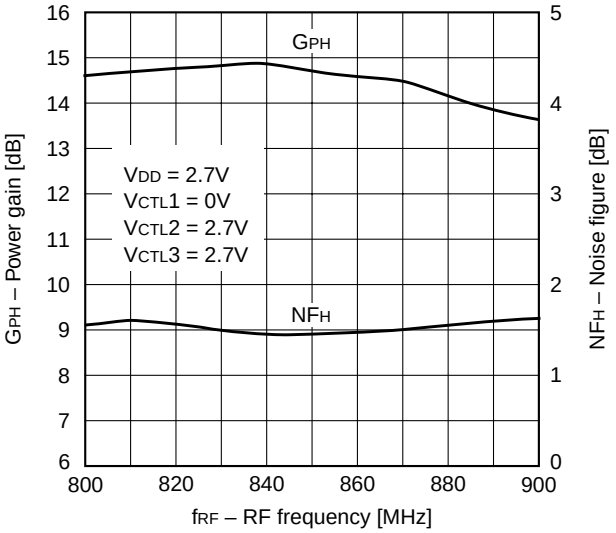
CDMA G_{PM}, NF_M vs. f_{RF}



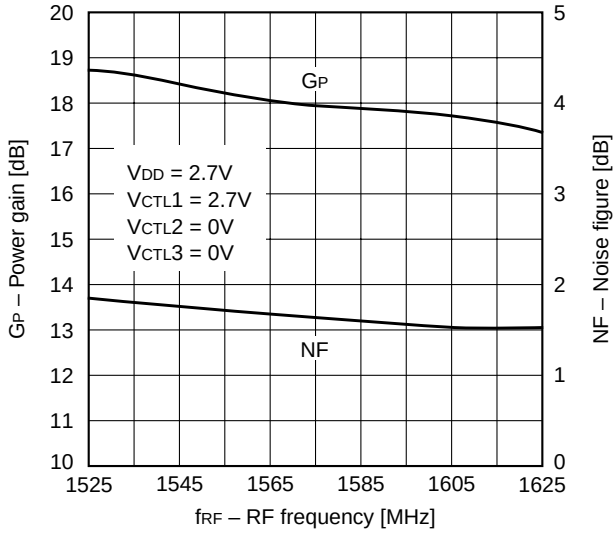
CDMA GPL, N_{FL} vs. f_{RF}



CDMA G_{PH}, NF_H vs. f_{RF}

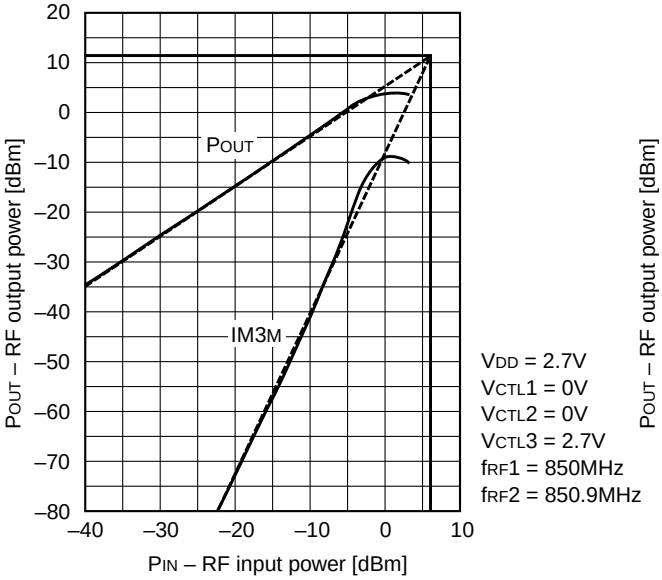


GPS G_P, NF vs. f_{RF}



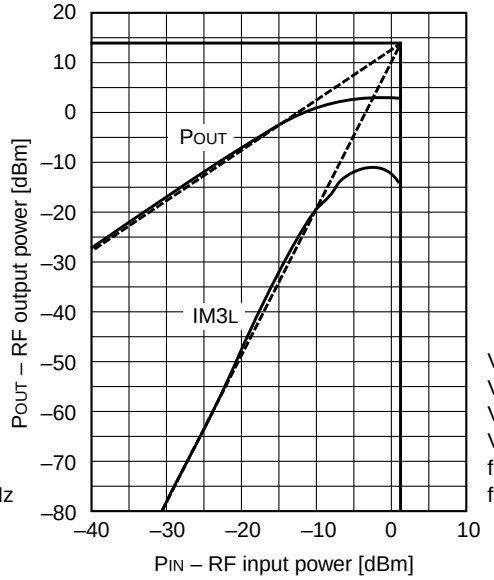
Low Noise Amplifier Block

CDMA POUT, IM3M vs. PIN



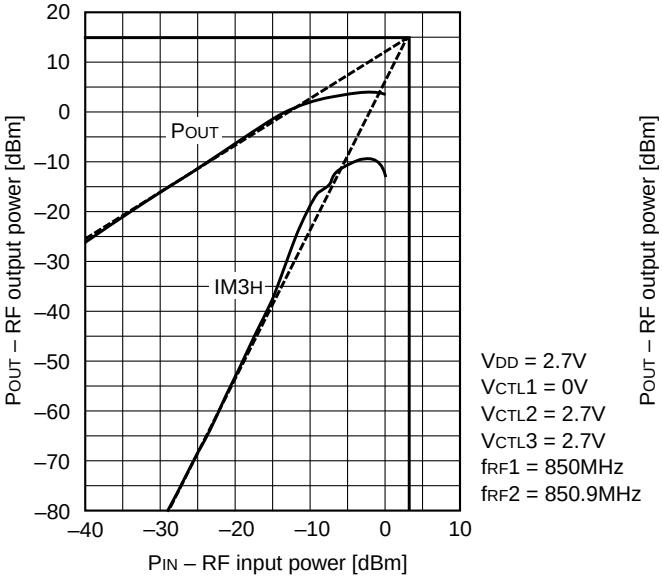
VDD = 2.7V
VCTL1 = 0V
VCTL2 = 0V
VCTL3 = 2.7V
fRF1 = 850MHz
fRF2 = 850.9MHz

CDMA POUT IM3L vs. PIN



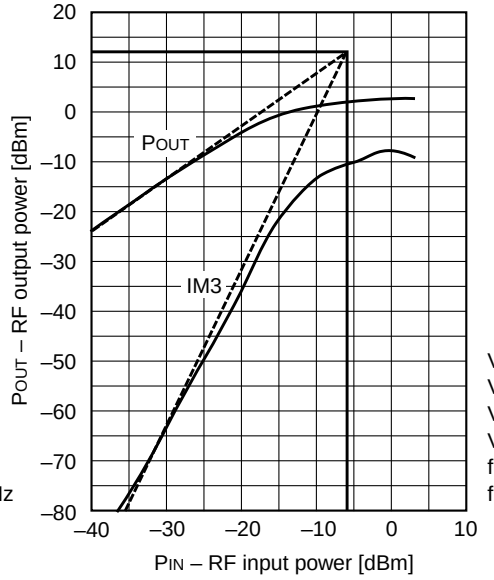
VDD = 2.7V
VCTL1 = 0V
VCTL2 = 2.7V
VCTL3 = 0V
fRF1 = 850MHz
fRF2 = 850.9MHz

CDMA POUT, IM3H vs. PIN



VDD = 2.7V
VCTL1 = 0V
VCTL2 = 2.7V
VCTL3 = 2.7V
fRF1 = 850MHz
fRF2 = 850.9MHz

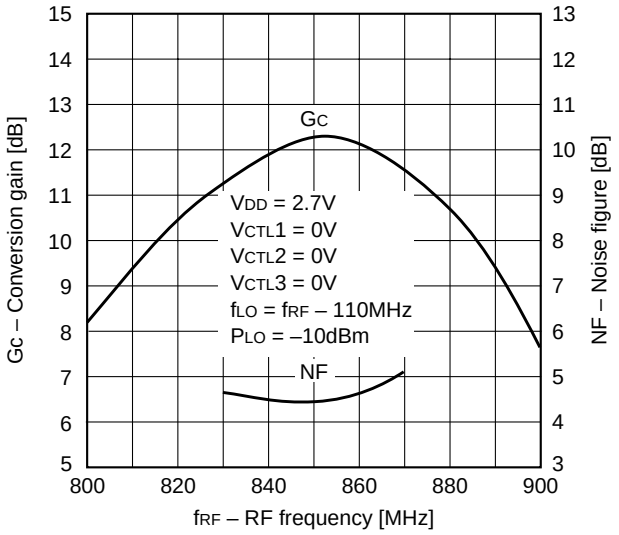
GPS POUT IM3 vs. PIN



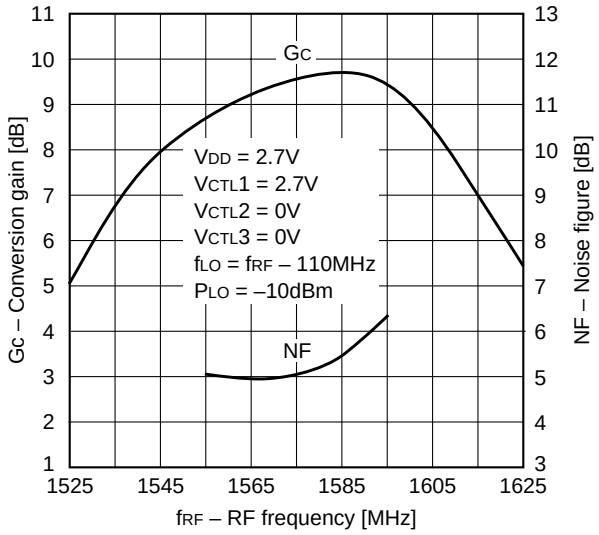
VDD = 2.7V
VCTL1 = 2.7V
VCTL2 = 0V
VCTL3 = 0V
fRF1 = 1574.5MHz
fRF2 = 1575.5MHz

Mixer Block

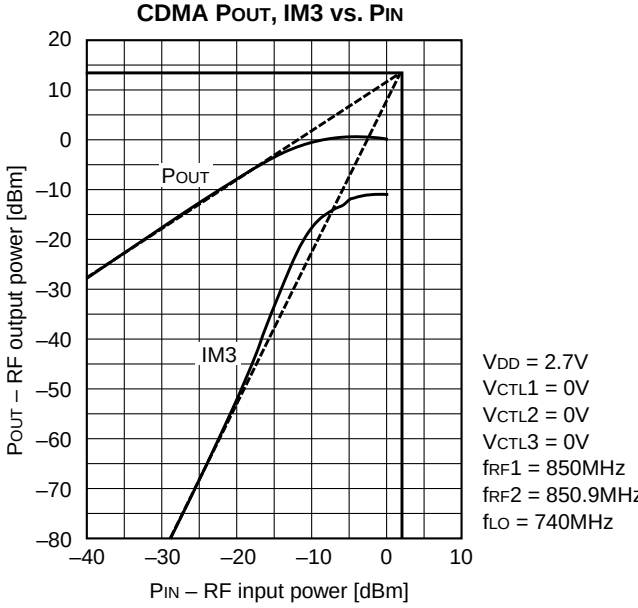
CDMA Gc, NF vs. f_{RF}



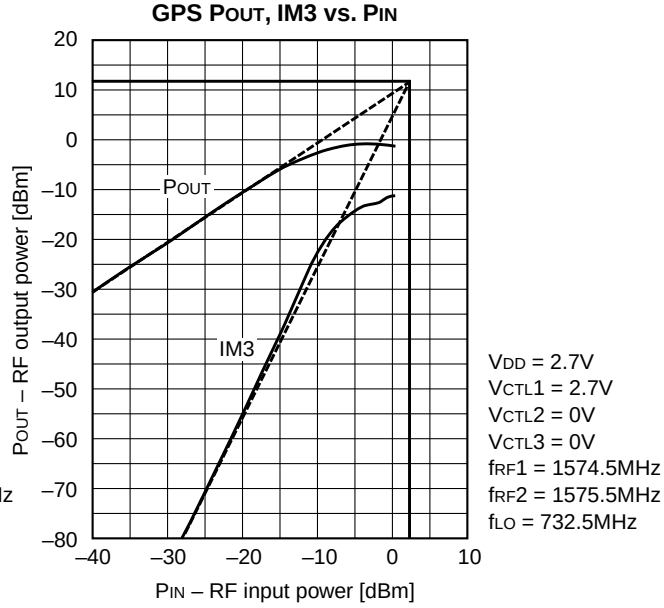
GPS Gc, NF vs. f_{RF}



CDMA P_{OUT}, IM3 vs. P_{IN}

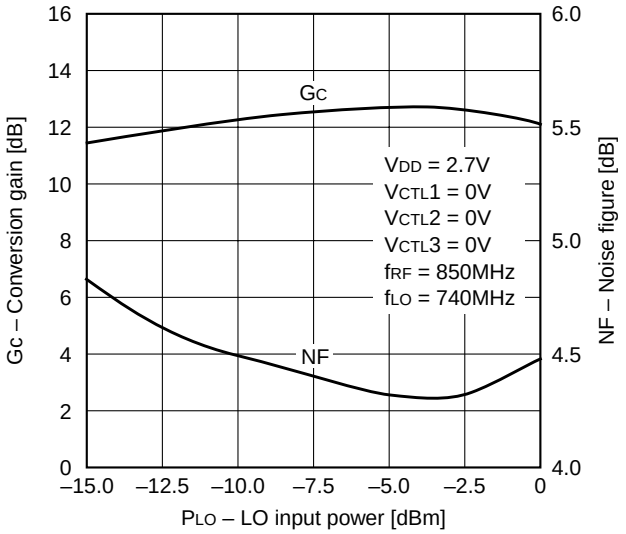


GPS P_{OUT}, IM3 vs. P_{IN}

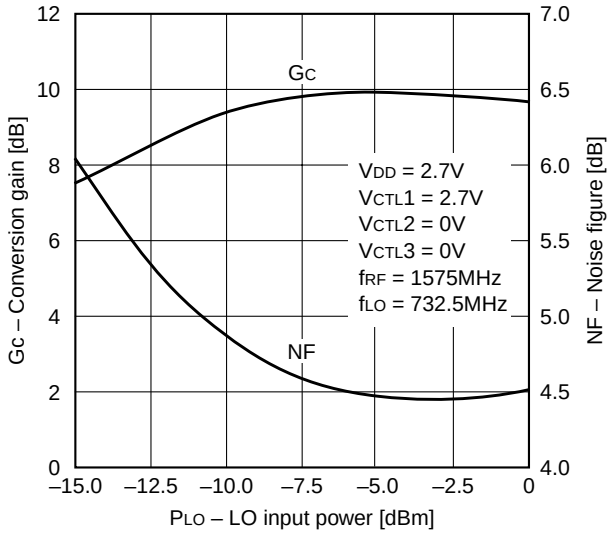


Mixer Block

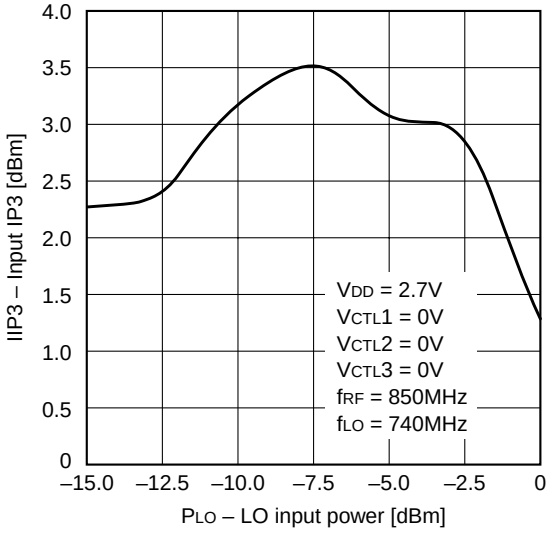
CDMA Gc, NF vs. PLO



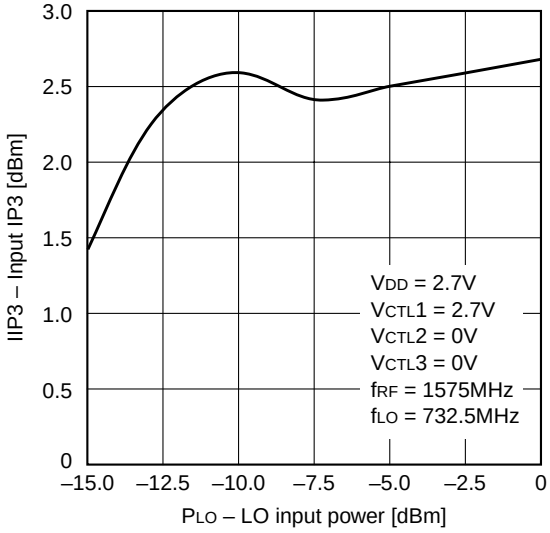
GPS Gc, NF vs. PLO



CDMA IIP3 vs. PLO



GPS IIP3 vs. PLO

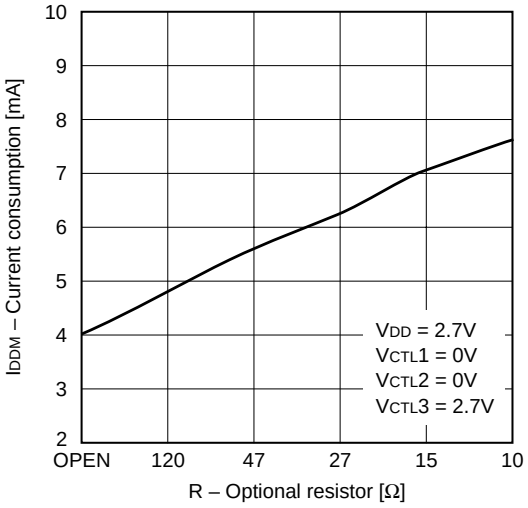


Characteristics Example When the Optional Resistor R is Added (Ta = 25°C)

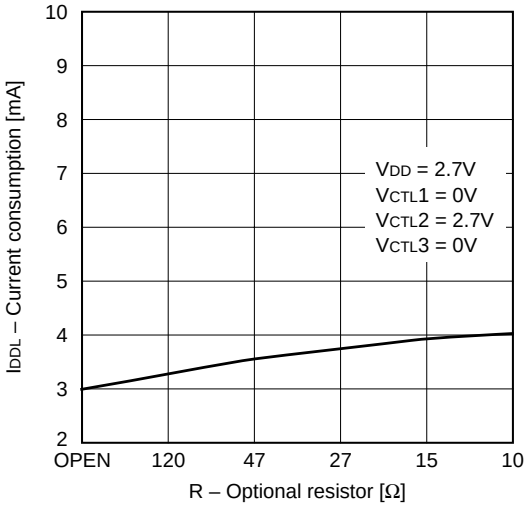
Low Noise Amplifier Block

* Measured with the choke inductor (L = 33nH) for decoupling inserted to Pin 9 (LNA OPT pin) in series.

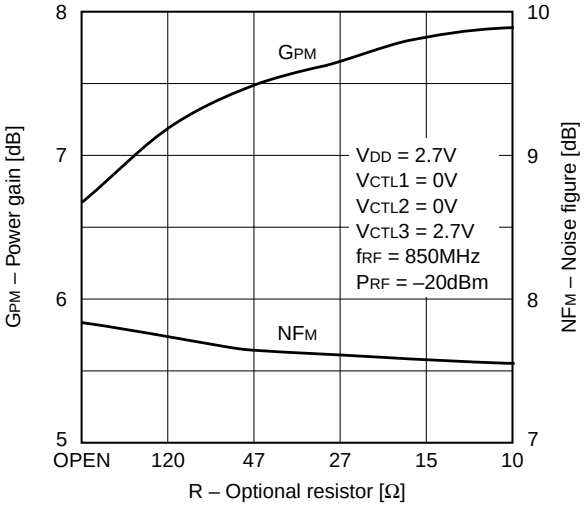
CDMA I_{DDM} vs. R



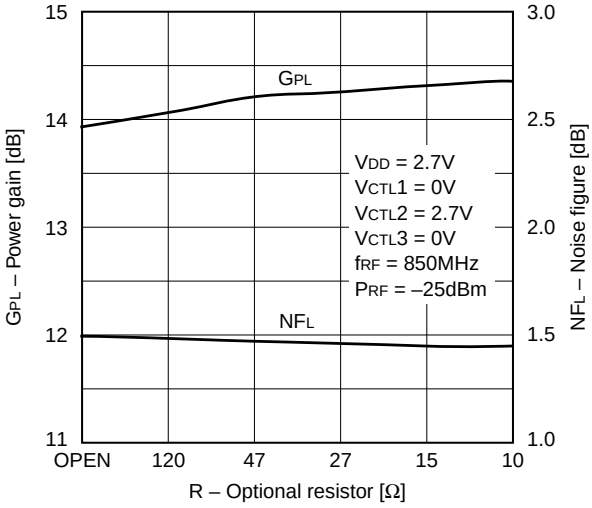
CDMA I_{DDL} vs. R



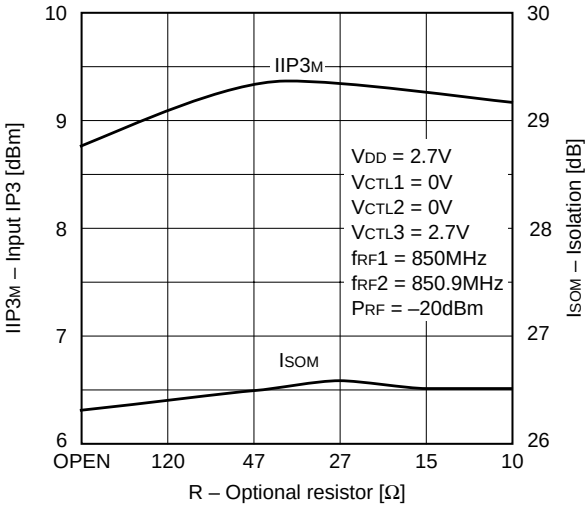
CDMA G_{PM}, NF_M vs. R



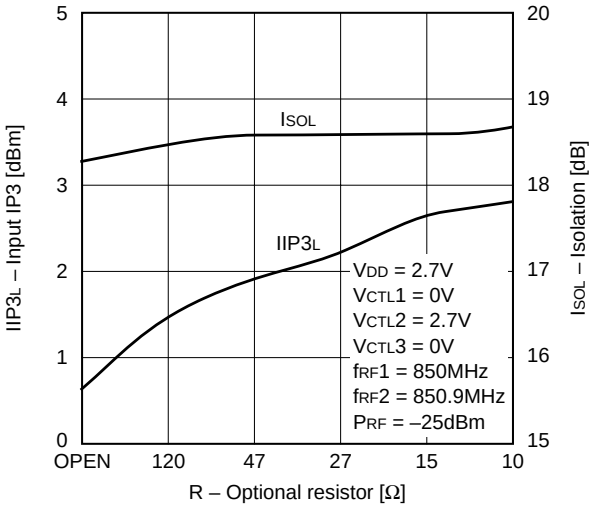
CDMA G_{PL}, NF_L vs. R



CDMA $IIP3_M$, I_{SOM} vs. R



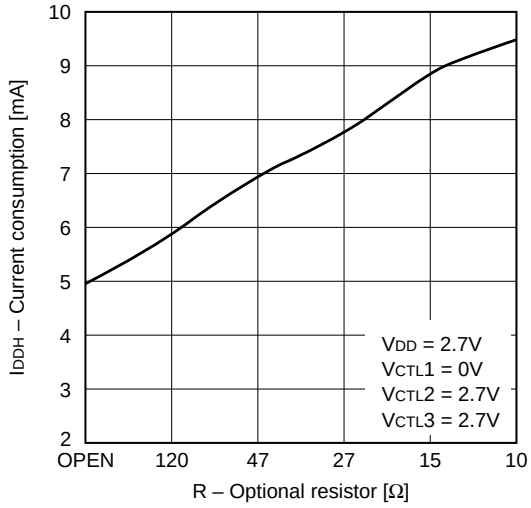
CDMA $IIP3_L$, I_{SOL} vs. R



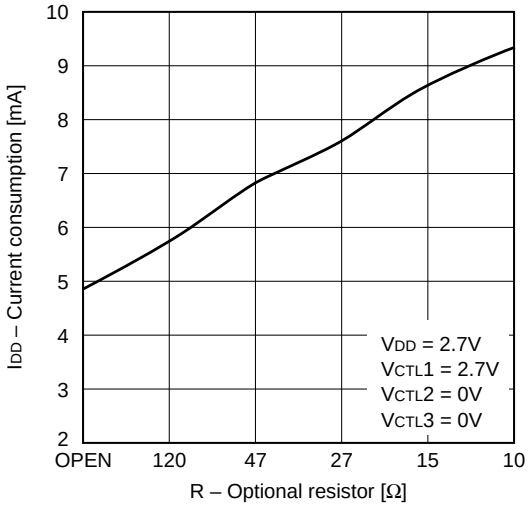
Low Noise Amplifier Block

* Measured with the choke inductor (L = 33nH) for decoupling inserted to Pin 9 (LNA OPT pin) in series.

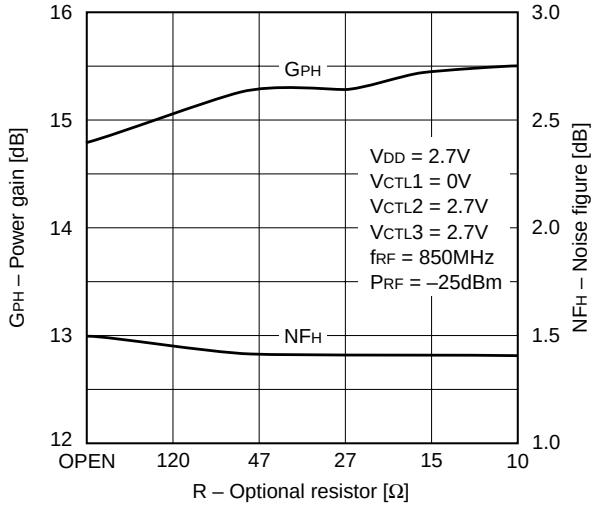
CDMA I_{DDH} vs. R



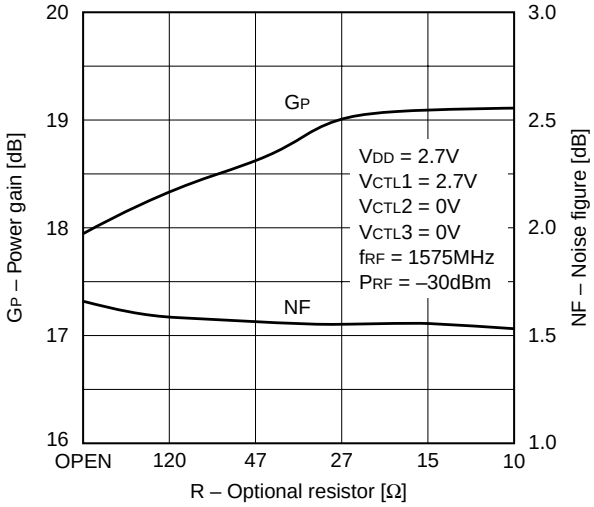
GPS I_{DD} vs. R



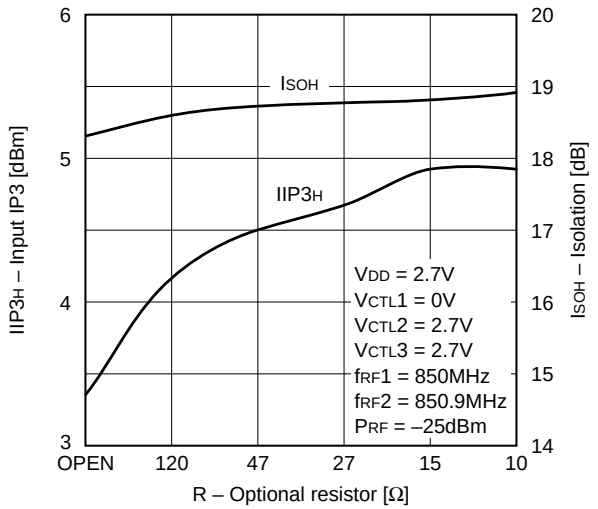
CDMA G_{PH}, NF_H vs. R



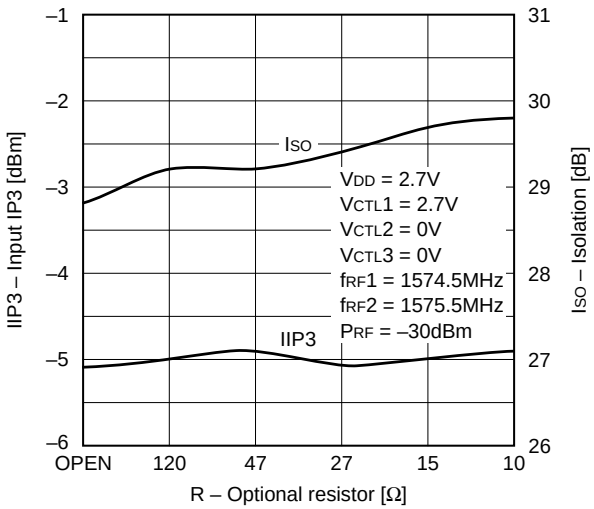
GPS G_P, NF vs. R



CDMA $IIP3_H$, I_{SOH} vs. R



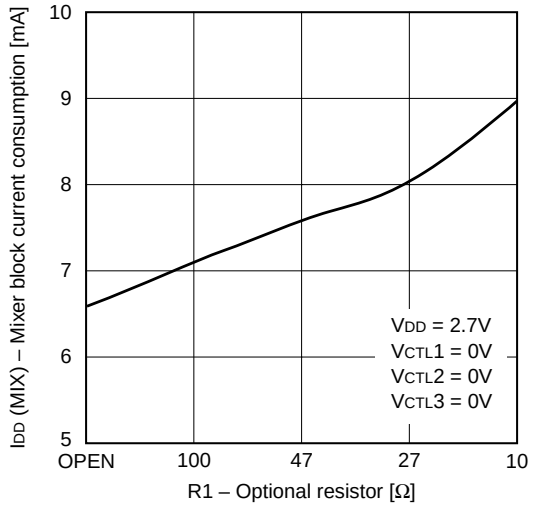
GPS IIP3, I_{SO} vs. R



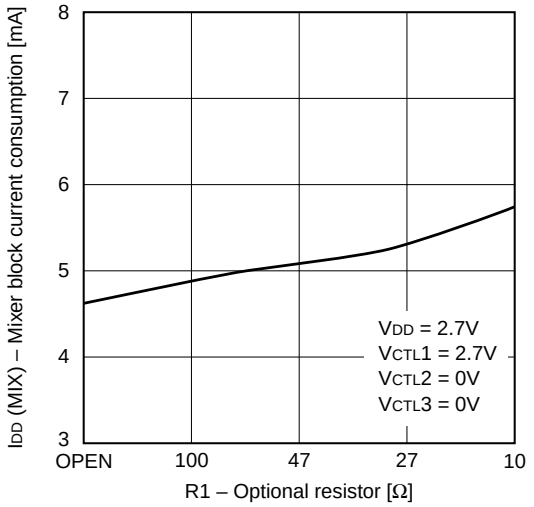
Characteristics Example When the Optional Resistor R is Added (Ta = 25°C)

Mixer Block

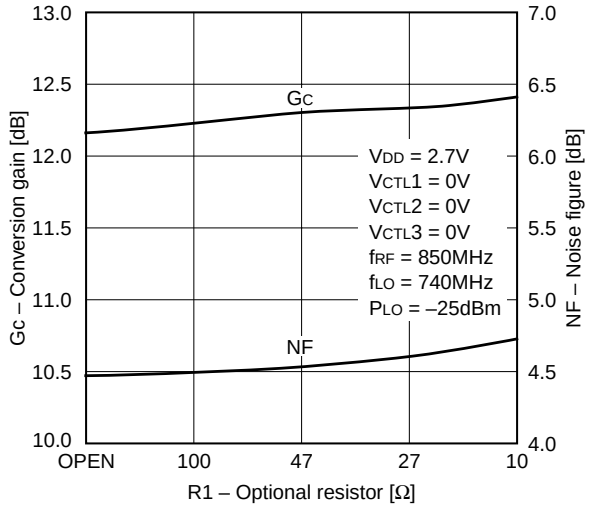
CDMA I_{DD} (MIX) vs. R1



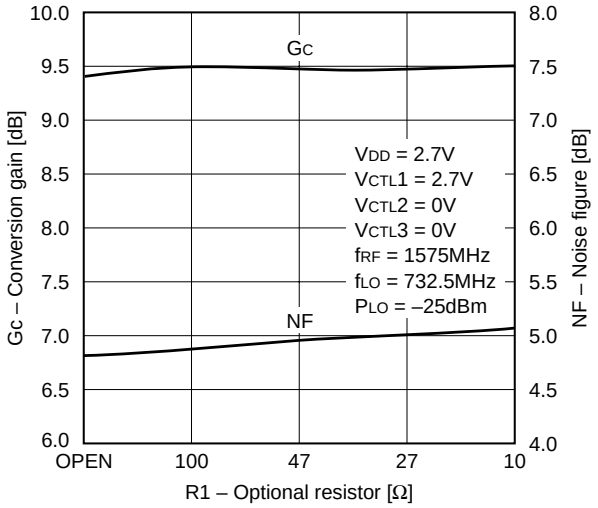
GPS I_{DD} (MIX) vs. R1



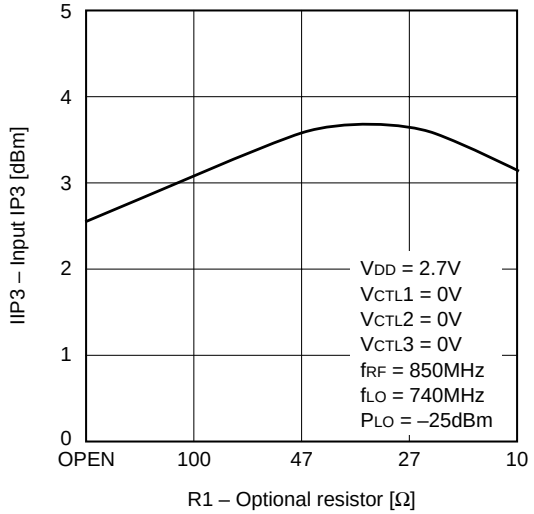
CDMA Gc, NF vs. R1



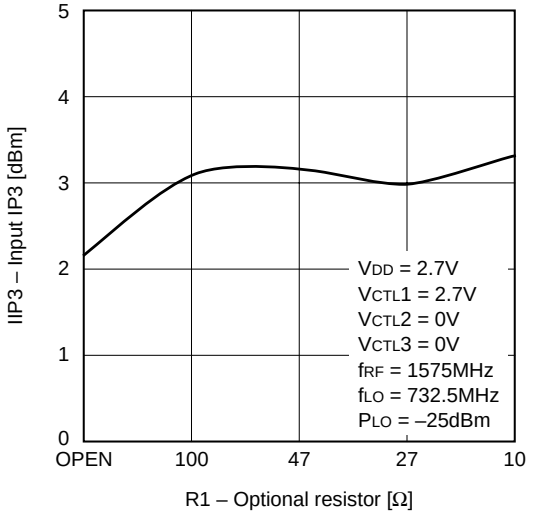
GPS Gc, NF vs. R1



CDMA IIP3 vs. R1

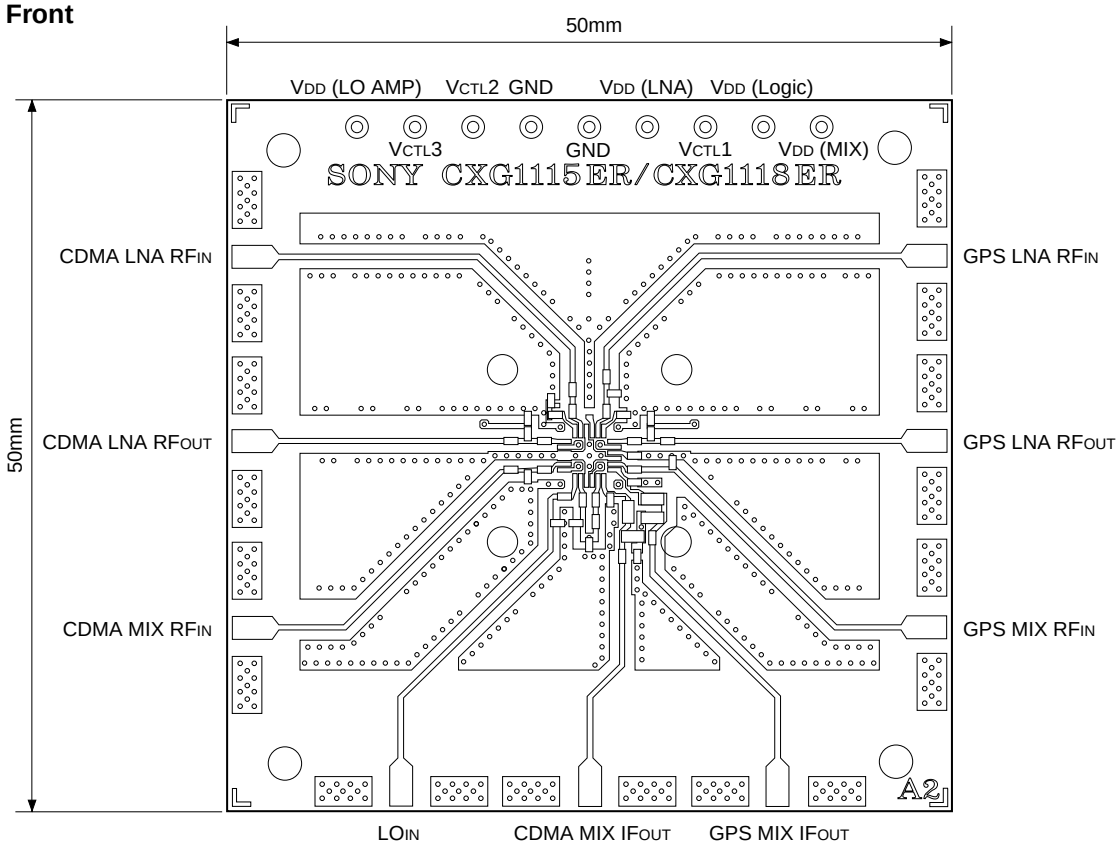


GPS IIP3 vs. R1



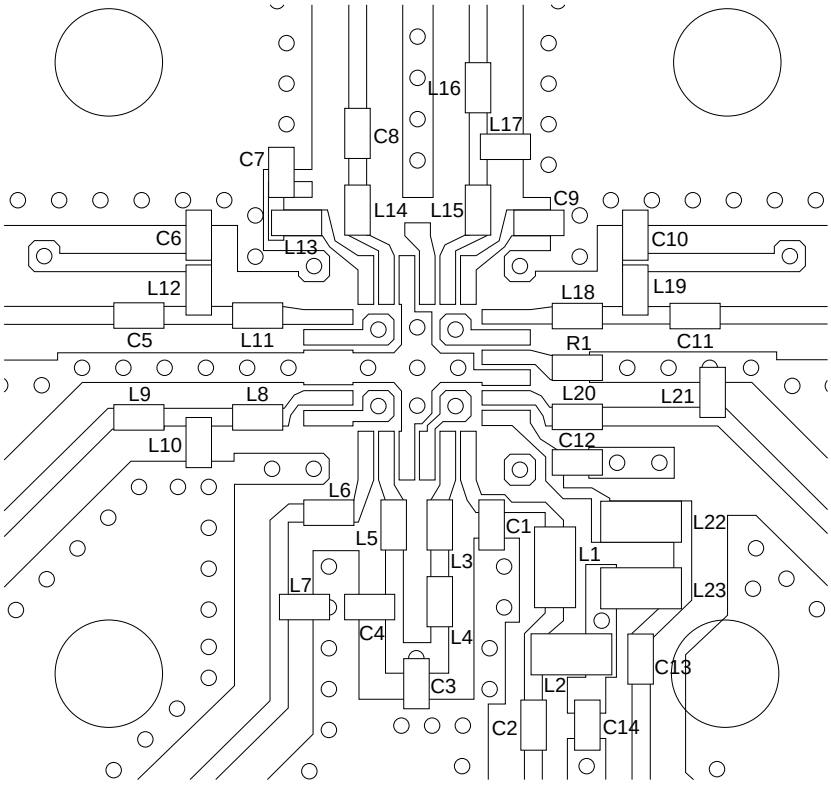
Recommended Evaluation Board

Front



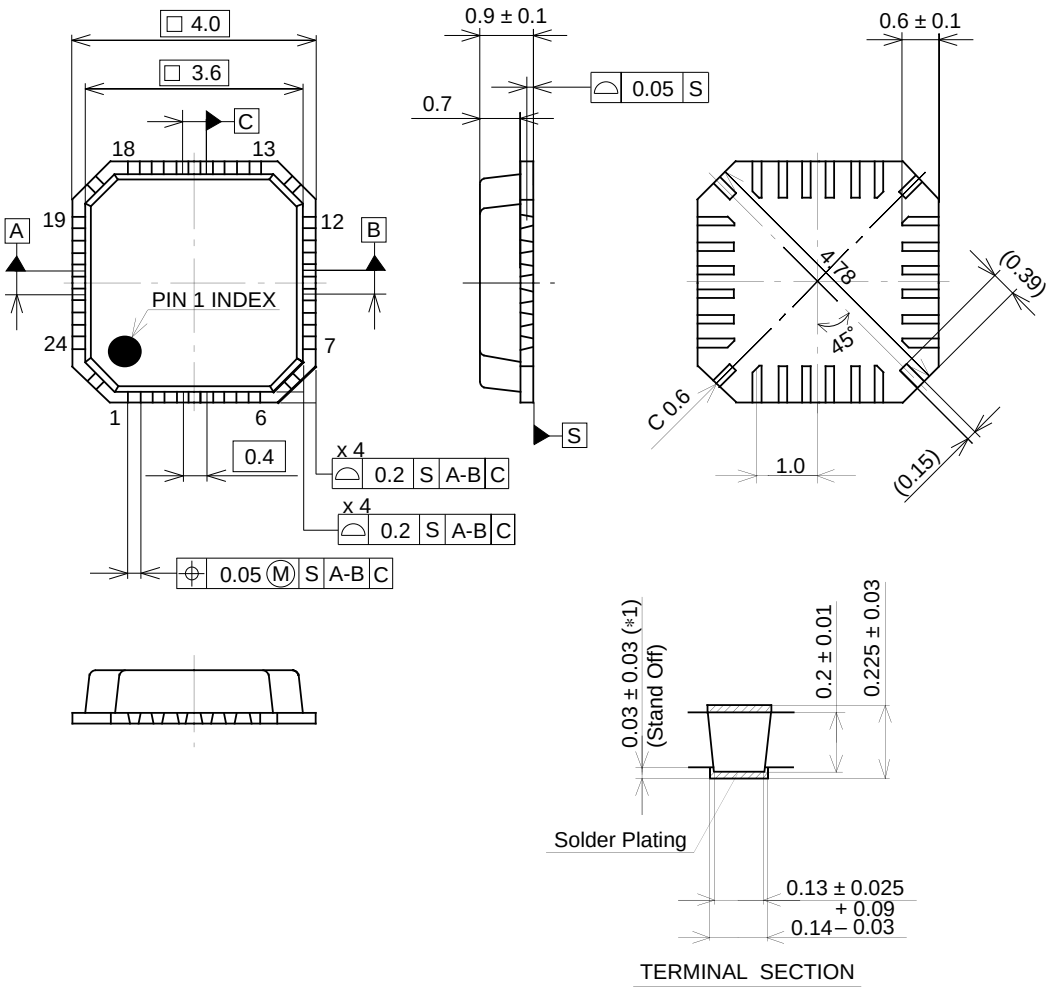
Glass fabric-base 4-layer epoxy board (thickness: 0.2mm × 2)
GND for the whole 2nd and 3rd layers

Enlarged Diagram of Center Part



Package Outline Unit: mm

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER PLATING	Sn-Bi Bi:1-4wt%
LEAD TREATMENT THICKNESS	5-18µm