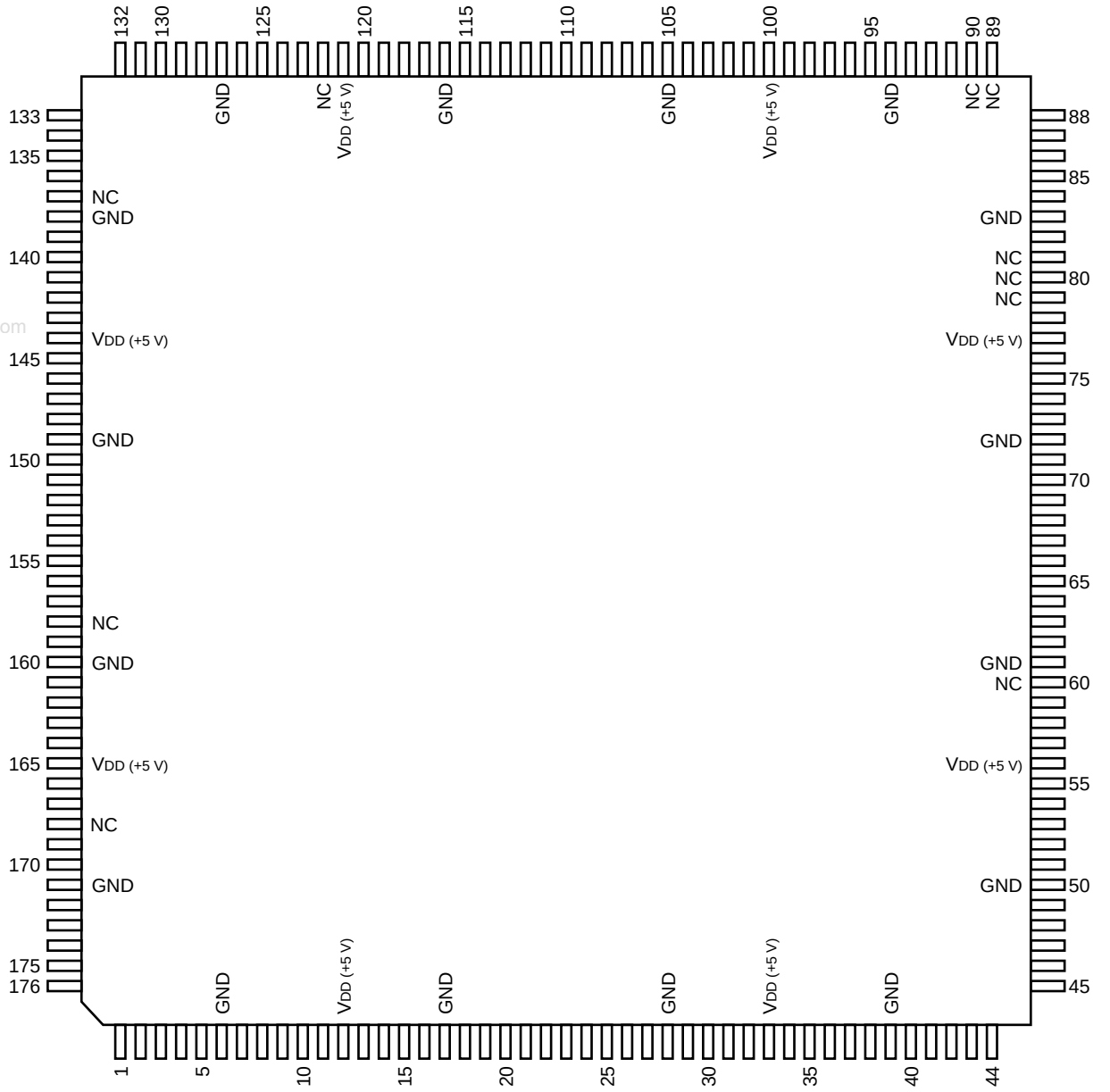
C-MOS A/V DATA PB PROCESS (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	RFADR5	45	O	$\overline{INT\_OUT}$	89	—	NC	133	I	SYSA5
2	O	RFADR6	46	O	$\overline{TCWEN}$	90	—	NC	134	I	SYSA6
3	O	RFADR7	47	O	$\overline{TCWRSTN}$	91	O	$\overline{WSYSEN}$	135	I	SYSA7
4	O	TABLE_A_EN	48	O	VEND	92	I	$\overline{EXT\_SPC\_FDO}$	136	I	SYSA8
5	O	TABLE_B_EN	49	O	VSYNC	93	O	$\overline{SPC\_FDO}$	137	—	NC
6	—	GND	50	—	GND	94	—	GND	138	—	GND
7	O	OE1	51	O	DOUT0	95	O	WFADR0	139	I	CLK
8	O	OE2	52	O	DOUT1	96	O	WFADR1	140	O	TEST1
9	O	OE3	53	O	DOUT2	97	O	WFADR2	141	O	TEST2
10	O	OE4	54	O	DOUT3	98	O	WFADR3	142	O	TEST3
11	O	OE5	55	O	DOUT4	99	O	WFADR4	143	O	TEST4
12	—	V_{DD}	56	—	V_{DD}	100	—	V_{DD}	144	—	V_{DD}
13	O	OE6	57	O	DOUT5	101	O	WFADR5	145	O	TEST5
14	O	OE7	58	O	DOUT6	102	O	WFADR6	146	O	TEST6
15	O	$\overline{READLOPLS}$	59	O	DOUT7	103	O	WFADR7	147	O	TEST7
16	O	$\overline{READRSTART}$	60	—	NC	104	O	$\overline{MWRST}$	148	O	TEST8
17	—	GND	61	—	GND	105	—	GND	149	—	GND
18	O	RE1	62	O	$\overline{VWE}$	106	O	GPI1	150	I	DATA0
19	I	$\overline{RCB\_L4}$	63	O	$\overline{VWRST}$	107	O	GPI2	151	I	DATA1
20	I	RCB_RE1	64	O	$\overline{VRE}$	108	I/O	SYSD0	152	I	DATA2
21	I	$\overline{RCB\_AGOP\_ST}$	65	O	$\overline{VRRST}$	109	I/O	SYSD1	153	I	DATA3
22	I	$\overline{RCB\_VGOP\_ST}$	66	O	FIFOEN	110	I/O	SYSD2	154	I	DATA4
23	I	TEST_DC	67	O	$\overline{AWE}$	111	I/O	SYSD3	155	I	DATA5
24	I	TEST_RCB	68	O	$\overline{AWRST}$	112	I/O	SYSD4	156	I	DATA6
25	I	$\overline{RCB\_N\_GOP\_GET}$	69	O	$\overline{ARE}$	113	I/O	SYSD5	157	I	DATA7
26	I	$\overline{RCB\_E\_OF\_V\_S}$	70	O	$\overline{ARRST}$	114	I/O	SYSD6	158	—	NC
27	I	$\overline{RCB\_RSYSPEN}$	71	O	$\overline{FIFORS}$	115	I/O	SYSD7	159	O	$\overline{APEN}$
28	—	GND	72	—	GND	116	—	GND	160	—	GND
29	I	HD	73	O	$\overline{CMDRRSTN}$	117	O	GPI3	161	O	$\overline{REVOUT}$
30	I	FP	74	I	$\overline{ADEN1}$	118	O	GPI4	162	I	MB2_RSYSPEN
31	O	REFH	75	I	$\overline{ADEN2}$	119	O	GPI5	163	I	MB2_NEXT_GET
32	O	REFF	76	I	$\overline{WSCFULL\_IN}$	120	O	GPI6	164	I	MB2_END_SECTOR
33	—	V_{DD}	77	—	V_{DD}	121	—	V_{DD}	165	—	V_{DD}
34	O	OE8	78	I	TEST_MODE	122	—	NC	166	I	AUDIO_CORE_WE
35	O	$\overline{RECFULL}$	79	—	NC	123	I	$\overline{RICCS}$	167	I	TEST_MODE2
36	O	$\overline{WSCFULL}$	80	—	NC	124	I	$\overline{SYSRD}$	168	—	NC
37	O	$\overline{WSTART}$	81	—	NC	125	I	$\overline{SYSWR}$	169	I	EXT_RE
38	O	$\overline{READ\_GATE}$	82	O	$\overline{TX\_GATE}$	126	I	$\overline{SYSRST}$	170	O	$\overline{MRRST}$
39	—	GND	83	—	GND	127	—	GND	171	—	GND
40	O	ASYNC	84	O	$\overline{BUF01REN1}$	128	I	SYSA0	172	O	RFADR0
41	O	AEND	85	O	$\overline{BUF01OE}$	129	I	SYSA1	173	O	RFADR1
42	I	INT0	86	O	$\overline{BUF02REN1}$	130	I	SYSA2	174	O	RFADR2
43	I	INT1	87	O	$\overline{BUF02OE}$	131	I	SYSA3	175	O	RFADR3
44	I	INT2	88	O	$\overline{BUF01EF}$	132	I	SYSA4	176	O	RFADR4

INPUT

$\overline{\text{ADEN1}}$, $\overline{\text{ADEN2}}$	; SDDI APPLICATION DATA ENABLE 1, 2
AUDIO_CORE_WE	; AUDIO CORE WRITE ENABLE
CLK	; SYSTEM CLOCK
DATA0 - DATA7	; DATA IN 0 - 7
EXT_$\overline{\text{RE}}$	; EXTERNAL READ ENABLE
$\overline{\text{EXT\_SPC\_FDO}}$	; TEST PIN
FP	; REFERENCE FRAME
HD	; REFERENCE H
INT0 - INT2	; SDDI INT 0 - 2
MB2_END_SECTOR	; END OF VIDEO SECTOR PULSE IN
MB2_NEXT_GET	; NEXT GOP GET START PULSE IN
MB2_RSYSPEN	; READ SYSTEM PRE ENABLE IN
$\overline{\text{RCB\_AGOP\_ST}}$	; READ CONTROL AUDIO GOP START
$\overline{\text{RCB\_E\_OF\_V\_S}}$	; READ CONTROL END OF VIDEO SECTOR
$\overline{\text{RCB\_L4}}$	; READ CONTROL LENGTH 4
$\overline{\text{RCB\_N\_GOP\_GET}}$	; READ CONTROL NEXT GOP GET PULSE
RCB_RE1	; READ CONTROL READ ENABLE 1
$\overline{\text{RCB\_RSYSPEN}}$	; READ CONTROL READ SYSTEM PRE ENABLE
$\overline{\text{RCB\_VGOP\_ST}}$	; READ CONTROL VIDEO GOP START
$\overline{\text{RICCS}}$	; CXD8991R CHIP SELECT
SYSA0 - SYSA8	; CPU ADDRESS 0 - 8
$\overline{\text{SYSRST}}$	; SYSTEM RESET
$\overline{\text{SYSRD}}$	; CXD8991R READ ENABLE
$\overline{\text{SYSWR}}$	; CXD8991R WRITE ENABLE
TEST_DC	; TEST PIN
TEST_MODE	; TEST PIN
TEST_MODE2	; TEST PIN
TEST_RCB	; TEST PIN
$\overline{\text{WSCFULL\_IN}}$	; WRITE SECTOR FULL IN

INPUT/OUTPUT

SYSD0 - SYSD7	; CPU DATA BUS 0 - 7

OUTPUT

AEND	; AUDIO END PULSE
$\overline{\text{APEN}}$	; AUDIO PROCESS ENABLE
ARE	; AUDIO CORE READ ENABLE
$\overline{\text{ARRST}}$	; AUDIO CORE READ RESET
ASYNC	; AUDIO SYNC BIT
$\overline{\text{AWE}}$	; AUDIO CORE WRITE ENABLE
AWRST	; AUDIO CORE WRITE RESET
$\overline{\text{BUF01EF}}$	; SPC I/F* : BUFFER 1 EMPTY FLAG
$\overline{\text{BUF01OE}}$, $\overline{\text{BUF02OE}}$	; SPC I/F* : BUFFER 1, 2 OUT ENABLE
$\overline{\text{BUF01REN1}}$, $\overline{\text{BUF02REN1}}$	; SPC I/F* : BUFFER 1, 2 READ ENABLE
$\overline{\text{CMDRRSTN}}$	; COMMAND FIFO READ RESET
DOUT0 - DOUT7	; DATA OUT 0 - 7
$\overline{\text{FIFOEN}}$	; FIFO POWER ON ENABLE
$\overline{\text{FIFORS}}$	; FIFO POWER ON RESET
GPI1 - GPI6	; GPI PORT 1 - 6
$\overline{\text{INT\_OUT}}$	; INTERRUPT TO CPU
$\overline{\text{MRRST}}$	; MAIN MEMORY READ RESET
$\overline{\text{MWRST}}$	; MAIN MEMORY WRITE RESET
OE1 - OE8	; MAIN MEMORY OUTPUT ENABLE 1 - 8
RE1	; MAIN MEMORY READ ENABLE 1
$\overline{\text{READ\_GATE}}$	; MAIN MEMORY READ GATE
$\overline{\text{READLOPLS}}$	; READ ADDRESS LOAD PULSE
$\overline{\text{READRSTART}}$	; READ ADDRESS START PULSE
$\overline{\text{RECFULL}}$	; READ SECTOR FULL PULSE
REFF	; REFERENCE FRAME
REFH	; REFERENCE H
$\overline{\text{REVOUT}}$	; MAIN MEMORY VIDEO READ ENABLE
RFADR0 - RFADR7	; MAIN MEMORY READ ADDRESS 0 - 7
$\overline{\text{SPC\_FDO}}$	; MAIN MEMORY WRITE ENABLE
TABLE_A_EN, TABLE_B_EN	; TABLE A, B ENABLE
$\overline{\text{TCWEN}}$	; MESSAGE FIFO WRITE ENABLE
$\overline{\text{TCWRSTN}}$	; MESSAGE FIFO WRITE RESET
TEST1 - TEST8	; TEST PIN 1 - 8
$\overline{\text{TX\_GATE}}$	; SDDI CORE IC ENABLE
VEND	; VIDEO END PULSE
$\overline{\text{VRE}}$	; VIDEO CORE READ ENABLE
$\overline{\text{VRRST}}$	; VIDEO CORE READ RESET
VSYNC	; VIDEO SYNC BIT
$\overline{\text{VWE}}$	; VIDEO CORE WRITE ENABLE
$\overline{\text{VWRST}}$	; VIDEO CORE WRITE RESET
WFADR0 - WFADR7	; MAIN MEMORY WRITE ADDRESS 0 - 7
$\overline{\text{WSCFULL}}$	; WRITE SECTOR FULL PULSE
$\overline{\text{WSTART}}$	; WRITE START PULSE
$\overline{\text{WSYSEN}}$	; WRITE SYSTEM ENABLE

* SPC I/F : SCSI PROTOCOL CONTROLLER INTERFACE