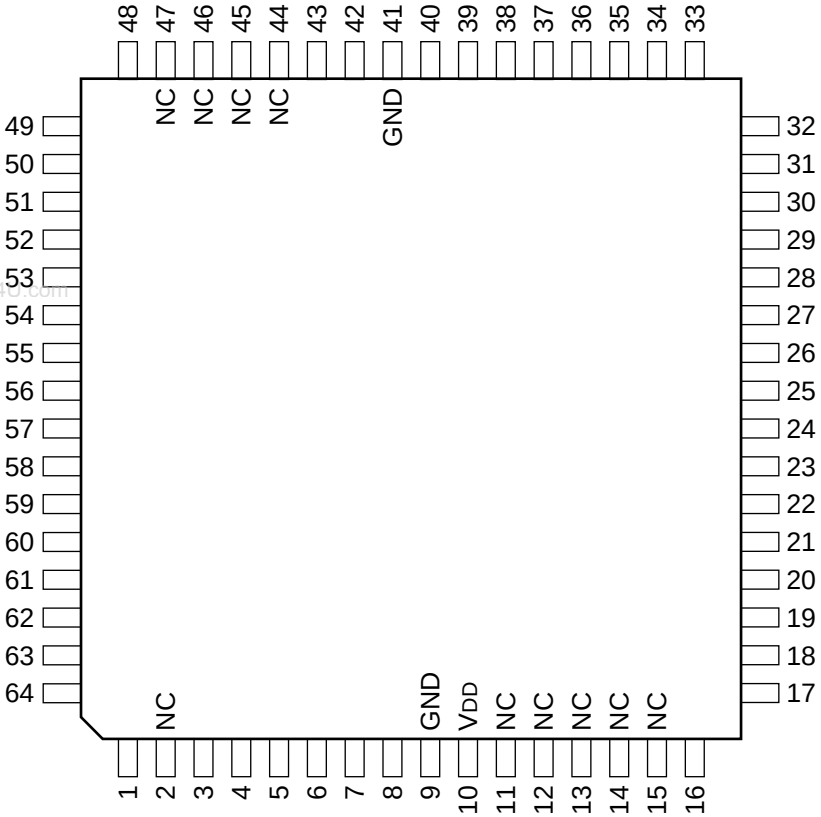
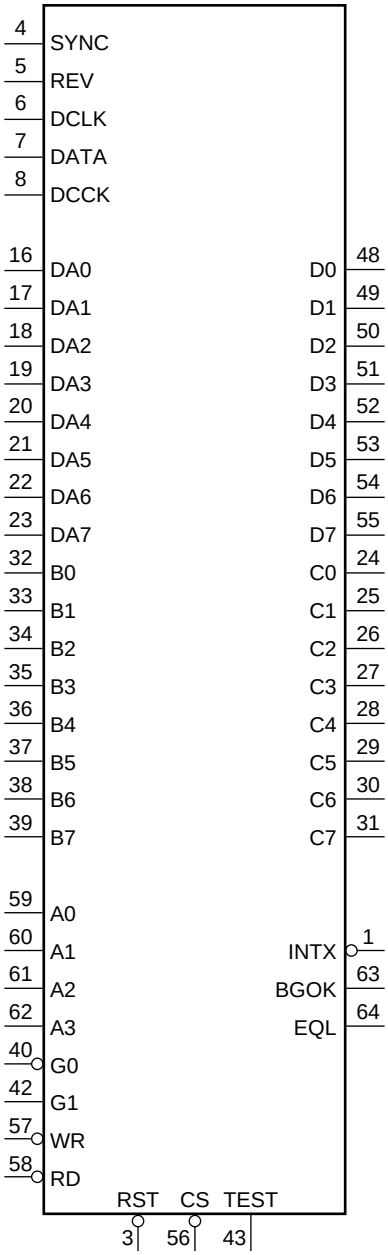
C-MOS USER-BIT MARKER DETECTOR

—TOP VIEW—





INPUT

A0 - A3	;	ADDRESS BUS
B0 - B7	;	ADDING DATA
$\overline{CS}$	;	CHIP SELECT
DA0 - DA7	;	ADDING OR THROUGH DATA
DATA	;	DEMODULATED SERIAL DATA
DCCK	;	LTC DECODE CLOCK
DCLK	;	DEMODULATED CLOCK
$\overline{G0}$, G1	;	GATE
$\overline{RST}$	;	SYSTEM RESET
$\overline{RD}$	;	READ
SYNC	;	SYNC WORD DATA
REV	;	REV/FWD BIT
TEST	;	TEST
$\overline{WR}$	;	WRITE

OUTPUT

BGOK	;	BINARY GROUP COINCIDENCE
C0 - C7	;	ADDED DATA
$\overline{EQL}$	;	USER-BIT MARK COINCIDENCE
$\overline{INTX}$	;	USER-BIT MARK

INPUT/OUTPUT

D0 - D7	;	DATA BUS

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	$\overline{INTX}$	17	I	DA1	33	I	B1	49	I/O	D1
2	—	NC	18	I	DA2	34	I	B2	50	I/O	D2
3	I	$\overline{RST}$	19	I	DA3	35	I	B3	51	I/O	D3
4	I	SYNC	20	I	DA4	36	I	B4	52	I/O	D4
5	I	REV	21	I	DA5	37	I	B5	53	I/O	D5
6	I	DCLK	22	I	DA6	38	I	B6	54	I/O	D6
7	I	DATA	23	I	DA7	39	I	B7	55	I/O	D7
8	I	DCCK	24	O	C0	40	I	$\overline{G0}$	56	I	$\overline{CS}$
9	—	GND	25	O	C1	41	—	GND	57	I	$\overline{WR}$
10	—	V_{DD}	26	O	C2	42	I	G1	58	I	$\overline{RD}$
11	—	NC	27	O	C3	43	I	TEST	59	I	A0
12	—	NC	28	O	C4	44	—	NC	60	I	A1
13	—	NC	29	O	C5	45	—	NC	61	I	A2
14	—	NC	30	O	C6	46	—	NC	62	I	A3
15	—	NC	31	O	C7	47	—	NC	63	O	BGOK
16	I	DA0	32	I	B0	48	I/O	D0	64	O	EQL