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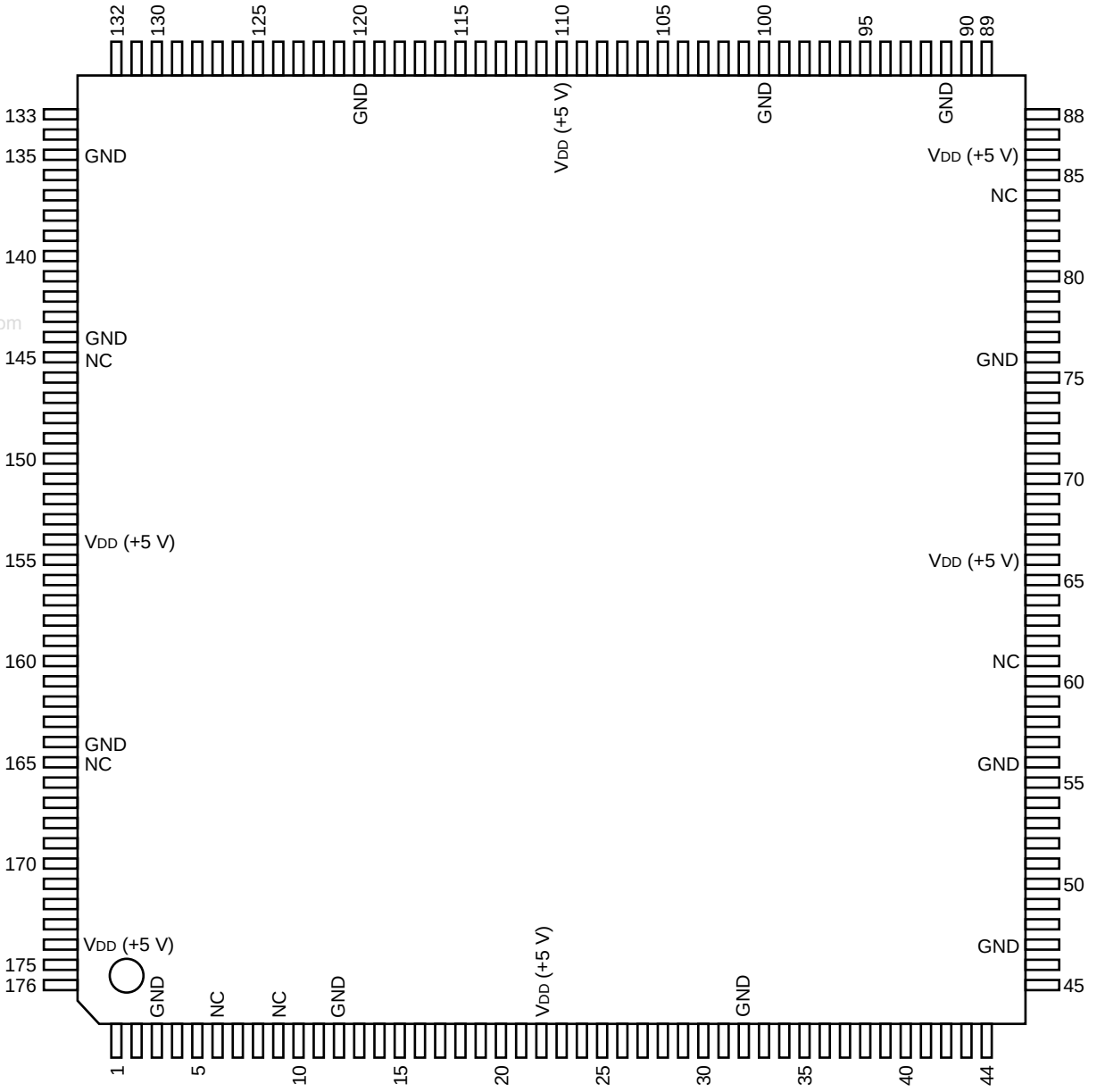
IL11

C-MOS PERIPHERAL CONTROL IC FOR R3000 (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	$\overline{BE8CS}$	45	O	RAM2CS	89	I	$\overline{IO\_STROBE}$	133	O	$\overline{AF4CS}$
2	O	$\overline{BECCS}$	46	O	RAM1CS	90	O	$\overline{EXTDATAEN}$	134	O	$\overline{AF0CS}$
3	—	GND	47	—	GND	91	—	GND	135	—	GND
4	O	$\overline{SCSIRD}$	48	I/O	D0	92	O	$\overline{RXFIFO3EN}$	136	O	$\overline{B40CS}$
5	O	$\overline{SCSIWR}$	49	I/O	D1	93	O	$\overline{RXFIFO2EN}$	137	O	$\overline{B44CS}$
6	—	NC	50	I/O	D2	94	O	$\overline{RXFIFO1EN}$	138	O	$\overline{B48CS}$
7	O	$\overline{SCSICS1}$	51	I/O	D3	95	O	$\overline{RXFIFO0EN}$	139	O	$\overline{B4CCS}$
8	O	$\overline{SCSICS0}$	52	I/O	D4	96	O	$\overline{TXFIFO3EN}$	140	O	$\overline{B50CS}$
9	—	NC	53	I/O	D5	97	O	$\overline{TXFIFO2EN}$	141	O	$\overline{B54CS}$
10	O	DBCLK	54	I/O	D6	98	O	$\overline{DIAGFIFO1EN}$	142	O	$\overline{B58CS}$
11	O	$\overline{DMACCS}$	55	I/O	D7	99	O	$\overline{DIAGFIFO0EN}$	143	O	$\overline{B5CCS}$
12	—	GND	56	—	GND	100	—	GND	144	—	GND
13	I/O	$\overline{IORD}$	57	O	$\overline{WRENA}$	101	O	RXFIFO_RCK	145	—	NC
14	I/O	$\overline{IOWR}$	58	O	$\overline{WRENB}$	102	O	TXFIFO_WCK	146	O	$\overline{B80CS}$
15	I	$\overline{MRD}$	59	O	$\overline{WRENC}$	103	O	$\overline{SDC\_RECEN}$	147	O	$\overline{B84CS}$
16	I	$\overline{MWR}$	60	O	$\overline{WREND}$	104	O	$\overline{SDC\_PBEN}$	148	O	$\overline{B88CS}$
17	I	DMA_AEN	61	—	NC	105	I	$\overline{DBWAIT}$	149	O	$\overline{B8CCS}$
18	I	DMAAK3	62	I	BEN0	106	O	$\overline{PIO\_RESET}$	150	O	$\overline{B90CS}$
19	I	DMAAK2	63	I	BEN1	107	O	$\overline{LTC\_WEN}$	151	O	$\overline{B94CS}$
20	I	DMAAK1	64	I	BEN2	108	O	CA2CRCK	152	O	$\overline{B98CS}$
21	I	DMAAK0	65	I	BEN3	109	O	CA1CRCK	153	O	$\overline{B9CCS}$
22	—	V_{DD}	66	—	V_{DD}	110	—	V_{DD}	154	—	V_{DD}
23	I	SYS_FRAME	67	I	A0	111	O	$\overline{ACCCS}$	155	O	$\overline{AFCCS}$
24	I	SYS_1/2V	68	I	A1	112	O	$\overline{AC8CS}$	156	O	$\overline{BA0CS}$
25	O	SYS_FIELD	69	I	A22	113	O	$\overline{AC4CS}$	157	O	$\overline{BA4CS}$
26	O	$\overline{RDEN}$	70	I	A23	114	O	$\overline{AC0CS}$	158	O	$\overline{BA8CS}$
27	O	$\overline{WREN}$	71	I	A24	115	O	$\overline{SDDIRX2CS}$	159	O	$\overline{BACCS}$
28	O	$\overline{IOEN}$	72	I	A25	116	O	$\overline{SDDIRX1CS}$	160	O	$\overline{BB0CS}$
29	I	VSBUS_RXDATA	73	I	A26	117	O	$\overline{SDDITX2CS}$	161	O	$\overline{BB4CS}$
30	O	VSBUS_RXCLK	74	I	A27	118	O	$\overline{SDDITX1CS}$	162	O	$\overline{BB8CS}$
31	I	$\overline{VSBUS\_RESET}$	75	I	A28	119	O	$\overline{SDC\_SDDIRDEN}$	163	O	$\overline{BBCCS}$
32	—	GND	76	—	GND	120	—	GND	164	—	GND
33	O	SIOBA	77	I	$\overline{BURST}$	121	O	DSP_HBCK	165	—	NC
34	O	SIOCD	78	I	$\overline{LAST}$	122	O	DSP_HRS	166	O	$\overline{BC0CS}$
35	O	$\overline{SIO2RD}$	79	I	$\overline{RD}$	123	O	DSP_HXS	167	O	$\overline{BC4CS}$
36	O	$\overline{SIO2WR}$	80	I	$\overline{WR}$	124	O	DSP_HR	168	O	$\overline{BC8CS}$
37	O	$\overline{SIO1RD}$	81	I	$\overline{DATAEN}$	125	I	DSP_HX	169	O	$\overline{BCCCS}$
38	O	$\overline{SIO1WR}$	82	I	$\overline{SYSCLK}$	126	O	ENC_ENN3_3	170	O	$\overline{BD0CS}$
39	O	$\overline{PIO3CS}$	83	I	$\overline{SYS\_RESET}$	127	O	ENC_ENN2	171	O	$\overline{BD4CS}$
40	O	$\overline{PIO2CS}$	84	—	NC	128	O	ENC_ENN1	172	O	$\overline{BD8CS}$
41	O	$\overline{PIO1CS}$	85	O	$\overline{ACK}$	129	O	DEC_ENN3_3	173	O	$\overline{BDCCS}$
42	O	$\overline{CTC2CS}$	86	—	V_{DD}	130	O	DEC_ENN2	174	—	V_{DD}
43	O	$\overline{CTC1CS}$	87	O	$\overline{RDCEN}$	131	O	DEC_ENN1	175	O	$\overline{BE0CS}$
44	O	$\overline{FLASHCS}$	88	I	$\overline{M\_STROBE}$	132	O	$\overline{AF8CS}$	176	O	$\overline{BE4CS}$

INPUT/OUTPUT

D0 - 7	; CPU DATA BUS 0 - 7
IORD	; I/O READ PULSE FOR DMA CONTROLLER
IOWR	; I/O WRITE PULSE FOR DMA CONTROLLER

INPUT

A0, A1, A22 - A28	; CPU ADDRESS BUS 0, 1, and 22 - 28
BEN0 - 3	; CPU BYTE ENABLE 0 - 3
BURST	; BURST STATE
DATAEN	; DATA ENABLE PULSE
DBWAIT	; CPU WAIT
DMA_AEN	; DMA ADDRESS ENABLE
DMAAK0 - 3	; DMA ACKNOWLEDGE 0 - 3
DSP_HX	; RECEIVE DATA FOR AUDIO DSP I/F
IO_STROBE	; I/O STROBE PULSE
LAST	; LAST STATE
M_STROBE	; MEMORY STROBE PULSE
MRD	; MEMORY READ FOR CONTROLLER
MWR	; MEMORY WRITE FOR CONTROLLER
RD	; CPU READ PULSE
SYS_1/2V	; SYSTEM 1/2 V PULSE
SYS_FRAME	; SYSTEM FRAME PULSE
SYS_RESET	; SYSTEM RESET
SYSCLK	; 20 MHz REFERENCE CLOCK
VSBUS_RESET	; VSBUS RX CLOCK RESET
VSBUS_RXDATA	; VSBUS INPUT DATA
WR	; CPU WRITE PULSE

OUTPUT

***CS	; CHIP SELECT (ADDRESS : ***xxxxxH)
ACK	; ACKNOWLEDGE
B4CCS	; INTERRUPT ACKNOWLEDGE (ADDRESS : B4CxxxxxH)
B48CS	; INTERRUPT CONTROLLER CHIP SELECT (ADDRESS : B48xxxxxH)
CA1CRCK, CA2CRCK	; SDI AUDIO DATA WRITE CLOCK
CTC1CS	; CTC 1 CHIP SELECT (ADDRESS : A60xxxxxH)
CTC2CS	; CTC 2 CHIP SELECT (ADDRESS : A70xxxxxH)
DBCLK	; 1/2 DIVIDING SYSCLK
DEC_ENN1, 2, 3_3	; ADDRESS ENABLE 1 - 3 FOR DEC-79
DIAGFIFO0EN	; CHIP SELECT (ADDRESS : B60xxxxxH)
DIAGFIFO1EN	; CHIP SELECT (ADDRESS : B64xxxxxH)
DMACCS	; DMA CONTROLLER CHIP SELECT (ADDRESS : AD0xxxxxH)
DSP_HBCK	; BIT CLOCK FOR AUDIO DSP I/F
DSP_HR	; SEND DATA FOR AUDIO DSP I/F
DSP_HRS	; SEND START FOR AUDIO DSP I/F
DSP_HXS	; RECEIVE START FOR AUDIO DSP I/F
ENC_ENN1, 2, 3_3	; ADDRESS ENABLE 1 - 3 FOR ENC-29
EXTDATAEN	; EXTENDED DATA ENABLE
FLASHCS	; FLASH CHIP SELECT (ADDRESS : BF0xxxxxH)
IOEN	; I/O ENABLE
LTC_WEN	; LTC WRITE ENABLE
PIO_RESET	; PARALLEL I/O RESET
PIO1CS	; PIO 1 CHIP SELECT (ADDRESS : A40xxxxxH)
PIO2CS	; PIO 2 CHIP SELECT (ADDRESS : A50xxxxxH)
PIO3CS	; PIO 3 CHIP SELECT (ADDRESS : A58xxxxxH)
RAM1CS	; SRAM CHIP SELECT (ADDRESS : A00xxxxxH)
RAM2CS	; SRAM CHIP SELECT (ADDRESS : A10xxxxxH)
RDCEN	; READ CHIP ENABLE
RDEN	; READ ENABLE
RXFIFO_RCK	; READ CLOCK FOR RX FIFO
RXFIFO0EN	; CHIP SELECT (ADDRESS : B70xxxxxH)
RXFIFO1EN	; CHIP SELECT (ADDRESS : B74xxxxxH)
RXFIFO2EN	; CHIP SELECT (ADDRESS : B78xxxxxH)
RXFIFO3EN	; CHIP SELECT (ADDRESS : B7CxxxxxH)
SCSICS0	; SPCR8 (ADDRESS : AE8xxxxxH) or SPCR16 (ADDRESS : B10xxxxxH)
SCSICS1	; SPCDMA CHIP SELECT (ADDRESS : B00xxxxxH)
SCSIRD	; L : READ FOR SCSI
SCSIWR	; SPCR8 LOWER BYTE WRITE ENABLE
SDC_PBEN	; SDC PB DATA BUS ENABLE
SDC_RECEN	; SDC REC DATA BUS ENABLE
SDC_SDDIRDEN	; SDC SDDI READ ENABLE
SDDIRX1CS	; SDDI DECODER 2 CHIP SELECT (ADDRESS : AB0xxxxxH)
SDDIRX2CS	; SDDI DECODER 1 CHIP SELECT (ADDRESS : AB8xxxxxH)
SDDITX1CS	; SDDI ENCODER 2 CHIP SELECT (ADDRESS : AA0xxxxxH)
SDDITX2CS	; SDDI ENCODER 1 CHIP SELECT (ADDRESS : AA8xxxxxH)
SIO1RD	; SIO 1 READ ENABLE (ADDRESS : A80xxxxxH)
SIO1WR	; SIO 1 WRITE ENABLE (ADDRESS : A80xxxxxH)
SIO2RD	; SIO 2 READ ENABLE (ADDRESS : A90xxxxxH)
SIO2WR	; SIO 2 WRITE ENABLE (ADDRESS : A90xxxxxH)
SIOBA	; SIO BA REGISTER SELECT
SIOCD	; SIO CD REGISTER SELECT
SYS_FIELD	; SYSTEM FIELD PULSE
TXFIFO_WCK	; WRITE CLOCK FOR TX FIFO
TXFIFO2EN	; CHIP SELECT (ADDRESS : B68xxxxxH)
TXFIFO3EN	; CHIP SELECT (ADDRESS : B6CxxxxxH)
VSBUS_RXCLK	; VSBUS RX CLOCK
WREN	; WRITE ENABLE
WRENA - WREND	; SRAM A - D WRITE ENABLE