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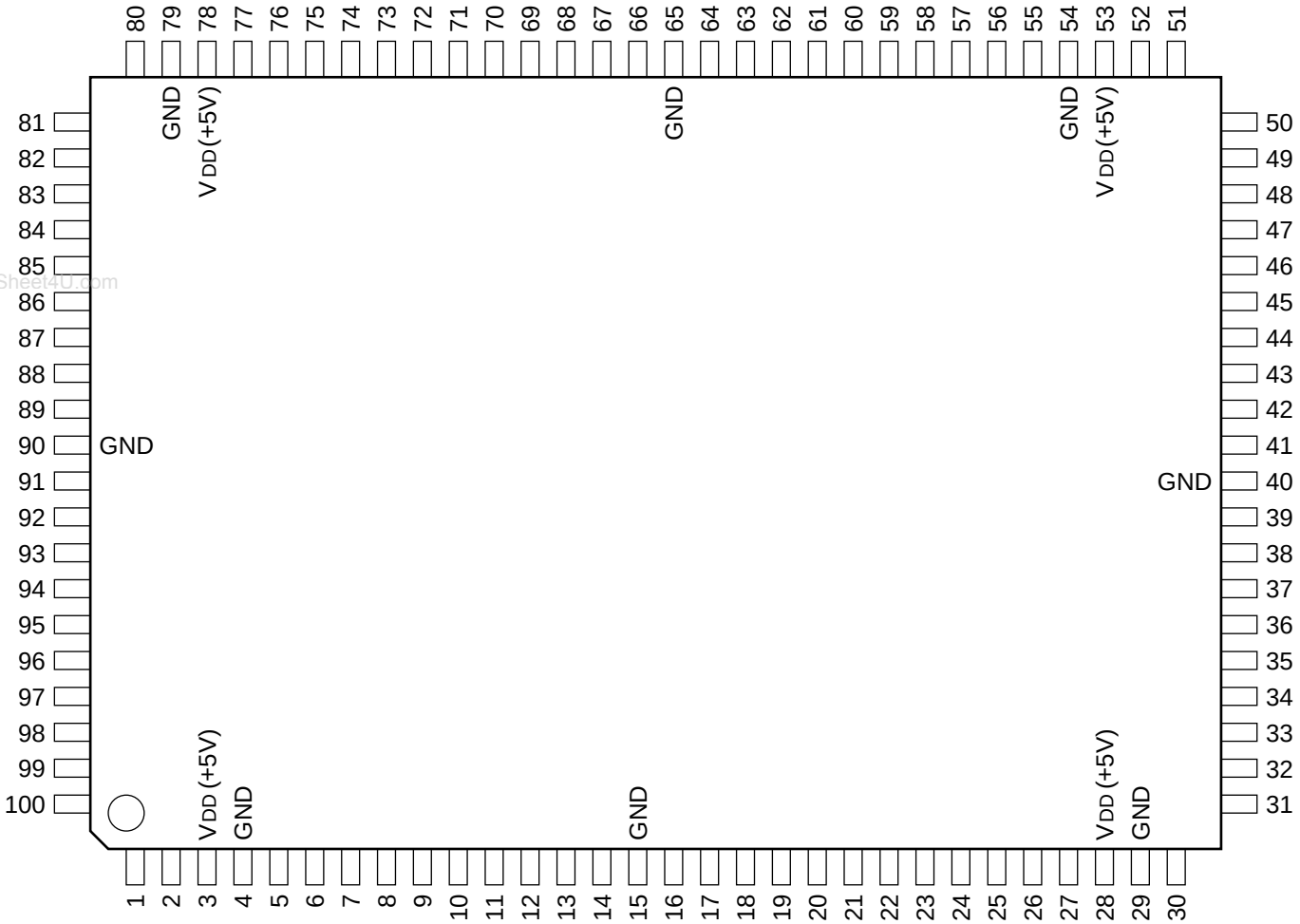
IL08

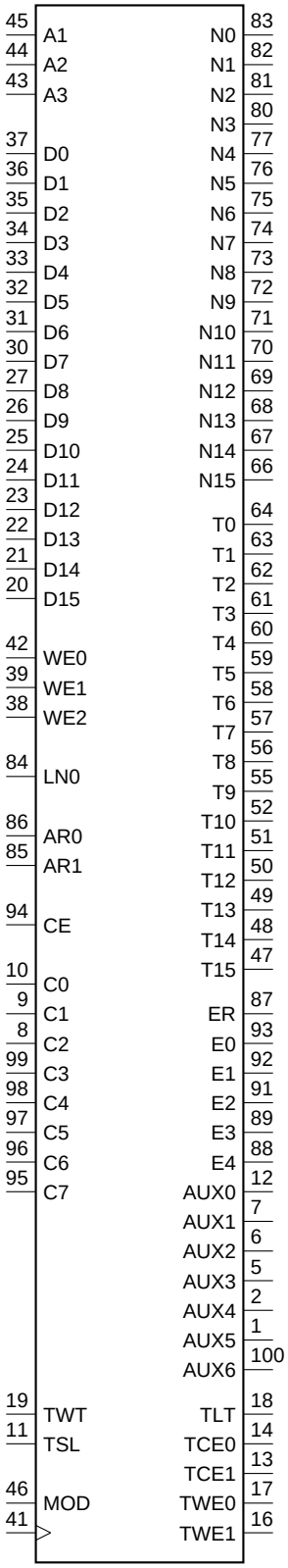
C-MOS ADDRESS ARITHMETIC PROCESSOR

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	AUX5	26	I	D9	51	O	T11	76	O	N5
2	O	AUX4	27	I	D8	52	O	T10	77	O	N4
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	AUX3	30	I	D7	55	O	T9	80	O	N3
6	O	AUX2	31	I	D6	56	O	T8	81	O	N2
7	O	AUX1	32	I	D5	57	O	T7	82	O	N1
8	I	C2	33	I	D4	58	O	T6	83	O	N0
9	I	C1	34	I	D3	59	O	T5	84	I	LN0
10	I	C0	35	I	D2	60	O	T4	85	I	AR1
11	I	TSL	36	I	D1	61	O	T3	86	I	AR0
12	O	AUX0	37	I	D0	62	O	T2	87	O	ER
13	O	TCE1	38	I	WE2	63	O	T1	88	O	E4
14	O	TCE0	39	I	WE1	64	O	T0	89	O	E3
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	TWE1	41	I	CK	66	O	N15	91	O	E2
17	O	TWE0	42	I	WE0	67	O	N14	92	O	E1
18	O	TLT	43	I	A3	68	O	N13	93	O	E0
19	I	TWT	44	I	A2	69	O	N12	94	I	CE
20	I	D15	45	I	A1	70	O	N11	95	I	C7
21	I	D14	46	I	MODE	71	O	N10	96	I	C6
22	I	D13	47	O	T15	72	O	N9	97	I	C5
23	I	D12	48	O	T14	73	O	N8	98	I	C4
24	I	D11	49	O	T13	74	O	N7	99	I	C3
25	I	D10	50	O	T12	75	O	N6	100	O	AUX6



INPUT

A1-A3	; ADDRESS
AR0, AR1	; FP (FRONT PROCESSOR) CONTROL SIGNAL (AREA) AT COMMAND INTERFACE MODE
C0-C7	; FP (FRONT PROCESSOR) CONTROL COMMAND AT COMMAND DIRECT MODE
CE	; FP (FRONT PROCESSOR) CONTROL COMMAND ENABLE
CK	; CLOCK
D0-D15	; DATA
LN0	; FP (FRONT PROCESSOR) CONTROL SIGNAL (LINE) AT COMMAND INTERFACE MODE
MODE	; OPERATING MODE SELECT
TSL	; TABLE RAM BANK SELECT
TWT	; TABLE RAM WRITE TRIGGER
WE0-WE2	; WRITE ENABLE

OUTPUT

AUX	; GENERAL PURPOSE REGISTER DATA
E0-E4	; EXPONENT PART DATA
ER	; ARITHMETIC STATUS
N0-N15	; N SYSTEM ARITHMETIC SIGNAL
T0-T15	; T SYSTEM ARITHMETIC SIGNAL
TCE0, TCE1	; TABLE RAM CHIP ENABLE
TLT	; TABLE RAM ADDRESS AND DATA BUS LACH
TWE0, TWE1	; TABLE RAM WRITE ENABLE