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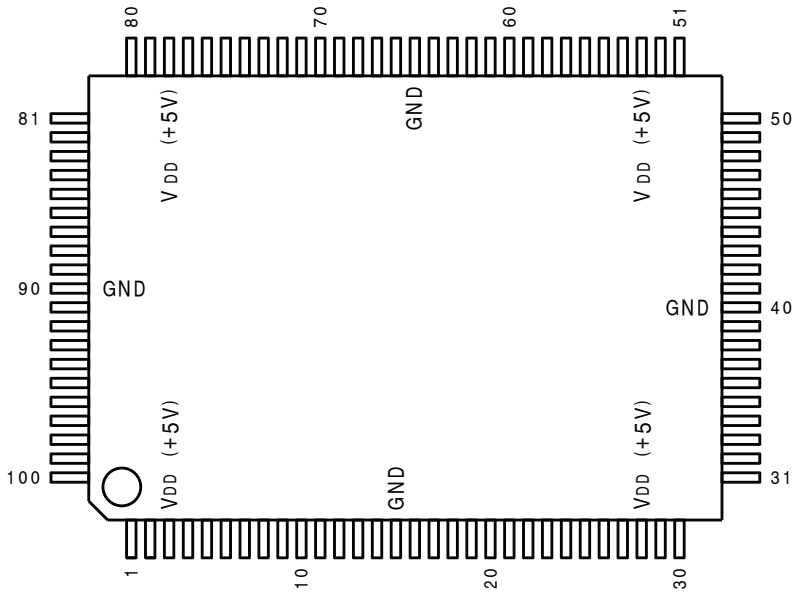
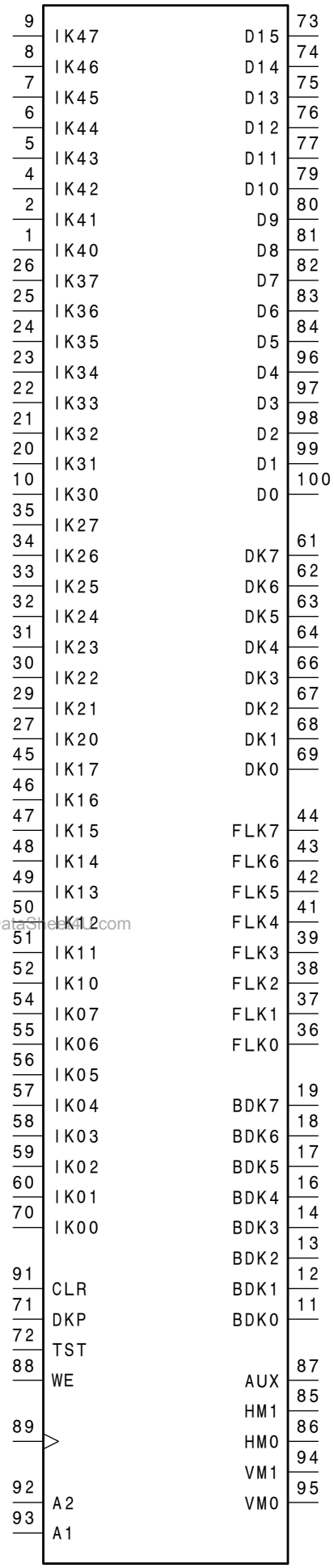
BOARDER PROCESSOR

-TOP VIEW-



(V_{DD}=+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	IK40	26	I	IK37	51	I	IK11	76	I	D12
2	I	IK41	27	I	IK20	52	I	IK10	77	I	D11
3	–	VDD	28	–	VDD	53	–	VDD	78	–	VDD
4	I	IK42	29	I	IK21	54	I	IK07	79	I	D10
5	I	IK43	30	I	IK22	55	I	IK06	80	I	D9
6	I	IK44	31	I	IK23	56	I	IK05	81	I	D8
7	I	IK45	32	I	IK24	57	I	IK04	82	I	D7
8	I	IK46	33	I	IK25	58	I	IKO3	83	I	D6
9	I	IK47	34	I	IK26	59	I	IKO2	84	I	D5
10	I	IK30	35	I	IK27	60	I	IKO1	85	O	HM1
11	O	BDK0	36	O	FLK0	61	O	DK7	86	O	HM0
12	O	BDK1	37	O	FLK1	62	O	DK6	87	O	AUX
13	O	BDK2	38	O	FLK2	63	O	DK5	88	I	WE
14	O	BDK3	39	O	FLK3	64	O	DK4	89	I	CLK
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	BDK4	41	O	FLK4	66	O	DK3	91	I	CLR
17	O	BDK5	42	O	FLK5	67	O	DK2	92	I	A2
18	O	BDK6	43	O	FLK6	68	O	DK1	93	I	A1
19	O	BDK7	44	O	FLK7	69	O	DK0	94	O	VM1
20	I	IK31	45	I	IK17	70	I	IK00	95	O	VM0
21	I	IK32	46	I	IK16	71	I	DKP	96	I	D4
22	I	IK33	47	I	IK15	72	I	TST	97	I	D3
23	I	IK34	48	I	IK14	73	I	D15	98	I	D2
24	I	IK35	49	I	IK13	74	I	D14	99	I	D1
25	I	IK36	50	I	IK12	75	I	D13	100	I	D0



INPUT

A1-A2	;ADDRESS (2 BIT)
CLK	;CLOCK
CLR	;CLEAR
DKP	;SELECT DK POLE
D0-D15	;DATA (16 BIT)
IK00-IK07	;INPUT KEY SIGNAL FOR 0H DELAY (8 BIT)
IK10-IK17	;INPUT KEY SIGNAL FOR 1H DELAY (8 BIT)
IK20-IK27	;INPUT KEY SIGNAL FOR 2H DELAY (8 BIT)
IK30-IK37	;INPUT KEY SIGNAL FOR 3H DELAY (8 BIT)
IK40-IK47	;INPUT KEY SIGNAL FOR 4H DELAY (8 BIT)
TST	;MULTIPLIER TEST
WE	;WRITE ENABLE

OUTPUT

AUX	;DISPLAY DATA OUTPUT ENABLE (1 BIT)
BDK0-BDK7	;BODER KEY SIGNAL (8 BIT)
DK0-DK7	;DOWN STREM KEY SIGNAL (8 BIT)
FLK0-FLK7	;FILLKEY SIGNAL (8 BIT)
HM0-HM1	;DIAPLAY HORIZONTAL MEMORY RESISTOR (2 BIT)
VM0-VM1	;DISPLAY VERTICAL MEMORY RESISTOR (2 BIT)