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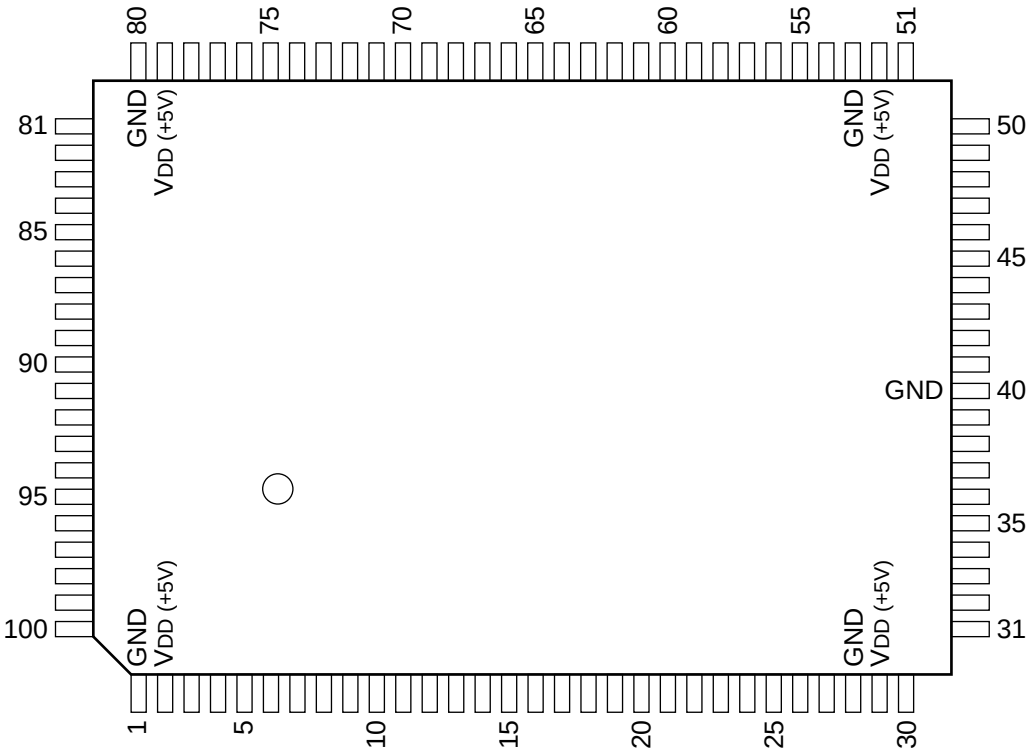
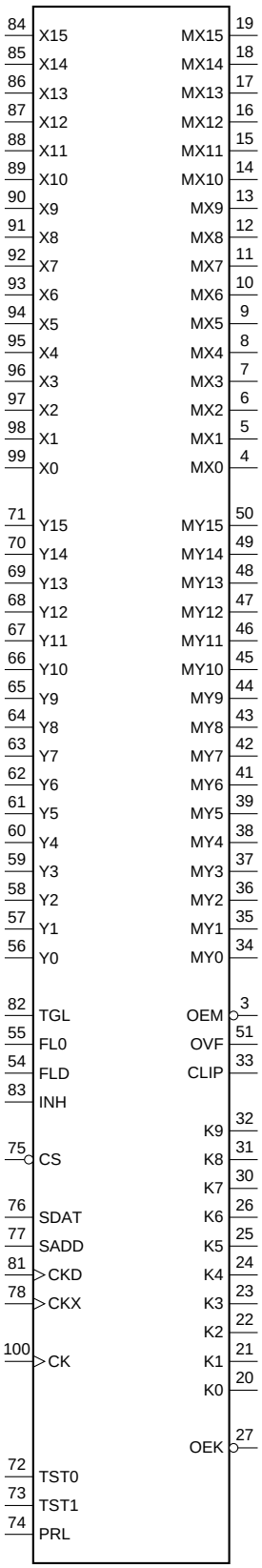
C-MOS ADDRESS-KEY SIGNAL GENERATOR

-TOP VIEW-



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	21	O	K1	41	O	MY6	61	I	Y5	81	I	CKD
2	—	VDD	22	O	K2	42	O	MY7	62	I	Y6	82	I	TGL
3	I	$\overline{OEM}$	23	O	K3	43	O	MY8	63	I	Y7	83	I	INH
4	O	MX0	24	O	K4	44	O	MY9	64	I	Y8	84	I	X15
5	O	MX1	25	O	K5	45	O	MY10	65	I	Y9	85	I	X14
6	O	MX2	26	O	K6	46	O	MY11	66	I	Y10	86	I	X13
7	O	MX3	27	I	$\overline{OEK}$	47	O	MY12	67	I	Y11	87	I	X12
8	O	MX4	28	—	GND	48	O	MY13	68	I	Y12	88	I	X11
9	O	MX5	29	—	VDD	49	O	MY14	69	I	Y13	89	I	X10
10	O	MX6	30	O	K7	50	O	MY15	70	I	Y14	90	I	X9
11	O	MX7	31	O	K8	51	O	OVF	71	I	Y15	91	I	X8
12	O	MX8	32	O	K9	52	—	VDD	72	I	TST0	92	I	X7
13	O	MX9	33	O	CLIP	53.	—	GND	73	I	TST1	93	I	X6
14	O	MX10	34	O	MY0	54	I	FLD	74	I	PRL	94	I	X5
15	O	MX11	35	O	MY1	55	I	FL0	75	I	$\overline{CS}$	95	I	X4
16	O	MX12	36	O	MY2	56	I	Y0	76	I	SDAT	96	I	X3
17	O	MX13	37	O	MY3	57	I	Y1	77	I	SADD	97	I	X2
18	O	MX14	38	O	MY4	58	I	Y2	78	I	CKX	98	I	X1
19	O	MX15	39	O	MY5	59	I	Y3	79	—	VDD	99	I	X0
20	O	K0	40	—	GND	60	I	Y4	80	—	GND	100	I	CK



INPUT

CK	;	SYSTEM CLOCK
CKD	;	SERIAL INTERFACE CLOCK
$\overline{CKX}$	;	SWITCHING TIMING PLUS
$\overline{CS}$	;	CHIP SELECT (LOW ACTIVE)
FLD, FL0	;	FIELD-OFFSET CONTROL FOR MY OUTPUT
$\overline{INH}$	;	SET ADDRESS-KEY TO 0 (HIGH TO 0)
$\overline{OEK}$	;	OUTPUT ENABLE OF ADDRESS-KEY (LOW ENABLE)
$\overline{OEM}$	;	OUTPUT ENABLE OF MX, MY OUTPUT (LOW ENABLE)
PRL	;	SET PARALLEL MODE FOR REGISTER
SADD	;	SERIAL ADDRESS
SDAT	;	SERIAL DATA
TGL	;	SWITCH INTERNAL REGISTER REG (0, 4) <=> REG (1, 5)
TST1, TST0	;	SET TEST MODE ((0, 0) FOR NORMAL)
X15 - X0	;	X ADDRESS
Y15 - Y0	;	Y ADDRESS

OUTPUT

CLIP	;	ADDRESS-KEY = 0 AREA FLAG
K9 - K0	;	ADDRESS-KEY SIGNAL
OVF	;	OVERFLOW FLAG
MX15 - MX0	;	X ADDRESS
MY15 - MY0	;	Y ADDRESS