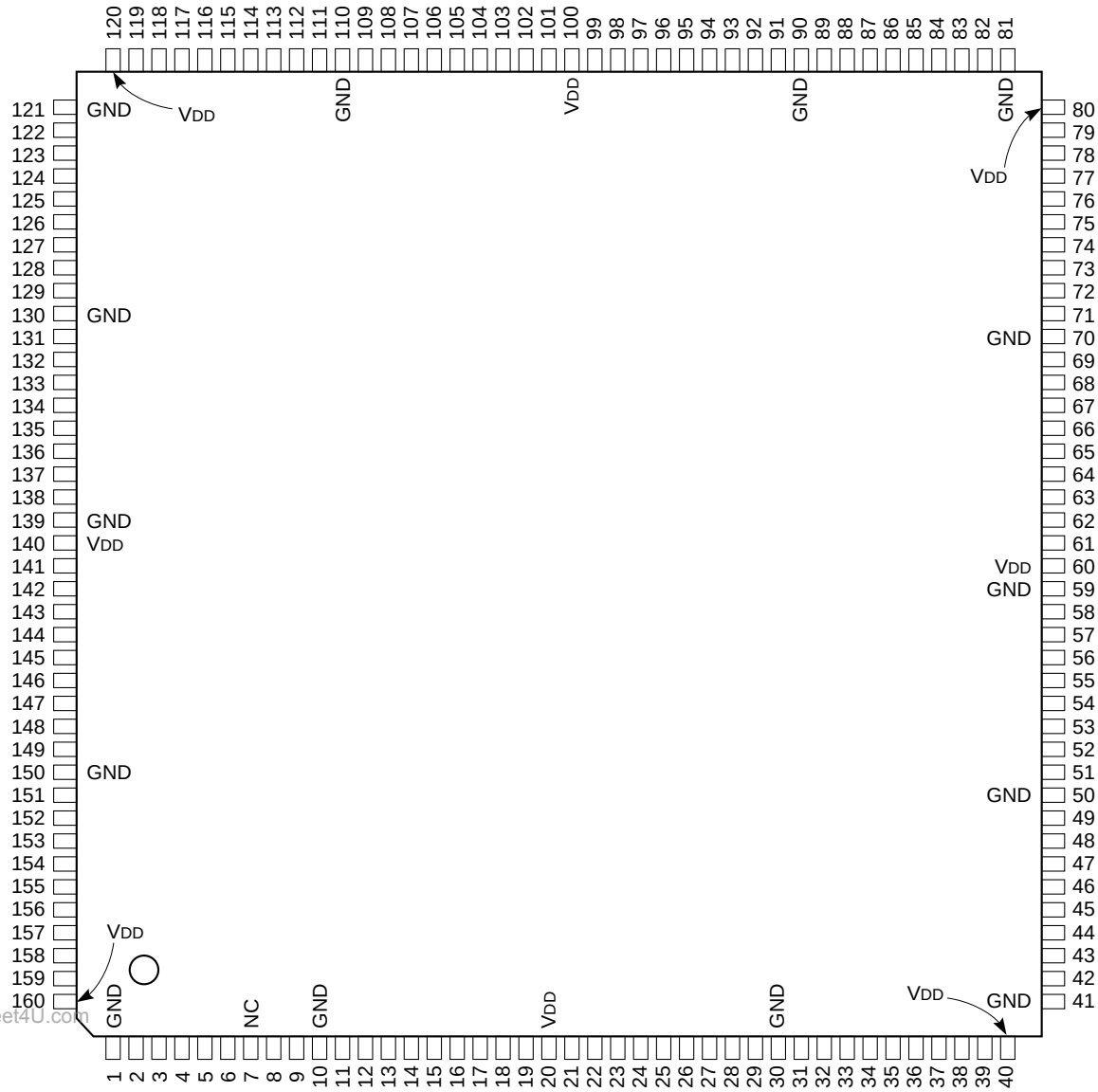
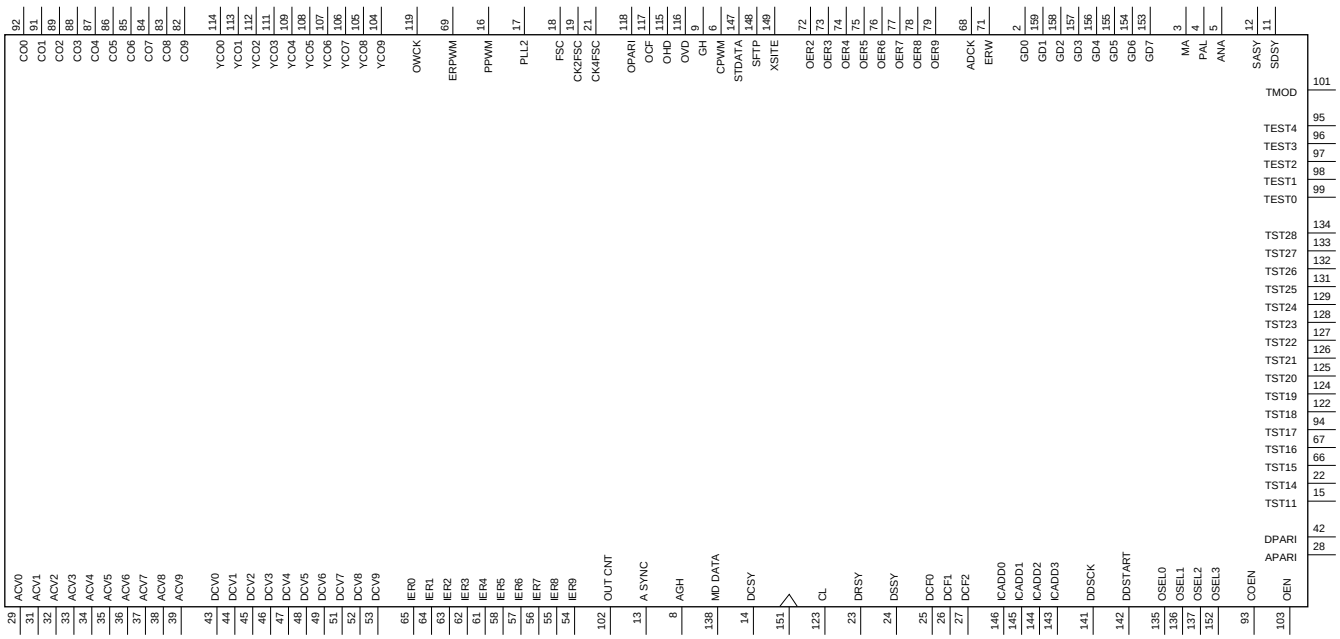
C-MOS DIGITAL VIDEO SIGNAL DECODER

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	41	—	GND	81	—	GND	121	—	GND
2	O	GD0	42	I	DPARI	82	O	CO9	122	I	TST18
3	O	MA	43	I	DCV0	83	O	CO8	123	I	CL
4	O	PAL	44	I	DCV1	84	O	CO7	124	I	TST19
5	O	ANA	45	I	DCV2	85	O	CO6	125	I	TST20
6	O	CPWM	46	I	DCV3	86	O	CO5	126	I	TST21
7	—	NC	47	I	DCV4	87	O	CO4	127	I	TST22
8	I	AGH	48	I	DCV5	88	O	CO3	128	I	TST23
9	O	GH	49	I	DCV6	89	O	CO2	129	I	TST24
10	—	GND	50	—	GND	90	—	GND	130	—	GND
11	O	SDSY	51	I	DCV7	91	O	CO1	131	I	TST25
12	O	SASY	52	I	DCV8	92	O	CO0	132	I	TST26
13	I	ASYNC	53	I	DCV9	93	I	COEN	133	I	TST27
14	I	DCSY	54	I	IER9	94	I	TST17	134	I	TST28
15	I	TST11	55	I	IER8	95	I	TEST4	135	I	OSEL0
16	O	PPWM	56	I	IER7	96	I	TEST3	136	I	OSEL1
17	O	PLL2	57	I	IER6	97	I	TEST2	137	I	OSEL2
18	O	FSC	58	I	IER5	98	I	TEST1	138	I	MDDATA
19	O	CK2FSC	59	—	GND	99	I	TEST0	139	—	GND
20	—	V_{DD}	60	—	V_{DD}	100	—	V_{DD}	140	—	V_{DD}
21	O	CK4FSC	61	I	IER4	101	I	TMOD	141	I	DD SCK
22	I	TST14	62	I	IER3	102	I	OUTCNT	142	I	DDSTART
23	I	DRSY	63	I	IER2	103	I	OEN	143	I	ICADD3
24	I	DSSY	64	I	IER1	104	O	YCO9	144	I	ICADD2
25	I	DCF0	65	I	IER0	105	O	YCO8	145	I	ICADD1
26	I	DCF1	66	I	TST15	106	O	YCO7	146	I	ICADD0
27	I	DCF2	67	I	TST16	107	O	YCO6	147	O	STDATA
28	I	APARI	68	O	ADCK	108	O	YCO5	148	O	SFTP
29	I	ACV0	69	O	ERPWM	109	O	YCO4	149	O	XSITE
30	—	GND	70	—	GND	110	—	GND	150	—	GND
31	I	ACV1	71	O	ERW	111	O	YCO3	151	I	CK
32	I	ACV2	72	O	OER2	112	O	YCO2	152	I	OSEL3
33	I	ACV3	73	O	OER3	113	O	YCO1	153	O	GD7
34	I	ACV4	74	O	OER4	114	O	YCO0	154	O	GD6
35	I	ACV5	75	O	OER5	115	O	OHD	155	O	GD5
36	I	ACV6	76	O	OER6	116	O	OVD	156	O	GD4
37	I	ACV7	77	O	OER7	117	O	OCF	157	O	GD3
38	I	ACV8	78	O	OER8	118	O	OPARI	158	O	GD2
39	I	ACV9	79	O	OER9	119	O	OWCK	159	O	GD1
40	—	V_{DD}	80	—	V_{DD}	120	—	V_{DD}	160	—	V_{DD}



INPUT

ACV0 - ACV9	:	ANALOG INPUT DATA (0 - 9)
AGH	:	ANALOG GATED H
APARI	:	PARITY OF ANALOG INPUT DATA
ASYNC	:	ANALOG COMPOSITE SYNC
CK	:	INPUT 8 fsc CK
CL	:	POWER ON RESET
COEN	:	CHROMA OUTPUT ENABLE
DCF0 - DCF2	:	D2 INPUT CF (0 - 2)
DCSY	:	DELAYED COMPOSITE SYNC
DCV0 - DCV9	:	DIGITAL INPUT DATA (0 - 9)
DDSCK	:	CK FOR SERIAL MODE DATA
DDSTART	:	START PULSE OF SERIAL COMMUNICATION
DPARI	:	PARITY OF DIGITAL INPUT DATA
DRSY	:	DIGITAL DELAYED SYNC ($\overline{8\ fsc} \times 8N$)
DSSY	:	DIGITAL DELAYED SYNC (8 fsc × 8N)
ICADD0 - ICADD3	:	IC ADDRESS (0 - 3)
IER0 - IER9	:	NON STANDARD PLL ERROR INPUT (0 - 9)
MDDATA	:	SERIAL MODE DATA FROM CPU
OEN	:	Y (Y/C) OUTPUT ENABLE
OSEL0 - OSEL3	:	TEST (0 - 3)
OUTCNT	:	OUTPUT CONTROL : Y/YC MULTIPLEX
TEST0 - TEST4	:	TEST (0 - 4)
TMOD	:	TEST MODE
TST11	:	TEST11
TST14 - TST28	:	TEST (14 - 28)

OUTPUT

ADCK	:	NON STANDARD PLL ERROR SAMPLING CK
ANA	:	ANALOG/DIGITAL
CK2FSC	:	INTERNAL 2 fsc CK
CK4FSC	:	INTERNAL 4 fsc CK
CO0 - CO9	:	CHROMA OUT (0 - 9)
CPWM	:	CLAMP ERROR PWM
ERPWM	:	NON STANDARD PLL ERROR SAMPLING PWM
ERW	:	NON STANDARD PLL ERROR WIDTH
FSC	:	INTERNAL fsc CK
GD0 - GD7	:	GAIN DATA (0 - 7)
GH	:	GATED H
MA	:	MANUAL/AUTO (AGC MODE)
OCF	:	CF INFORMATION
OER2 - OER9	:	NON STANDARD PLL ERROR OUTPUT (2 - 9)
OHD	:	HD
OPARI	:	PARITY OF OUTPUT DATA
OVD	:	VD
OWCK	:	PSEUDO 13.5 MHz/27 MHz
PAL	:	PAL/NTSC
PLL2	:	DIGITAL PLL FOR 2 fsc CK
PPWM	:	SAMPLING CK PLL ERROR PWM
SASY	:	ANALOG SYNC
SDSY	:	DIGITAL SYNC
SFTP	:	DIRECTION FOR SCH 0°
STDATA	:	SERIAL OUTPUT DATA TO CPU
XSITE	:	COMPONENT/COMPOSITE
YCO0 - YCO9	:	Y (Y/C) OUTPUT (0 - 9)