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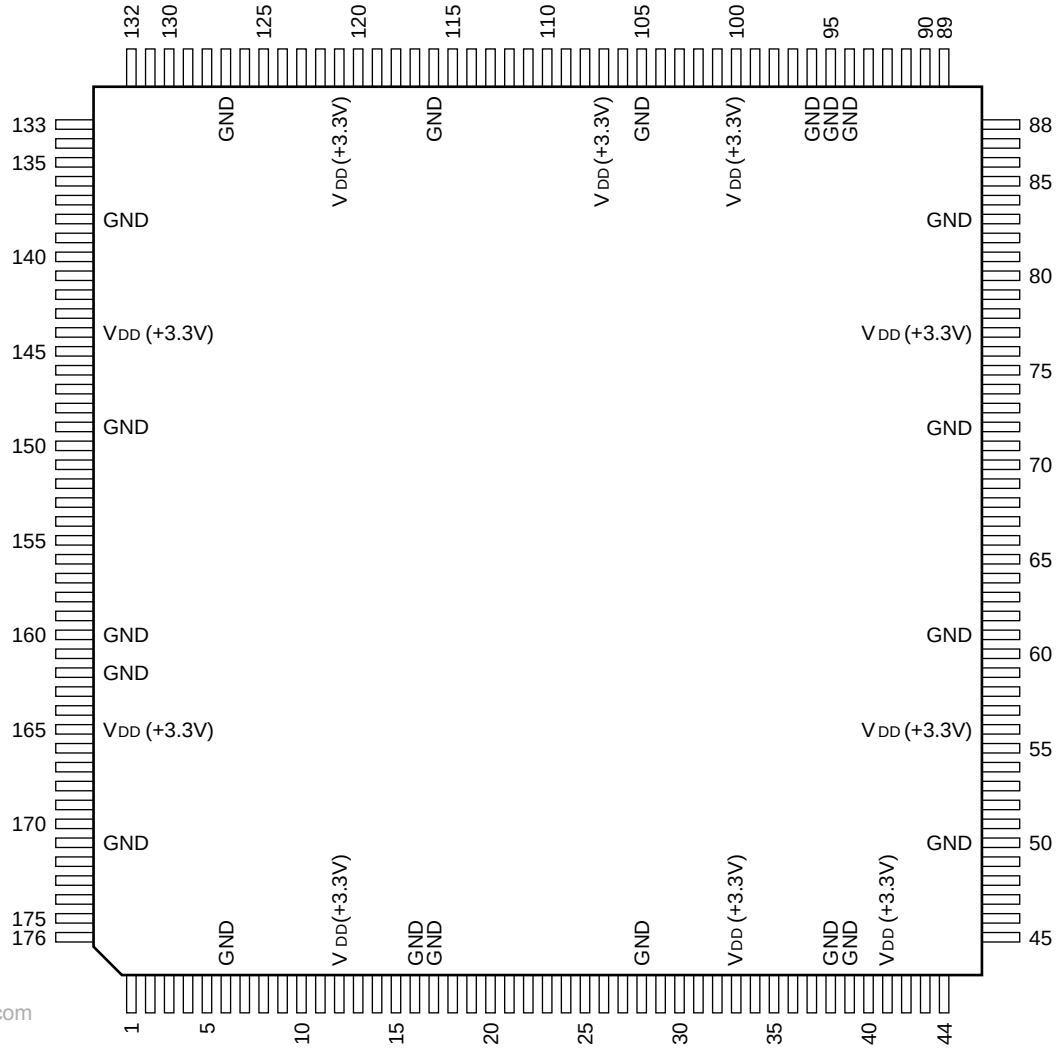
IL08

C-MOS OUTER ERROR CORRECTION DECODER

- TOP VIEW -



(V_{DD}=+3.3V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	F5PSO	45	I	AVSTI	89	I/O	TDI4	133	I/O	VDMIOA8
2	O	TDO8	46	I	ASYNCI	90	I/O	TDI3	134	I/O	VDMIOA7
3	O	TDO7	47	I	AUCHI	91	I/O	TDI2	135	I/O	VDMIOA6
4	O	TDO6	48	I	AUXSYI	92	I/O	TDI1	136	I/O	VDMIOA5
5	O	TDO5	49	I	FS5FI	93	I/O	TDI0	137	I/O	VDMIOA4
6	–	GND	50	–	GND	94	–	GND	138	–	GND
7	O	TDO4	51	I	VAIN8	95	–	GND	139	I/O	VDMIOA3
8	O	TDO3	52	I	VAIN7	96	–	GND	140	I/O	VDMIOA2
9	O	TDO2	53	I	VAIN6	97	O	VEOUT	141	I/O	VDMIOA1
10	O	TDO1	54	I	VAIN5	98	O	VDOUT7	142	I/O	VDMIOA0
11	O	TDO0	55	I	VAIN4	99	O	VDOUT6	143	O	$\overline{\text{VMDC}}$
12	–	V_{DD}	56	–	V_{DD}	100	–	V_{DD}	144	–	V_{DD}
13	I	REV	57	I	VAIN3	101	O	VDOUT5	145	O	$\overline{\text{VMWE}}$
14	I	JUMP	58	I	VAIN2	102	O	VDOUT4	146	I/O	VDMIOB8
15	I	F5MDI	59	I	VAIN1	103	O	VDOUT3	147	I/O	VDMIOB7
16	–	GND	60	I	VAIN0	104	O	VDOUT2	148	I/O	VDMIOB6
17	–	GND	61	–	GND	105	5	GND	149	–	GND
18	I/O	SYSIO7	62	I	VIN8	106	O	VDOUT1	150	I/O	VDMIOB5
19	I/O	SYSIO6	63	I	VIN7	107	–	V_{DD}	151	I/O	VDMIOB4
20	I/O	SYSIO5	64	I	VIN6	108	O	VDOUT0	152	I/O	VDMIOB3
21	I/O	SYSIO4	65	I	VIN5	109	O	VSYNCO	153	I/O	VDMIOB2
22	I/O	SYSIO3	66	I	VIN4	110	O	VPRTO	154	I/O	VDMIOB1
23	I/O	SYSIO2	67	I	VIN3	111	O	VMADD16A	155	I/O	VDMIOB0
24	I/O	SYSIO1	68	I	VIN2	112	O	VMADD16B	156	O	MON
25	I/O	SYSIO0	69	I	VIN1	113	O	VMADD15	157	O	ADOUT1
26	O	$\overline{\text{OBUSEN}}$	70	I	VIN0	114	O	VMADD14	158	O	ADOUT2
27	I	IBUSEN	71	I	MCK	115	O	VMADD13	159	O	AVSTO
28	–	GND	72	–	GND	116	–	GND	160	–	GND
29	I	STAT1	73	I	MCKP	117	O	VMADD12	161	I	FS128
30	I	STAT0	74	I	VVSTI	118	O	VMADD11	162	–	GND
31	I	STRB	75	I	VSYNCI	119	O	VMADD10	163	I	FS
32	I	SCS	76	I	VBLKI	120	O	VMADD9	164	I	TAI9
33	–	V_{DD}	77	–	V_{DD}	121	–	V_{DD}	165	–	V_{DD}
34	I	CHIPID1	78	I	VPRTI	122	O	VMADD8	166	I	TAI8
35	I	CHIPID0	79	I	$\overline{\text{SHUTTLE}}$	123	O	VMADD7	167	I	TAI7
36	I	$\overline{\text{CPTEST}}$	80	I	$\overline{\text{TRE}}$	124	O	VMADD6	168	I	TAI6
37	I	$\overline{\text{CPTSRB}}$	81	I	$\overline{\text{TWE}}$	125	O	VMADD5	169	I	TAI5
38	–	GND	82	I	$\overline{\text{XMM}}$	126	O	VMADD4	170	I	FS256
39	–	GND	83	–	GND	127	–	GND	171	–	GND
40	I	$\overline{\text{RESET}}$	84	I	$\overline{\text{TDIEN}}$	128	O	VMADD3	172	I	TAI4
41	–	V_{DD}	85	I/O	TDI8	129	O	VMADD2	173	I	TAI3
42	I	REFV	86	I/O	TDI7	130	O	VMADD1	174	I	TAI2
43	I	REFVP	87	I/O	TDI6	131	O	VMADD0	175	I	TAI1
44	I	APRTI	88	I/O	TDI5	132	O	VRE	176	I	TAI0

INPUT

APRTI	; AUDIO PARITY
ASYNCI	; AUDIO SYNC TIMMING
AUCHI	; AUDIO CHANNEL TIMMING
AUXSYI	; AUDIO AUX SYNC TIMMING
AVSTI	; AUDIO V SYNC TIMMING
CHIPID0, CHIPID1	; ID NUMBER
$\overline{\text{CPTEST}}$	; IC TEST MODE (NORMAL "1")
$\overline{\text{CPTSRB}}$	; TEST MODE SETTING TIMMING
F5MDI	; 5 FILD SEQUENCE TREATMENT MODE
FS128	; AUDIO SAMPLING FREQUENCY 128 CLOCK
FS256	; AUDIO SAMPLING FREQUENCY 256 CLOCK
FS5FI	; 5 FILD TIMMING
FS	; AUDIO SAMPLING FREQUENCY CLOCK
IBUSEN	; SYSIO0–SYSIO7 TEMINAL I/O CONTROL
JUMP	; DT JUMP TIMMING (NORMAL "1")
MCK	; CLOCK
MCKP	; PROGRAM PLAY CLOCK
REFV	; VIDEO REFERENCE V SYNC SIGNAL
REFVP	; VIDEO REFERENCE V SYNC SIGNAL (PROGRAM PLAY)
$\overline{\text{RESET}}$	; RESET
REV	; REVERSE PLAYBACK MODE (NORMAL PLAY "1")
SCS	; SYSTEM CONTROL CLOCK SELECT
SHUTTLE	; OUTSIDE MEMORY WRITE ENABLE
STAT0, STAT1	; SYSIO0–SYSIO7 SIGNAL DATA ATTRIBUTE DISTINCTION
STRB	; SYSTEM CONTROL CLOCK
TAI0–TAI9	; TEST DATA
TDIEN	; OUTSIDE MEMORY ADDRESS LINE
TRE	; INSIDE MEMORY READ ENABLE
TWE	; INSIDE MEMORY WRITE ENABLE
VAIN0–VAIN8	; VIDEO B/D ch DATA + AUDIO DATA
VBLKI	; VIDEO BLOCK TIMMING
VIN0–VIN8	; VIDEO A/C ch DATA
VPRTI	; VIDEO PARITY
VSYNCI	; VIDEO TIMMING
VVSTI	; VIDEO V SYNC TIMMING
XMM	; OUTSIDE MEMORY ADDRESS LINE

OUTPUT

ADOUT0, ADOUT1	; AUDIO DATA CH3/CH4, CH1/CH2
AVSTO	; AUDIO TIMMING SIGNAL
F5PSO	; 5 FILD TIMMING PULS
MON	; VIDEO OUTPUT TIMMING MONITOR
$\overline{\text{OBUSEN}}$	; SYSIO0–SYSIO7 TERMINAL I/O CONTROL
TDO0–TDO8	; TEST DATA
VDOUT0–VDOUT7	; VIDEO DATA
VEOUT	; VIDEO ERROR FLAG
VMADD0–VMADD15	; OUTSIDE MEMORY ADDRESS LINE
VMADD16A, 16B	; OUTSID MEMORY (A), (B) ADDRESS LINE
$\overline{\text{VMDC}}$	; OUTSIDE MEMORY CONTROL SIGNAL
$\overline{\text{VMWE}}$	; OUTSIDE MEMORY WRITE TIMMING
VPRITO	; VIDEO PARITY
VRE	; OUTSIDE MEMORY READ ENABLE
VSYNCO	; VIDEO SYNC TIMMING

INPUT/OUTPUT

SYSIO0–SYSIO7	; SYSTEM CONTROL SIGNAL DATA
TDI0–TDI8	; TEST DATA
VDMIOA0–VDMIOA8	; OUTSIDE MEMORY (A) DATA
VDMIOB0–VDMIOB8	; OUTSIDE MEMORY (B) DATA