SONY

CXD3500R

Timing Generator for LCD Panels

Description

The CXD3500R is a timing signal generator for driving the LCD panels of Sony data projectors. This chip has a built-in serial interface circuit which supports various SXGA (skip scan display), XGA, SVGA and VGA signals, and (double speed) NTSC and PAL signals through external control from a microcomputer, etc.

Direct drive of LCD panels is possible using 5V drive.

Features

- Generates the drive pulses for the LCD panels of Sony high-temperature polycrystalline silicon TFT data projectors.
- Supports various SXGA, XGA, SVGA and VGA signals.
- Programmable output signals allow the optimal pulse output settings for each panel.
- Programmable skip scan display allows skip scan display of various signals (SXGA → XGA, XGA → SVGA, Macintosh16 → SVGA, etc.)
- Supports NTSC and PAL signals with line double-speed display using a built-in double-speed controller. (clock frequency: 36MHz or less) (Line memory: µPD485505: NEC)
- Allows control of sample-and-hold position of CXA2112R sample-and-hold driver.
- Supports up/down inversion and/or right/left inversion.
- Supports line inversion and field inversion.
- AC drive of LCD panels during no signal

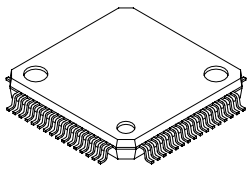
Applications

LCD projectors, etc.

Structure

Silicon gate CMOS IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

• Supply voltage	V_{DD}	Vss – 0.5 to +7.0	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

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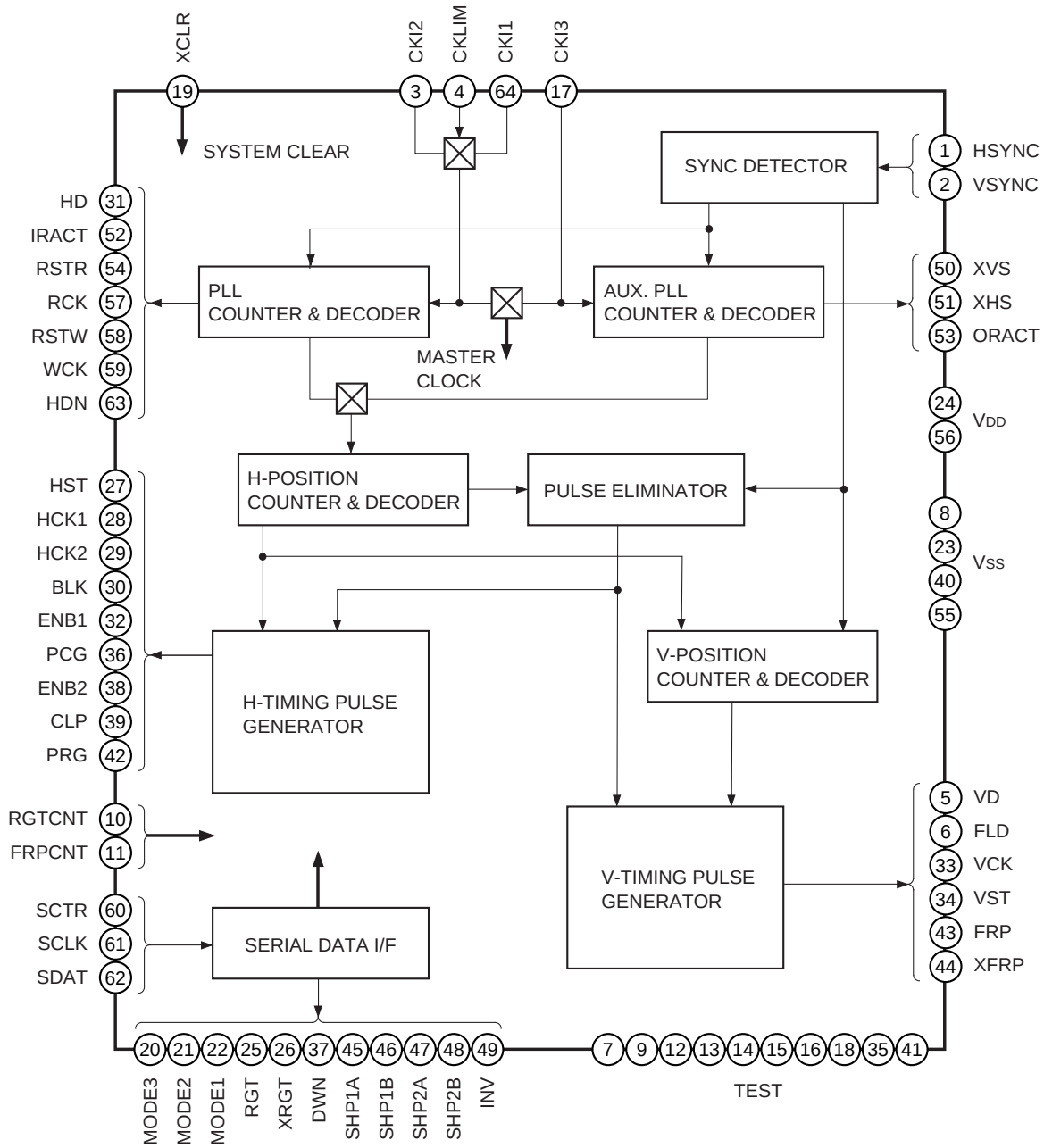
E99112-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	HSYNC	I	Horizontal sync signal input	—
2	VSYNC	I	Vertical sync signal input	—
3	CKI2	I/O	Clock 2 input (Small signal: Vth = V_{DD}/2, min. Vp-p = 0.5V)	—
4	CKLIM	I	Clock input selector (CKI1 selected when open.)	H
5	VD	O	VD pulse output	—
6	FLD	I/O	FLD pulse I/O	—
7	TEST0	—	Test (Not connected.)	—
8	V_{SS}0	—	GND	—
9	TEST1	—	Test (Not connected.)	—
10	RGTCNT	I	Right/left inversion external control	—
11	FRPCNT	I	FRP pulse inversion external control	H
12	TEST2	—	Test (Not connected.)	—
13	TEST3	—	Test (Not connected.)	—
14	TEST4	—	Test (Not connected.)	—
15	TEST5	—	Test (Not connected.)	—
16	TEST6	—	Test (Connect to GND.)	—
17	CKI3	I	Clock 3 input (for LAP)	—
18	TEST7	—	Test (Not connected.)	H
19	XCLR	I	System clear (L: set to SVGA 60Hz)	H
20	MODE3	O	Parallel Out 3 output (Panel mode switching 3 output)	—
21	MODE2	O	Parallel Out 2 output (Panel mode switching 2 output)	—
22	MODE1	O	Parallel Out 1 output (Panel mode switching 1 output)	—
23	V_{SS}1	—	GND	—
24	V_{DD}0	—	V_{DD}	—
25	RGT	O	Right/left inversion discrimination signal output (H: Normal, L: Reverse)	—
26	XRGT	O	Right/left inversion discrimination signal output (reverse polarity of RGT)	—
27	HST	O	Horizontal display start pulse output	—
28	HCK1	O	Horizontal display clock pulse output	—
29	HCK2	O	Horizontal display clock pulse output	—
30	BLK	O	BLK pulse output	—
31	HD	O	HD pulse output	—
32	ENB1	O	ENB1 pulse output	—
33	VCK	O	Vertical display clock pulse output	—

* H: Pull up

Pin No.	Symbol	I/O	Description	Input pin for open status
34	VST	O	Vertical display start pulse output	—
35	TEST8	—	Test (Not connected.)	—
36	PCG	O	Precharge timing pulse output	—
37	DWN	O	Up/down inversion discrimination signal output (H: Down, L: Up)	—
38	ENB2	O	ENB2 pulse output	—
39	CLP	O	Pedestal clamp pulse output for CXA2112R	—
40	$V_{SS}2$	—	GND	—
41	TEST9	—	Test (Not connected.)	—
42	PRG	O	Precharge signal pulse output	—
43	FRP	O	AC drive inversion timing output	—
44	XFRP	O	AC drive inversion timing output (reverse polarity of FRP)	—
45	SHP1A	O	External sample-and-hold driver control signal (for CXA2112R)	—
46	SHP1B	O	External sample-and-hold driver control signal (for CXA2112R)	—
47	SHP2A	O	External sample-and-hold driver control signal (for CXA2112R)	—
48	SHP2B	O	External sample-and-hold driver control signal (for CXA2112R)	—
49	INV	O	External sample-and-hold driver control signal (for CXA2112R)	—
50	XVS	O	Vertical auxiliary pulse output	—
51	XHS	O	Horizontal auxiliary pulse output	—
52	IRACT	O	LAP control pulse output	—
53	ORACT	O	LAP control pulse output	—
54	RSTR	O	Reset read output (for high-speed line buffer)	—
55	$V_{SS}3$	—	GND	—
56	$V_{DD}1$	—	V_{DD}	—
57	RCK	O	Read clock output (for high-speed line buffer)	—
58	RSTW	O	Reset write output (for high-speed line buffer)	—
59	WCK	O	Write clock output (for high-speed line buffer)	—
60	SCTR	I	Chip select input (serial transfer block)	—
61	SCLK	I	Serial clock input (serial transfer block)	—
62	SDAT	I	Serial data input (serial transfer block)	—
63	HDN	O	Phase comparator pulse output	—
64	CKI1	I	Clock 1 input (TTL)	—

* H: Pull up

Electrical Characteristics

1. DC characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
Input, output voltages	V_I, V_O		V_{SS}		V_{DD}	V	
Input voltage 1	V_{IH}	TTL input	2.2			V	CKI1
	V_{IL}				0.8		
Logical threshold value	Vth	Small amplitude input		V_{DD}/2		V	CKI2
Input voltage 2	V_{IH}		0.7V_{DD}				
	V_{IL}				0.3V_{DD}		
Input amplitude	V_{IN}	50MHz sine wave	0.5			Vp-p	
Feedback resistor	R_{FB}	V_{IN} = Vss or V_{DD}	250k	1M	2.5M	Ω	
Input voltage 3	V_{IH}	CMOS input	0.7V_{DD}			V	*1
	V_{IL}				0.3V_{DD}		
Input voltage 4	V_{T+}	TTL Schmitt trigger input	2.2			V	HSYNC, VSYNC, SCTR, SCLK, SDAT
	V_{T-}				0.8		
	$V_{T+} – V_{T-}$			0.4			
Output voltage 1	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	*2
	V_{OL}	I_{OL} = 4mA			0.4		
Output voltage 2	V_{OH}	I_{OH} = –6mA	V_{DD} – 0.8			V	*3
	V_{OL}	I_{OL} = 4mA			0.4		
Output voltage 3	V_{OH}	I_{OH} = –8mA	V_{DD} – 0.8			V	*4
	V_{OL}	I_{OL} = 8mA			0.4		
Input leak current	I_I	*5	–10		10	µA	*6
	I_{IL}	*7	–40	–100	–240		*8
	I_I	*9	–40		40		FLD
Output leak current	I_{OZ}	*10	–40		40	µA	SHP1A, SHP2A
Current consumption	I_{DD}	*11		58		mA	At a 30pF load

*1 CKLIM, RGTCNT, FRPCNT, CKI3, TEST7, XCLR
*2 MODE1, MODE2, MODE3, RGT, XRGT, DWN, SHP1B, SHP2B, INV
*3 VD, BLK, HD, ENB1, ENB2, VCK, VST, PCG, CLP, PRG, FRP, XFRP, XVS, XHS, IRACT, ORACT, HDN
*4 HST, HCK1, HCK2, RSTR, RCK, RSTW, WCK
*5 Normal input pins (V_{IN} = Vss or V_{DD})
*6 HSYNC, VSYNC, RGTCNT, CKI3, SCTR, SCLK, SDAT, CKI1
*7 Pins with pull-up resistors (V_{IN} = Vss)
*8 CKLIM, FRPCNT, TEST7, XCLR
*9 Bidirectional pins (V_{IN} = Vss or V_{DD})
*10 Tri-state (at high impedance, V_{IN} = Vss or V_{DD})
*11 V_{DD} = 5.0V, 55MHz input (actual measurement)

2. AC characteristics (V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Applicable pins	Min.	Typ.	Max.	Conditions	Unit
Clock input cycle		CKI1	18.2				ns
		CKI2	18.2				
Output rise time	tr	All outputs			20	CL = 30pF	
Output fall time	tf	All outputs			20		
Cross-point time difference	Δt	HCK1, 2	–10		10		
HCK1 Duty	$t_H/(t_H + t_L)$	HCK1	48		52		%
HCK2 Duty	$t_L/(t_H + t_L)$	HCK2	48		52		

Note) The minimum value for the clock input cycle (CKI1) when using the built-in double-speed controller is 27ns.

3. Serial transfer AC characteristics (V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Symbol	Item	Min.	Typ.	Max.
t_{s0}	SCTR setup time with respect to rise of SCLK	4Tns		
t_{s1}	SDAT setup time with respect to rise of SCLK	2Tns		
t_{h0}	SCTR hold time with respect to rise of SCLK	4Tns		
t_{h1}	SDAT hold time with respect to rise of SCLK	2Tns		
t_{w1L}	SCLK L level pulse width	2Tns		
t_{w1H}	SCLK H level pulse width	2Tns		
t_{w2}		5Tns		
t_{w3}		5Tns		

T: Input clock cycle

Note) Consider the frequency at free running (no signal). When the above characteristic specification is not satisfied at free running, IC operation including serial transfer is not guaranteed.

4. External clock input AC characteristics (V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
t_{s0}	HSYNC setup time with respect to rise of CKI1	SLCK*1: H CKPOL*2: H SLRS*3: L	4			ns
t_{h0}	HSYNC hold time with respect to rise of CKI1		7			
t_{s0}	HSYNC setup time with respect to rise of CKI2		2			
t_{h0}	HSYNC hold time with respect to rise of CKI2		9			
t_{wL}/t_{wH}	CKI1,2 L/H level pulse width		6	T/2		
t_{s0}	HSYNC setup time with respect to rise of CKI1	SLCK*1: L CKPOL*2: H	0			
t_{h0}	HSYNC hold time with respect to rise of CKI1		6			
t_{s0}	HSYNC setup time with respect to rise of CKI2		0			
t_{h0}	HSYNC hold time with respect to rise of CKI2		8			
t_{wL}/t_{wH}	CKI1,2 L/H level pulse width		40	50	60	%

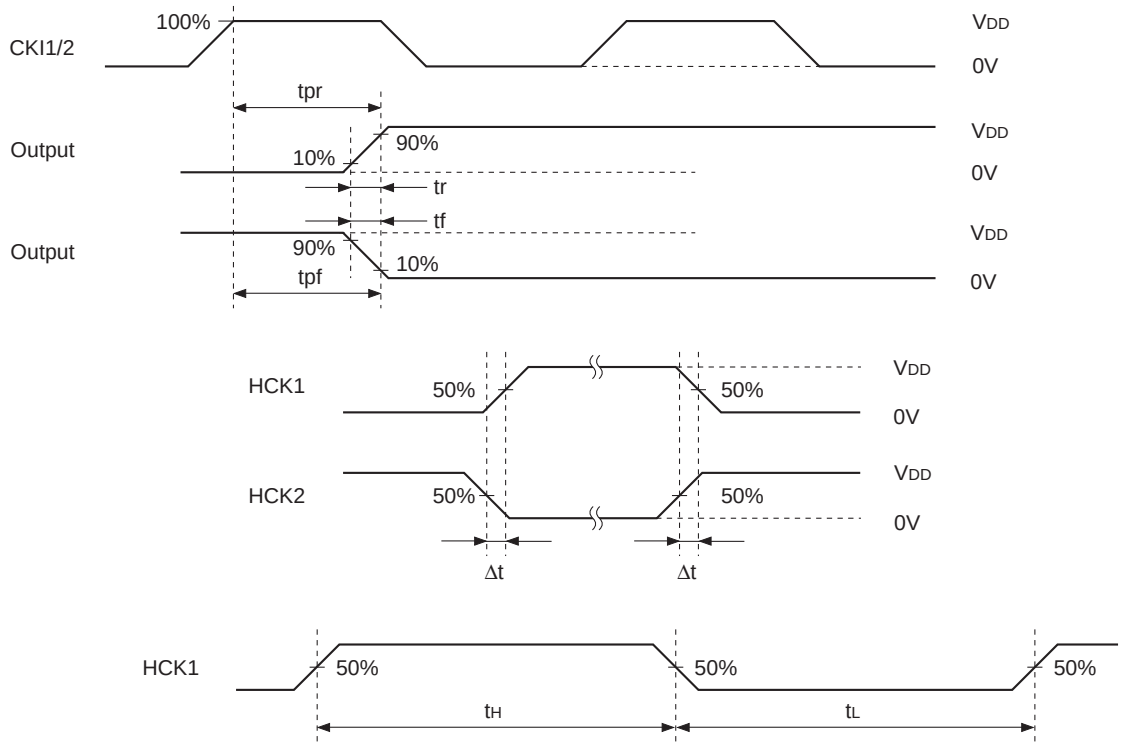
*1, 2, 3: Serial data Add. 0A

T: Input clock cycle

Note) During external clock input, set serial data HR to L. The pulse synchronized to the horizontal sync signal is generated by detecting the front edge of the horizontal sync signal and then resetting the internal PLL counter.

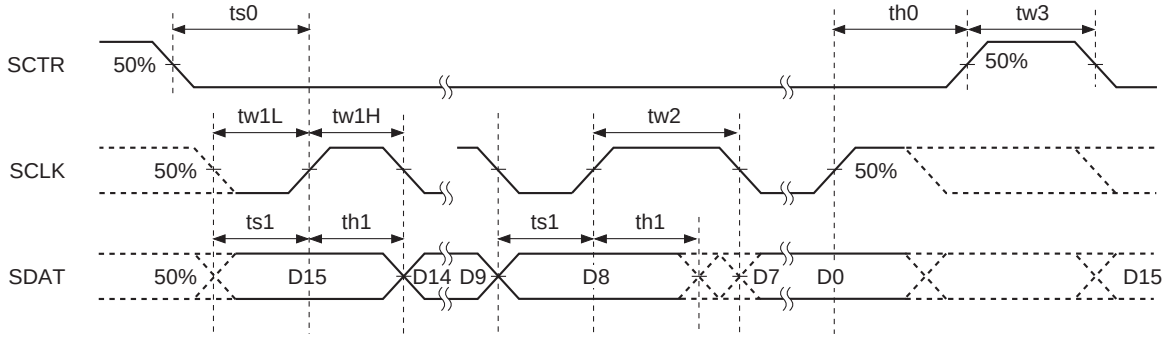
5. Timing definitions

AC characteristics



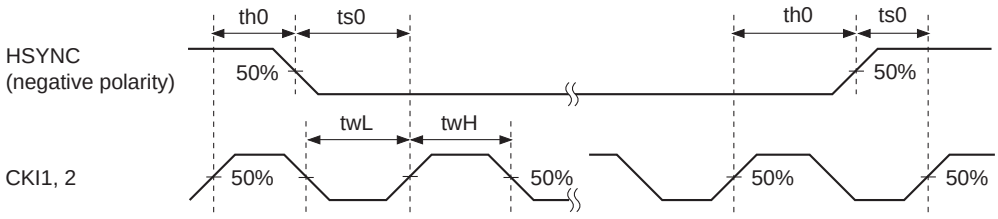
Note) HCK2 is the reverse phase of HCK1.

Serial transfer AC characteristics



Note) See "Serial transfer timing" on page 11 for the timing relationship between D15 to D0 and each pulse.

External clock input AC characteristics



Input Signal Protocol

1. Horizontal sync signal

a) A standard signal (HSYNC) should be input for each mode.
However, since the CXD3500R requires a double-speed signal as input during NTSC/PAL double-speed display when not using the built-in double-speed controller, the input specifications at that time are similar to those for normal data type sync signals, and there should not be a 1/2 offset with respect to the vertical sync signal.

b) The input sync signal polarity is not fixed, and is set by the serial data (HPOL).

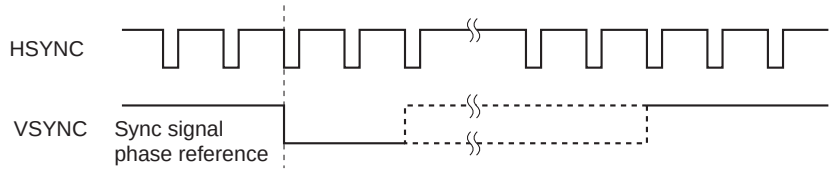
2. Vertical sync signal

a) A sync-separated, normal-speed VSYNC should be input as the vertical sync signal.

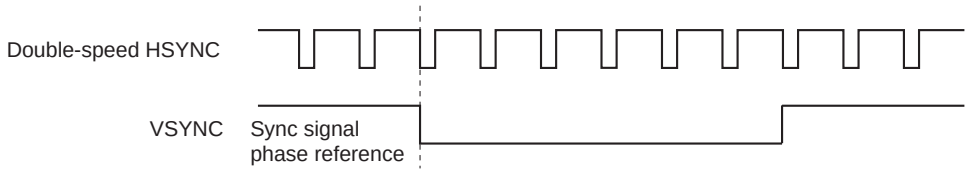
b) The input sync signal polarity is not fixed, and is set by the serial data (VPOL).

c) The phase relationship between HSYNC and VSYNC is specified as follows for the CXD3500R.

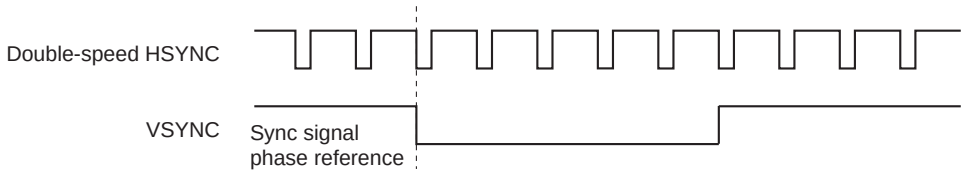
(1) XGA, Macintosh16, SVGA, VGA, PC-98



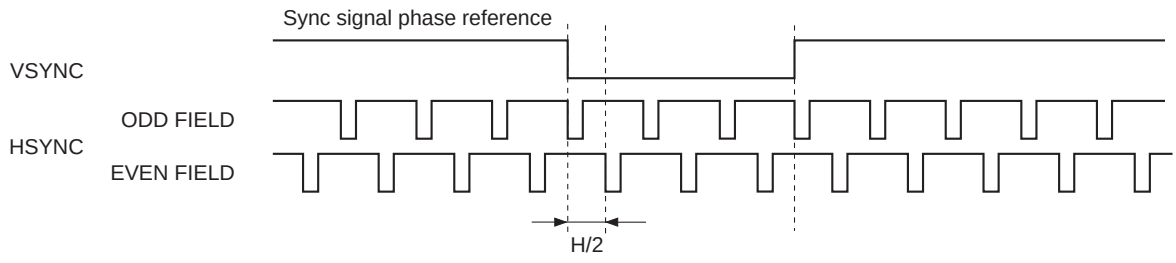
(2) Double-speed NTSC



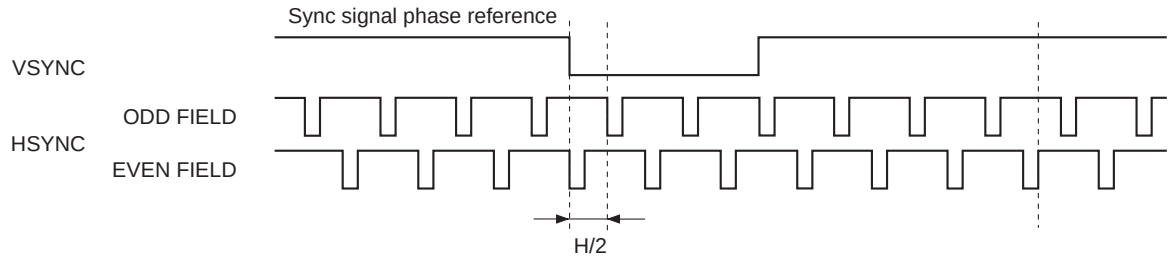
(3) Double-speed PAL



(4) NTSC



(5) PAL



Notes) (2) and (3) show the timing when supporting input of double-speed signals.
(4) and (5) show the timing when using the built-in double-speed controller (CXD3500R) and a line memory (µPD485505: NEC)

Description of Operation

Sync signal input

The HSYNC and VSYNC input pins support separate SYNC only. When using a composite SYNC input, perform sync separation using a separate sync separation IC, etc.

Clock input

(1) CKI1 and 2 pins

CKI1 and 2 are the clock input pins from an external PLL IC. CKI1 is TTL level input, and CKI2 is small amplitude clock input. Internal operation is performed at 1/2 clock, so the CXD3500R has a built-in frequency divider which halves the input master clock, and can select this halved clock or a 1/2 clock input from an external source by the serial interface setting. However, the input clock should be 55MHz or less, so when using a master clock of more than 55MHz, input the 1/2 clock.

The 1/N frequency divider output for the PLL IC is output from the HDN pin. The HDN polarity at this time is set by serial data HDNPOL.

(2) CKI3 pin

CKI3 is the clock input pin when using a scan converter that operates with the input sync signals and an asynchronous clock in the system. Since two types of clock are input in this case, the circuits that basically operate with the respective clocks of CKI1 and CKI2 are asynchronous. The input clock should be 55MHz or less. For details, see the explanation of pulse setting for the scan converter in this data sheet (starting on page 34).

AC driving of LCD panels for no signal

The following measures have been adopted to allow AC driving of LCD panels even when there is no signal. However, master clock CKI1 or CKI2 must be input even during free running.

Note that the recommended PLL IC CXA3106(A)Q does not output the clock when there is no HSYNC input.

Horizontal direction pulse

The PLL is set to free running status. Therefore, the frequency of the horizontal direction pulse is dependent on the PLL free-running frequency.

Vertical direction pulse

The number of lines is counted by an internal counter and the vertical direction pulses (VST, FRP) are output at a specified cycle. For the CXD3500R, no signal (free running) status is judged if there is no VSYNC input for longer than the following periods (free running detection timing).

PLSSL2, 1, 0	V cycle for no signal	Free running detection
L L L or L L H	701H	700H
L H L to H L L	1001H	1000H
H L H to H H H	1301H	1300H

XCLR pin

The CXD3500R should be forcibly reset during power on in order to initialize the serial transfer block and other internal circuits. At this time, the serial interface circuit is reset to the initial status (preset status). See page 38 for the preset settings.

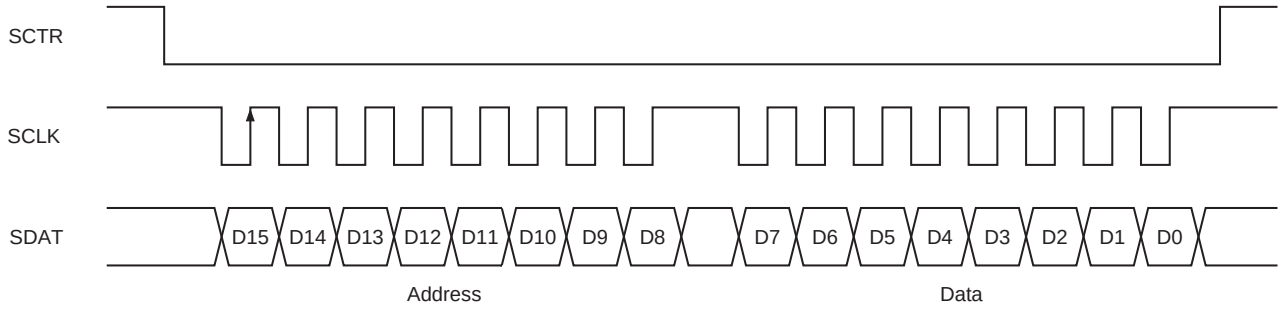
Serial transfer operation

1. Control method

The CXD3500R operation timing is controlled by serial data.

The control data is comprised of an 8-bit address and 8-bit data, and the individual data is loaded at the rise of SCLK. This loading operation starts from the fall of SCTR and is completed at the next rise of SCTR.

Serial transfer timing



2. Control data

When using the CXD3500R, set the control data corresponding to each LCD panel and video signal according to the formats in the table below.

Address								Data							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	PLLP11	PLLP10	PLLP9	PLLP8	PLLP7	PLLP6	PLLP5	PLLP4
0	0	0	0	0	0	0	1	PLLP3	PLLP2	PLLP1	PLLP0	HP11	HP10	HP9	HP8
0	0	0	0	0	0	1	0	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
0	0	0	0	0	0	1	1	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
0	0	0	0	0	1	0	0	HSTW1	HSTW0	HSTP5	HSTP4	HSTP3	HSTP2	HSTP1	HSTP0
0	0	0	0	0	1	0	1	PCGU2	PCGU1	PCGU0	PCGD4	PCGD3	PCGD2	PCGD1	PCGD0
0	0	0	0	0	1	1	0	—	—	—	PRGD4	PRGD3	PRGD2	PRGD1	PRGD0
0	0	0	0	0	1	1	1	set 0	PCG	FRP1	FRP0	FRPP3	FRPP2	FRPP1	FRPP0
0	0	0	0	1	0	0	0	VSTFX	HCKFX	HCKM	INV	SHP3	SHP2	SHP1	SHP0
0	0	0	0	1	0	0	1	VSTPOL	HCKPOL	VPOL	HPOL	HDNPOL	CLPPOL	CLPW	CLPP
0	0	0	0	1	0	1	0	SLCNT	SLFLD	SLRS	CKPOL	SLCK	PLSSL2	PLSSL1	PLSSL0
0	0	0	0	1	0	1	1	BLKON	BLKPOL	FMBK	MBKA4	MBKA3	MBKA2	MBKA1	MBKA0
0	0	0	0	1	1	0	0	MBKZ3	MBKZ2	MBKZ1	MBKZ0	MBKB3	MBKB2	MBKB1	MBKB0
0	0	0	0	1	1	0	1	VGAV	HR	DWN	RGT	DSP	PO/MODE3	PO/MODE2	PO/MODE1
0	0	0	0	1	1	1	0	XGBK	HDON	HAXON	VAXON	set 0	set 0	set 0	SPON
0	0	0	0	1	1	1	1	—	—	—	—	—	—	set 0	set 0
0	0	0	1	0	0	0	0	SLLAP	LPCK	SLCKL	ORRS4	ORRS3	ORRS2	ORRS1	ORRS0
0	0	0	1	0	0	0	1	IRD11	IRD10	IRD9	IRD8	IRD7	IRD6	IRD5	IRD4
0	0	0	1	0	0	1	0	IRD3	IRD2	IRD1	IRD0	IRU11	IRU10	IRU9	IRU8
0	0	0	1	0	0	1	1	IRU7	IRU6	IRU5	IRU4	IRU3	IRU2	IRU1	IRU0
0	0	0	1	0	1	0	0	VRSP3	VRSP2	VRSP1	VRSP0	ORP11	ORP10	ORP9	ORP8
0	0	0	1	0	1	0	1	ORP7	ORP6	ORP5	ORP4	ORP3	ORP2	ORP1	ORP0
0	0	0	1	0	1	1	0	ORD11	ORD10	ORD9	ORD8	ORD7	ORD6	ORD5	ORD4
0	0	0	1	0	1	1	1	ORD3	ORD2	ORD1	ORD0	ORU11	ORU10	ORU9	ORU8
0	0	0	1	1	0	0	0	ORU7	ORU6	ORU5	ORU4	ORU3	ORU2	ORU1	ORU0
0	0	0	1	1	0	0	1	HAXD11	HAXD10	HAXD9	HAXD8	HAXD7	HAXD6	HAXD5	HAXD4
0	0	0	1	1	0	1	0	HAXD3	HAXD2	HAXD1	HAXD0	HAXU11	HAXU10	HAXU9	HAXU8
0	0	0	1	1	0	1	1	HAXU7	HAXU6	HAXU5	HAXU4	HAXU3	HAXU2	HAXU1	HAXU0
0	0	0	1	1	1	0	0	VAXD11	VAXD10	VAXD9	VAXD8	VAXD7	VAXD6	VAXD5	VAXD4
0	0	0	1	1	1	0	1	VAXD3	VAXD2	VAXD1	VAXD0	VAXU11	VAXU10	VAXU9	VAXU8
0	0	0	1	1	1	1	0	VAXU7	VAXU6	VAXU5	VAXU4	VAXU3	VAXU2	VAXU1	VAXU0
								— or ▭ : Setting invalid.							

Note) PLLP0, HP0, VP0, HSTW0, HSTP0, PCGU0, PCGD0, PRGD0, FRPP0, SHP0, MBKA0, MBKB0, MBKZ0, IRD0, IRU0, ORRS0, ORP0, ORD0, ORU0, HAXD0, HAXU0, VAXD0, VAXU0: LSB.
Shaded bits (PLLP0, IRU0, ORPU, ORU0 and HAXU0) are indicated for reference, and actual data setting to these bits is invalid.

Each control data is described in detail below.

The following descriptions define the width of one dot clock as "clk".

PLLP11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These bits set the frequency division ratio (master clock) of the internal 1/N frequency divider for the PLL. The data is 12 bits and the frequency division ratio can be set up to 4096. However, the internal logic circuits of this TG operate at 1/2 clock, so the PLLP0 setting is invalid. When N is an odd number, use an external frequency divider.

The actual frequency division ratio should be set as follows.

Number of clk for the horizontal period – 2 = Actual number of dots set

Examples of settings for major modes are shown below.

Note) When using an external frequency divider (serial data HR is L), these settings are not necessary. (They can also be set to all L.)

1) Macintosh16 (832 × 624)

PLLP setting value = 1152 (horizontal period) – 2 → 1150 (LHLLLHHHHHHL: LSB)

PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	L	L	L	H	H	H	H	H	H	L

2) SVGA (800 × 600)

PLLP setting value = 1056 (horizontal period) – 2 → 1054 (LHLLLLLHHHHL: LSB)

PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	L	L	L	L	L	L	H	H	H	L

* VESA SVGA60

3) VGA (640 × 480)

PLLP setting value = 800 (horizontal period) – 2 → 798 (LLHHLLLHHHHL: LSB)

PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	L	H	H	L	L	L	H	H	H	H	L

* VGA60

4) PC98 (640 × 400)

PLLP setting value = 848 (horizontal period) – 2 → 846 (LLHHLHLLHHHL: LSB)

PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	L	H	H	L	H	L	L	H	H	H	L

5) NTSC double speed (640 × 480)

PLLP setting value = 1560 (horizontal period) – 2 → 1558 (LHHLLLLHLHHL: LSB)

PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	L	L	L	H	L	H	H	L

6) PAL double speed (762 × 572)

PLLP setting value = 1880 (horizontal period) – 2 → 1878 (LHHHLHLHLHHL: LSB)

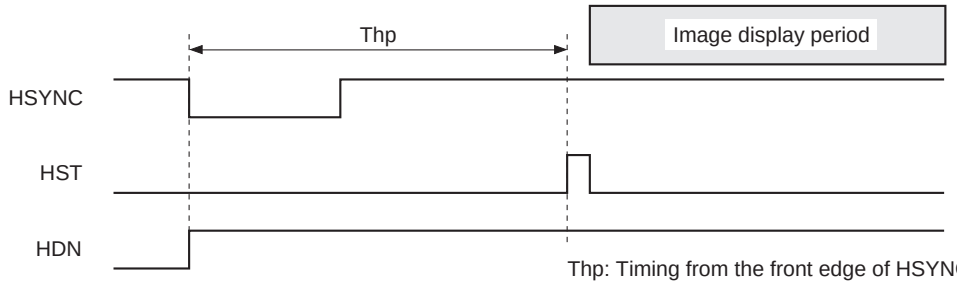
PLLP	11	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	H	L	H	L	H	L	H	H	L

HP11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These bits set the horizontal display start position. The minimum adjustment width is 1 dot, and adjustment of with 12 bits is possible using the front edge of HSYNC as the reference. The HP setting range is from 0 to (N – 1). However, do not set HP to the number of frequency divisions N or higher, as the various pulses will not be output.

The horizontal direction timing is interlinked using the falling edges of ENB1 and 2 as the reference. The following pulses are interlinked according to the HP11 to 0 setting.

HST, HCK1, HCK2, ENB1, ENB2, PCG, PRG, CLP, BLK, VD, VCK transition point, FRP transition point, XFRP transition point, BLK transition point and VD transition point



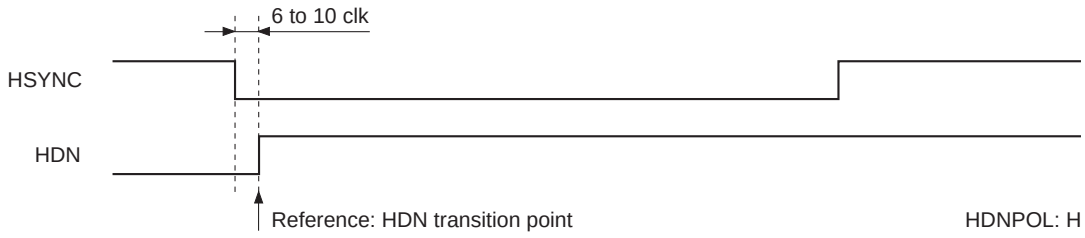
Thp: Timing from the front edge of HSYNC to the HST pulse
HSTP5 to 0: LLLLL, HDNPOL: H

Minimum Thp setting values for each mode

PLSSL2, 1, 0	Thp
L L L	72 clk
L L H	92 clk
L H L	118 clk
L H H	146 clk
H L L	178 clk
H L H	188 clk
H H L	204 clk
H H H	232 clk

* HSTP5, 4, 3, 2, 1, 0: All L

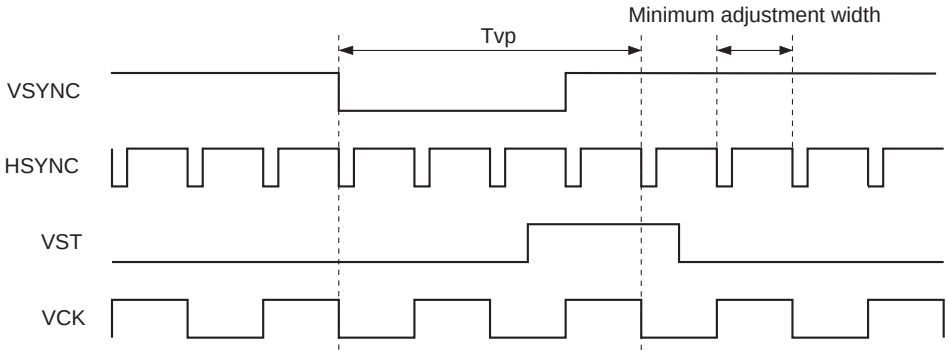
Note) The time from HST until image display starts differs for each panel and its display area switching mode. In modes which apply a reset at the front edge of HSYNC (HR: L), the HDN pulse transition point is delayed by several dots relative to HSYNC. In these modes, Thp in the table above indicates the value using the HDN pulse transition point as the reference.



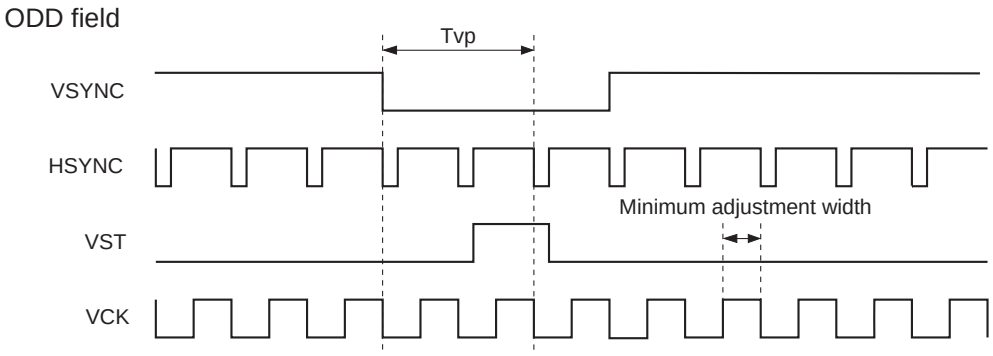
VP7, 6, 5, 4, 3, 2, 1, 0

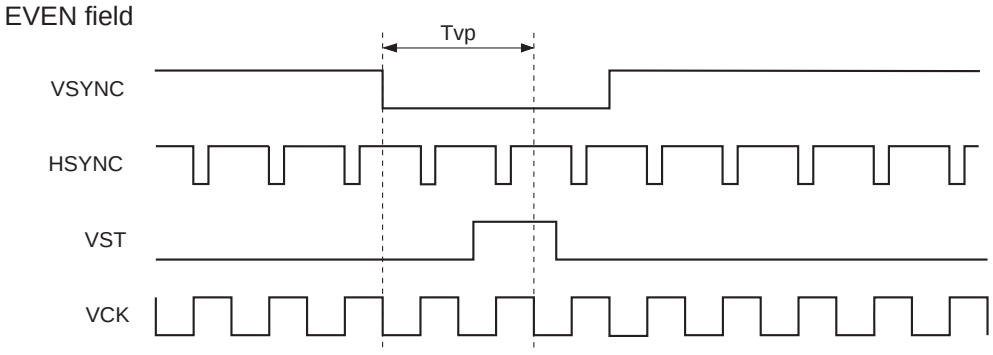
These bits set the vertical display start position. The minimum adjustment width is 1H of the output signal, and adjustment of up to 256H with 8 bits is possible using the front edge of VSYNC as the reference.
In interlace signal double-speed mode, the vertical display start position can be set within a width of 1H relative to the double-speed converted signal.

a) Non-interlace



b) When using an interlace double-speed controller





Minimum and maximum Tvp setting values

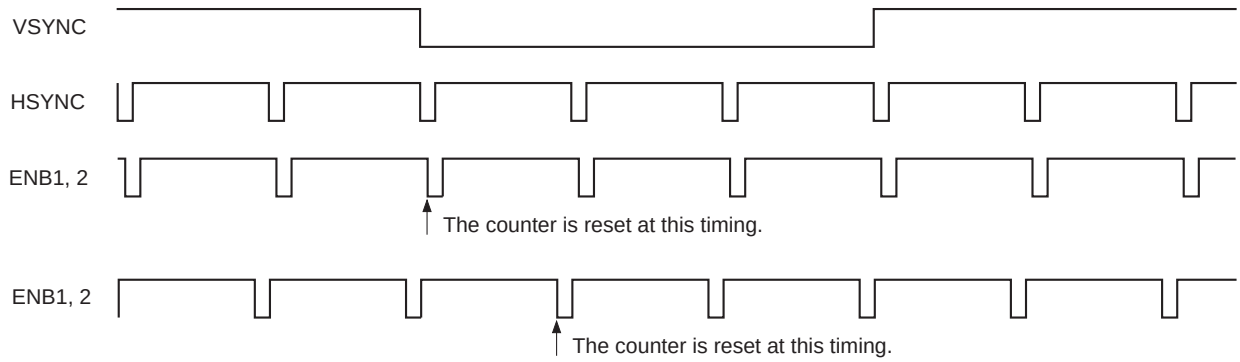
VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	4H
Max.	H	H	H	H	H	H	H	H	259H

Note) The time from VST until image display starts differs for each panel.
Also see the data sheets of the used panels.

VP

The vertical display start position setting VP sets the value used to decode the internal counter. This internal counter is reset at the ENB1 and 2 pulse fall position when VSYNC is input, and counts up at each ENB1 and 2 pulse fall position thereafter.

Therefore, when VSYNC is delayed relative to HSYNC and serial data HP is all L or a similar value, or when the HP11 to 0 setting is large and the ENB pulses fall near the end of the horizontal period, the vertical display start position is offset by 1H.



When the HP11 to 0 setting is large.

Horizontal direction pulses

The horizontal direction timing pulses for driving LCD panels are advanced and delayed interlinked with serial data HP11 to 0. The reference at this time is the falling edge of the ENB1 and 2 pulses.

Except for during skip scan, the ENB1 and 2 pulse width is fixed by serial data PLSSL, and the pulse position is determined by serial data HP11 to 0. (See the Timing Charts.) The horizontal direction pulse position for other panels is generated by the internal counter that is reset at the ENB1 and 2 pulse fall position.

HSTW1, 0

These bits set the HST pulse width. Normally set HSTW1 and 0 to LL for 6-dot simultaneous sampling panels (VGA, SVGA), and to HL for 12-dot simultaneous sampling panels (XGA).

HSTW1, 0	HST pulse width
L L	12 clk
L H	18 clk
H L	24 clk
H H	48 clk

HSTP5, 4

This sets the HST pulse rise position. The HST pulse rise position from the falling edge of the ENB1 and 2 pulses is as shown in the table below according to the PLSSL2, 1, 0 setting.

However, note that the HSTP5 setting is invalid when PLSSL2 to 0 (described hereafter) is set from LLL to HLL.

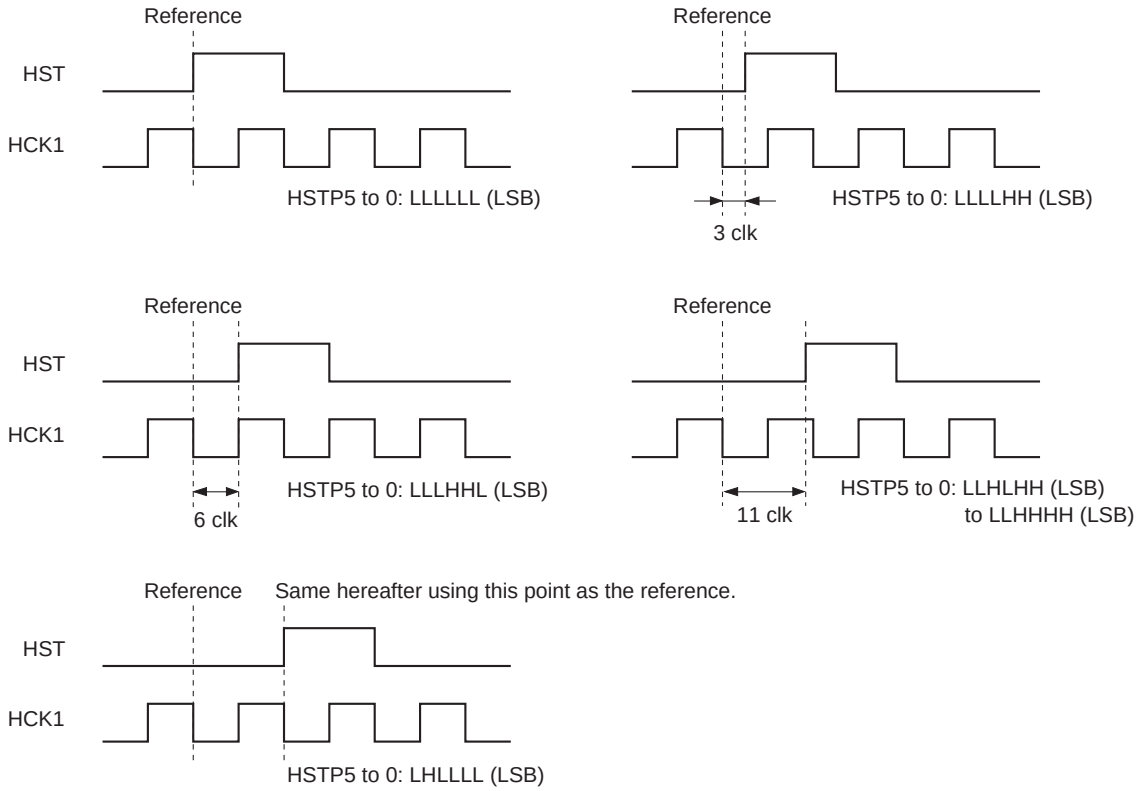
Thst rise position

PLSSL2, 1, 0	HSTP5, 4			
	L L	L H	H L	H H
L L L	70 clk	82 clk	70 clk	82 clk
L L H	90 clk	102 clk	90 clk	102 clk
L H L	116 clk	128 clk	116 clk	128 clk
L H H	144 clk	156 clk	144 clk	156 clk
H L L	176 clk	188 clk	176 clk	188 clk
H L H	186 clk	198 clk	210 clk	222 clk
H H L	202 clk	214 clk	226 clk	238 clk
H H H	230 clk	242 clk	254 clk	266 clk

Note) HST3, 2, 1, 0: LLLL

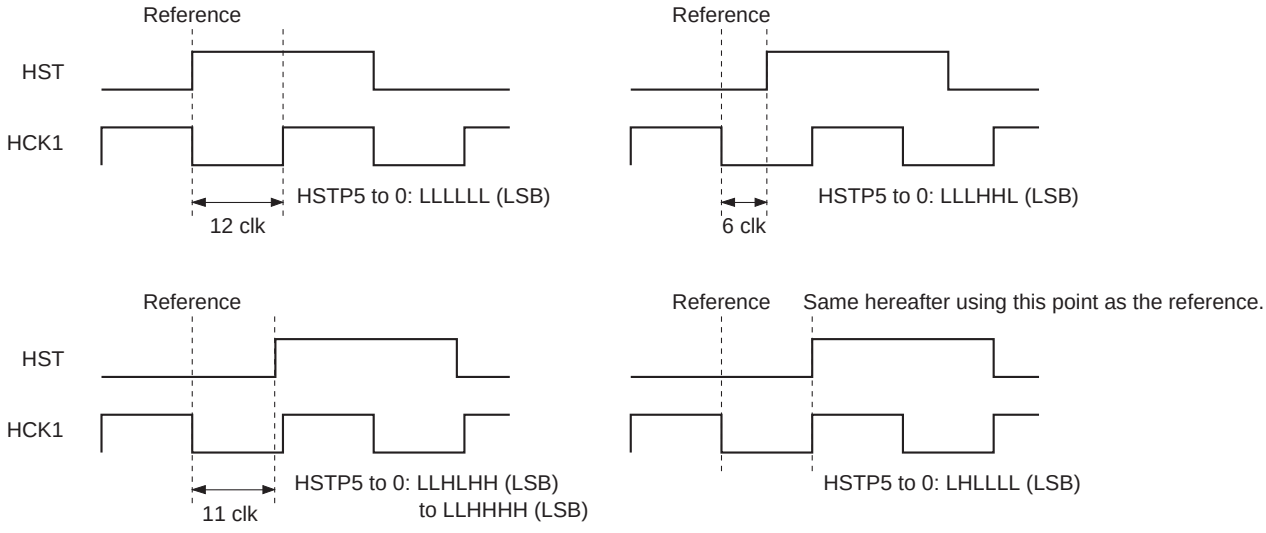
HSTP3, 2, 1, 0
These bits adjust the HST pulse start phase relative to HCK in 1-dot units.
Set these bits as follows using HSTP5 to 0: LLLLLL (LSB) as the reference.

Serial setting HCKM: L (6-dot simultaneous sampling)



Note) HCK2 is the reverse polarity of HCK1. The timings shown above are for RGT: H, HCKPOL: H and HCKFX: L.

Serial setting HCKM: H (12-dot simultaneous sampling)



Note) HCK2 is the reverse polarity of HCK1. The timings shown above are for RGT: H, HCKPOL: H and HCKFX: L.

PCGU2, 1, 0

These bits adjust the PCG pulse rise position in 2-dot units. (However, serial data PCG: H)
When serial data PCG is L, the PCGU2 to 0 setting is invalid and the PCG pulse rises at the same position as the FRP pulse transition point regardless of this setting. (interlinked with FRPP3, 2, 1, 0)

PCGD4, 3, 2, 1, 0

These bits adjust the PCG pulse fall position in 2-dot units.
However, the PCGD4 setting is invalid when PLSSL2, 1, 0 is set from LLL to HLL.

The PCGU2, 1, 0 and PCGD4, 3, 2, 1, 0 setting ranges are shown in the table below.

PLSSL2, 1, 0	Tpcu		Tpcd	
	PCGU2, 1, 0		PCGD4*, 3, 2, 1, 0	
	L L L	H H H	L L L L L	H H H H H
L L L	12 clk	28 clk	56 clk	86 clk
L L H	18 clk	32 clk	74 clk	104 clk
L H L	26 clk	40 clk	98 clk	128 clk
L H H	36 clk	50 clk	124 clk	154 clk
H L L	46 clk	60 clk	152 clk	182 clk
H L H	48 clk	62 clk	150 clk	212 clk
H H L	52 clk	66 clk	164 clk	226 clk
H H H	58 clk	72 clk	190 clk	252 clk

*: The PCGD4 setting is invalid when PLSSL2, 1, 0 is set from LLL to HLL.

Adjust the PCG pulse width to match the specifications for each LCD panel with the PCGU2 to 0 and PCGD4 to 0 settings. See the data sheets of the used panel for the PCG pulse width.

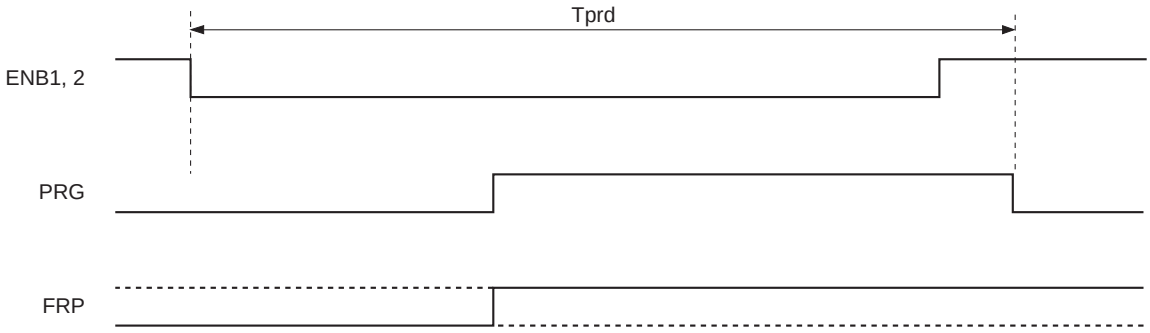
PRGD4, 3, 2, 1, 0

These bits adjust the PRG pulse fall position in 2-dot units.

However, the PRGD4 setting is invalid when PLSSL2, 1, 0 is set from LLL to HLL.

The PRG pulse rise position is the same as the FRP pulse transition point. (interlinked with FRPP3, 2, 1, 0)

The PRGD4, 3, 2, 1, 0 setting range is shown in the table below.



Tpru setting range

PLSSL2, 1, 0	PCGD4*, 3, 2, 1, 0		PCGD4*, 3, 2, 1, 0	
	L L L L L	L H H H H	H L L L L	H H H H H
L L L	62 clk	92 clk	62 clk	92 clk
L L H	82 clk	112 clk	82 clk	112 clk
L H L	108 clk	138 clk	108 clk	138 clk
L H H	136 clk	166 clk	136 clk	166 clk
H L L	168 clk	198 clk	168 clk	198 clk
H L H	136 clk	166 clk	182 clk	212 clk
H H L	142 clk	172 clk	196 clk	226 clk
H H H	162 clk	192 clk	222 clk	252 clk

*: The PRGD4 setting is invalid when PLSSL2, 1, 0 is set from LLL to HLL.

PCG

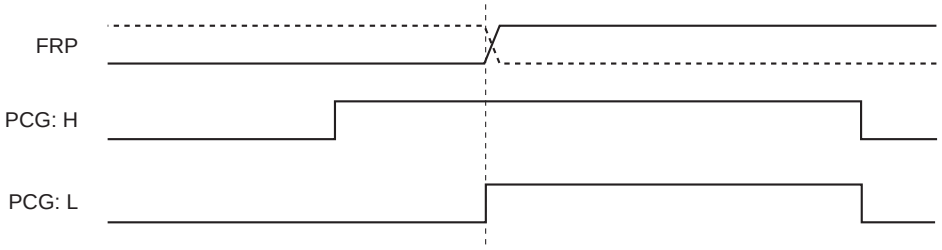
This bit selects the new and old PCG pulse timing.

When PCG is H, the PCGU2 to 0 setting shown on the previous page is selected. (new timing)

When PCG is L, the PCG pulse rise position is interlinked with the FRP pulse transition point. (old timing)

Set to match the timing specifications of the LCD panel.

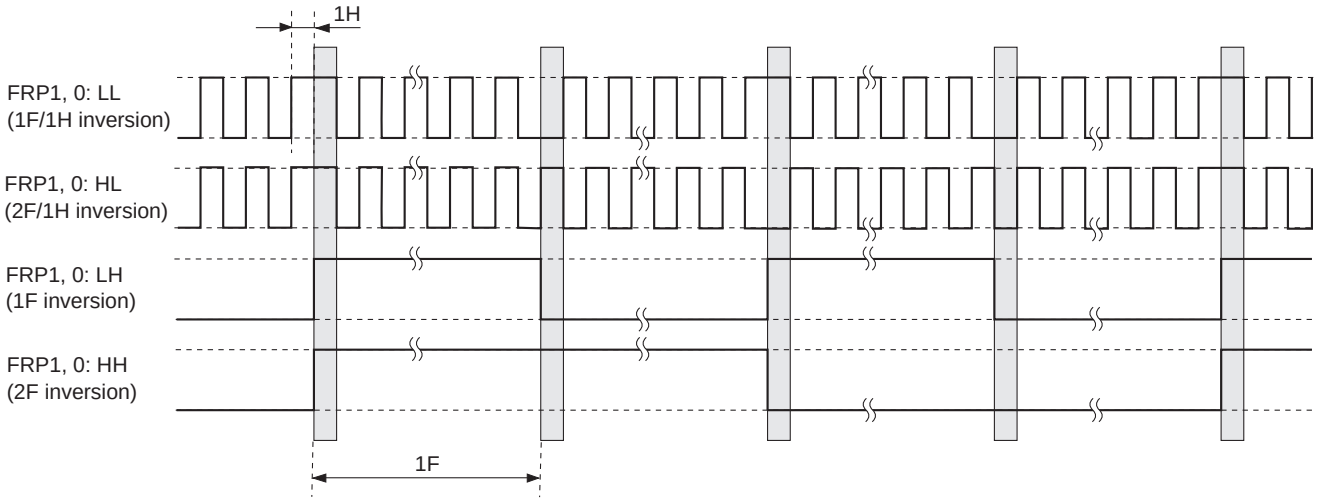
Set PCG to H for SVGA panels that support two-step precharge, and to L for other panels.



FRP1, 0

These bits are the data for switching the LCD AC conversion signal FRP pulse cycle. Normally set FRP1, 0 to LL.

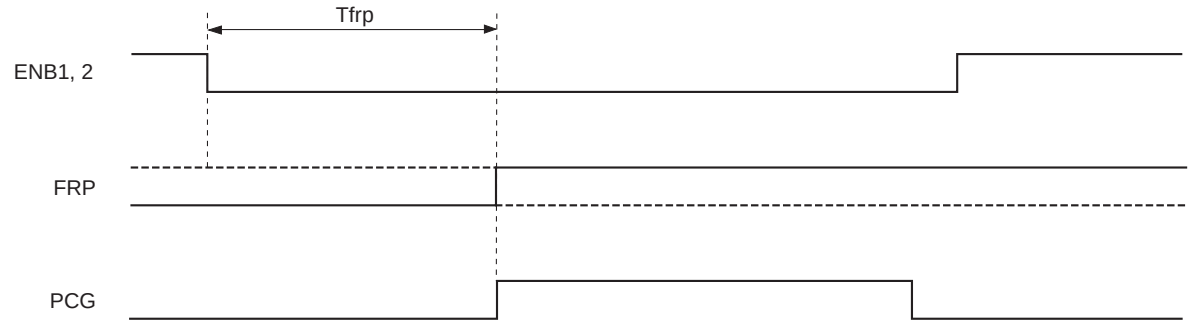
FRP0 can also be controlled externally. → See SLCNT.



FRPP3, 2, 1, 0

These bits adjust the FRP pulse transition point in 2-dot units.

The PRG pulse rise position is the same as the FRP pulse transition point, and is interlinked with FRPP3 to 0.



Tfrp setting range

PLSSL2, 1, 0	FRPP3, 2, 1, 0	
	L L L L	H H H H
L L L	16 clk	46 clk
L L H	24 clk	54 clk
L H L	36 clk	66 clk
L H H	52 clk	82 clk
H L L	68 clk	98 clk
H L H	58 clk	88 clk
H H L	62 clk	92 clk
H H H	72 clk	102 clk

VSTFX, VSTPOL

These bits set the VST pulse polarity. When VSTFX is H, the polarity of the VST pulse is positive regardless of other settings. Normally set VSTPOL to H. See the table below for details.

Panel	VSTFX	VSTPOL	DWN	VST pulse polarity
XGA	H	—	—	
	L	L	L	
	L	L	H	
SVGA	L	H	L	
	L	H	H	

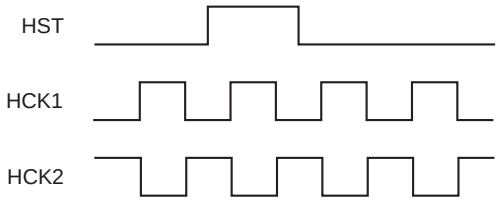
* —: don't care

HCKFX, HCKPOL

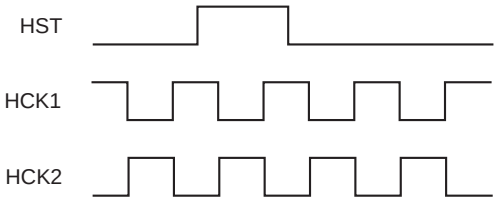
These bits set the HCK1 and 2 pulse polarity. When HCKFX is H, the HCK1 and 2 pulse polarity is fixed regardless of the right/left inversion control setting RGT. However, the polarity is inverted by HCKPOL.
See the table and figures below for details.

HCKFX	RGT	HCKPOL	HCK polarity
H	—	L	B
H	—	H	A
L	L	L	A
L	L	H	B
L	H	L	B
L	H	H	A

* —: don't care



A in the table above



B in the table above

HSTW1, 0: LL, HSTP5 to 0: LLLLHH, HCKM: L

HCKM

This bit sets the HCK1 and 2 pulse width. When HCKM is L, the HCK1 and 2 pulse for 6-dot simultaneous sampling is output. When HCKM is H, the HCK1 and 2 pulse for 12-dot simultaneous sampling is output. Set the width to match the panel specifications.

SVGA panel → 6-dot simultaneous sampling → HCKM: L
XGA panel → 12-dot simultaneous sampling → HCKM: H

INV, SHP3, 2, 1, 0

This IC does not have a sample-and-hold pulse output, but instead allows control of the sample-and-hold position of the CXA2112R sample-and-hold driver and control of master clock inversion by setting the CXD3500R serial data and connecting the control pins.

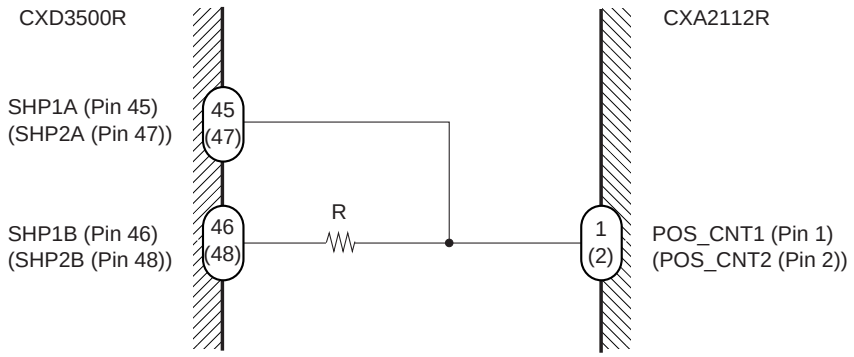
INV set by serial data is output as is from the INV (Pin 49). Connect this INV to INV_CNT (Pin 52) of the CXA2112R to allow CXA2112R dot clock phase inversion control from the TG.

In addition, data set with SHP3, 2, 1, 0 is reflected to the SHP1A, SHP1B, SHP2A and SHP2B outputs (Pins 45, 46, 47 and 48) as shown in the table below.

SHP3, 2, 1, 0	SHP2A, 2B, 1A, 1B	SHP3, 2, 1, 0	SHP2A, 2B, 1A, 1B
L L L L	L L L L	H L L L	Z H L L
L L L H	L L Z L	H L L H	Z H Z L
L L H L	L L Z H	H L H L	Z H Z H
L L H H	L L H H	H L H H	Z H H H
L H L L	Z L L L	H H L L	H H L L
L H L H	Z L Z L	H H L H	H H Z L
L H H L	Z L Z H	H H H L	H H Z H
L H H H	Z L H H	H H H H	H H H H

* Z: High Impedance State

The sample-and-hold position of the CXA2112R can be set by connecting SHP1A, 1B, 2A and 2B as shown in the figure below. See the CXA2112R data sheet for further details.



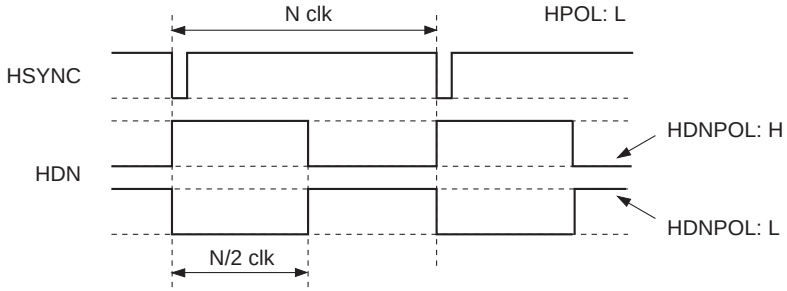
Note) The value of resistor R in the figure above differs according to the number of connected CXA2112R.

VPOL, HPOL

These bits are the data for switching the input vertical and horizontal sync signal polarity. Since signal processing is performed with the sync signal polarity fixed to positive by the internal logic, the data must be switched according to the polarity of the input sync signal.
Therefore, individually set VPOL and HPOL to H when the polarity of the input sync signal is positive, and to L when the polarity is negative.
VSYNC may not be detected if the opposite polarity is set, so be sure to set the correct polarity.

HDNPOL

HDN (H return pulse) is the 1/N frequency divider output pulse for the PLL IC. The width of the HDN pulse is calculated according to the setting of PLLP11 to 1 for the value of frequency division N, and that value is N/2. HDNPOL is the data for setting the output polarity of this HDN pulse, and the relationship between its setting and the pulse polarity is shown in the figure below.

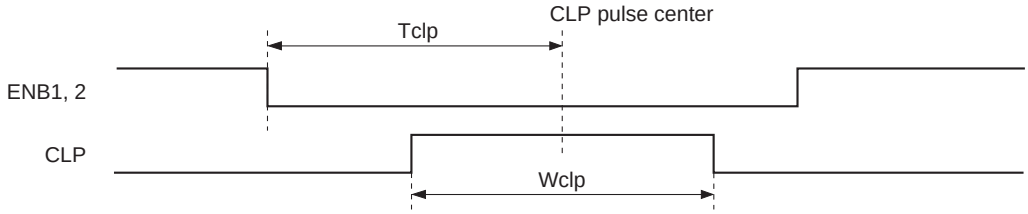


CLPPOL

This bit sets the output polarity of pedestal clamp pulse CLP. When CLPPOL is H, the polarity of the CLP pulse is positive, and when CLPPOL is L, the polarity of the CLP pulse is negative.

CLPW, CLPP

These bits set the CLP pulse output width and output phase. Both the width and the phase can be set to two positions using 1 bit.
The CLP pulse center position is fixed regardless of the CLPW setting.



PLSSL2, 1, 0	Wclp		Tclp	
	CLPW: L	CLPW: H	CLPP: L	CLPP: H
L L L	32 clk	48 clk	48 clk	32 clk
L L H	40 clk	60 clk	60 clk	40 clk
L H L	50 clk	74 clk	77 clk	53 clk
L H H	64 clk	96 clk	100 clk	68 clk
H L L	80 clk	120 clk	124 clk	84 clk
H L H	80 clk	120 clk	124 clk	84 clk
H H L	86 clk	130 clk	133 clk	89 clk
H H H	96 clk	144 clk	148 clk	100 clk

SLCNT

Setting via the external control pins can be selected by setting SLCNT to H.

The settings that can be made using the external pins are the right/left inversion discrimination settings RGT and XRGT, and the setting for switching the LCD panel AC conversion signal FRP and XFRP pulse cycle.

SLCNT: L	SLCNT: H
Address: 0C Data 4 RGT	External pin RGTCNT (Pin 10)
Address: 07 Data 4 FRP0	External pin FRPCNT (Pin 11)

SLFLD

This bit selects FLD (Pin 6) IN/OUT pin input and output. The CXD3500R performs field identification internally. When SLFLD is L, the internally generated FLD pulse is selected and used for the internal circuit logic.

The external FLD pulse is selected by setting SLFLD to H.

For normal data type signals, the field identification pulse FLD is inverted every vertical period. The polarity at this time is not specified.

Note) When inputting the FLD pulse from an external source, make sure that the FLD pulse transition point is 2H or more before the rising edge of VST.

SLRS

This bit switches the HSYNC edge-based 1/2 frequency divider reset on/off when generating the 1/2 clock using the internal frequency divider.

When SLRS is H, reset is not applied; when SLRS is low, reset is applied every 1H.

There is no need to set this bit when inputting a 1/2 clock from an external source.

CKPOL

This bit performs the input clock polarity switching settings. CLK1 and 2 pass through this clock polarity switching setting immediately after input. When CKPOL is L, the internal circuits operate according to the input clock and the reverse polarity clock.

When setup and hold cannot be maintained because the phases of the HSYNC input and the master clock input to the TG are offset due to the set system, set CKPOL to a value that provides sufficient margin.

SLCK

This bit switches the clock between the internal 1/2 frequency division and external 1/2 clock input.

When inputting an external 1/1 clock, set SLCK to H to 1/2 frequency divide the clock internally. When inputting an external 1/2 clock, set SLCK to L.

When the master clock is 55MHz or more, input an external 1/2 frequency-divided clock and set SLCK to L.

Note) Pulses with positions that can be set in 1-dot units (HST, HCK1, HCK2, ENB1, ENB2, PCG, PRG, CLP, BLK, VCK transition point, FRP transition point and XFRP transition point) use the internally inverted clock, so when inputting a 1/2 clock using an external frequency divider, these pulses may be offset if the 1/2 clock duty deviates from 50%. Therefore, set the duty of the input 1/2 clock as close to 50% as possible.

PLSSL2, 1, 0

These bits set the output timing mode. Switch the setting according to the dot clock frequency and blanking width of the input signal. When using a Sony SVGA panel, select one of the 5 modes from PLSSL2 to 0: LLL to HLL. When using a XGA panel, select one of the 3 modes from PLSSL2 to 0: HLH to HHH. The setting reference is shown in the table below.

PLSSL2, 1, 0	LCD panel	Setting reference
L L L	SVGA	Dot clock: 20 to 30MHz
L L H		Dot clock: 25 to 40MHz
L H L		Dot clock: 35 to 50MHz
L H H		Dot clock: 45 to 63MHz
H L L		Dot clock: 55 to 75MHz
H L H	XGA	Dot clock: 65 to 80MHz
H H L		Dot clock: 75 to 85MHz
H H H		Dot clock: 80 to 96MHz

Note) When the horizontal blanking width is sufficient, use the mode one higher than the setting that results in the maximum value for that mode.

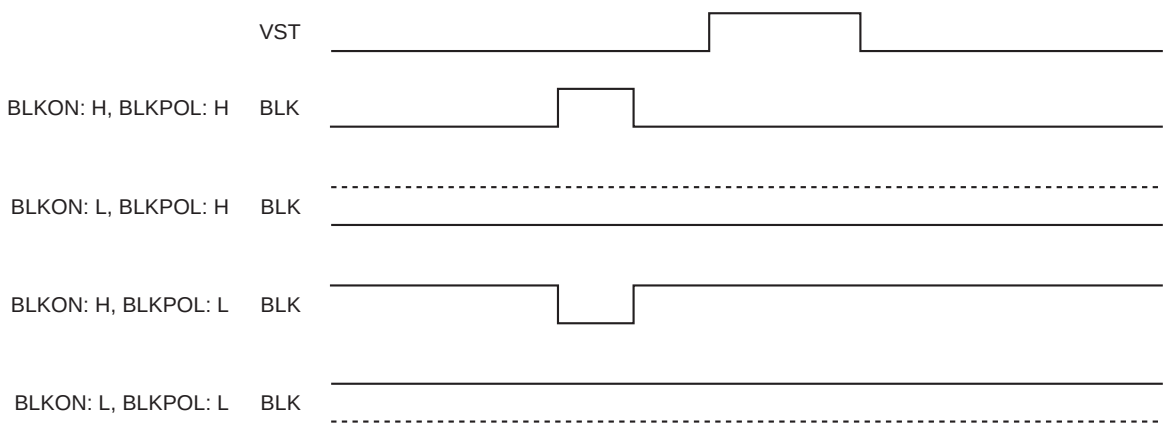
Example) SVGA 60Hz: Dot clock 40MHz

PLSSL2, 1, 0 can be set to LLH, but should be set to LHL instead in order to ensure sufficient margin.

BLKON, BLKPOL

These bits are switch the black frame display pulse BLK on/off and set the BLK polarity, respectively. When BLKON is H, the BLK pulse is output. In addition, the polarity of the BLK pulse is positive when BLKPOL is H, and negative when BLKPOL is L.

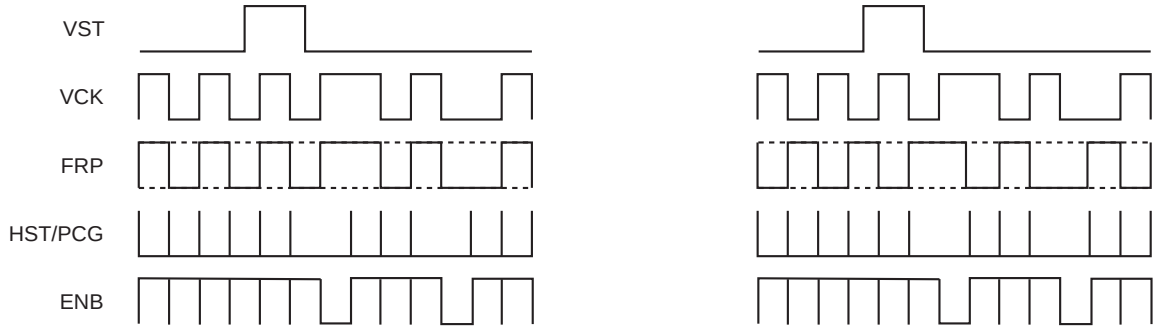
Set BLKPOL to H for Sony SVGA panels, and to L for XGA panels.



FMBK

This bit sets the FRP-related skip scan timing. When this bit is set, the FRP pulse transition point phase is offset by 1H relative to the VCK pulse. In this case, the skip scan position does not change when FMBK is either H or L.

See the figure below.



FMBK: H (MAIN) **FMBK: L (SUB)**

Note) Precautions when using skip scan

When configuring a system by combining the Sony CXA2112R sample-and-hold driver and this TG, input the ENB2 pulse to Pin 12 (ENB) of the CXA2112R instead of the ENB1 pulse that is connected to the panel.

If the ENB1 pulse is input to the CXA2112R and FMBK is L (SUB), the CXA2112R internal sample-and-hold circuit may not be reset, causing the characteristics of the CXA2112R to deteriorate.

When not using skip scan, either ENB1 or 2 may be input to Pin 12 (ENB) of the CXA2112R.

MBKA4, 3, 2, 1, 0 MBKB3, 2, 1, 0 MBKZ3, 2, 1, 0

These bits set the skip scan display related settings. When not performing skip scan display, set all bits to L.

See the setting examples on the next page.

MBKA4, 3, 2, 1, 0

These bits set the skip scan main cycle. The setting range is from 2 to 31 cycles.

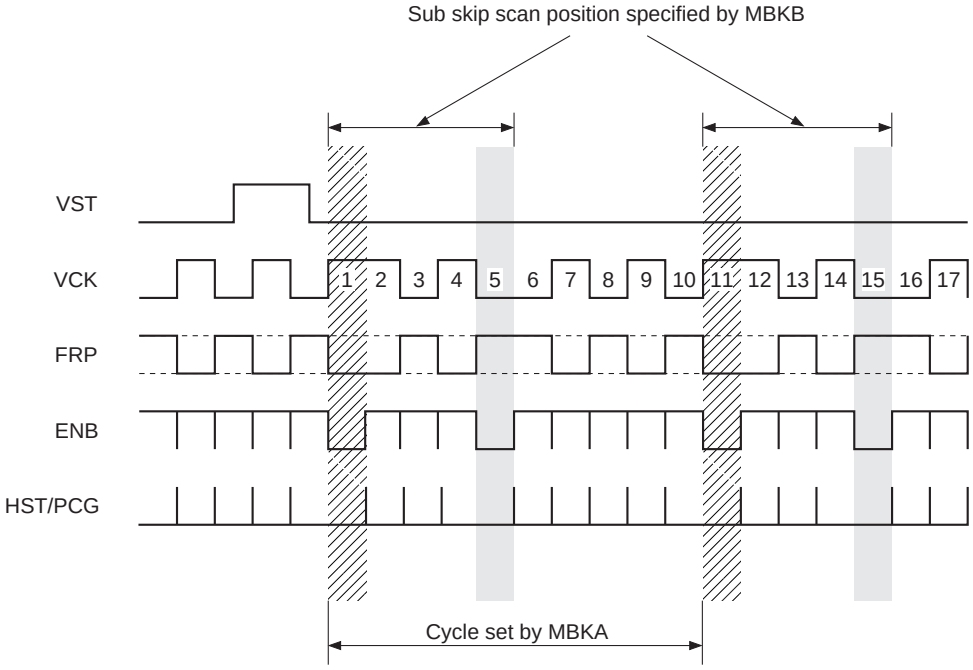
When MBKA4 to 0 is LLLLL or LLLLH, skip scan is not performed.

MBKB3, 2, 1, 0

These bits set the sub skip scan position. The setting range is from 2 to 15. See the figures on the next page.

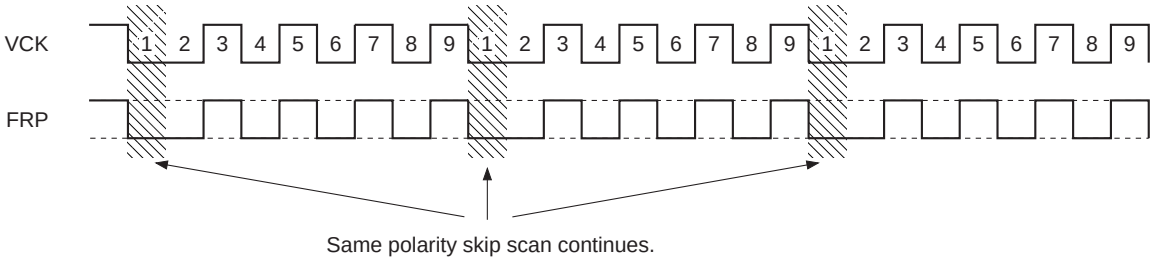
When MBKB3 to 0 is LLLL or LLLH, or when MBKB > MBKA, sub skip scan is not performed.

Example) MBKA4, 3, 2, 1, 0: LHLHL (10), MBKB3, 2, 1, 0: LHLH (5)

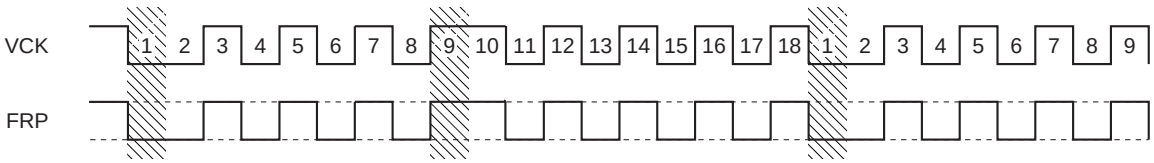


Note) Odd skip scan continuously skips only pulses of the same polarity. Depending on the system, this may cause DC to be applied to the panel. Therefore, set skip scan so that pulses of the same polarity are not continuously skipped.
This can be accomplished during odd skip scan by doubling the setting to make it an even number, and then setting skip scan for the odd lines.

Example) 1/9 skip scan → MBKA4 to 0: LHLLH, MBKB3 to 0: LLLL X



To set 2/18 skip scan and odd line skip scan → MBKA4 to 0: HLLHL, MBKB3 to 0: HLLH O



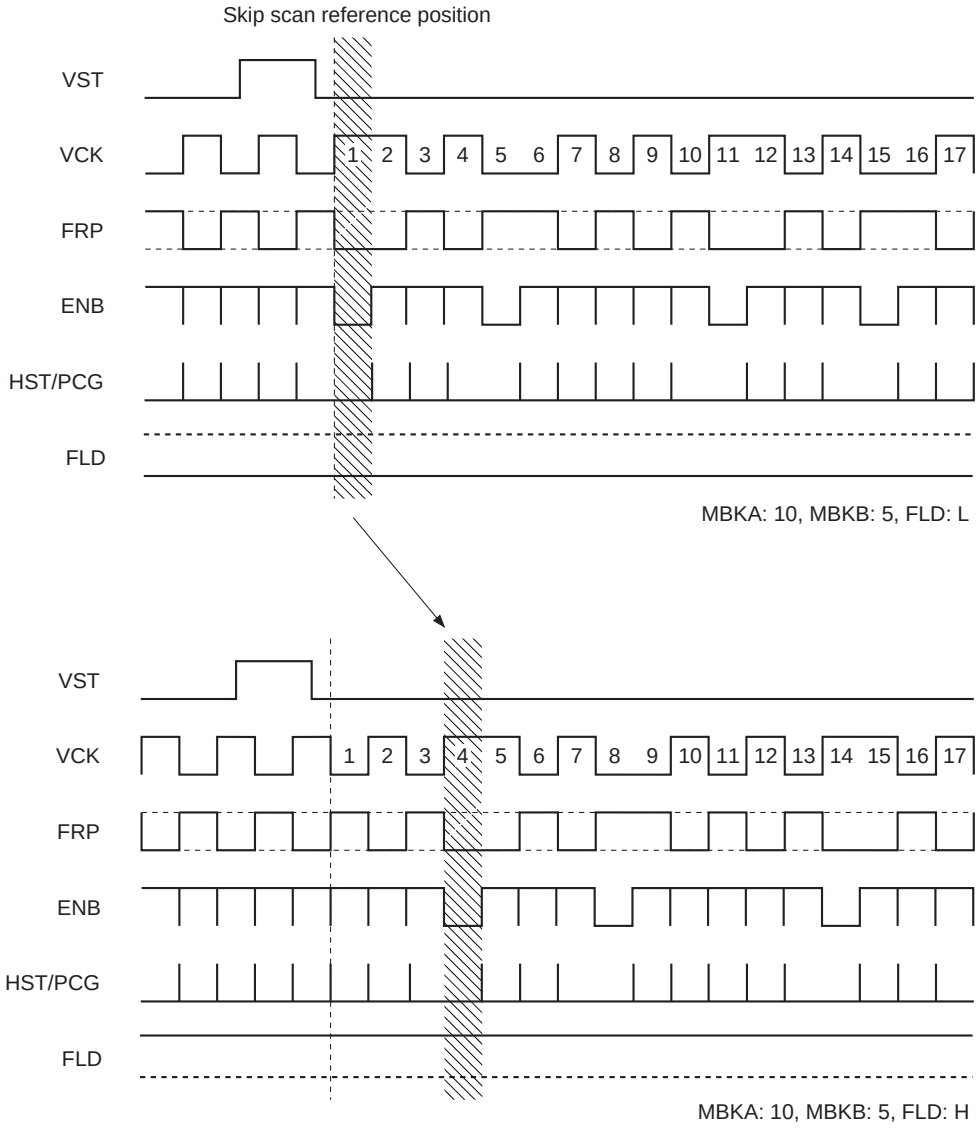
MBKZ3, 2, 1, 0

These bits change the skip scan timing for each V cycle.

These bits determine the skip scan timing for the next 1V period using the skip scan timing when the field identification pulse (FLD) is L as the reference. The optimal skip scan position can be set by setting a skip scan interval of 0 to 14H.

(When MBKZ3 to 0 is LLLL or HHHH, the same line is skipped each field.)

Example) MBKZ3, 2, 1, 0: LLHH (3)



Note) Observe the following points when setting MBKZ3 to 0.

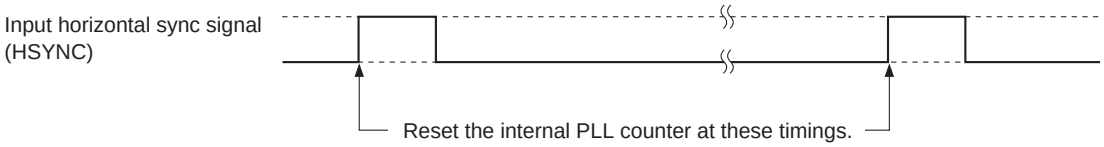
1. When MBKB is 0 or 1, set the MBKZ value to MBKA or less.
2. In all other cases, set the MBKZ value to MBKB or less.

VGAV

This bit switches the supported input signal between AV interlaced signals or data signals.
Set VGAV to H for data signal input, and to L for AV signal input.
When VGAV is L, the FLD pulse is generated by phase comparison using the value calculated from the serial setting PLLP11 to 0 value. Therefore, when using the FLD pulse generated by this TG, be sure to set PLLP11 to 0 regardless of the HR setting below (offset due to skip scan fields, etc.).

HR

This bit controls the input horizontal sync signal (HSYNC)-based PLL counter reset operation, and supports external clock input. (Reset operation is enabled when HR is L.)
Resetting the internal PLL counter at the front edge of the input HSYNC generates an output pulse synchronized to HSYNC. When HR is L, there is no need to set PLLP11 to 0.
This function should be used with systems which do not use a PLL.
In addition, the master clock is loaded and reset is applied at the front edge of HSYNC in this mode, so be sure to input the input signal in a manner that ensures sufficient setup and hold times.



Note) Since H-POSITION specifications described in this data sheet are not satisfied due to the configuration of the internal logic, the picture center must be adjusted each time.

DWN, RGT

These bits set the up/down and/or right/left inversion discrimination data. These settings allow display to be performed in accordance with each display system.
The serial setting DWN is reflected to the DWN (Pin 37). In addition, RGT is valid only when SLCNT is L. At this time the setting value is reflected to the RGT (Pin 25).
See page 22 of this data sheet for the relationship between the DWN and VST pulses and the RGT and HCK pulses.

DSP

This bit performs the double-speed display mode switching settings. Operation shifts to double-speed display mode when DSP is L. However, DSP should be set H for other modes.

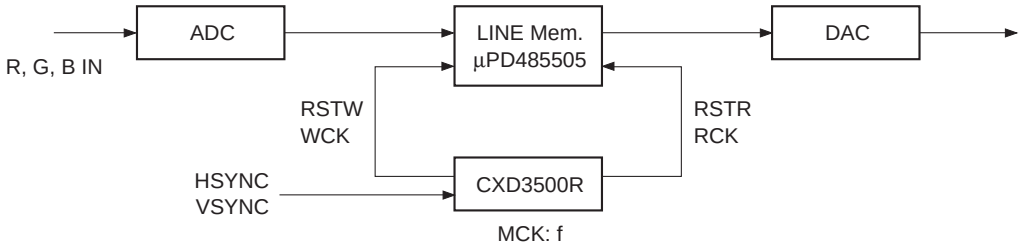
This function is only supported when the built-in double-speed controller is used. This controller is designed to use the µPD485505 (NEC/high-speed line buffer) as the system line memory IC, and generates the double-speed processing pulses RSTW (reset write), WCK (write clock), RSTR (reset read) and RCK (read clock).

The operation of the µPD485505 is as follows. Write operation is started at the RSTW timing, and this memory information is read at double speed at the RSTR timing which is delayed by 1/2H from the RSTW timing. Labeling the master clock frequency (MCK) as f, the write and read clock frequencies at this time are expressed as f/2 and f, respectively.

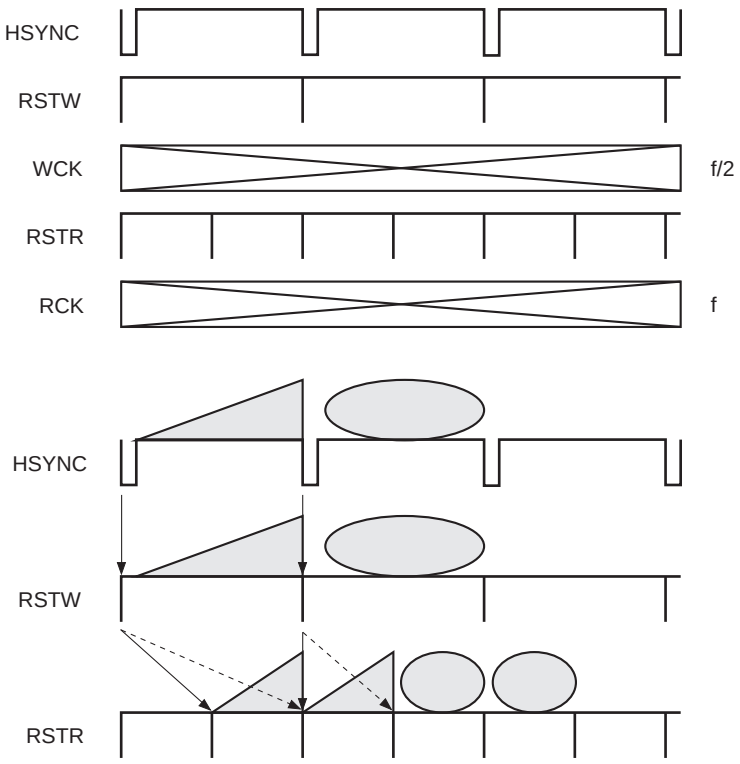
However, the master clock should have a frequency of 36MHz or less when using this mode.

See the data sheet for a detailed description of the µPD485505 operation.

Note) This function cannot be used in modes which input the 1/2 clock from an external source.
The RSTR position is calculated from the serial data PLLP11 to 0 setting value. Therefore, set serial data PLLP11 to 0 to the correct value when using this mode, regardless of the serial data HR setting.



Double-speed display system diagram



Double-speed display timing

PO/MODE3, 2, 1

These bits set the Parallel Out output. The values set by PO/MODE3, 2, 1 are output as is to MODE3 (Pin 20), MODE2 (Pin 21) and MODE1 (Pin 22).

These outputs are normally connected to the pins for the LCD panel display area switching, so they should be used to set the panel display area, etc. via the serial settings to the TG.

Examples) SVGA panels

LCX016, LCX026, LCX031: Input the MODE1, 2 and 3 outputs to the panel inputs of the same name.

LCX021: Input the MODE1 output to the MODE panel input pin.

XGA panels

LCX017, LCX023, LCX029: Input HB to MODE1 and VB to MODE2.

SPON

This bit switches on/off the special setting mode. The special setting mode is valid when this bit is H.

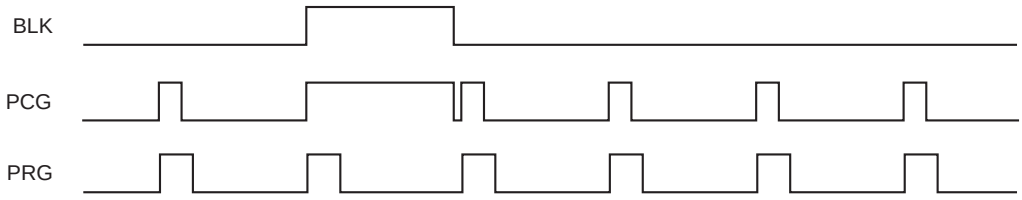
When SPON is L, the data at addresses 0E and 0F (HEX) is L regardless of the settings.

When SPON is L, the XGBK, HDON, HAXON and VAXON settings are all invalid, and the operation is in the mode where these settings are all L.

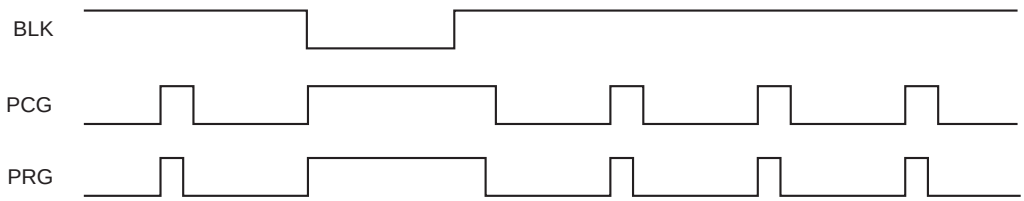
XGBK

This bit sets the timing output for black frame display on Sony XGA panels. When using the XGA panel black frame display mode, set XGBK to H. The output pulse timing is shown in the figure below. When not using black frame display, set XGBK to L.

When using SVGA panels, BLKON: H, BLKPOL: H, SPON: L



When using XGA panels, BLKON: H, BLKPOL: L, SPON: H, XGBK: H



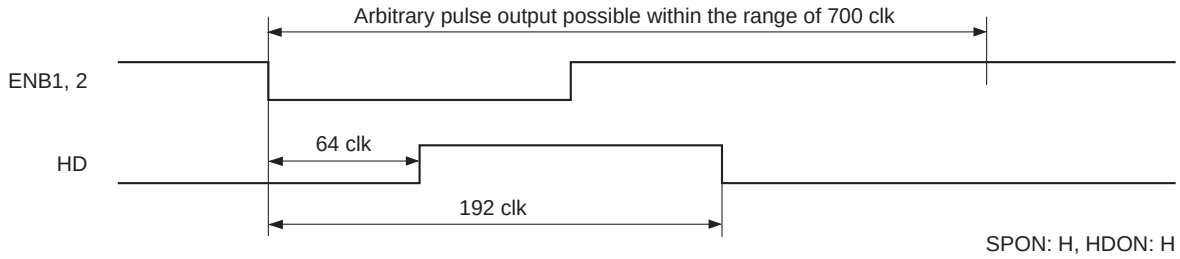
HDON

This bit performs the HD (Pin 31) pulse output switching settings.

When HDON is L, the horizontal direction reference pulse is output. (See the Timing Charts.) When HDON is H, HD outputs a programmable pulse that is interlinked with HP11 to 0. The fall position of this pulse can be set by serial data HAXD9 to 1, and the rise position can be set by serial data HAXU9 to 1.

A pulse of arbitrary position, width and polarity can be output at this position up to 700 clk from the ENB1 and 2 pulse fall position (reference).

Example) HAXD9 to 1: LLHHLLLLL, HAXU9 to 1: LLLHLLLLL



SPON: H, HDON: H

HAXON

This bit performs the XHS (Pin 51) pulse output switching settings.

When HAXON is L, the normal XHS pulse is output. (See the Timing Charts.) When HAXON is H, a pulse synchronized to HSYNC can be output at an arbitrary position (1-dot units) and width (2-dot units).

Set the pulse fall position in HAXD11 to 0, and the pulse rise position in HAXU11 to 0. However, the HAXU0 setting is invalid. When HAXD0 is H, the XHS pulse rise position also shifts backwards by 1 dot.

The setting range is from 0 to (N – 1), but do not set HAXD11 to 1 and HAXU11 to 1 to the same value.

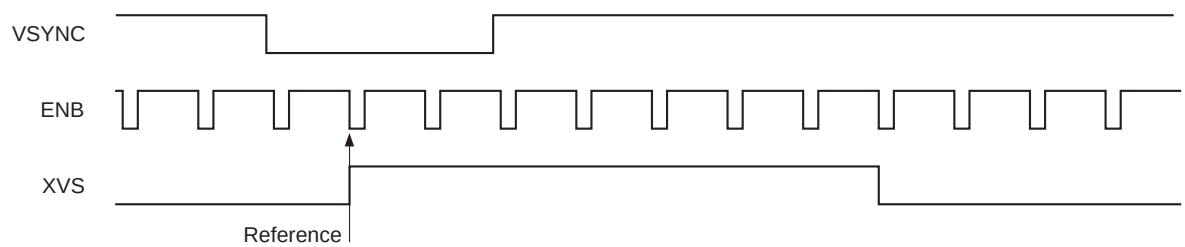
VAXON

This bit performs the XVS (Pin 50) pulse output switching settings.

When VAXON is L, the normal XVS pulse is output. (See the Timing Charts.) When VAXON is H, a pulse synchronized to VSYNC can be output at an arbitrary position (1H units) and width (1H units).

Set the pulse fall position in VAXD11 to 0, and the pulse rise position in VAXU11 to 0. The XVS pulse transition point at this time is the ENB1 and 2 pulse fall position.

The reference position is the front edge of the ENB1 and 2 pulse that is 1H from the front edge of VSYNC. Labeling this position as 0, the pulse can be set to an arbitrary position.



VAXON: H, VAXD11 to 0: LLLLLLLLLHHH, VAXU11 to 0: LLLLLLLLLLL

Scan converter pulse settings

Of the serial data below, set SLLAP to L when not using a scan converter that requires the control pulses output from this TG. In this case, other settings are not required.

SLLAP

SLLAP is used when converting the number of pixels using the scan converter, when the clock differs between input signals and output signals, etc.
When SLLAP is L, the normal operating mode is used.
When SLLAP is H, only the serial interface, PLL counter and phase comparator operate by the CKI1 or CKI2 synchronized to the input signal, and other internal blocks operate by CKI3.

LPCK

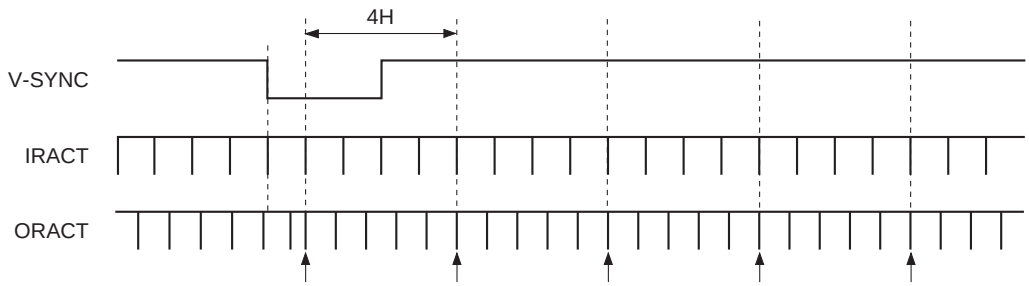
This setting is valid only when serial data SLLAP is H.
When LPCK is L, the CKI1 or CKI2 synchronized to the input HSYNC is selected; when LPCK is H, the external asynchronous clock CKI3 is selected, and an output pulse that is asynchronous with the input HSYNC is output according to the number of frequency divisions set by serial data ORP11 to 0.

SLCKL

This setting is valid only when serial data SLLAP is H.
This bit switches the clock between the internally 1/2 frequency-divided clock and the external 1/2 clock input.
When inputting an external 1/1 clock, set SLCKL to H to 1/2 frequency divide the clock internally. When inputting an external 1/2 clock, set SLCKL to L.

ORRS4, 3, 2, 1, 0

This setting is valid only when serial data SLLAP is H.
When serial data SLLAP is L, an arbitrary ORACT pulse can be output synchronized to the input HSYNC. When SLLAP is H, this pulse is generated from a dedicated counter (loop counter similar to the PLL counter, and referred to as AUX. PLL COUNTER = OR counter in the Block Diagram) that operates by CKI3, an independent clock that is asynchronous to the input signal. In addition, pulses for LCD panel driving pulses are also generated at this time based on the output of this counter, enabling the LCD panel to be driven with a horizontal cycle and clock that differ from the input signal.
The above OR counter applies a reset once every vertical period and at a specified input HSYNC cycle in order to synchronize to the input HSYNC. ORRS4 to 0 set the number of H cycles at which this HSYNC-based reset is performed. Reset is not applied at the H cycle when ORRS4 to 0 (LSB) is LLLLL, and applied at the set number of cycles for other settings. Reset can be applied from 1H to a maximum of 31H cycles.



Timing at which reset is applied to OR counter

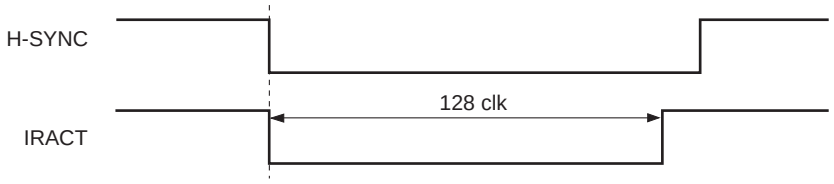
SLLAP: H, ORRS4 to 0: LLHLL, VRSP3 to 0: LLLH

IRD11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, IRU11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

IRACT (Pin 52) is an output pulse synchronized to the input HSYNC that can be output at an arbitrary position (1-dot units) and width (2-dot units).

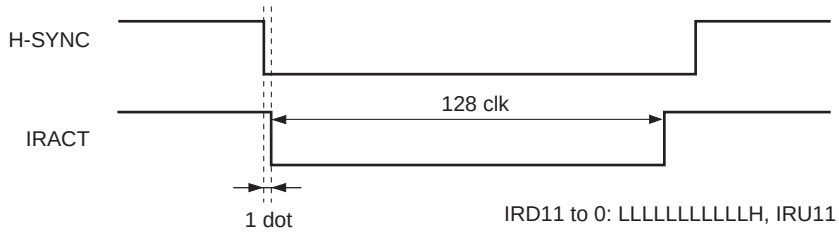
Set the pulse fall position in IRD11 to 0, and the pulse rise position in IRU11 to 0. However, the IRU0 setting is invalid. When IRD0 is H, the IRACT pulse rise position also shifts backwards by 1 dot.

The setting range is from 0 to (N – 1), but do not set IRD11 to 1 and IRU11 to 1 to the same value.



IRD11 to 0: LLLLLLLLLLLL, IRU11 to 0: LLLLHLLLLLLL, HR: H

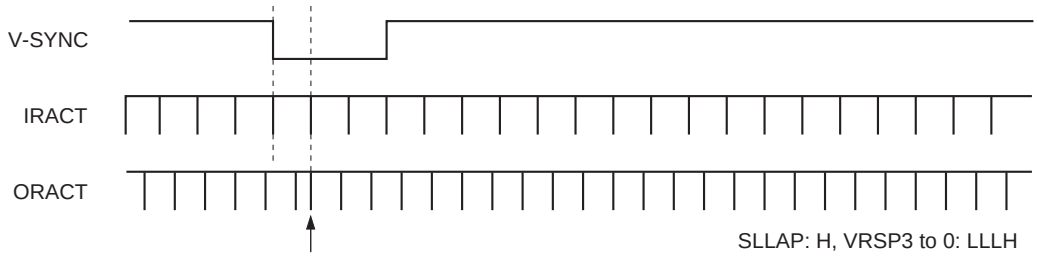
When IRD0 is H, the pulse is shifted backwards by one dot without changing the pulse width.



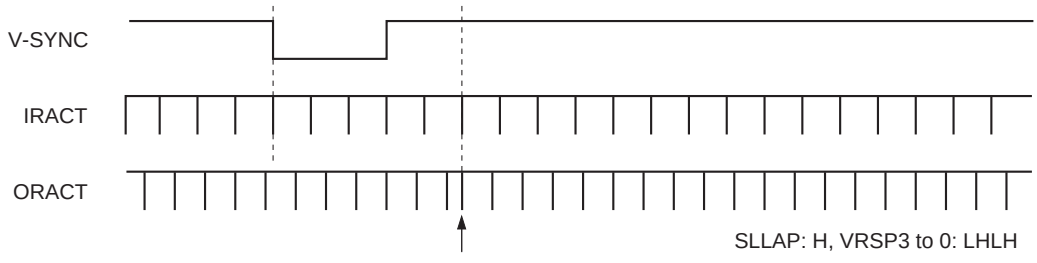
IRD11 to 0: LLLLLLLLLLLH, IRU11 to 0: LLLLHLLLLLLL, HR: H

VRSP3, 2, 1, 0

The above-mentioned OR counter applies a reset once every vertical period and at a specified input HSYNC cycle. VRSP3, 2, 1, 0 sets the number of H after VSYNC input at which this one reset every vertical period is applied. Reset is not applied when VRSP3 to 0 (LSB) is LLLL or HHHH, and applied at the set position from 1H to a maximum of 14H after VSYNC for other settings.



SLLAP: H, VRSP3 to 0: LLLH



SLLAP: H, VRSP3 to 0: LHLH

Timing at which reset is applied to OR counter

ORP11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

This setting is valid only when serial data SLLAP is H.

ORP sets the number of frequency divisions for the above-mentioned OR counter. Like PLLP11 to 0, ORP is 12-bit data and the number of frequency divisions can be set in 2-dot units up to 4096. Set the actual frequency division ratio M as follows.

M – 2 = Actual number of clk set

However, the ORP0 setting is invalid.

The number of frequency divisions set by ORP becomes the actual frequency division value of the horizontal direction timing pulses. Each pulse is asynchronous to the input HSYNC and output in sync with the OR counter.

ORD11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, ORU11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

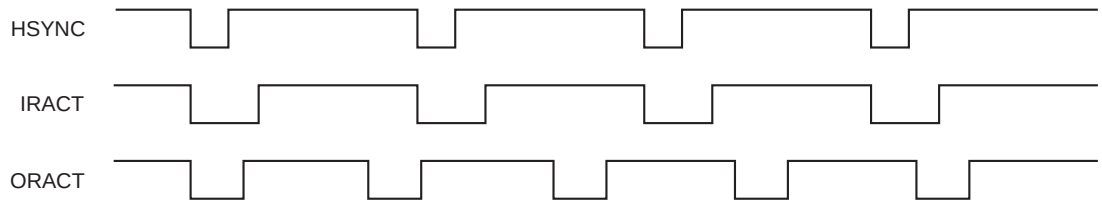
When serial data SLLAP is H, the ORACT (Pin 53) pulse is output synchronized to the OR counter that operates by the CKI3 clock that is asynchronous to the input HSYNC. This pulse can be output at an arbitrary position (1-dot units) and width (2-dot units).

Set the pulse fall position in ORD11 to 0, and the pulse rise position in ORU11 to 0. However, the ORU0 setting is invalid. When IRD0 is H, the ORACT pulse rise position also shifts backwards by 1 dot.

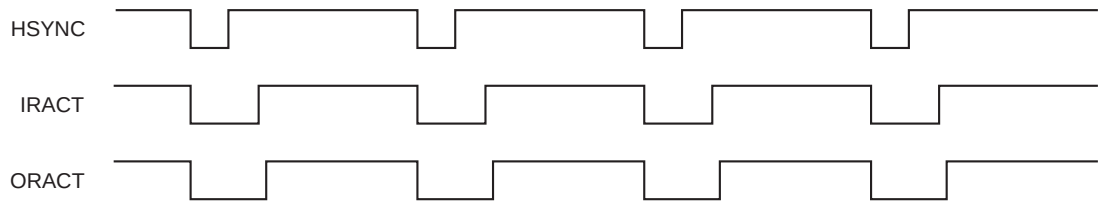
The setting range is from 0 to (M – 1), but do not set ORD11 to 1 and ORU11 to 1 to the same value.

When serial data SLLAP is L, ORACT outputs the same pulse as the IRACT pulse synchronized to the input HSYNC according to the serial data ORU11 to 0 and ORD11 to 0 settings. The IRACT and ORACT pulses can be set independently.

SLLAP: H (asynchronous to HSYNC)



SLLAP: L (synchronous to HSYNC)



IRD11 to 0: LLLLLLLLLLL, IRU11 to 0: LLLLHLLLLLL
ORD11 to 0: LLLLLLLLLLL, ORU11 to 0: LLLLHLLLLLL

Auxiliary pulse settings

HAXD11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, HAXU11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These settings are valid only when serial data SPON and HDON are H, or when SPON and HAXON are H. (See page 33.)

These bits are the setting data for the programmable pulses. When the above settings are made, the former switches the HD (Pin 31) output from the normal horizontal direction reference pulse to programmable pulse output, the latter switches the XHS (Pin 51) output to programmable pulse output, and this setting data is reflected.

The HD pulse is output synchronized to serial data HP11 to 0. In addition, the XHS pulse is synchronized to the internal PLL counter, and can be output at an arbitrary position within one horizontal period.

This setting is the same for both HDON and HAXON, so when both HDON and HAXON are H, the HD pulse and the XHS pulse cannot be adjusted independently.

VAXD11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, VAXU11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These settings are valid only when serial data SPON and VAXON are H.

These bits are the setting data for the programmable pulses. When the above settings are made, the XVS (Pin 50) output switches to programmable pulse output, and this setting data is reflected.

The XVS pulse is synchronized to the internal vertical counter, and can be output at an arbitrary position within one vertical period. (See page 33.)

Preset settings during power on

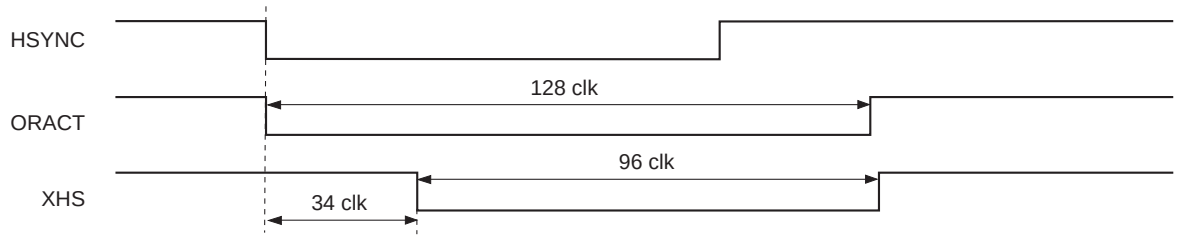
Set Pin 19 (XCLR, system clear) to L during power on to reset the system. At this time the serial data is set to the preset setting status. Set XCLR to H level and then make all the necessary settings.
The preset setting values are shown in the table below.

Address								Data							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	L	H	L	L	L	L	L	L
0	0	0	0	0	0	0	1	H	H	H	—	L	L	L	L
0	0	0	0	0	0	1	0	L	H	L	L	L	H	H	L
0	0	0	0	0	0	1	1	L	L	L	H	L	H	L	H
0	0	0	0	0	1	0	0	L	L	L	L	L	L	H	H
0	0	0	0	0	1	0	1	H	L	L	L	L	H	L	L
0	0	0	0	0	1	1	0	—	—	—	L	L	H	L	L
0	0	0	0	0	1	1	1	L	H	L	L	H	L	L	L
0	0	0	0	1	0	0	0	L	L	L	L	L	L	L	L
0	0	0	0	1	0	0	1	H	L	L	L	L	H	L	L
0	0	0	0	1	0	1	0	L	L	L	H	H	L	H	L
0	0	0	0	1	0	1	1	L	H	L	L	L	L	L	L
0	0	0	0	1	1	0	0	L	L	L	L	L	L	L	L
0	0	0	0	1	1	0	1	H	L	L	H	H	H	L	L
0	0	0	0	1	1	1	0	L	L	L	L	L	L	L	L
0	0	0	0	1	1	1	1	—	—	—	—	—	—	L	L
0	0	0	1	0	0	0	0	L	L	H	L	L	L	L	L
0	0	0	1	0	0	0	1	L	L	L	L	L	L	L	L
0	0	0	1	0	0	1	0	L	L	L	L	L	L	L	L
0	0	0	1	0	0	1	1	H	L	L	L	L	L	L	—
0	0	0	1	0	1	0	0	L	L	L	L	L	H	L	L
0	0	0	1	0	1	0	1	L	L	L	L	H	H	H	—
0	0	0	1	0	1	1	0	L	L	L	L	L	L	L	L
0	0	0	1	0	1	1	1	L	L	L	L	L	L	L	L
0	0	0	1	1	0	0	0	H	L	L	L	L	L	L	—
0	0	0	1	1	0	0	1	L	L	L	L	L	L	L	L
0	0	0	1	1	0	1	0	L	L	L	L	L	L	L	L
0	0	0	1	1	0	1	1	H	L	L	L	L	L	L	—
0	0	0	1	1	1	0	0	L	L	L	L	L	L	L	L
0	0	0	1	1	1	0	1	L	L	L	L	L	L	L	L
0	0	0	1	1	1	1	0	H	L	L	L	L	L	L	L
								—: Setting invalid							

XHS and XVS pulse output timing

XHS pulses

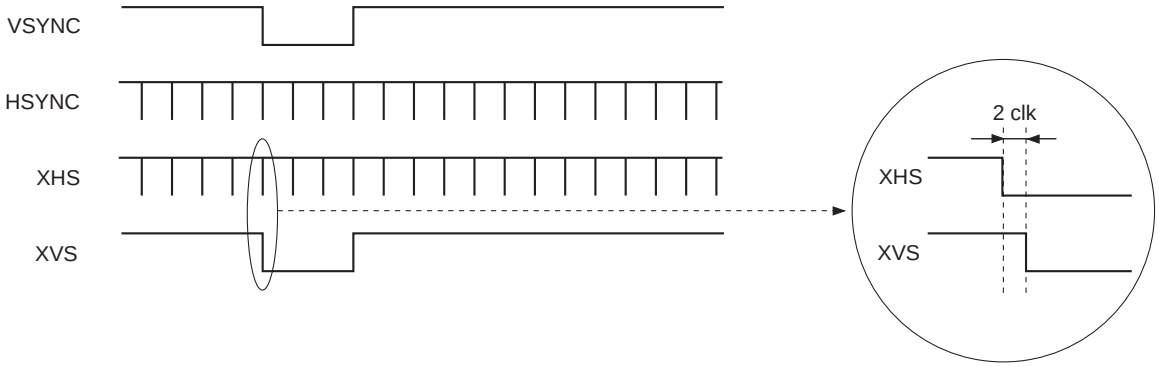
XHS pulses are output with negative polarity in 96-clock widths 34 clocks after the fall of the ORACT pulse when serial data HAXON is L. Therefore, in order to output XHS pulses correctly, set serial data ORD11 to 0 and ORU11 to 0, respectively. The preset timing is shown in the figure below.
In addition, programmable pulses are output when serial data HAXON is H.



ORD11 to 0: LLLLLLLLLLLL, ORU11 to 0: LLLLHLLLLLLL

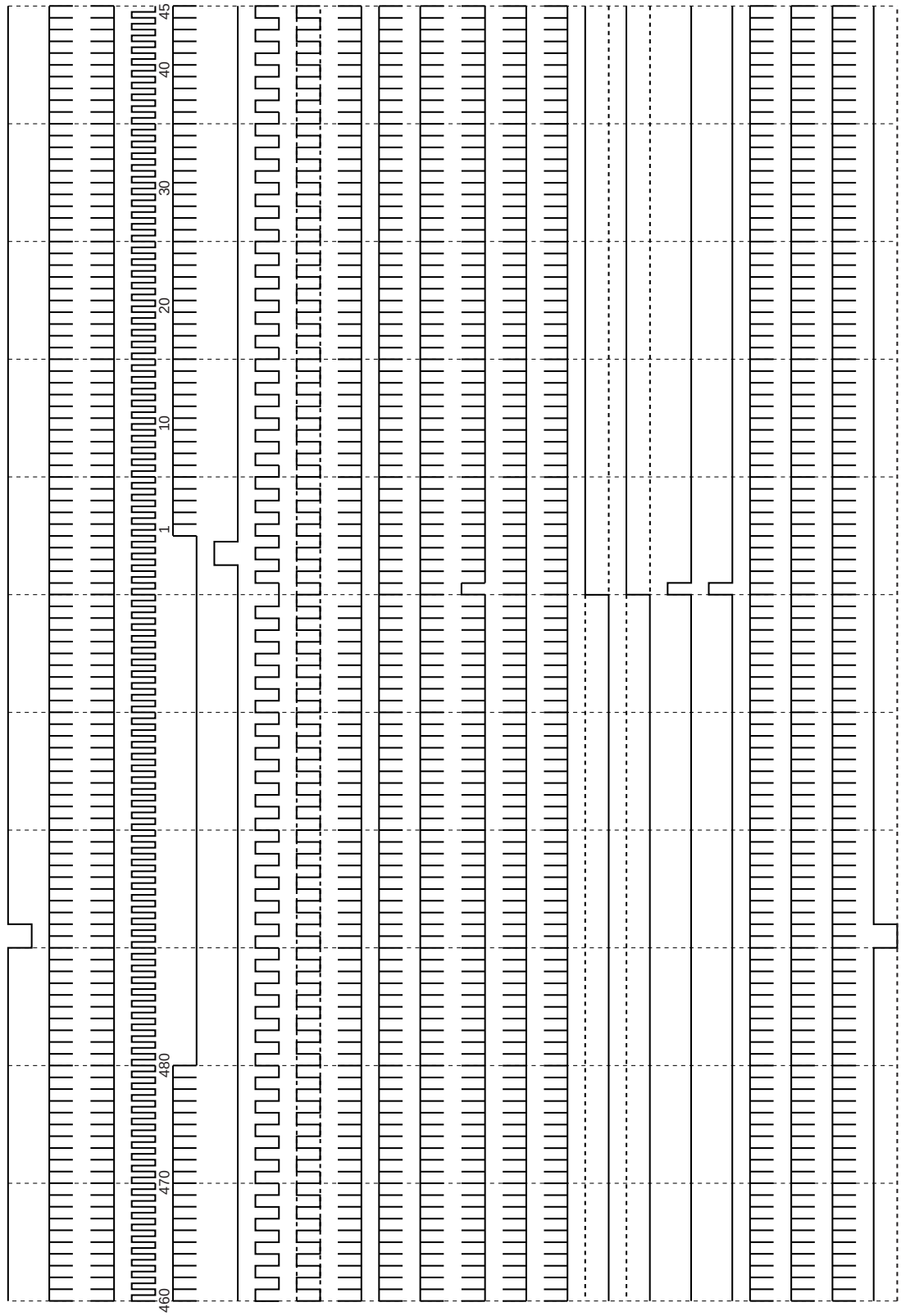
XVS pulses

XVS pulses are output with the VSYNC pulse that is latched by the XHS pulse when serial data VAXON is L. In addition, like XHS, programmable pulses are output when serial data VAXON is H.



VGA (IBM: fv 59.94Hz) 640 × 480

PLSSL2/1/0: L/L/L DWN: H VP: LLLHHHHL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/H/L

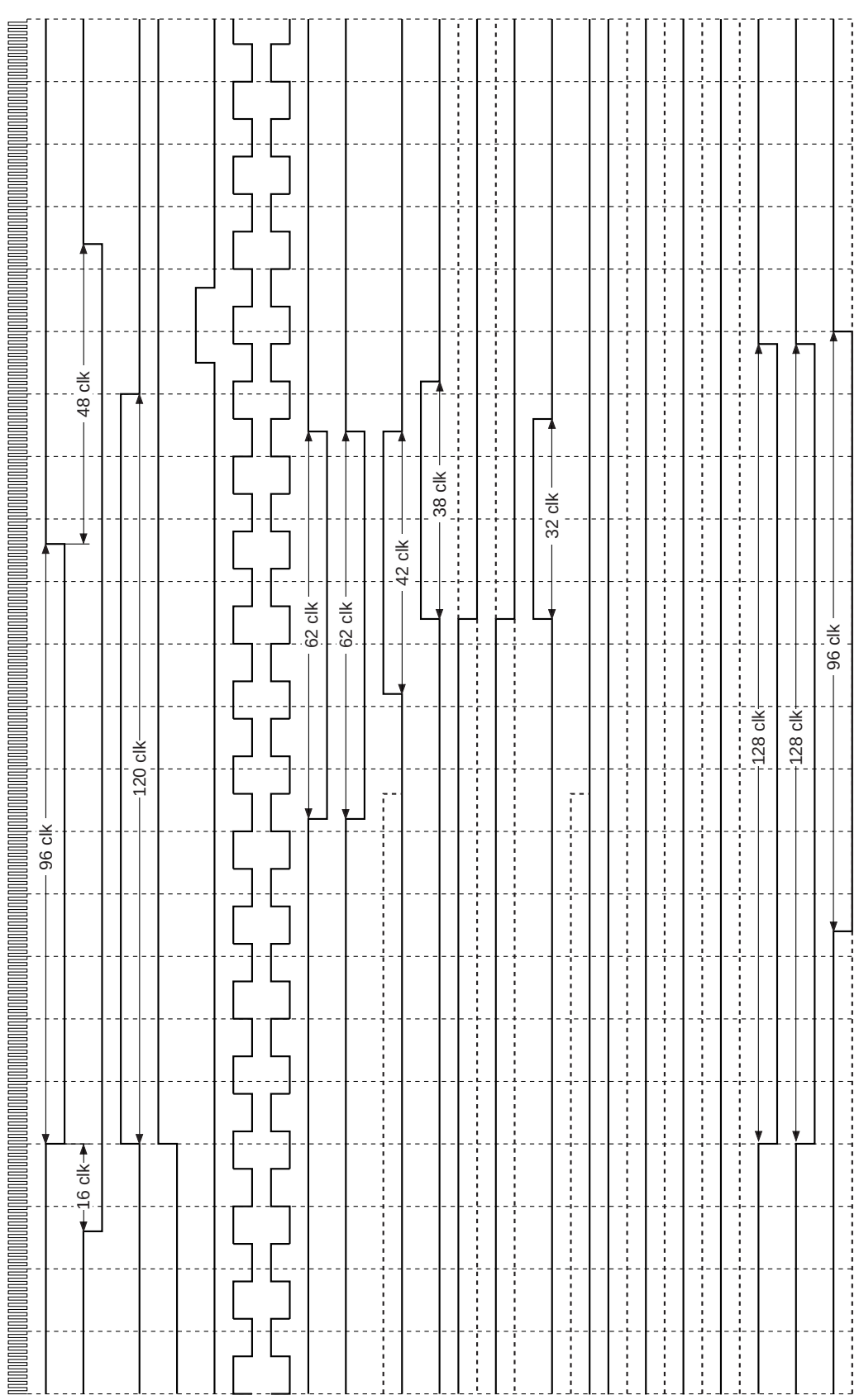


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

VGA (IBM: fv 59.94Hz) 640 × 480

PLSSL2/1/0: L/L/L PLLP: LLHHLLLHHHHL (LSB) HP: LLLLLLHHLLHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/H/L (SVGA panel, VGA mode)

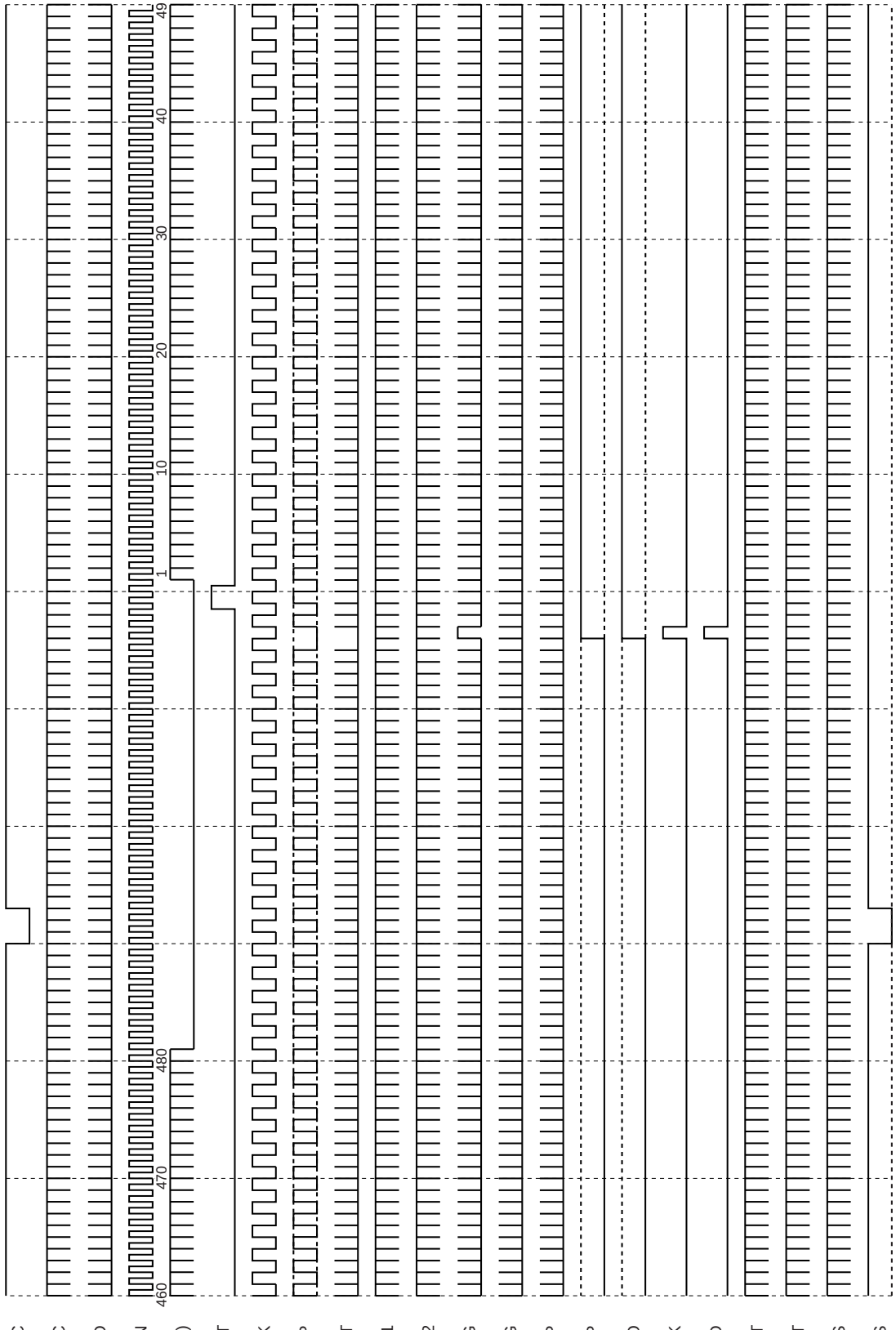
Loop Counter: 800 clk
MCK f: 25.18MHz (39.72ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

VGA (VESA72: fv 72.809Hz) 640 × 480

PLSSL2/1/0: L/L/H DWN: H VP: LLLHHLHL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/H/L

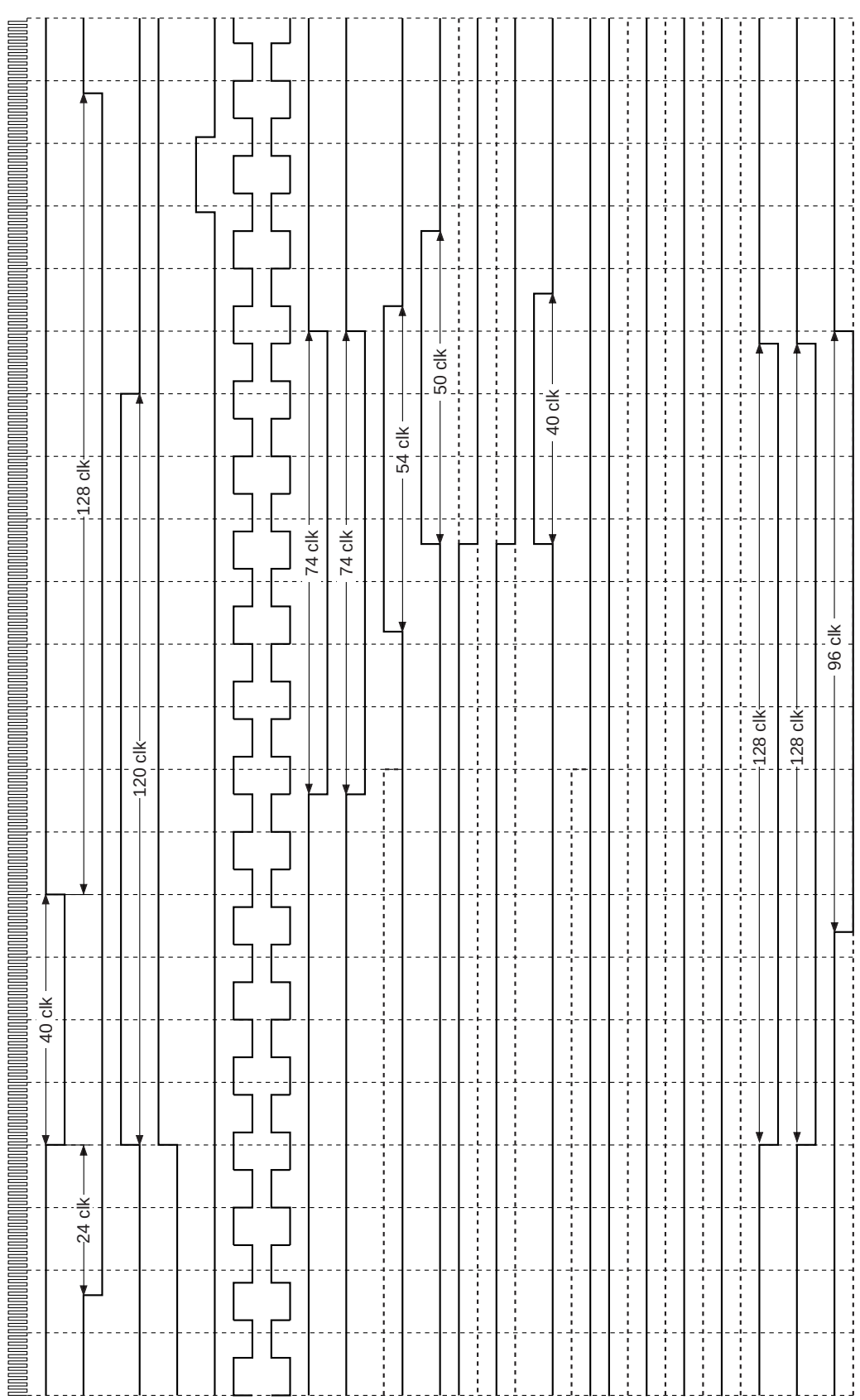


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

VGA (VESA72: fv 72.809Hz) 640 × 480

PLSSL2/1/0: L/L/H PLLP: LLHHLLHHHHHL (LSB) HP: LLLLLLHHLHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/H/L (SVGA panel, VGA mode)

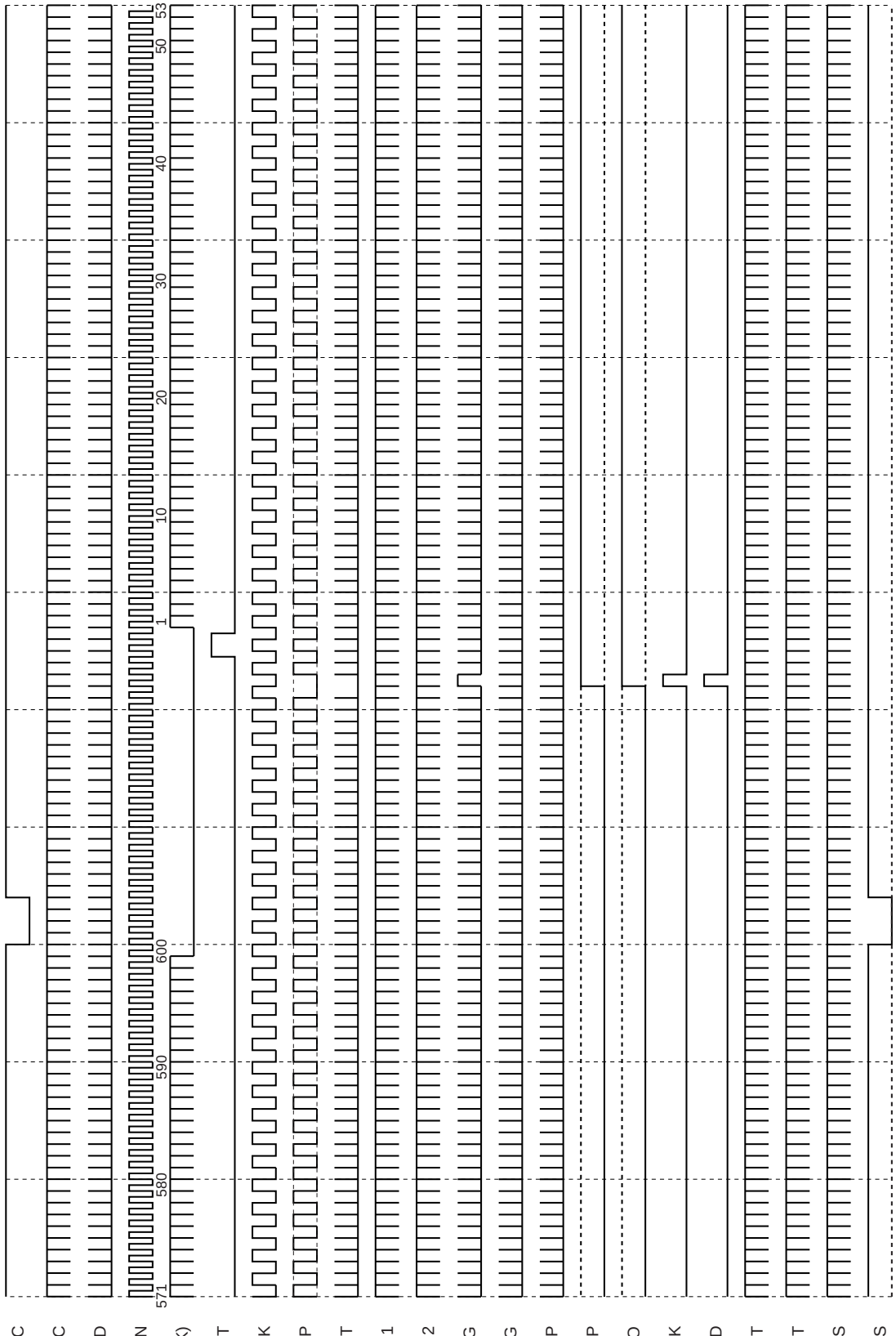
Loop Counter: 832 clk
MCK f: 31.50MHz (31.74ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA60: fv 60.32Hz) 800 × 600

PLSSL2/1/0: L/H/L DWN: H VP: LLLHLHHL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/L/L

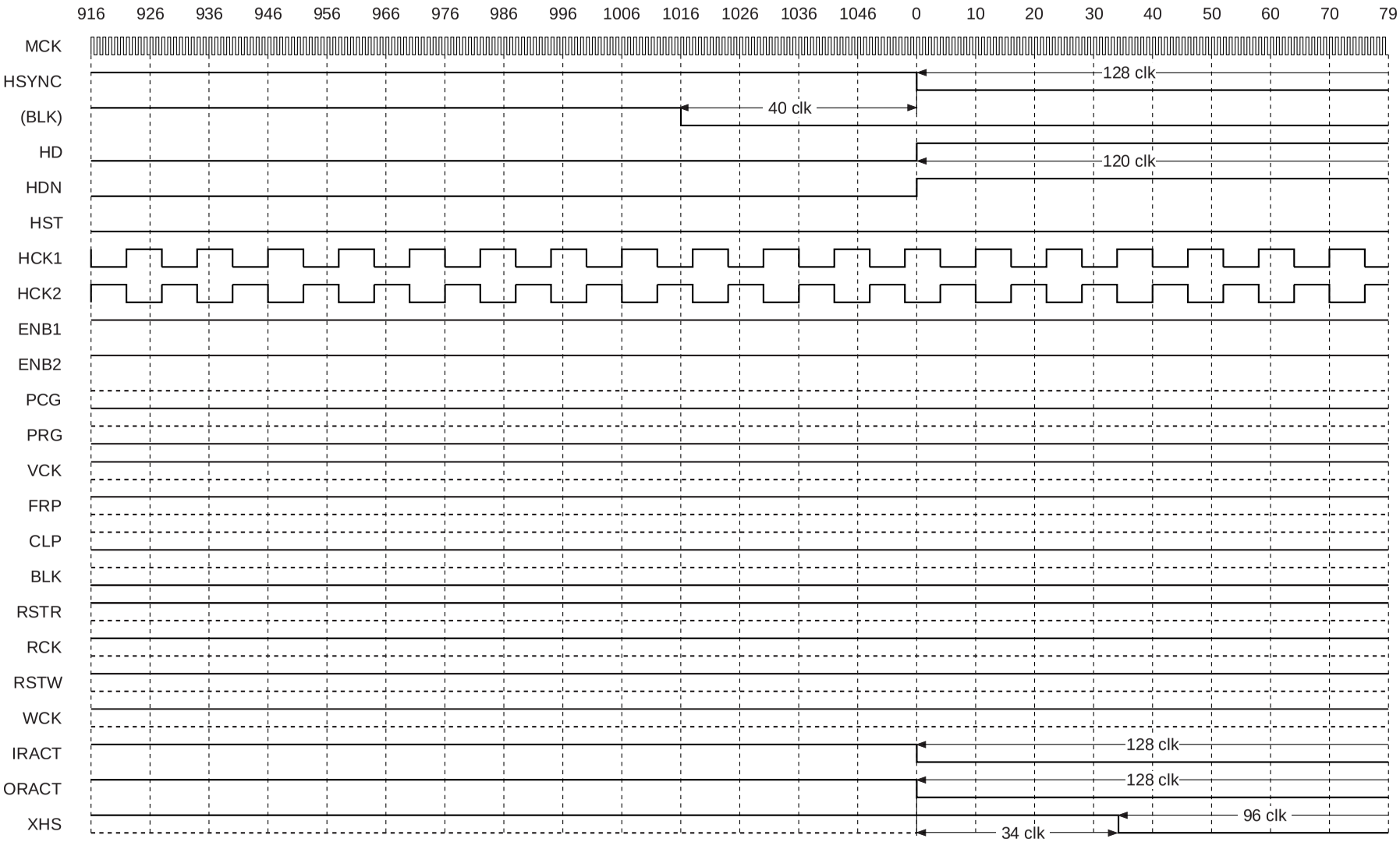


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA60: fv 60.32Hz) 800 × 600

PLSSL2/1/0: L/H/L PLLP: LHLLLLLHHHHL (LSB) HP: LLLLLHLHLLLL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: L HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/L/L (SVGA panel, SVGA mode)

Loop Counter: 1056 clk
MCK f: 40.00MHz (25.00ns)

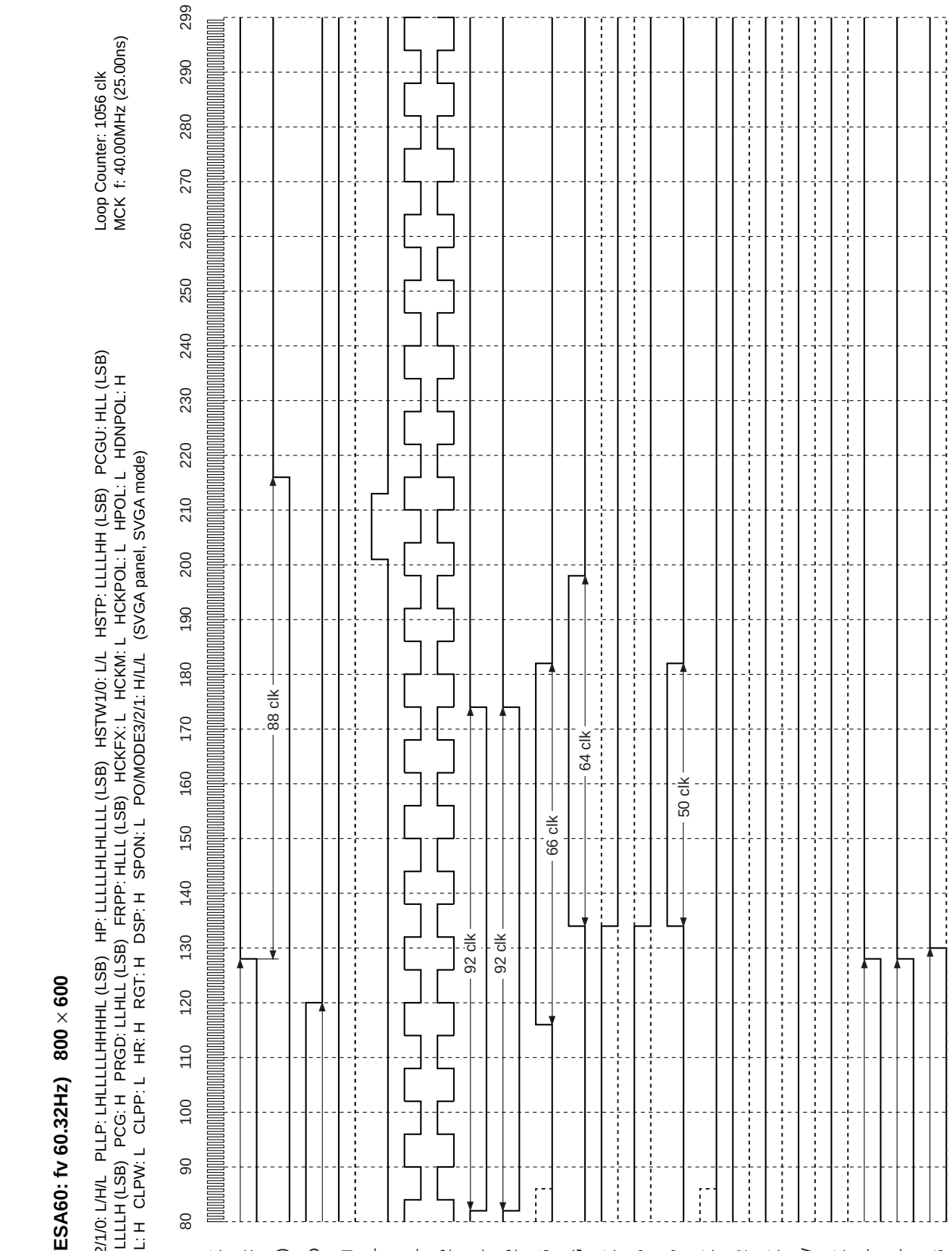


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA60: fv 60.32Hz) 800 × 600

PLSSL2/1/0: L/H/L PLLP: LHLLLLLHHHHL (LSB) HP: LLLLLHLHLLLL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: L HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/L/L (SVGA panel, SVGA mode)

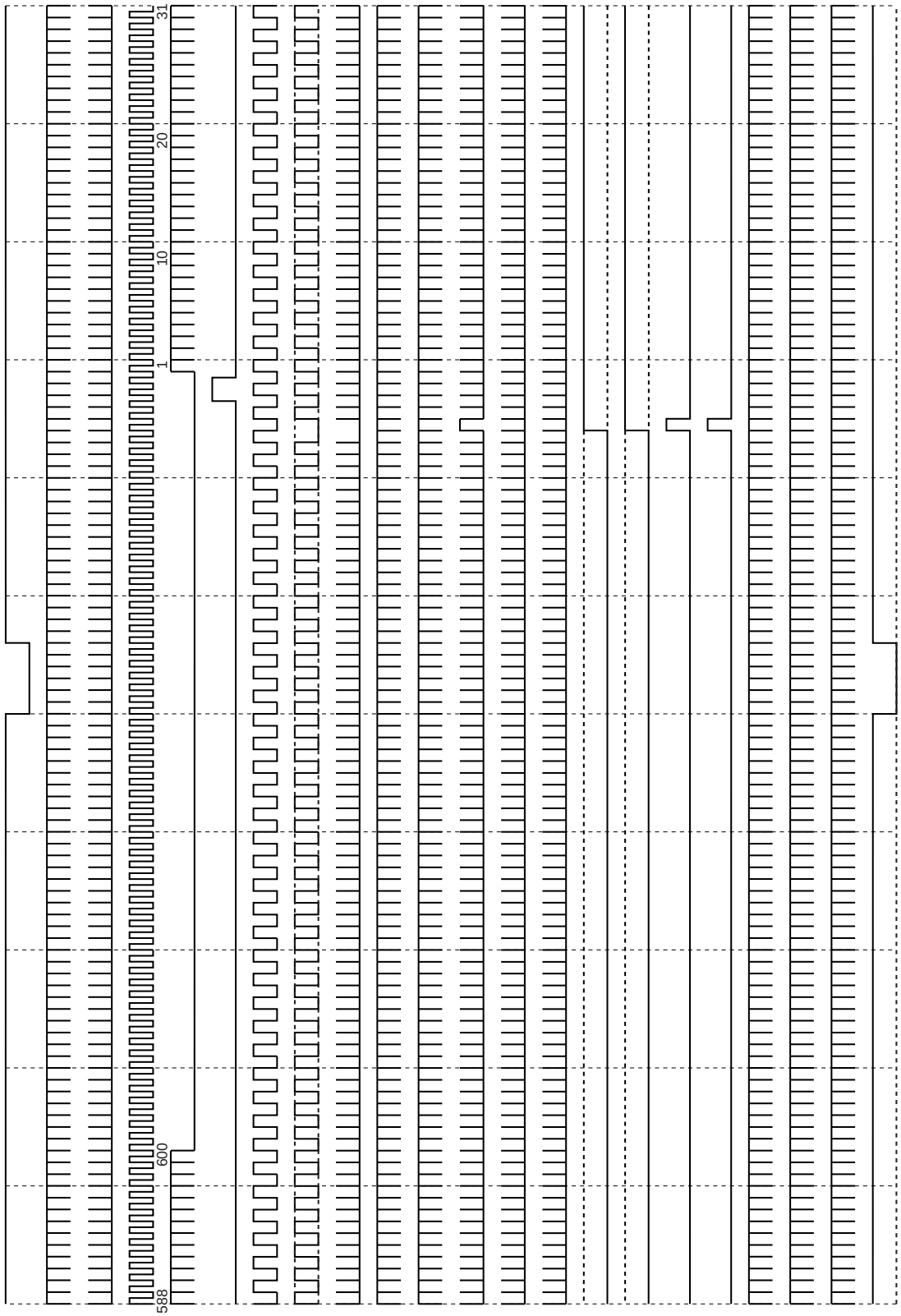
Loop Counter: 1056 clk
MCK f: 40.00MHz (25.00ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA72: fv 72.188Hz) 800 × 600

PLSSL2/1/0: L/H/H DWN: H VP: LLLHHLLL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/L/L

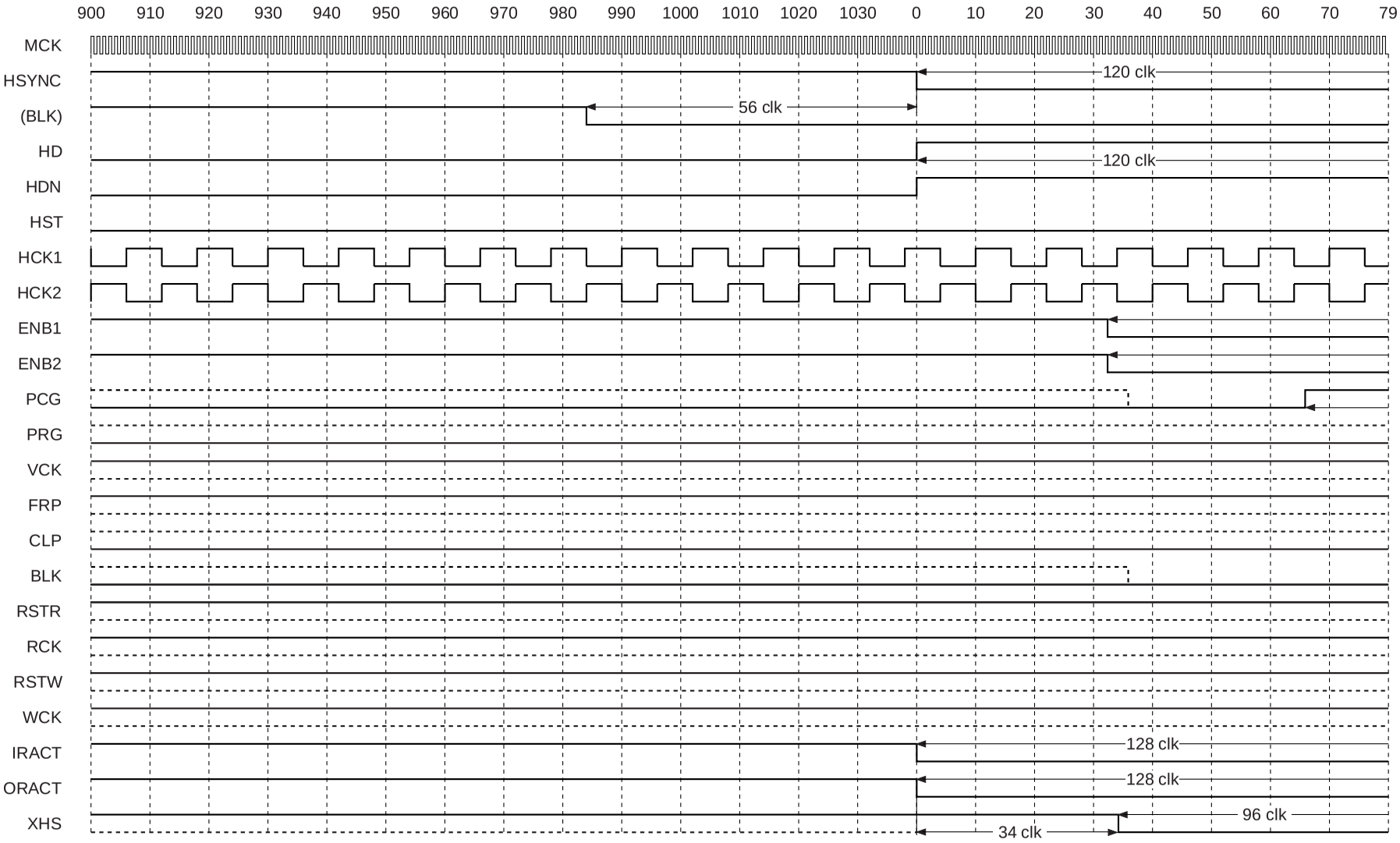


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA72: fv 72.188Hz) 800 × 600

PLSSL2/1/0: L/H/H PLLP: LHLLLLLLHHHL (LSB) HP: LLLLLLLHHHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHL (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: L HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/L/L (SVGA panel, SVGA mode)

Loop Counter: 1040 clk
MCK f: 50.00MHz (20.00ns)

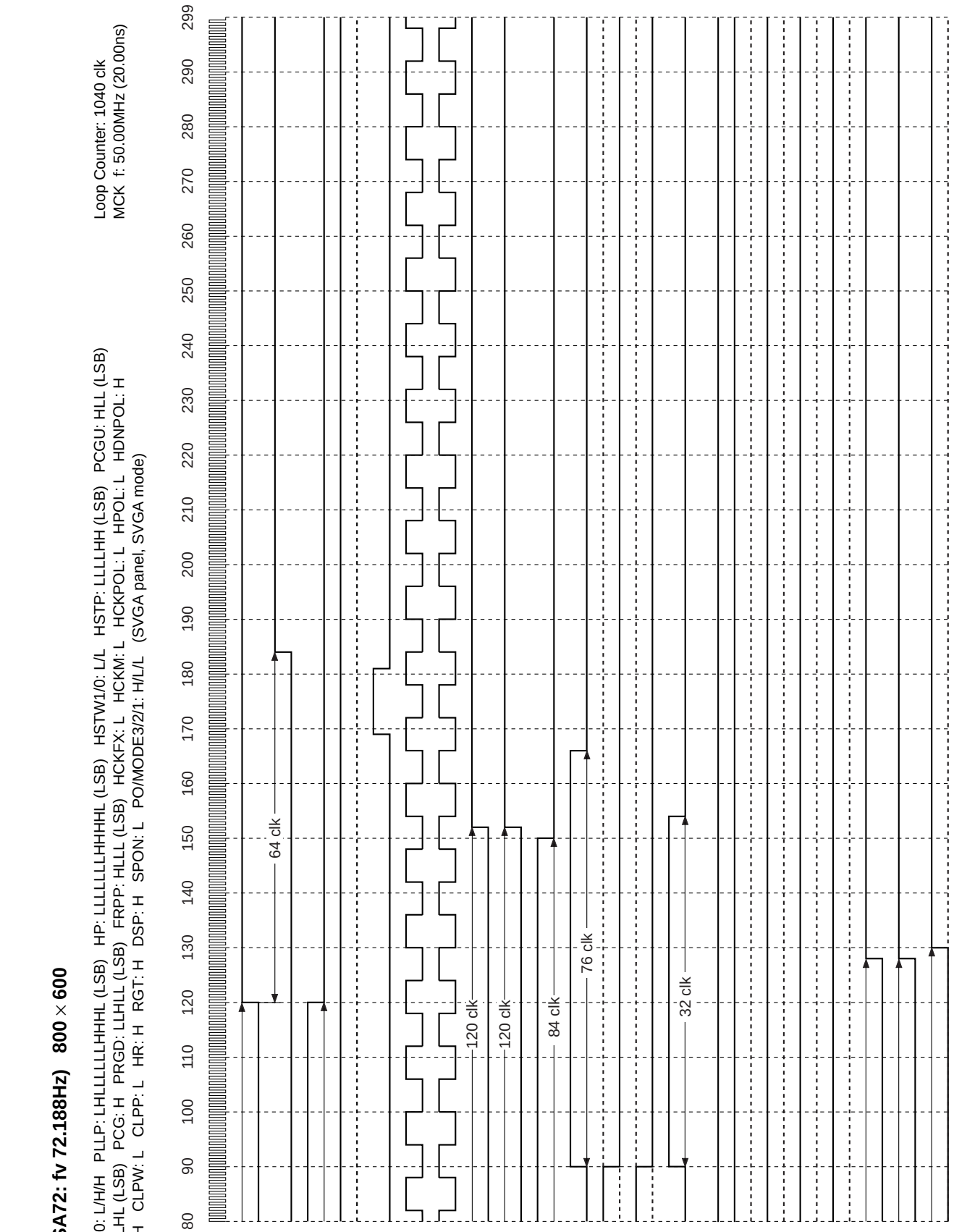


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SVGA (VESA72: fv 72.188Hz) 800 × 600

PLSSL2/1/0: L/H/H PLLP: LHLLLLLLHHHHL (LSB) HP: LLLLLLLHHHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHL (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: L HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: H/L/L (SVGA panel, SVGA mode)

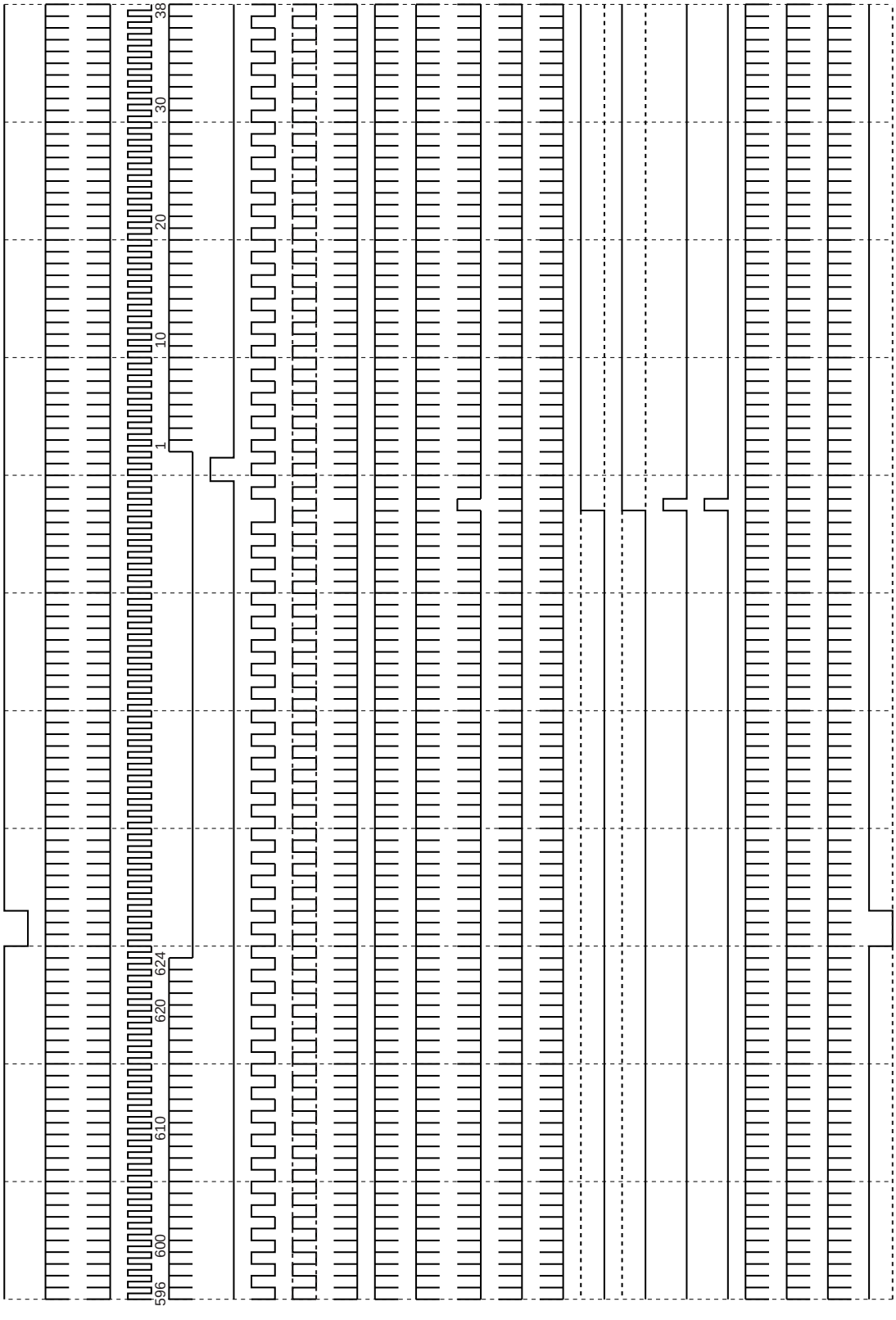
Loop Counter: 1040 clk
MCK f: 50.00MHz (20.00ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

Macintosh16 (fv 74.55Hz) 832 × 624

PLSSL2/1/0: H/L/L DWN: H VP: LLHLLHLH (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/L/L

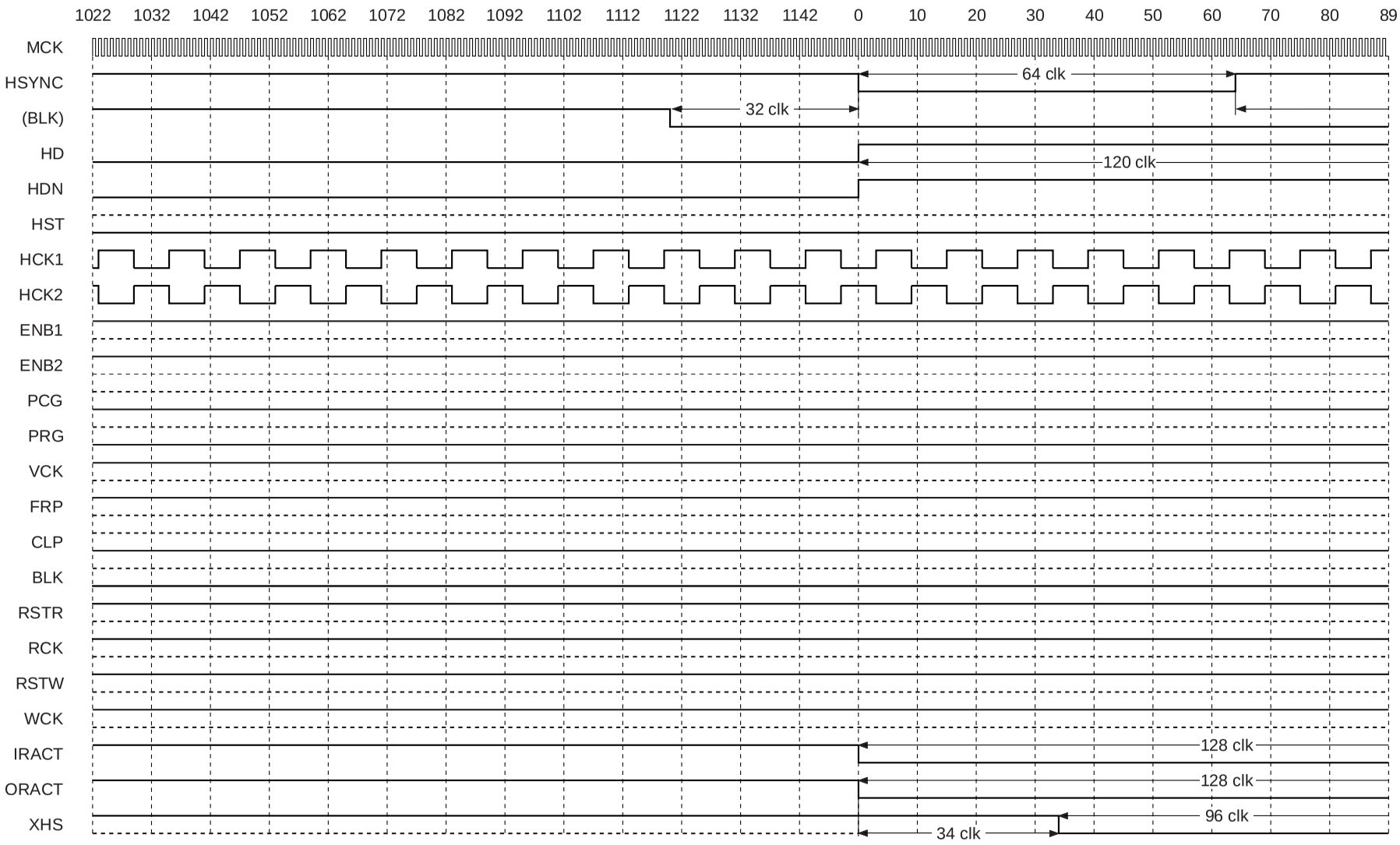


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

Macintosh16 (fv 74.55Hz) 832 × 624

PLSSL2/1/0: H/L/L PLLP: LHLLLHHHHHHL (LSB) HP: LLLLLHLHHHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/L/L (Mac16 panel, Mac16 mode)

Loop Counter: 1152 clk
MCK f: 57.28MHz (17.46ns)

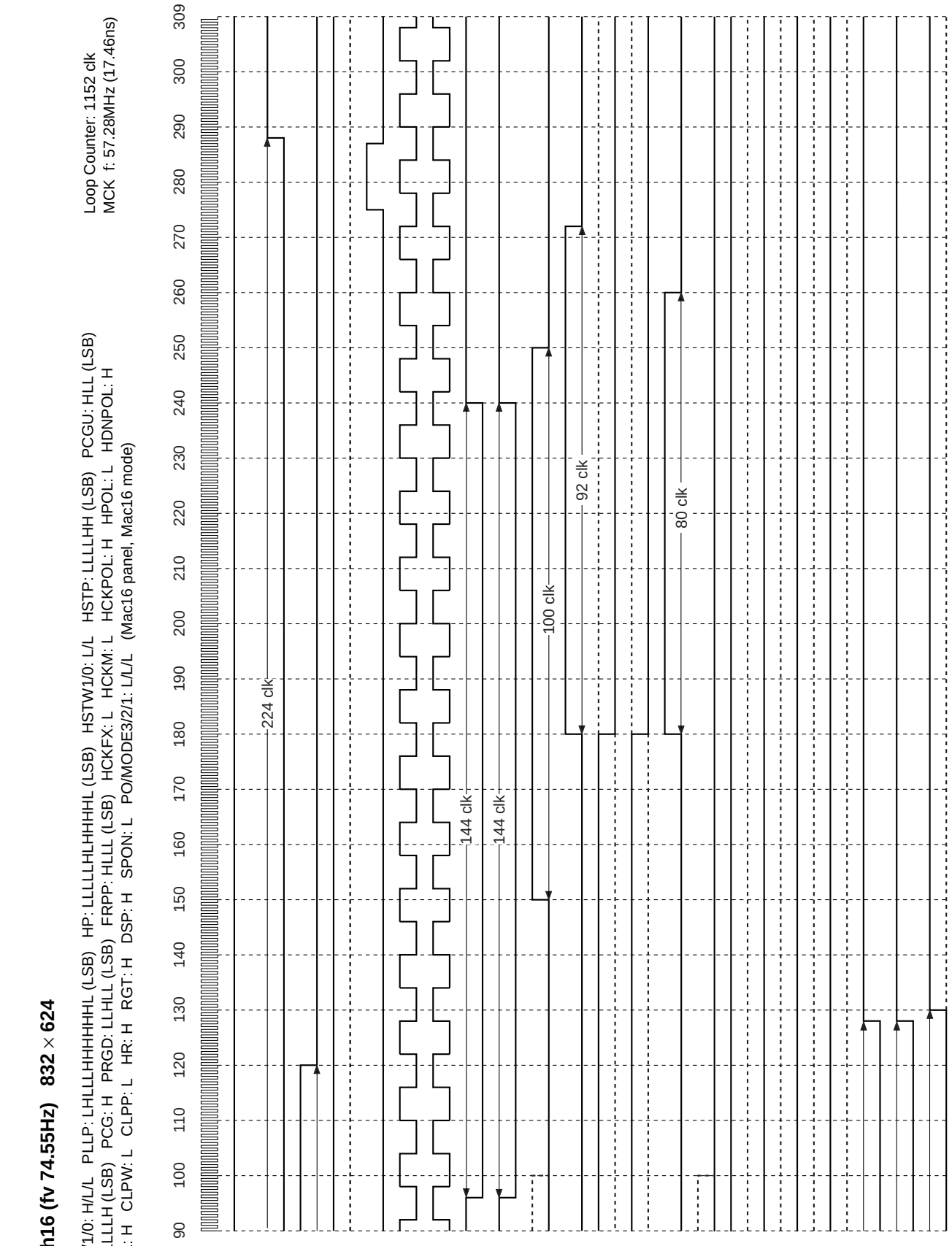


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

Macintosh16 (fv 74.55Hz) 832 × 624

PLSSL2/1/0: H/L/L PLLP: LHLLLHHHHHHL (LSB) HP: LLLLLHLHHHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/L/L (Mac16 mode)

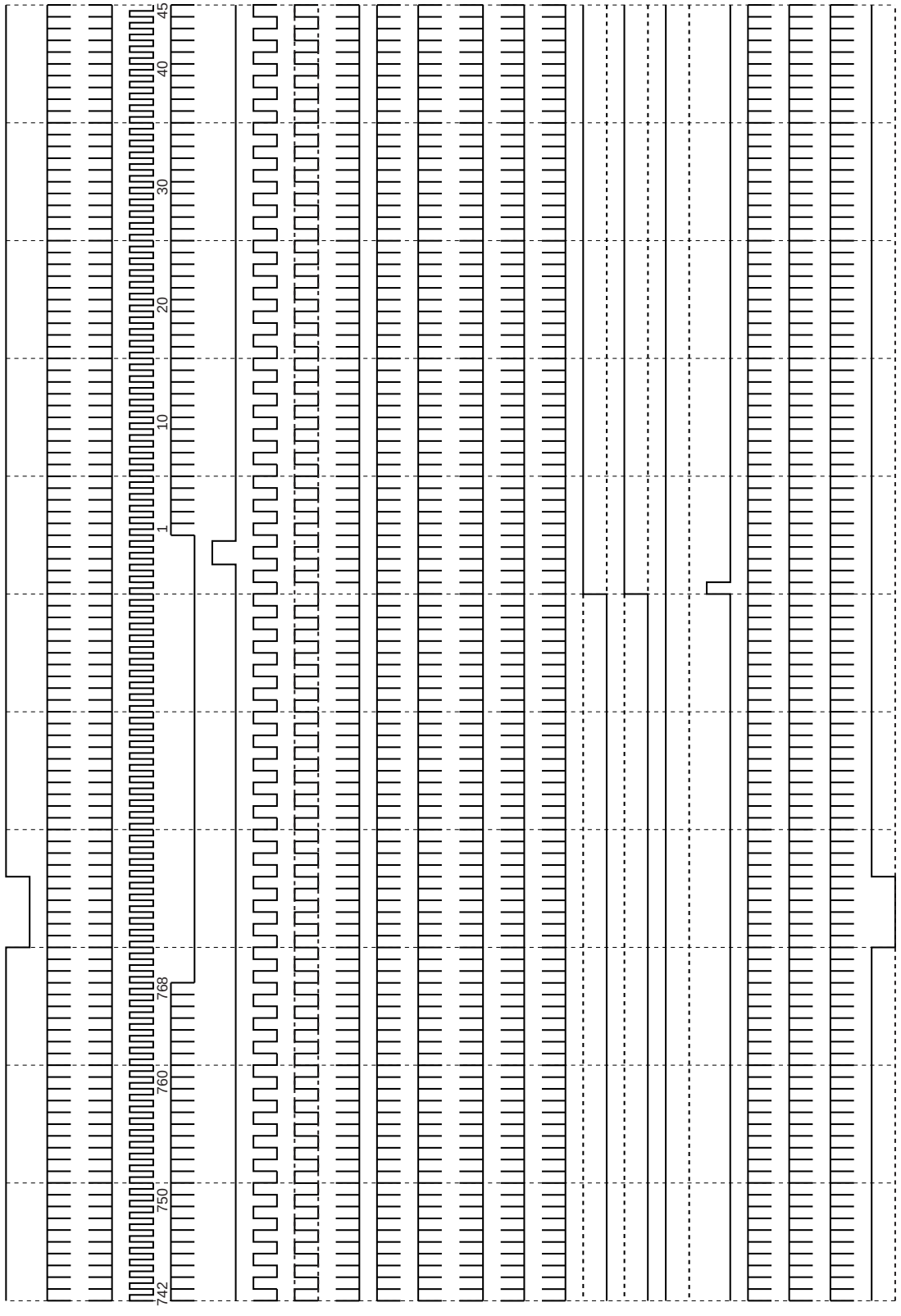
Loop Counter: 1152 clk
MCK f: 57.28MHz (17.46ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA60: fv 60.00Hz) 1024 × 768

PLSSL2/1/0: H/L/H DWN: H VP: LLLHHHHL (LSB) FRP1/0: L/L VSTFX: H VSTPOL: H VPOL: L VGAV: H BLKON: L BLKPOL: L
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/H/H

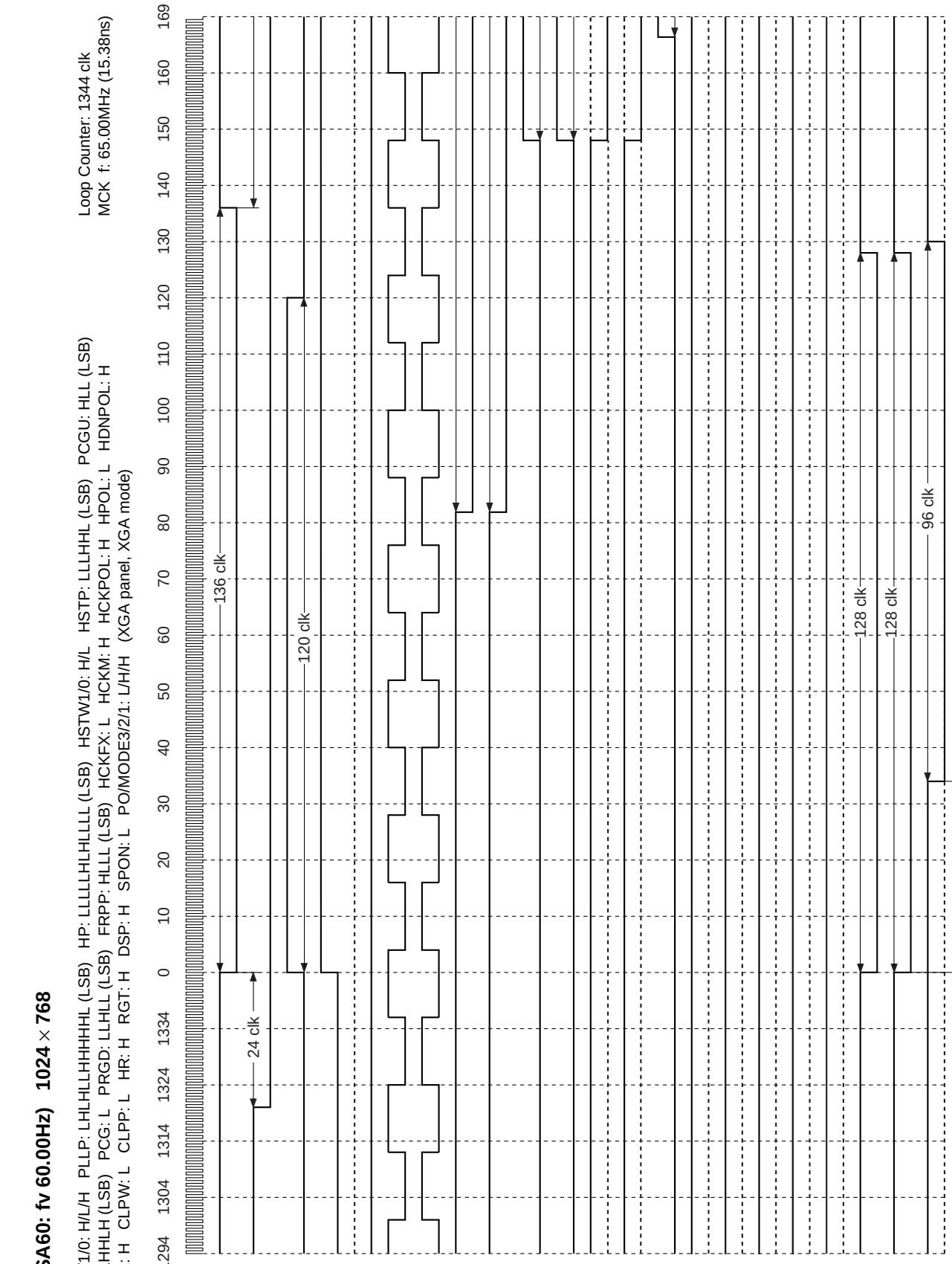


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA60: fv 60.00Hz) 1024 × 768

PLSSL2/1/0: H/L/H PLLP: LHLHLLHHHHHL (LSB) HP: LLLLLHLHLLLL (LSB) HSTW1/0: H/L HSTP: LLLHHL (LSB) PCGU: HLL (LSB)
PCGD: LHHLH (LSB) PCG: L PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, XGA mode)

Loop Counter: 1344 clk
MCK f: 65.00MHz (15.38ns)

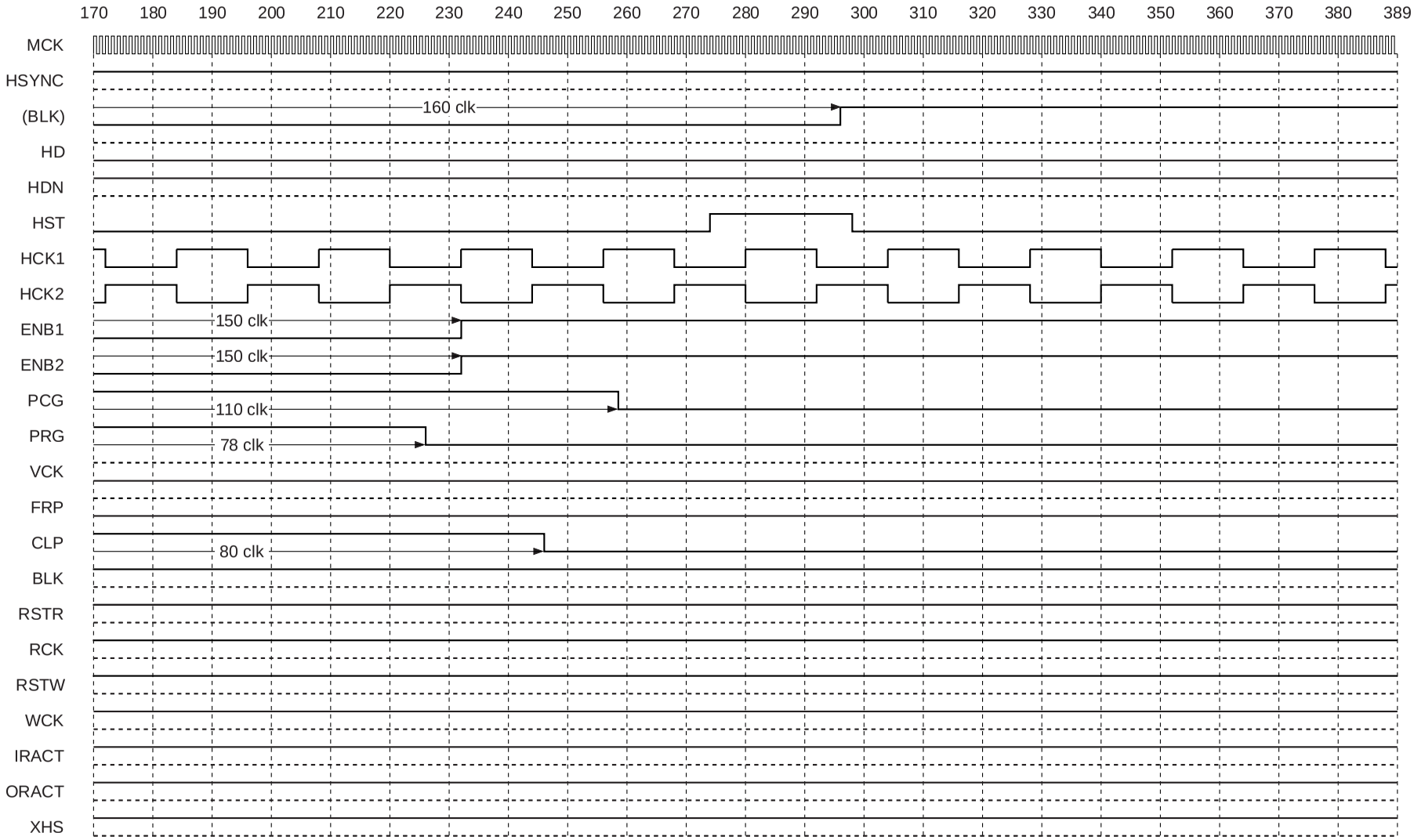


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA60: fv 60.00Hz) 1024 × 768

PLSSL2/1/0: H/L/H PLLP: LHLHLLHHHHHL (LSB) HP: LLLLLHLHLLLL (LSB) HSTW1/0: H/L HSTP: LLLHHL (LSB) PCGU: HLL (LSB)
PCGD: LHHLH (LSB) PCG: L PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, XGA mode)

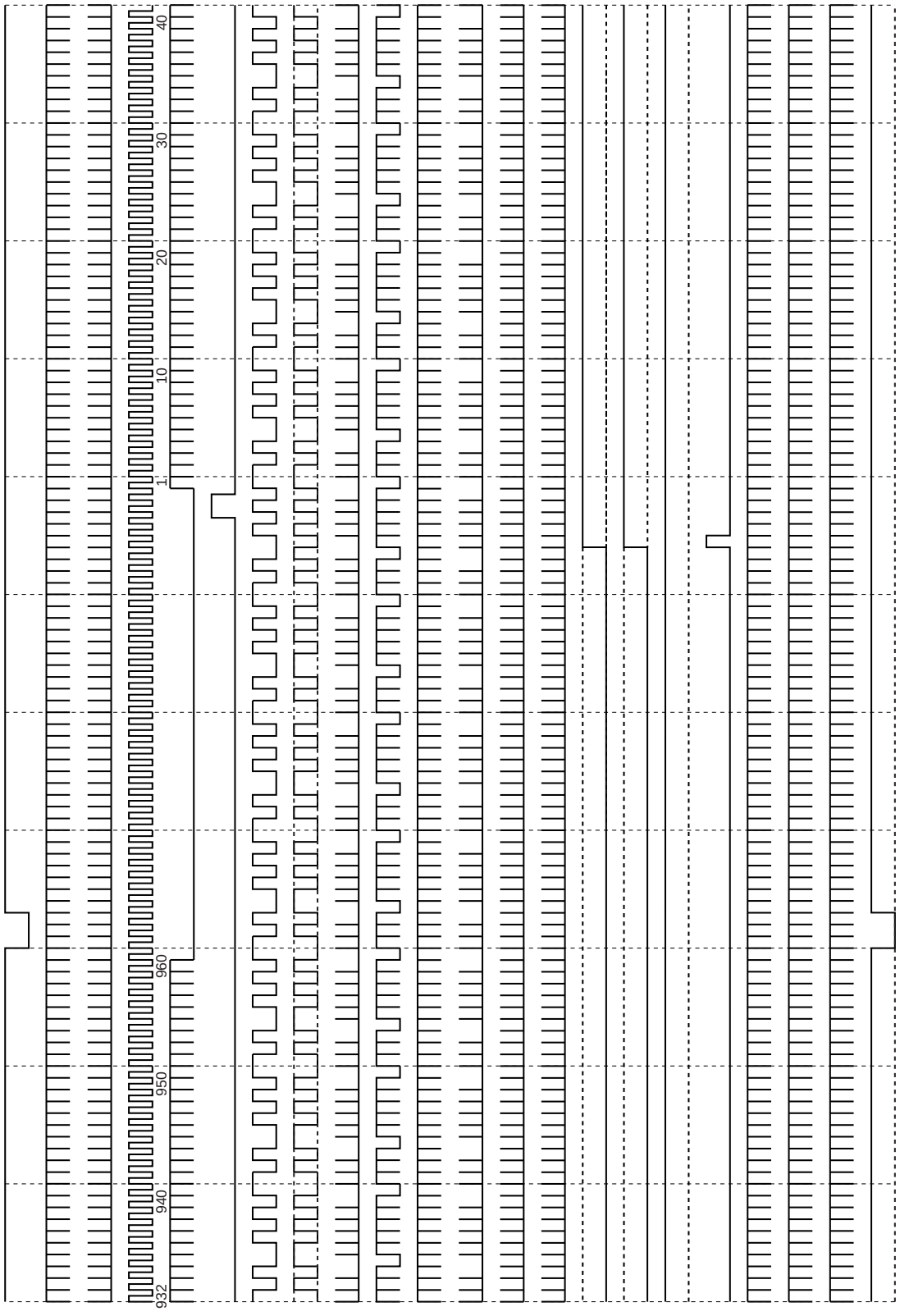
Loop Counter: 1344 clk
MCK f: 65.00MHz (15.38ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

(VESA60: fv 60.00Hz) 1280 × 960

PLSSL2/1/0: H/H/L DWN: H VP: LLHLLLHL (LSB) FRP1/0: L/L VSTFX: H VSTPOL: H VPOL: L VGAV: H BLKON: L BLKPOL: L
FMBK: H MBKA: LHLHL (LSB) MBKB: LHLH (LSB) MBKZ: LLHH (LSB) DWN: H PO/MODE3/2/1: L/H/H

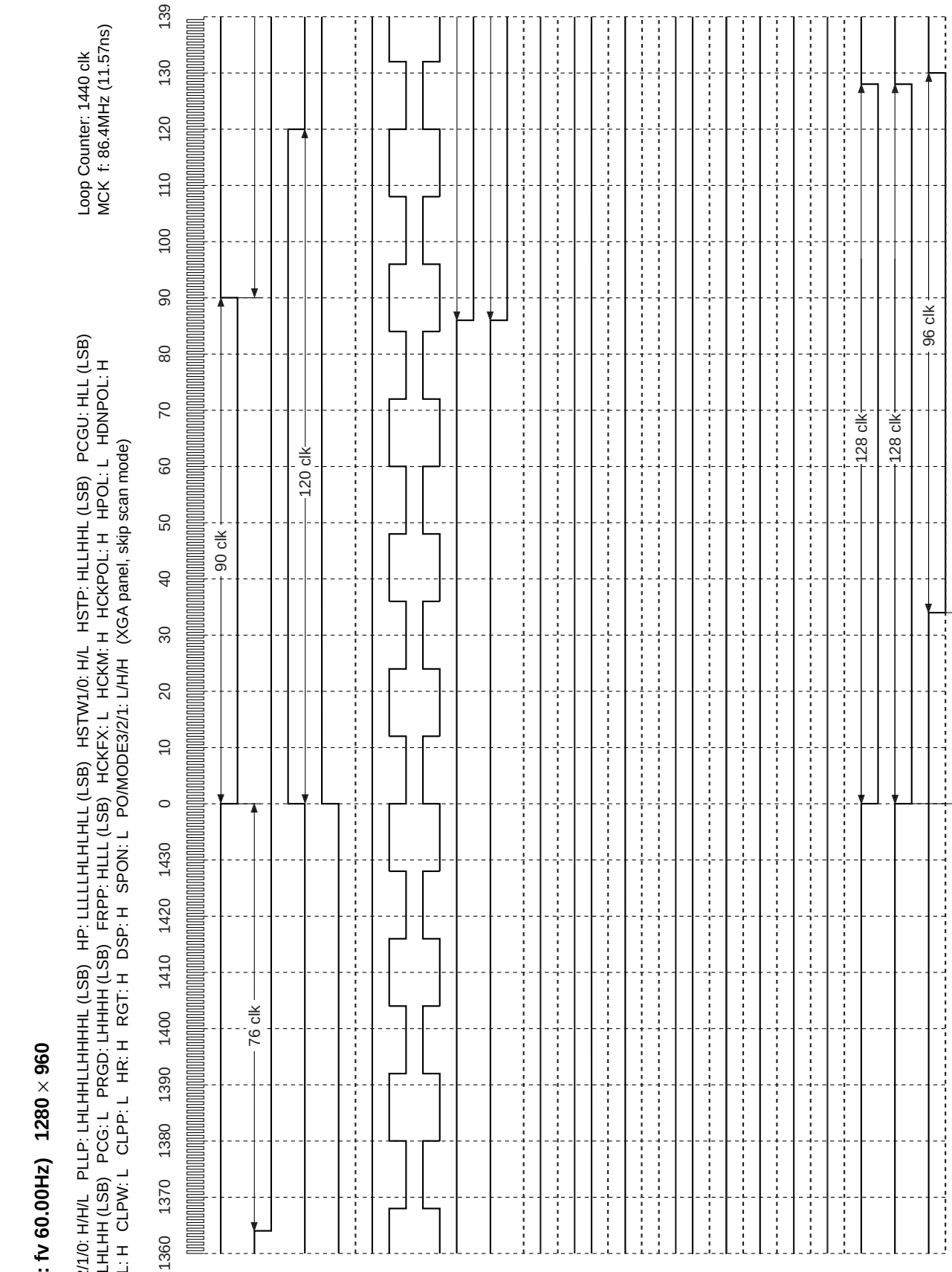


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

(VESA60: fv 60.00Hz) 1280 × 960

PLSSL2/1/0: H/H/L PLLP: LHLHHLLHHHHHL (LSB) HP: LLLLLHLHLHLL (LSB) HSTW1/0: H/L HSTP: HLLHHL (LSB) PCGU: HLL (LSB)
PCGD: LHLHH (LSB) PCG: L PRGD: LHHHH (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, skip scan mode)

Loop Counter: 1440 clk
MCK f: 86.4MHz (11.57ns)

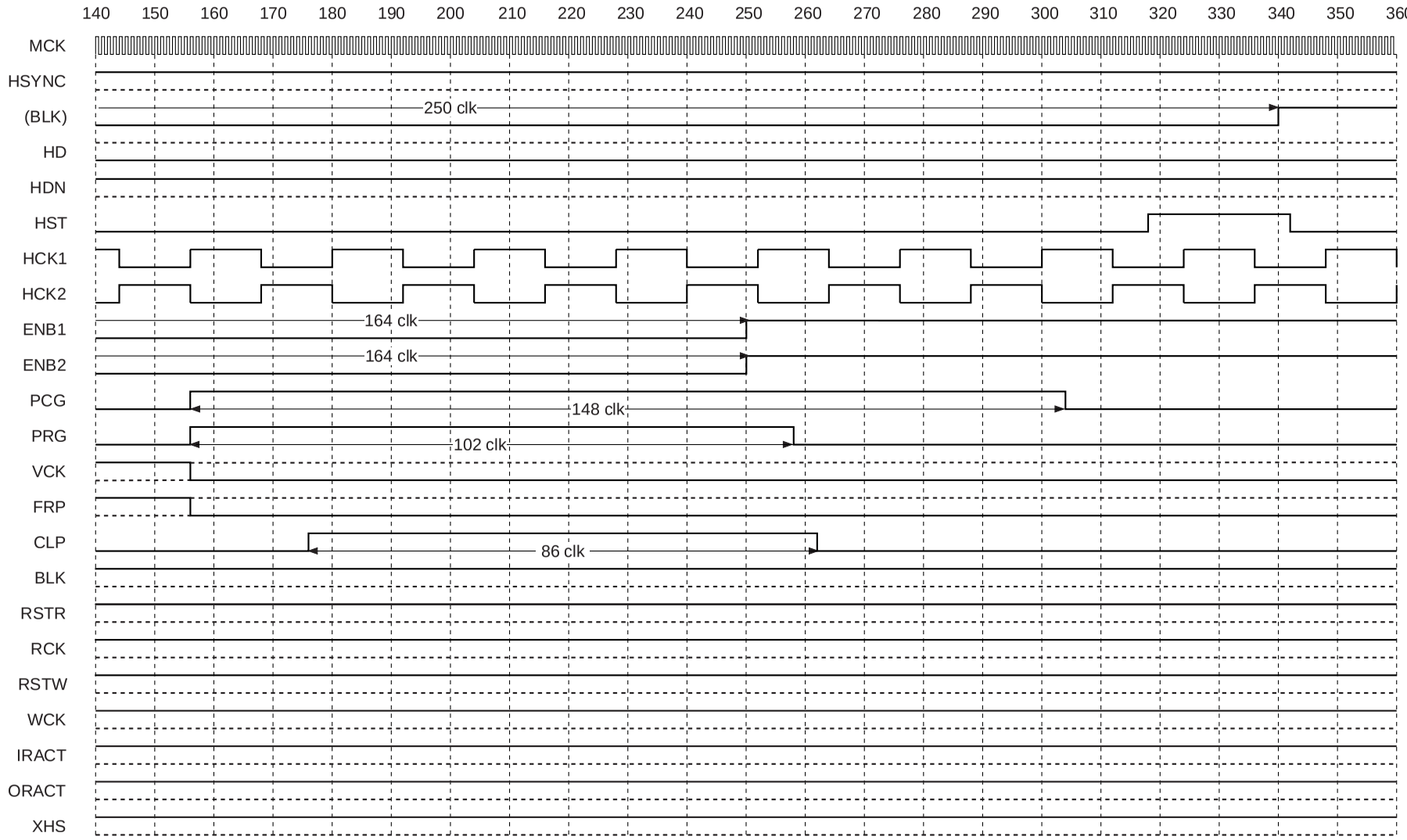


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

(VESA60: fv 60.00Hz) 1280 × 960

PLSSL2/1/0: H/H/L PLLP: LHLHHLLHHHHL (LSB) HP: LLLLLHLHLHLL (LSB) HSTW1/0: H/L HSTP: HLLHHL (LSB) PCGU: HLL (LSB)
PCGD: LHLHH (LSB) PCG: L PRGD: LHHHH (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, skip scan mode)

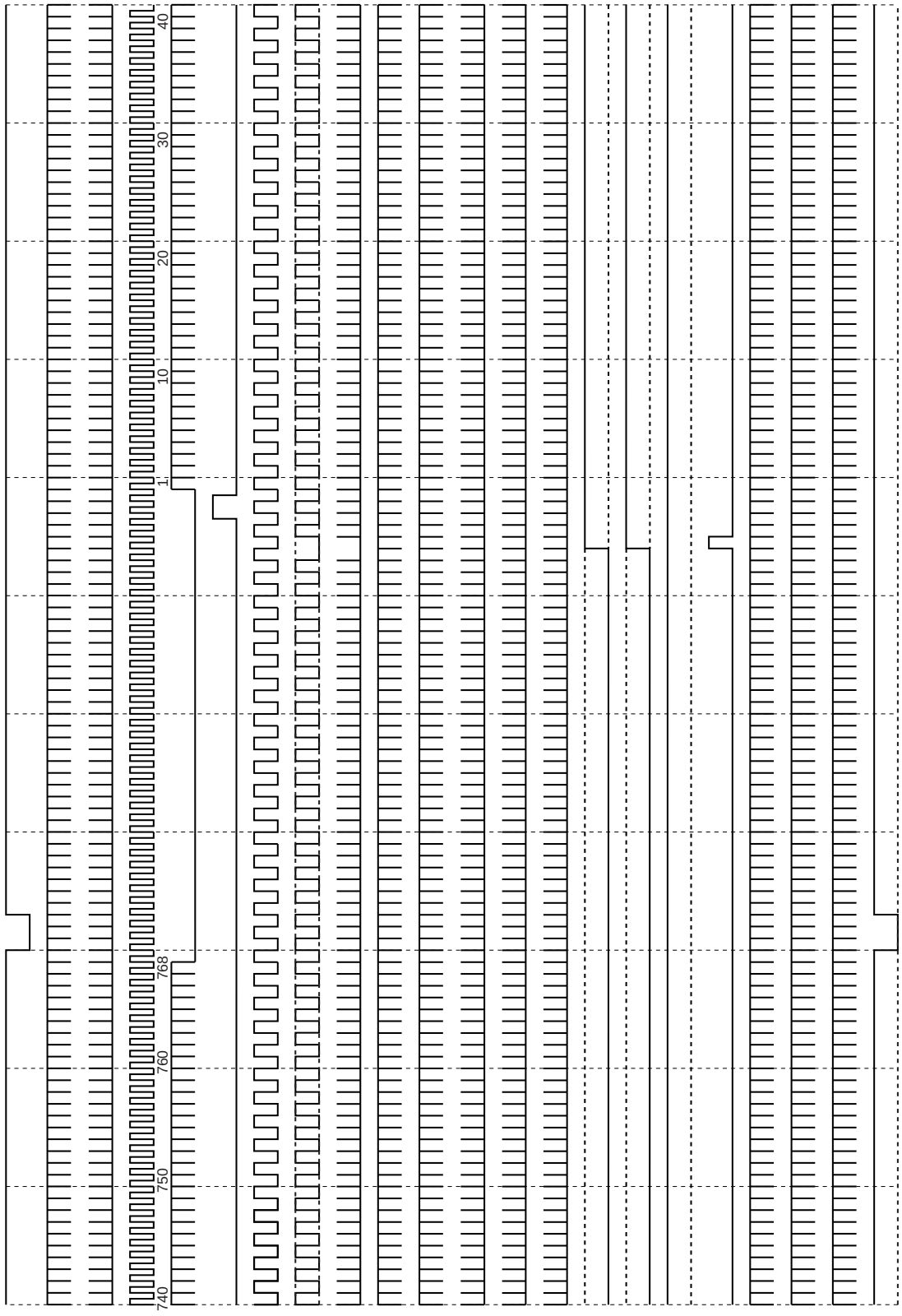
Loop Counter: 1440 clk
MCK f: 86.4MHz (11.57ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA85: fv 84.99Hz) 1024 × 768

PLSSL2/1/0: H/H/H DWN: H VP: LLHLLLHL (LSB) FRP1/0: L/L VSTFX: H VSTPOL: H VPOL: L VGAV: H BLKON: L BLKPOL: L
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/H/H

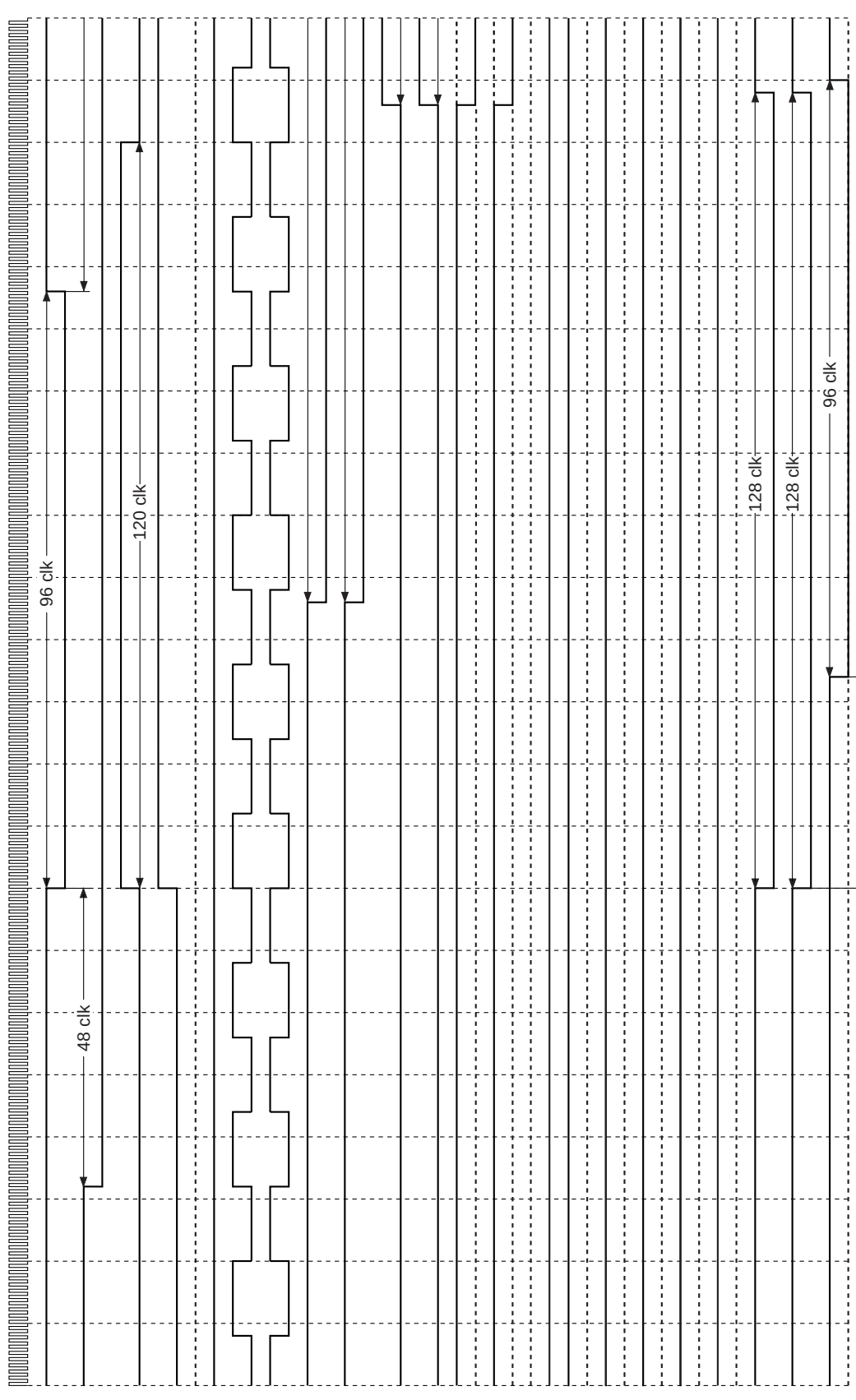


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA85: fv 84.99Hz) 1024 × 768

PLSSL2/1/0: H/H/H PLLP: LHLHLHLHHHHL (LSB) HP: LLLLLLHLHHLL (LSB) HSTW1/0: H/L HSTP: LLLHHL (LSB) PCGU: HLL (LSB)
PCGD: HHLLH (LSB) PCG: L PRGD: LHHHH (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, XGA mode)

Loop Counter: 1376 clk
MCK f: 94.50MHz (10.58ns)

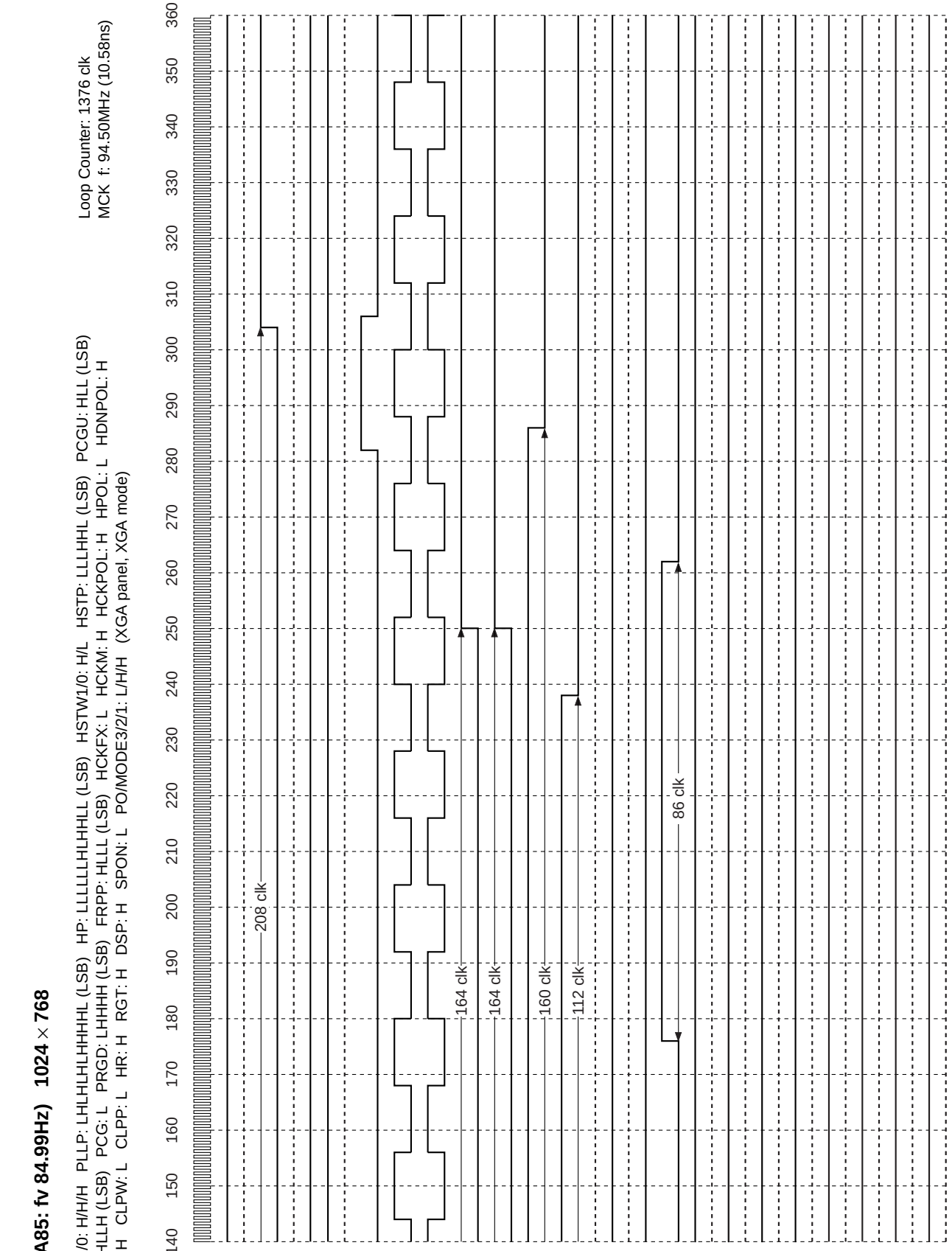


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

XGA (VESA85: fv 84.99Hz) 1024 × 768

PLSSL2/1/0: H/H/H PLLP: LHLHLHLHHHHL (LSB) HP: LLLLLLHLHHLL (LSB) HSTW1/0: H/L HSTP: LLLHHL (LSB) PCGU: HLL (LSB)
PCGD: HHLLH (LSB) PCG: L PRGD: LHHHH (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: H HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/H/H (XGA panel, XGA mode)

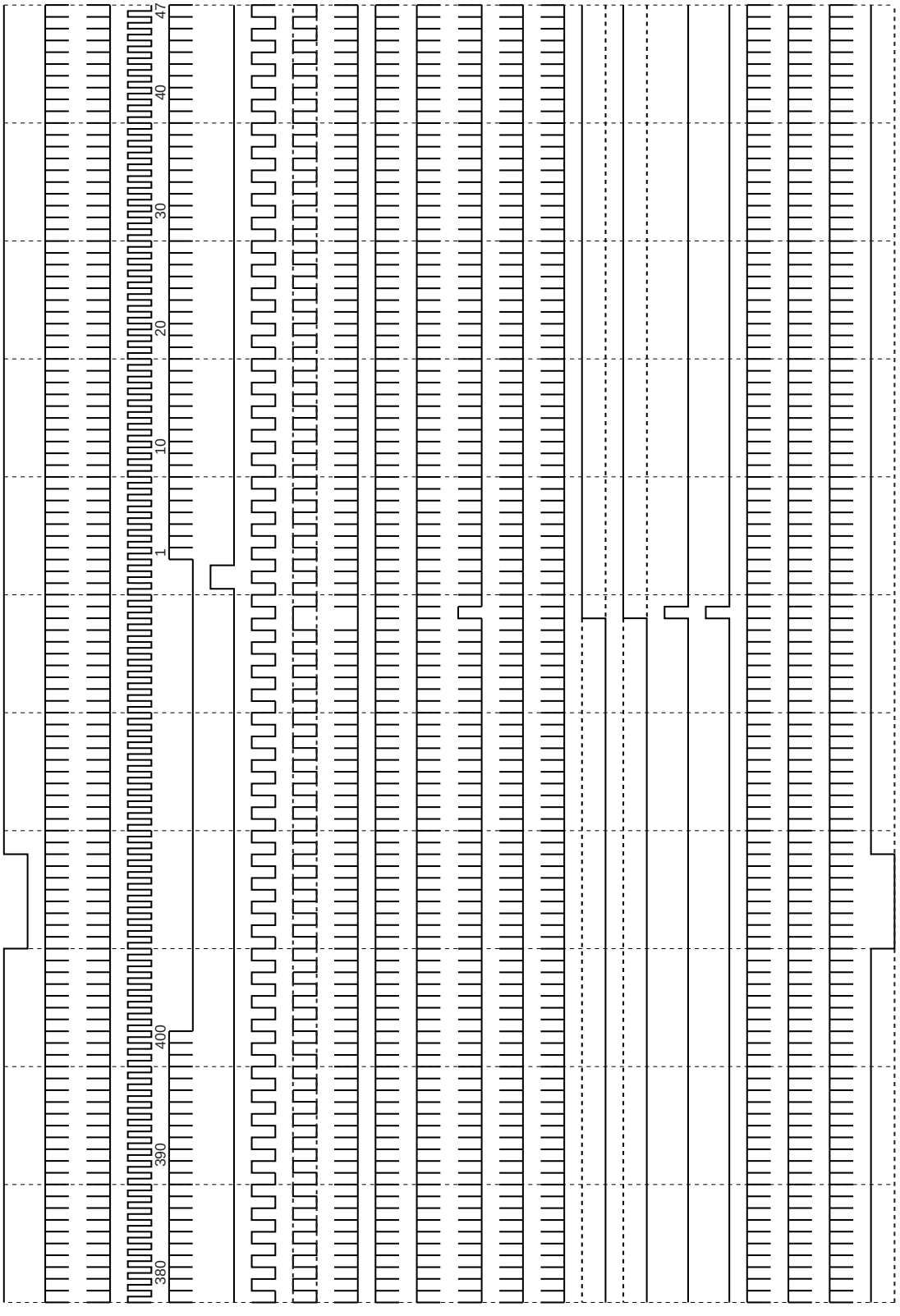
Loop Counter: 1376 clk
MCK f: 94.50MHz (10.58ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PC98 (PC98: fv 56.40Hz) 640 × 400

PLSSL2/1/0: L/L/L DWN: H VP: LLLHHHLL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: H BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/L/H

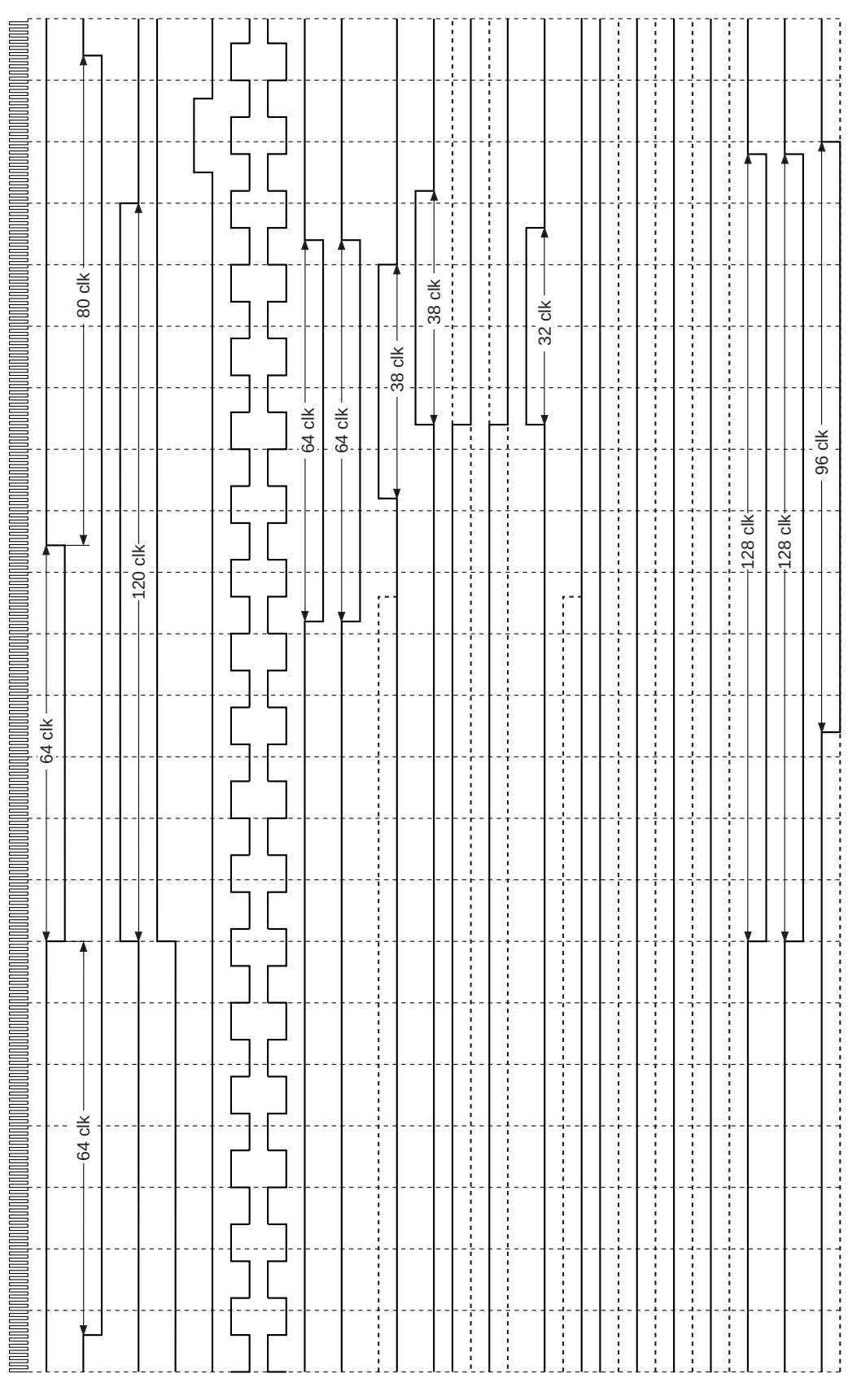


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PC98 (PC98: fv 56.40Hz) 640 × 400

PLSSL2/1/0: L/L/L PLLP: LLHHLHLLHHHL (LSB) HP: LLLLLLHHLLHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: L HR: H RGT: H DSP: H SPON: L PO/MODE3/2/1: L/L/H (SVGA panel, PC98 mode)

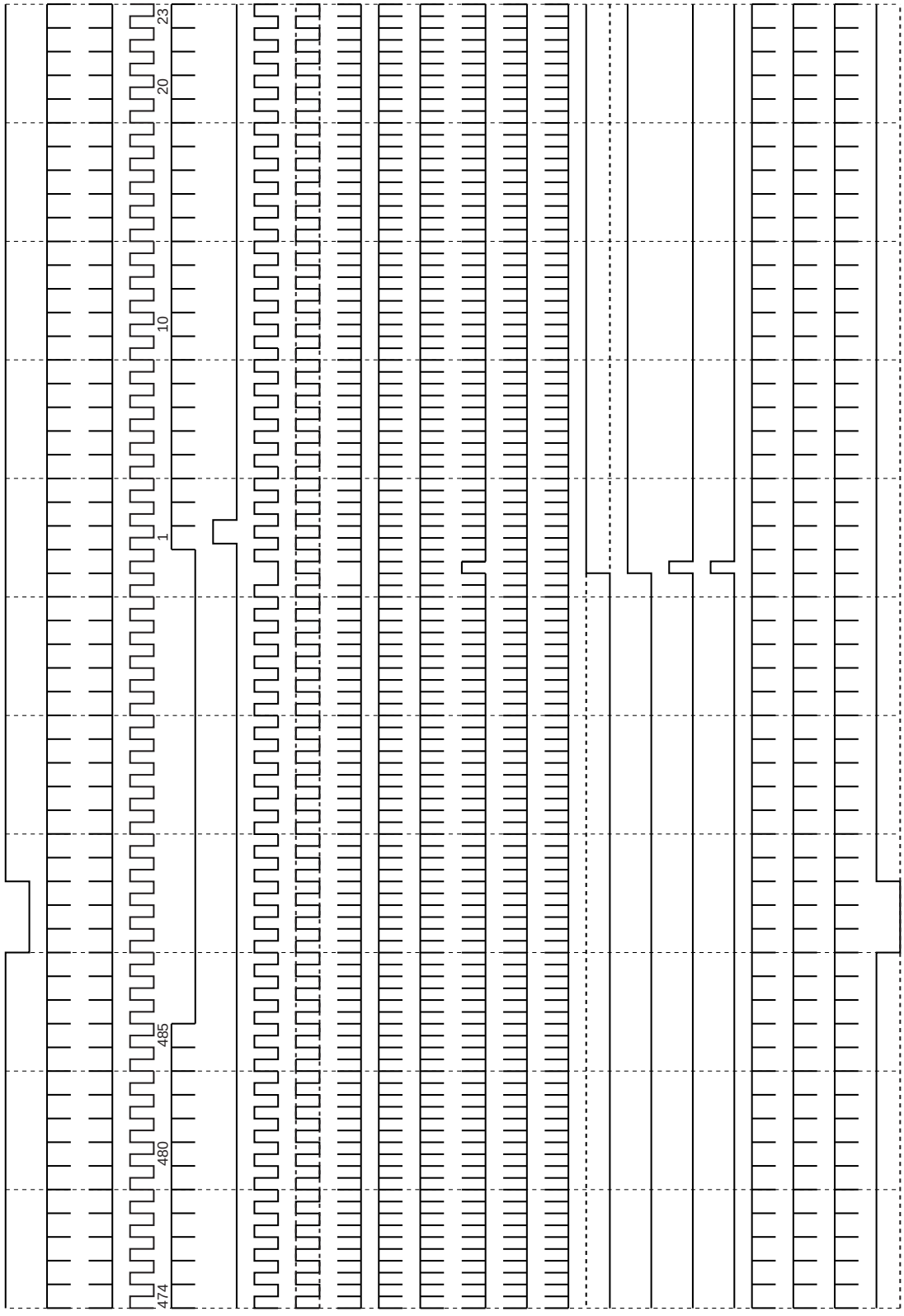
Loop Counter: 848 clk
MCK f: 21.05MHz (47.50ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

NTSC (ODD) 640 × 480

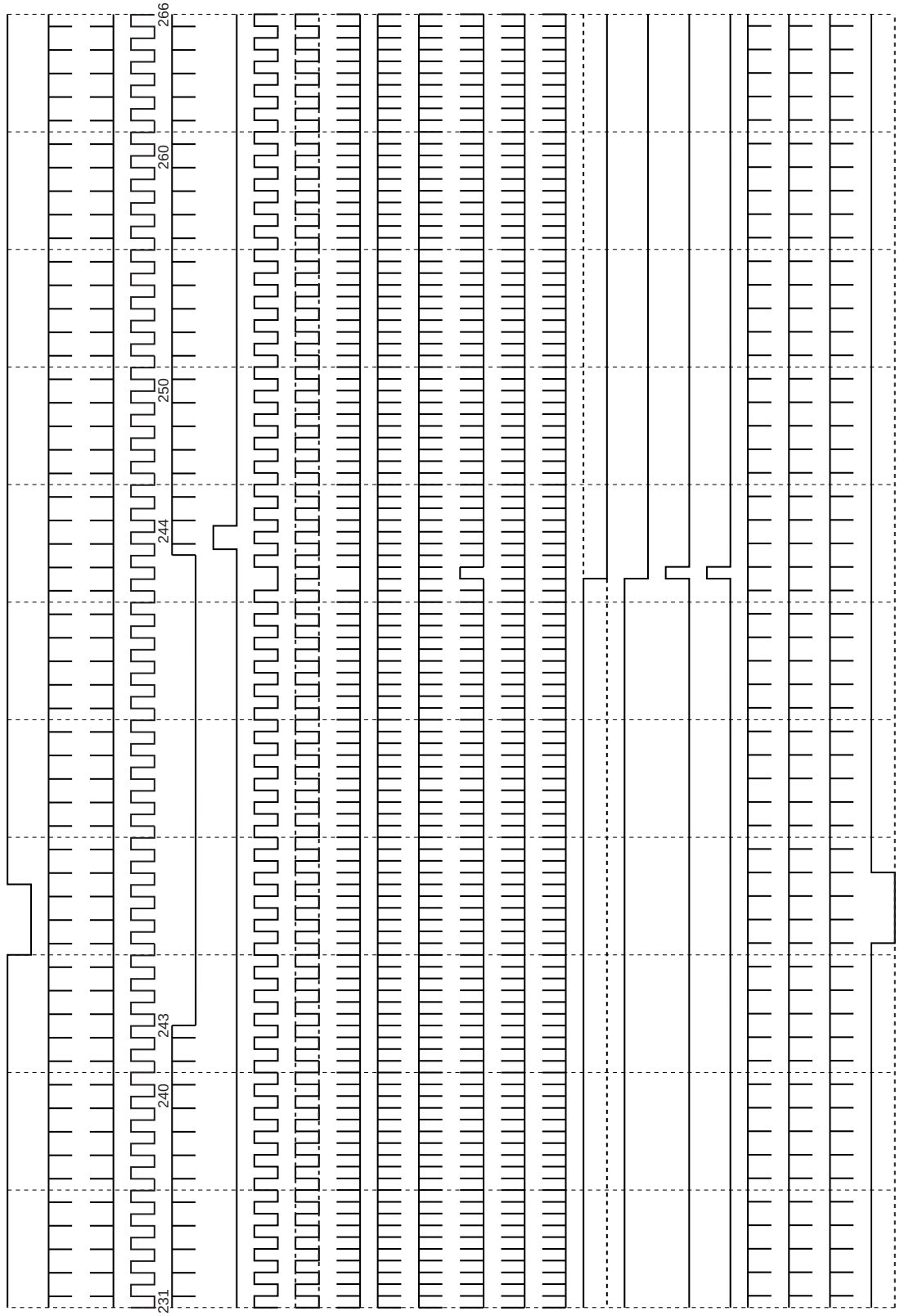
PLSSL2/1/0: L/L/L DWN: H VP: LLHLLLLL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: L BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/H/L



Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

NTSC (EVEN) 640 × 480

PLSSL2/1/0: L/L/L DWN: H VP: LLHLLLLL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: L BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: H/H/L

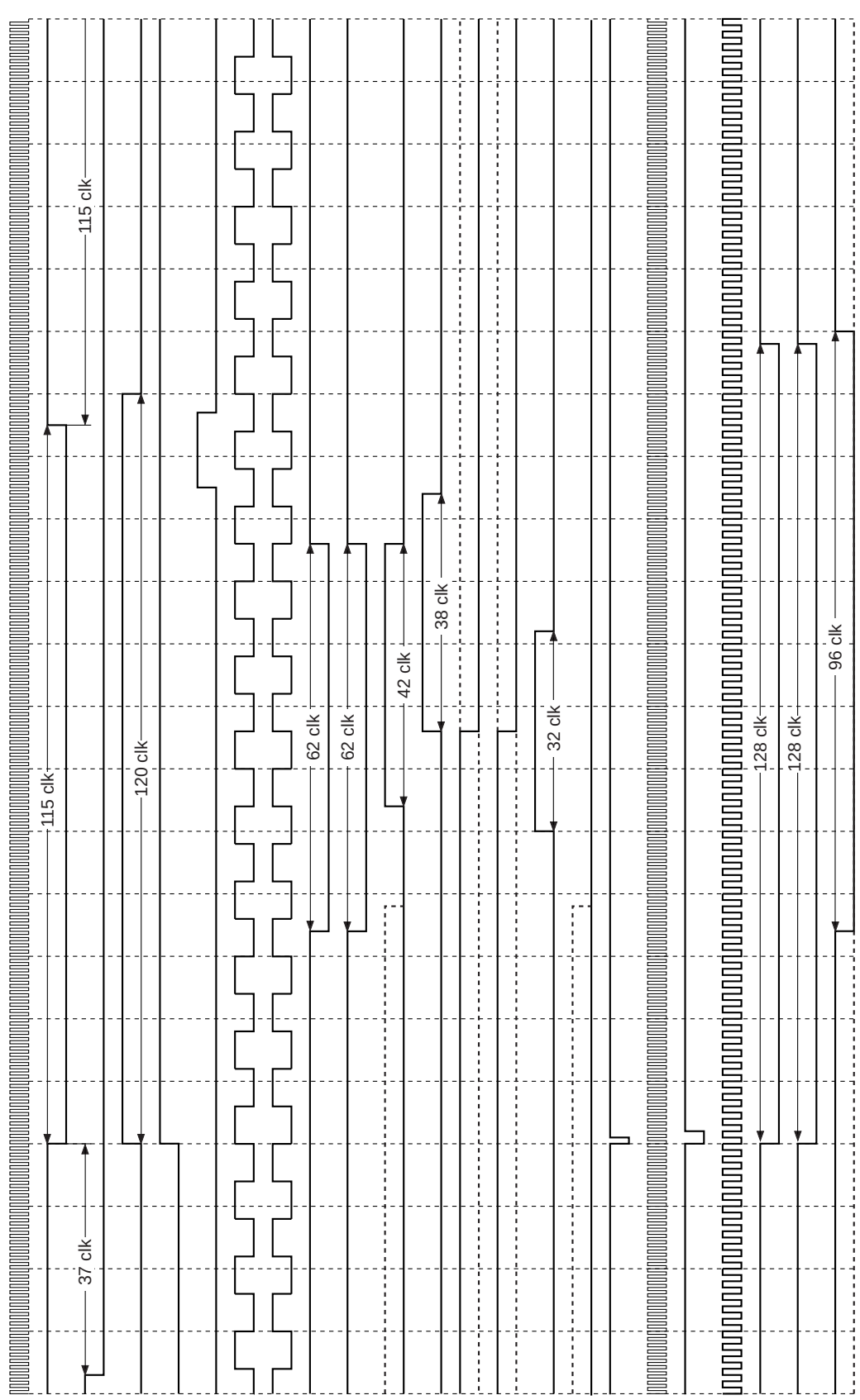


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

NTSC_1 640 × 480

PLSSL2/1/0: L/L/L PLLP: LHHLLLLHLHHL (LSB) HP: LLLLLLHLLLLL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHH (LSB) PCG: H PRGD: LLHLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: H HR: H RGT: H DSP: L SPON: L PO/MODE3/2/1: H/H/L (SVGA panel, VGA mode)

Loop Counter: 1560 clk
MCK f: 24.54MHz (40.75ns)

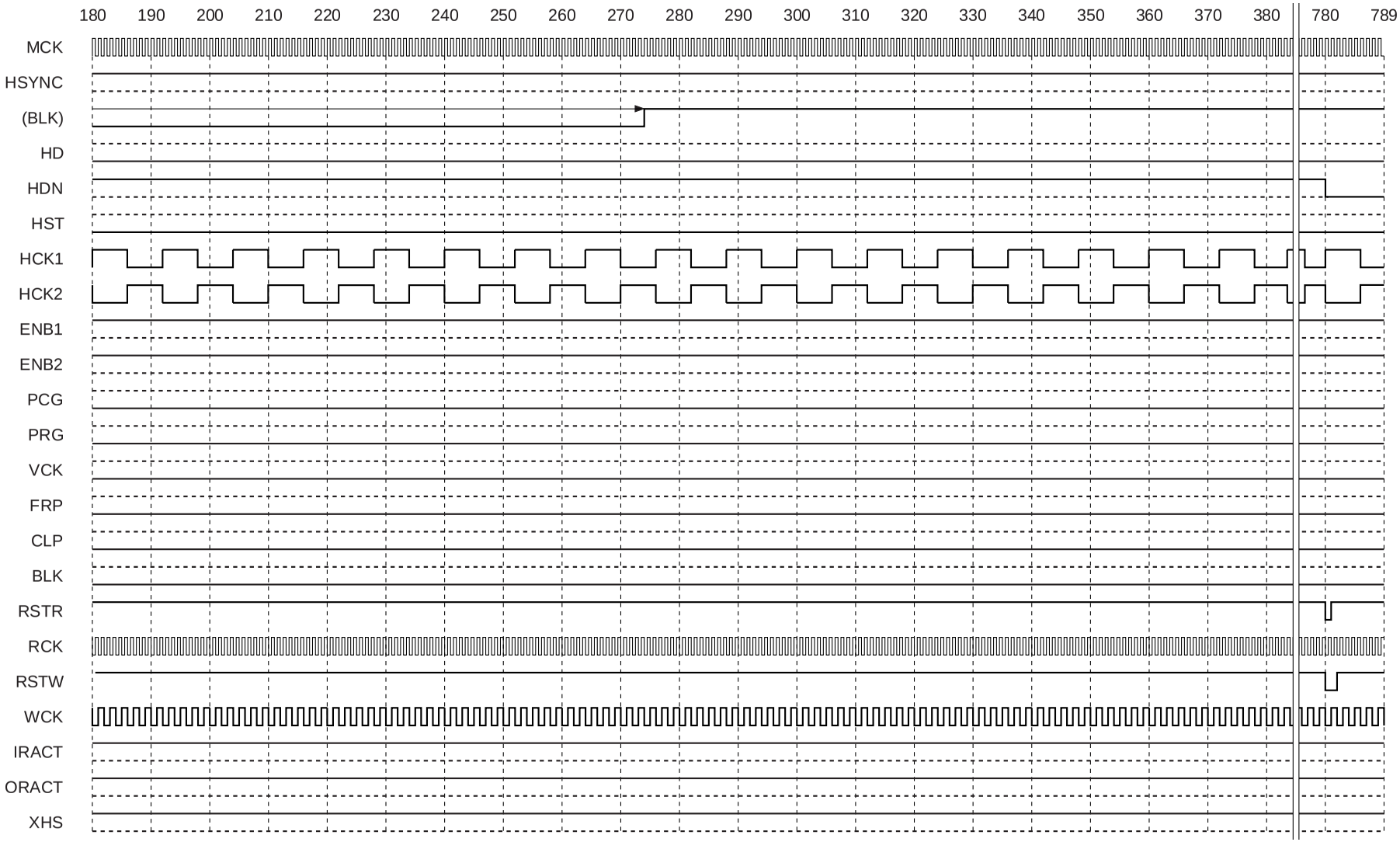


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

NTSC_2 640 × 480

PLSSL2/1/0: L/L/L PLLP: LHHLLLLHLHHL (LSB) HP: LLLLLLHLLLLL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLHH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: H HR: H RGT: H DSP: L SPON: L PO/MODE3/2/1: H/H/L (SVGA panel, VGA mode)

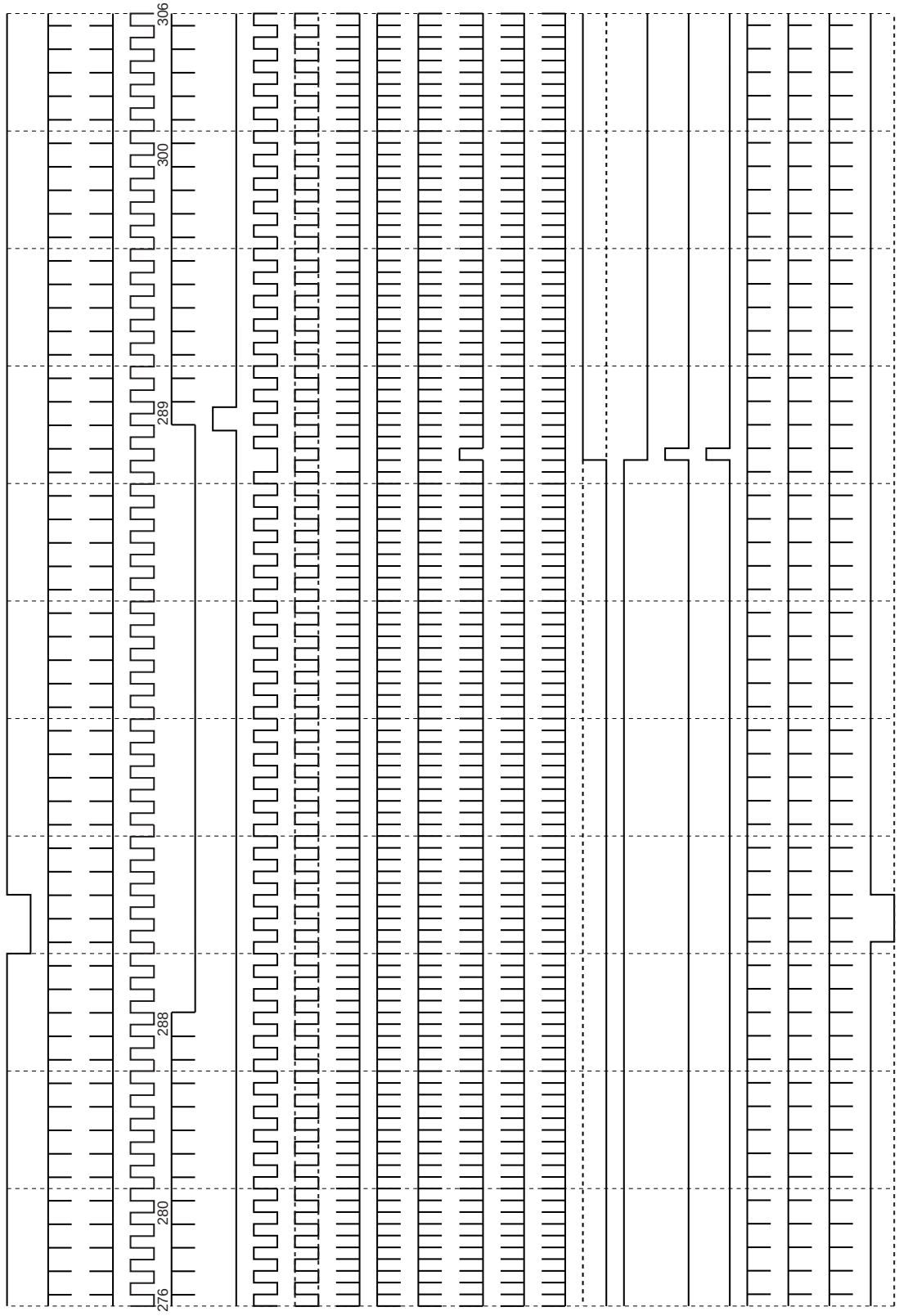
Loop Counter: 1560 clk
MCK f: 24.54MHz (40.75ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PAL (ODD) 762 × 572

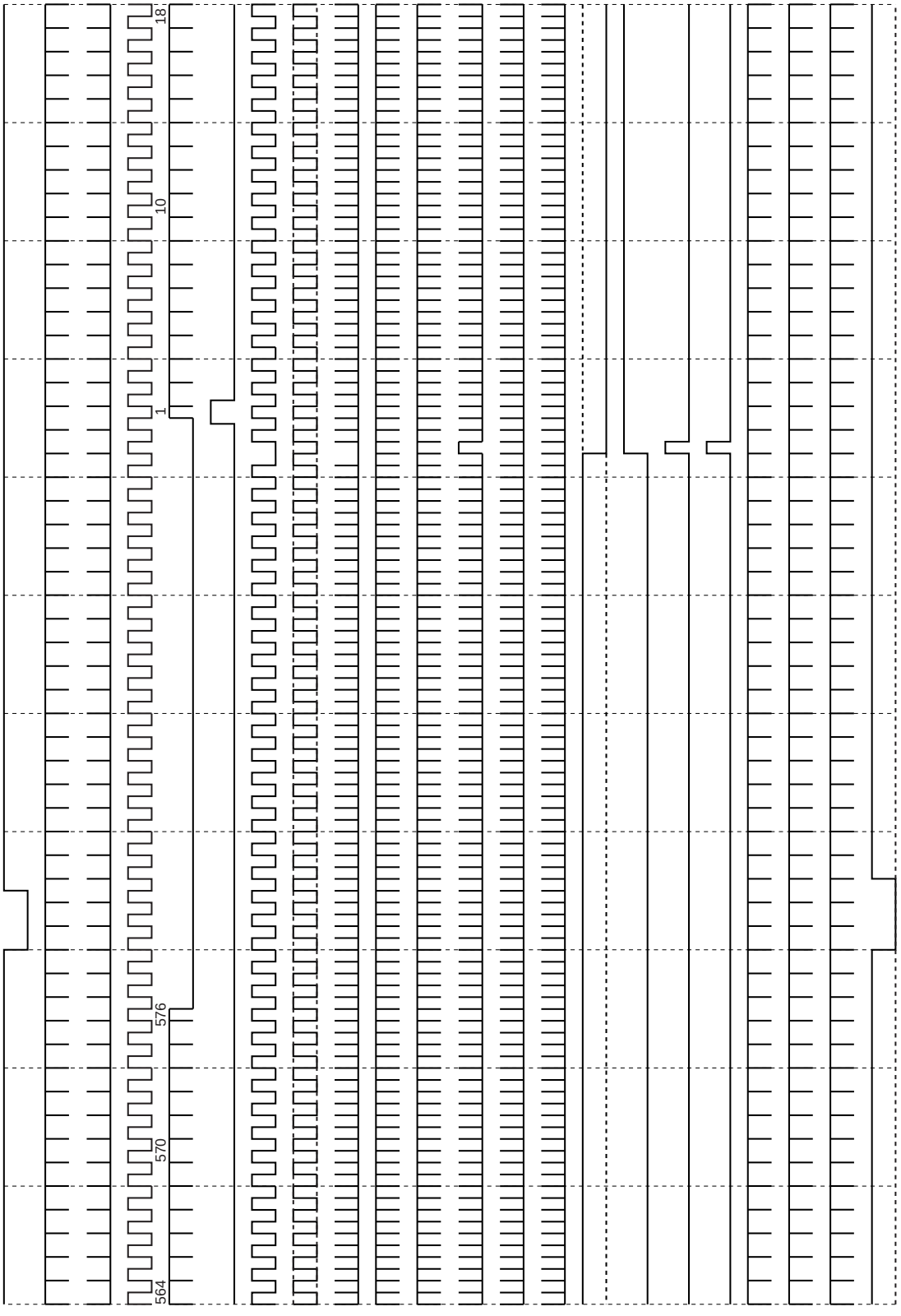
PLSSL2/1/0: L/L/H DWN: H VP: LLHLHLHL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: L BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/H/L



Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PAL (EVEN) 762 × 572

PLSSL2/1/0: L/L/H DWN: H VP: LLHLHLHL (LSB) FRP1/0: L/L VSTFX: L VSTPOL: H VPOL: L VGAV: L BLKON: H BLKPOL: H
FMBK: L MBKA: LLLLL (LSB) MBKB: LLLL (LSB) MBKZ: LLLL (LSB) DWN: H PO/MODE3/2/1: L/H/L

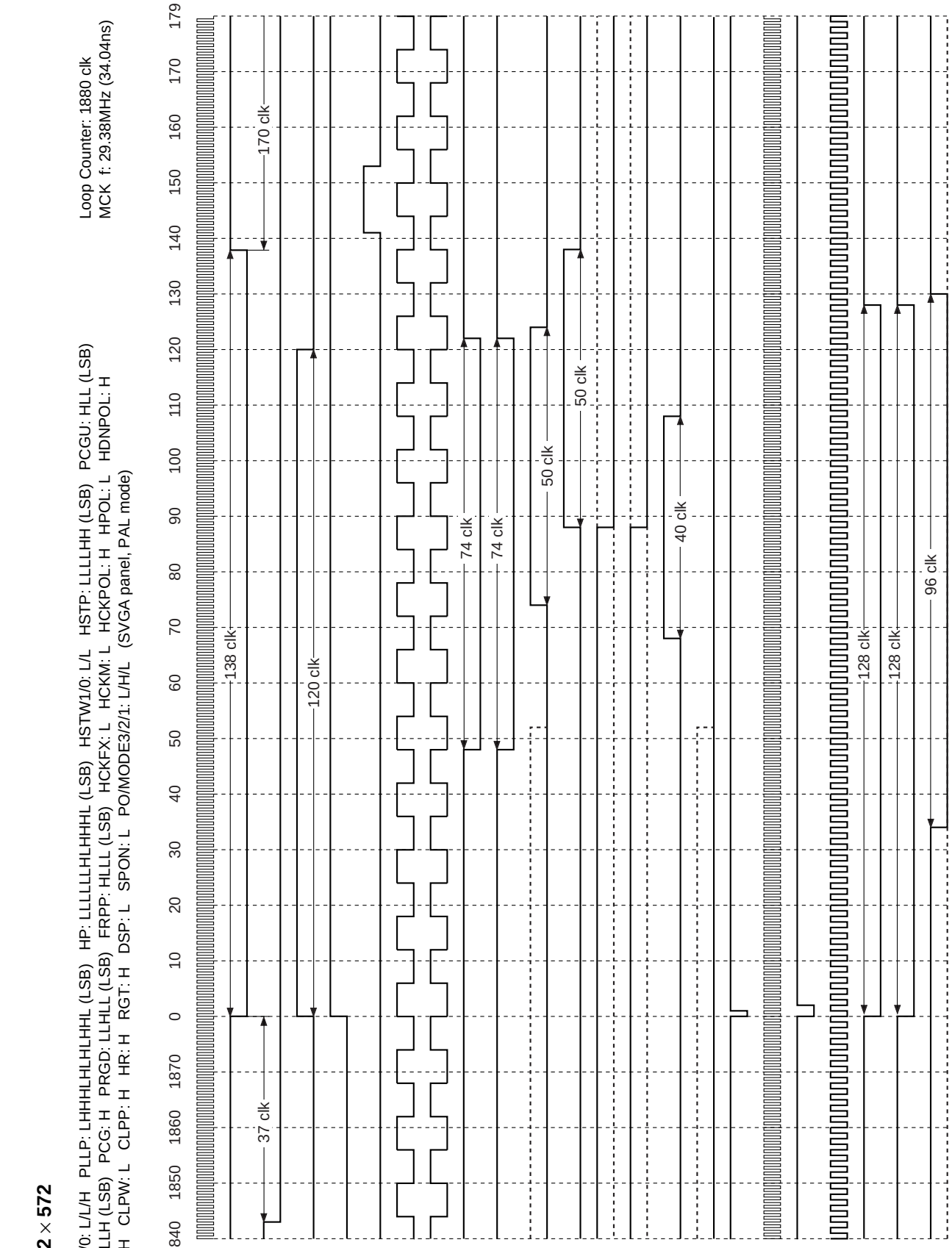


Note) The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PAL_1 762 × 572

PLSSL2/1/0: L/L/H PLLP: LHHHLHLHLHHL (LSB) HP: LLLLLLHLHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: H HR: H RGT: H DSP: L SPON: L PO/MODE3/2/1: L/H/L (SVGA panel, PAL mode)

Loop Counter: 1880 clk
MCK f: 29.38MHz (34.04ns)

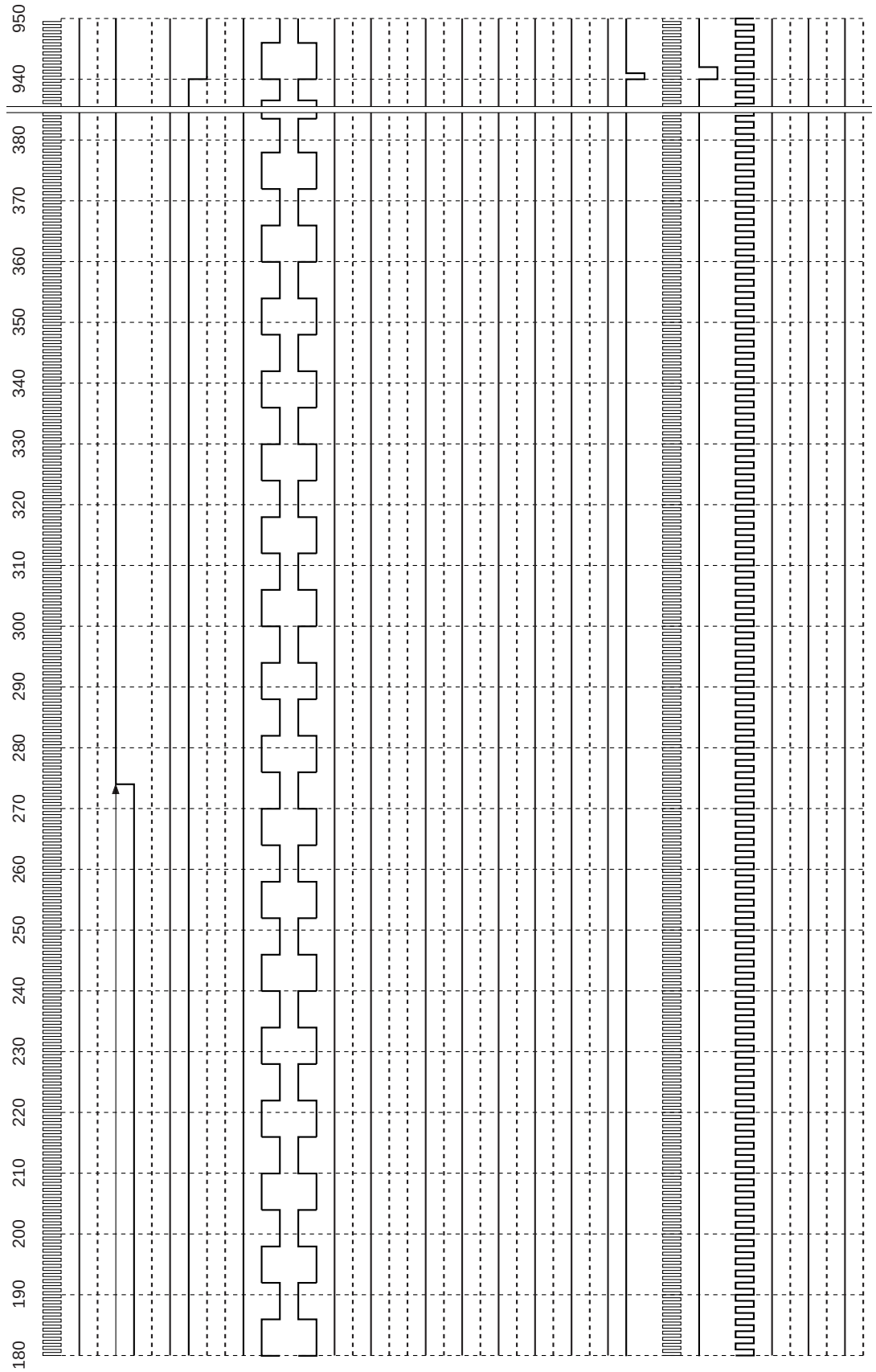


Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

PAL_2 762 × 572

PLSSL2/1/0: L/L/H PLLP: LHHHLHLHHL (LSB) HP: LLLLLLHLHHHL (LSB) HSTW1/0: L/L HSTP: LLLLHH (LSB) PCGU: HLL (LSB)
PCGD: LLLLH (LSB) PCG: H PRGD: LLHLL (LSB) FRPP: HLLL (LSB) HCKFX: L HCKM: L HCKPOL: H HPOL: L HDNPOL: H
CLPPOL: H CLPW: L CLPP: H HR: H RGT: H DSP: L SPON: L PO/MODE3/2/1: L/H/L (SVGA panel, PAL mode)

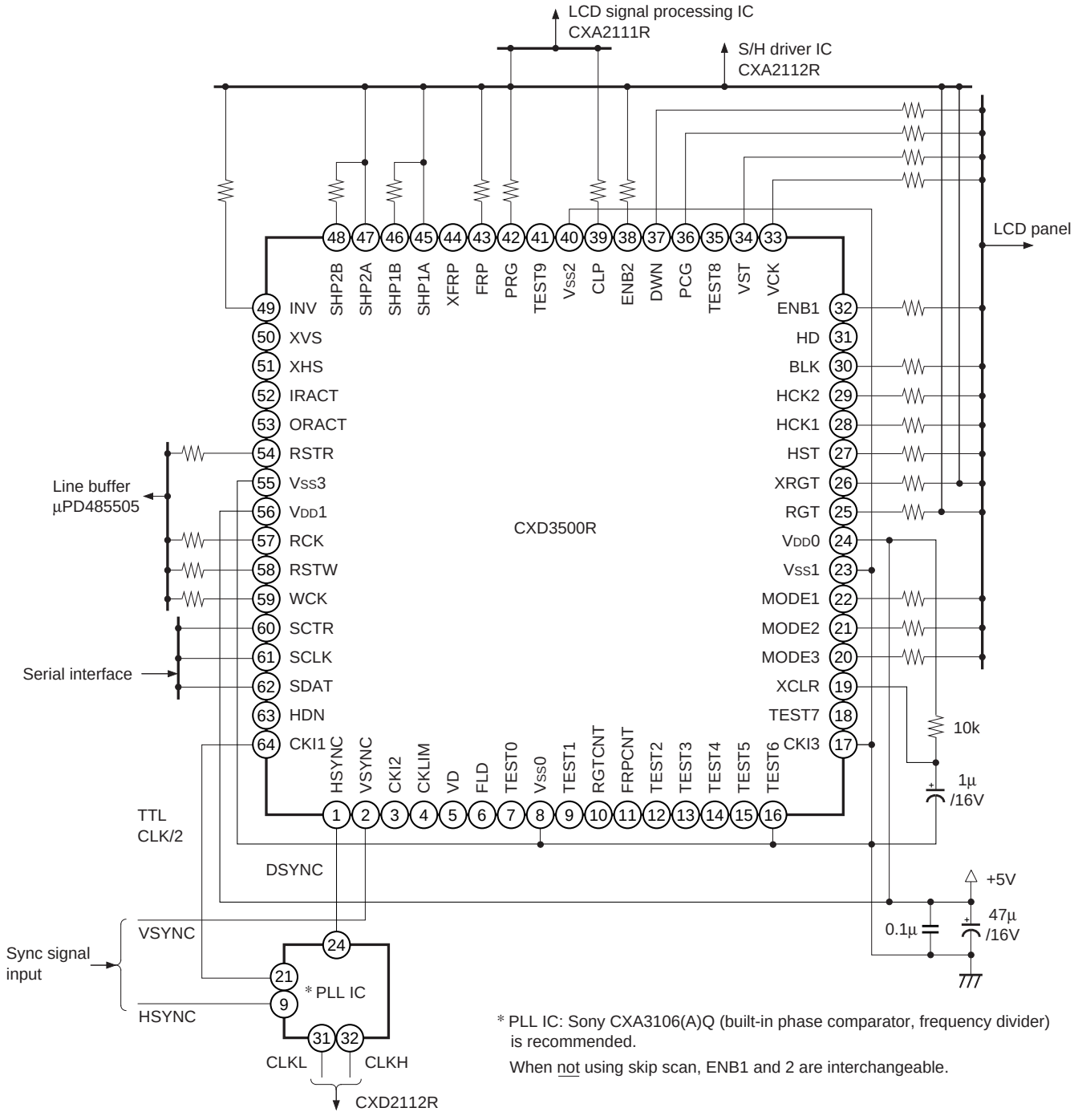
Loop Counter: 1880 clk
MCK f: 29.38MHz (34.04ns)



Note) The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

Application Circuit

This IC allows direct drive of LCD panels. However, in this case insert resistor of several Ω to several tens of Ω in series.



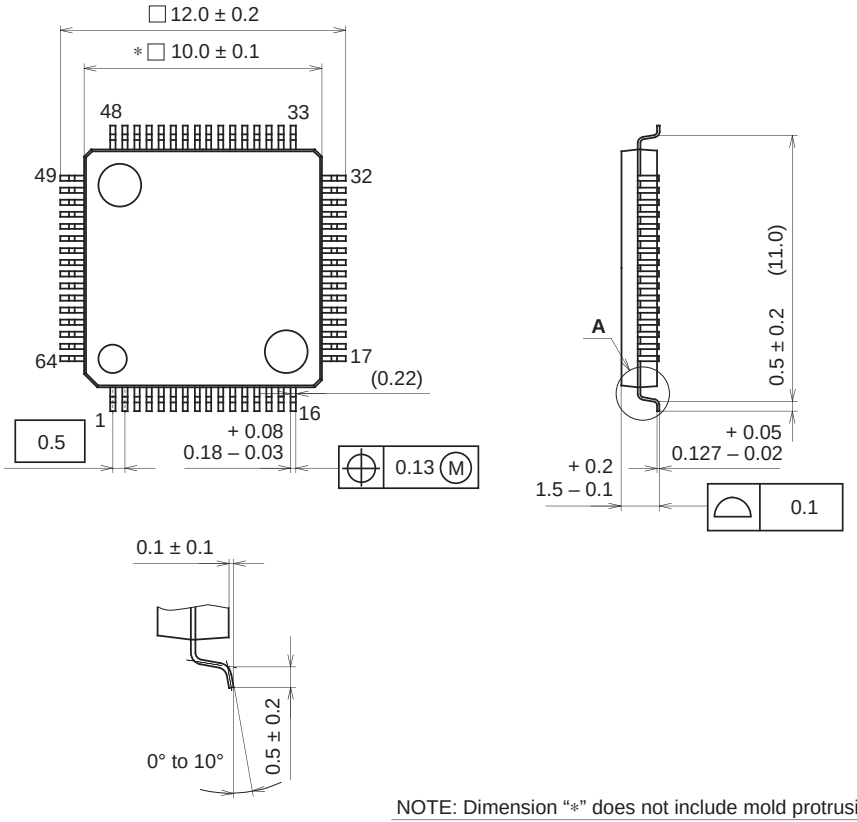
* PLL IC: Sony CXA3106(A)Q (built-in phase comparator, frequency divider) is recommended.

When not using skip scan, ENB1 and 2 are interchangeable.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g