SONY

CXD2932AGA-2

GPS Base Band LSI

For the availability of this product, please contact the sales office.

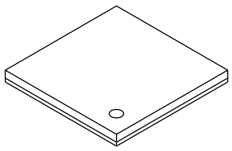
Description

The CXD2932AGA-2 is a dedicated LSI for the GPS (Global Positioning System) satellite-based position measurement system.

This LSI contains a 32-bit RISC CPU, satellite tracking circuit, 2M-bit mask ROM, RAM, UART, interval timer, and others.

This LSI, used together with the RF LSI, enables the configuration of a 2-chip system capable of measuring its position anywhere on the globe.

144 pin LFLGA (Plastic)



Features

- 16-channel GPS receiver capable of simultaneously receiving 16 satellites
- Supports differential GPS
  - —Conforms to RTCM SC-104 Ver. 2.1
  - —Supports DARC
- All-in-view measurement
- Timer supporting GPS time
- 32-bit RISC CPU
- 256K-byte program ROM
- 40K-byte RAM
- Power management function
- 1PPS supported
- 2-channel UART
- 4-channel interval timer
- 16-bit general-purpose I/O port
- 12-bit successive approximation system A/D converter (4-channel analog switch)

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to 4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–50 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–40 to +85	°C

Input/Output Pin Capacitance

• Input capacitance	C_{IN}	9 (Max.)	pF
• Output capacitance	C_{OUT}	11 (Max.)	pF
• I/O capacitance	$C_{I/O}$	11 (Max.)	pF

E03202A37

Performance

- 16-channel GPS receiver

- 32-bit RISC CPU

- Receiver frequency: 1575.42MHz (L1 band, CA code)

- Reception sensitivity
  Tracking sensitivity: –145dBm or less (typ.) when using the antenna of 25dBi, NF = 2dB and the RF amplifier with the 25dB gain for the RF block
  * Reference data using the Sony's reference board.
  This value is not guaranteed, depending on the conditions.

- Time to First Fix (time until initial measurement after power-on)
  Cold Start (without both ephemeris and almanac): 27 to 58s
  Warm Start (without ephemeris with almanac): 23 to 45s
  Hot Start (with both ephemeris and almanac): 6 to 17s
  * Reference data with elevation angle of 5° or more and no interception environment on June, 2002.
  Positioning time with 90% possibility.
  These values are not guaranteed, depending on the conditions.

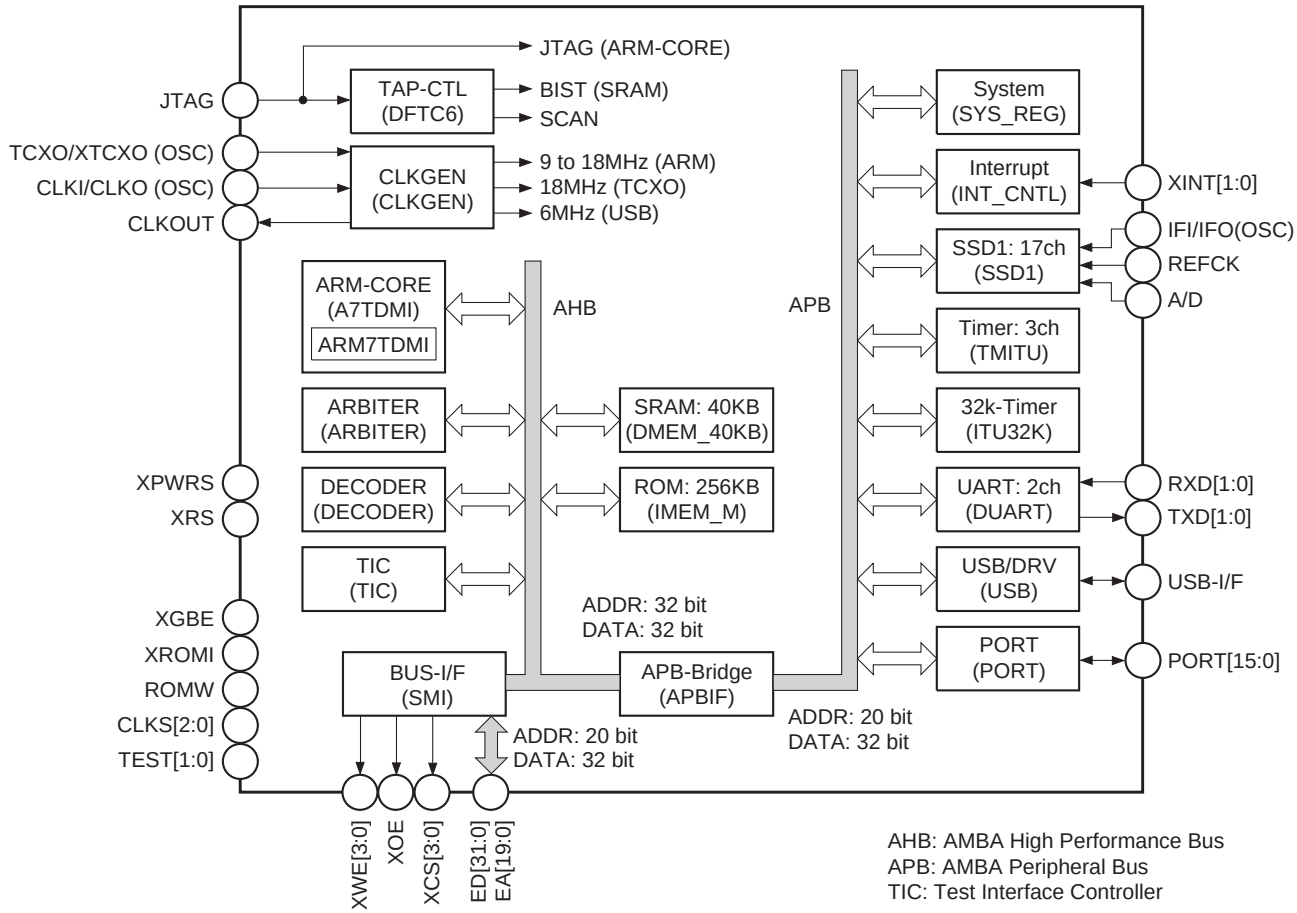
- Positioning accuracy
  2DRMS: approx. 5m
  * Reference data with elevation angle of 5° or more and no interception environment on June, 2002.
  This value is not guaranteed, depending on the conditions.

- Measurement data update time: 1s

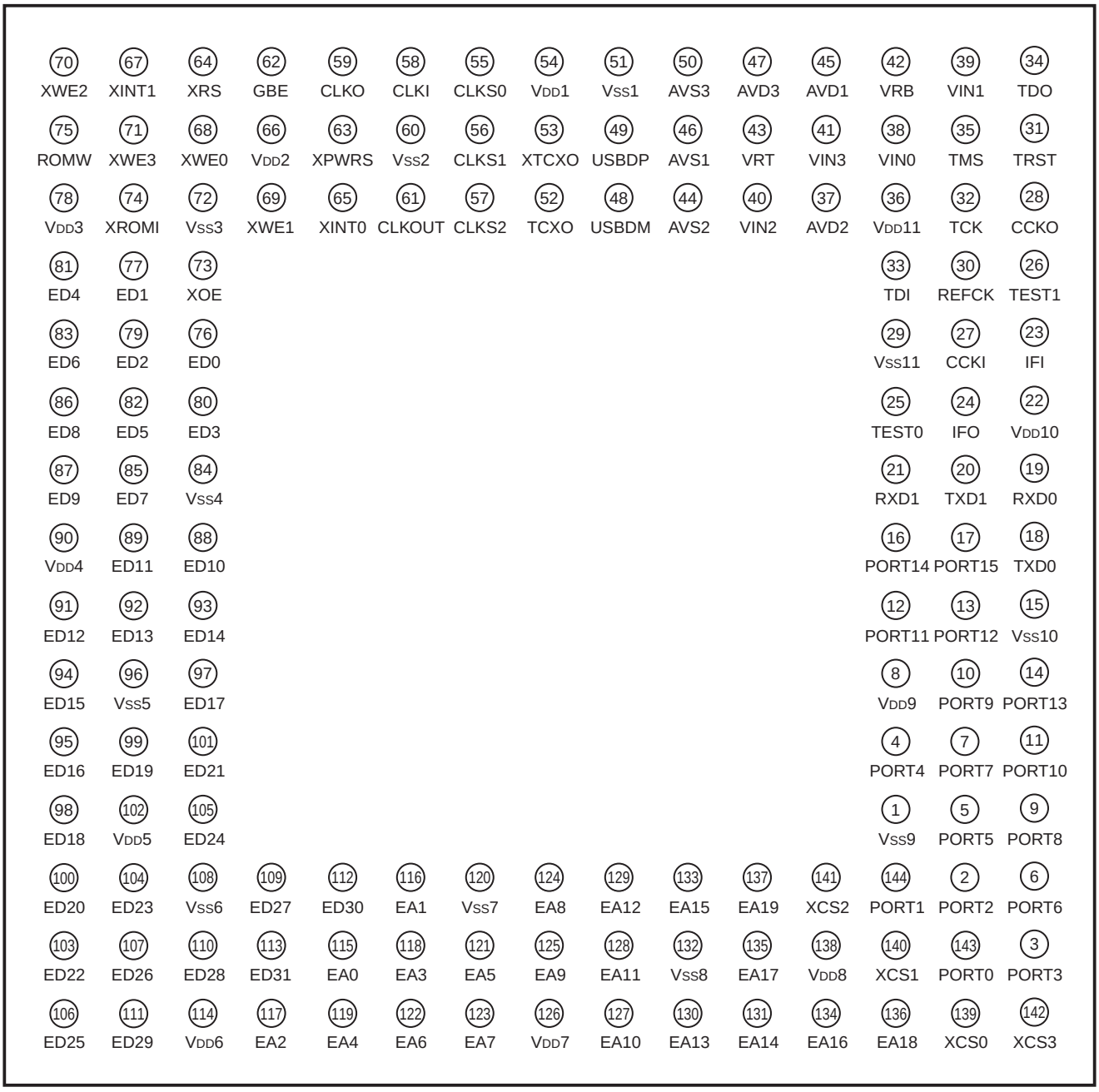
- Communication format: Sony Binary
  NMEA-0183
  Customized NMEA (9600bps)

- All-in-view

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	V_{SS}9	—	V_{SS}
2	PORT2	I/O/Z	I/O port 2 (See the Application Circuit for setting.)
3	PORT3	I/O/Z	I/O port 3 (See the Application Circuit for setting.)
4	PORT4	I/O/Z	I/O port 4 (See the Application Circuit for setting.)
5	PORT5	I/O/Z	I/O port 5 (See the Application Circuit for setting.)
6	PORT6	I/O/Z	I/O port 6 (See the Application Circuit for setting.)
7	PORT7	I/O/Z	I/O port 7 (See the Application Circuit for setting.)
8	V_{DD}9	—	V_{DD}
9	PORT8	I/O/Z	I/O port 8 (See the Application Circuit for setting.)
10	PORT9	I/O/Z	I/O port 9 (See the Application Circuit for setting.)
11	PORT10	I/O/Z	I/O port 10 (See the Application Circuit for setting.)
12	PORT11	I/O/Z	I/O port 11 (See the Application Circuit for setting.)
13	PORT12	I/O/Z	I/O port 12 (See the Application Circuit for setting.)
14	PORT13	I/O/Z	I/O port 13 (See the Application Circuit for setting.)
15	V_{SS}10	—	V_{SS}
16	PORT14	I/O/Z	I/O port 14
17	PORT15	I/O/Z	I/O port 15
18	TXD0	O/Z	UART transmission data (CH0)
19	RXD0	I	UART reception data (CH0)
20	TXD1	O/Z	UART transmission data (CH1)
21	RXD1	I	UART reception data (CH1)
22	V_{DD}10	—	V_{DD}
23	IFI	I	IF signal binary conversion circuit
24	IFO	O	
25	TEST0	I	Test (Low level fixed)
26	TEST1	I	Test (Low level fixed)
27	CCKI	I	Timer oscillation circuit (32.768kHz ± 100ppm)
28	CCKO	O	
29	V_{SS}11	—	V_{SS}
30	REFCK	I	Test (Low level fixed)
31	TRST	I	Test (Open)
32	TCK	I	Test (Open)
33	TDI	I	Test (Open)
34	TDO	O/Z	Test
35	TMS	I	Test (Open)
36	V_{DD}11	—	V_{DD}
37	AVD2	—	A/D converter V_{DD}

Pin No.	Symbol	I/O	Description
38	VIN0	I	Analog input (CH0)
39	VIN1	I	Analog input (CH1)
40	VIN2	I	Analog input (CH2)
41	VIN3	I	Analog input (CH3)
42	VRB	I	Reference input (Bottom)
43	VRT	I	Reference input (Top)
44	AVS2	—	A/D converter V_{SS}
45	AVD1	—	PLL V_{DD}
46	AVS1	—	PLL V_{SS}
47	AVD3	—	USB V_{DD}
48	USBDM	I/O/Z	USB data + (Not supported in this IC. Pull down with 15kΩ)
49	USBDP	I/O/Z	USB data – (Not supported in this IC. Pull down with 15kΩ)
50	AVS3	—	USB V_{SS}
51	V_{SS}1	—	V_{SS}
52	TCXO	I	TCXO crystal oscillator (18.414MHz ± 3ppm)
53	XTCXO	O	
54	V_{DD}1	—	V_{DD}
55	CLKS0	I	CPU clock selection (CLKS2, CLKS1, CLKS0) = (0, 0, 1): 18.414MHz (TCXO) (CLKS2, CLKS1, CLKS0) = (0, 1, 0): 27.671MHz (TCXO × 1.5)
56	CLKS1	I	
57	CLKS2	I	
58	CLKI	I	CPU clock oscillator
59	CLKO	O	
60	V_{SS}2	—	V_{SS}
61	CLKOUT	O/Z	1PPS output
62	GBE	I	External bus enable (H-Active)
63	XPWRS	I	Oscillator enable (H-Active)
64	XRS	I	Reset (L-Active)
65	XINT0	I	External interruption 0 (L-Active)
66	V_{DD}2	—	V_{DD}
67	XINT1	I	External interruption 1 (L-Active)
68	XWE0	O	External expansion write signal 0
69	XWE1	O	External expansion write signal 1
70	XWE2	O	External expansion write signal 2
71	XWE3	O	External expansion write signal 3
72	V_{SS}3	—	V_{SS}
73	XOE	O	External expansion read signal
74	XROMI	I	Program area selection (Low: Internal / High: External)

Pin No.	Symbol	I/O	Description
75	ROMW	I	Test (Low level fixed)
76	ED0	I/O/Z	External expansion data 0
77	ED1	I/O/Z	External expansion data 1
78	$V_{DD}3$	—	V_{DD}
79	ED2	I/O/Z	External expansion data 2
80	ED3	I/O/Z	External expansion data 3
81	ED4	I/O/Z	External expansion data 4
82	ED5	I/O/Z	External expansion data 5
83	ED6	I/O/Z	External expansion data 6
84	$V_{SS}4$	—	V_{SS}
85	ED7	I/O/Z	External expansion data 7
86	ED8	I/O/Z	External expansion data 8
87	ED9	I/O/Z	External expansion data 9
88	ED10	I/O/Z	External expansion data 10
89	ED11	I/O/Z	External expansion data 11
90	$V_{DD}4$	—	V_{DD}
91	ED12	I/O/Z	External expansion data 12
92	ED13	I/O/Z	External expansion data 13
93	ED14	I/O/Z	External expansion data 14
94	ED15	I/O/Z	External expansion data 15
95	ED16	I/O/Z	External expansion data 16
96	$V_{SS}5$	—	V_{SS}
97	ED17	I/O/Z	External expansion data 17
98	ED18	I/O/Z	External expansion data 18
99	ED19	I/O/Z	External expansion data 19
100	ED20	I/O/Z	External expansion data 20
101	ED21	I/O/Z	External expansion data 21
102	$V_{DD}5$	—	V_{DD}
103	ED22	I/O/Z	External expansion data 22
104	ED23	I/O/Z	External expansion data 23
105	ED24	I/O/Z	External expansion data 24
106	ED25	I/O/Z	External expansion data 25
107	ED26	I/O/Z	External expansion data 26
108	$V_{SS}6$	—	V_{SS}
109	ED27	I/O/Z	External expansion data 27
110	ED28	I/O/Z	External expansion data 28
111	ED29	I/O/Z	External expansion data 29

Pin No.	Symbol	I/O	Description
112	ED30	I/O/Z	External expansion data 30
113	ED31	I/O/Z	External expansion data 31
114	V_{DD}6	—	V_{DD}
115	EA0	O/Z	External expansion address 0
116	EA1	O/Z	External expansion address 1
117	EA2	O/Z	External expansion address 2
118	EA3	O/Z	External expansion address 3
119	EA4	O/Z	External expansion address 4
120	V_{SS}7	—	V_{SS}
121	EA5	O/Z	External expansion address 5
122	EA6	O/Z	External expansion address 6
123	EA7	O/Z	External expansion address 7
124	EA8	O/Z	External expansion address 8
125	EA9	O/Z	External expansion address 9
126	V_{DD}7	—	V_{DD}
127	EA10	O/Z	External expansion address 10
128	EA11	O/Z	External expansion address 11
129	EA12	O/Z	External expansion address 12
130	EA13	O/Z	External expansion address 13
131	EA14	O/Z	External expansion address 14
132	V_{SS}8	—	V_{SS}
133	EA15	O/Z	External expansion address 15
134	EA16	O/Z	External expansion address 16
135	EA17	O/Z	External expansion address 17
136	EA18	O/Z	External expansion address 18
137	EA19	O/Z	External expansion address 19
138	V_{DD}8	—	V_{DD}
139	XCS0	O	External expansion chip select 0
140	XCS1	O	External expansion chip select 1
141	XCS2	O	External expansion chip select 2
142	XCS3	O	External expansion chip select 3
143	PORT0	I/O/Z	I/O port 0 (See the Application Circuit for setting.)
144	PORT1	I/O/Z	I/O port 1 (See the Application Circuit for setting.)

Analog Characteristics

(1) A/D Converter Characteristics

(AVD = 3.0 to 3.6V, Topr = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Resolution					12	Bit	
Channel				4		Ch	
Differential linearity error (DLE)		AVD = 3.0V	–1.0		+1.0	LSB	
Integral linearity error (ILE)			–1.0		+1.0	LSB	
Sampling time		f = 18.414MHz	5			µs	
Conversion time			15			µs	
Reference power (Top)	VRT		VRB		AVD	V	*1
Reference power (Bottom)	VRB		0		VRT	V	*2
Analog input power	VIN0-3		VRB		VRT	V	*3
Current consumption		AVD = 3.0V		5		mA	

Applicable pins

*1 Pin 43

*2 Pin 42

*3 Pins 38 to 41

(2) USB Characteristics

(AVD = 3.0 to 3.6V, Topr = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output impedance	Zdrv	—	28		43	Ω
Output voltage (Low)	V_{OL}	RL = 1.5kΩ to 3.6V	—		0.3	V
Output voltage (High)	V_{OH}	RL = 1.5kΩ to GND	2.8		3.6	V
Data rise delay time	Tr	CL = 50pF	75		—	ns
		CL = 350pF	—		300	ns
Data fall delay time	Tf	CL = 50pF	75		—	ns
		CL = 350pF			300	ns
Data delay time ratio	Tr/Tf	CL = 50pF or 350pF	0.8		1.2	—
Crossover voltage	Vcrs	CL = 50pF or 350pF	1.3		2.0	V
Current consumption (during operation)	Ica	CL = 50pF and V_{CC} = 3.6V	—		20	mA
Current consumption (during suspension)	Icb	V_{CC} = 3.6V	—		2	mA

Applicable pins

Pins 48, 49

DC Characteristics (VDD = 3.0 to 3.6V, Topr = –40 to +85°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1) (COMS level)	High level	V_{IH}		0.7V_{DD}			V	*1
	Low level	V_{IL}				0.2V_{DD}	V	
Input voltage (2) (5V interface)	High level	V_{IH}		0.7V_{DD}		5.5	V	*2
	Low level	V_{IL}				0.2V_{DD}	V	
Input voltage (3) (Schmitt)	High level	V_{IH}		0.7V_{DD}			V	*3
	Low level	V_{IL}				0.2V_{DD}	V	
Output voltage (1)	High level	V_{OH}	I_{OH} = –4.0mA	V_{DD} – 0.4			V	*4
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	
Output voltage (2)	High level	V_{OH}	I_{OH} = –8.0mA	V_{DD} – 0.4			V	*5
	Low level	V_{OL}	I_{OL} = 8.0mA			0.4	V	
Output voltage (3)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*6
	Low level	V_{OL}	I_{OL} = 8.0mA			0.4	V	
Output voltage (4) (5V interface)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*7
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	
Current consumption (During normal operation)	When GPS measurement	Icur	3.0V, 18.414MHz		63		mA	
			3.0V, 27.671MHz		75		mA	
Current consumption (In backup mode)	When external timer used	Istb1	3.0V		3	60	µA	
	When internal timer used	Istb2	3.0V		5	100	µA	

Applicable pins

*1 Pins 25, 26, 31 to 33, 35, 55 to 57, 74 to 77, 79 to 83, 85 to 89, 91 to 95, 97 to 101, 103 to 107, 109 to 113

*2 Pins 2 to 7, 9 to 14, 16, 17, 19, 21, 30, 62, 65, 67, 143, 144 (Use the resistor of 4.7kΩ or less when the pull-down is performed.)

*3 Pins 63, 64

*4 Pins 34, 61

*5 Pins115 to 119, 121 to 125, 133 to 137, 139 to 142, 68 to 71, 73, 76, 77, 79 to 83, 85 to 89, 91 to 95, 97 to 101, 103 to 107, 109 to 113

*6 Pins 2 to 7, 9 to 14, 16, 17, 143, 144

*7 Pins 18, 20

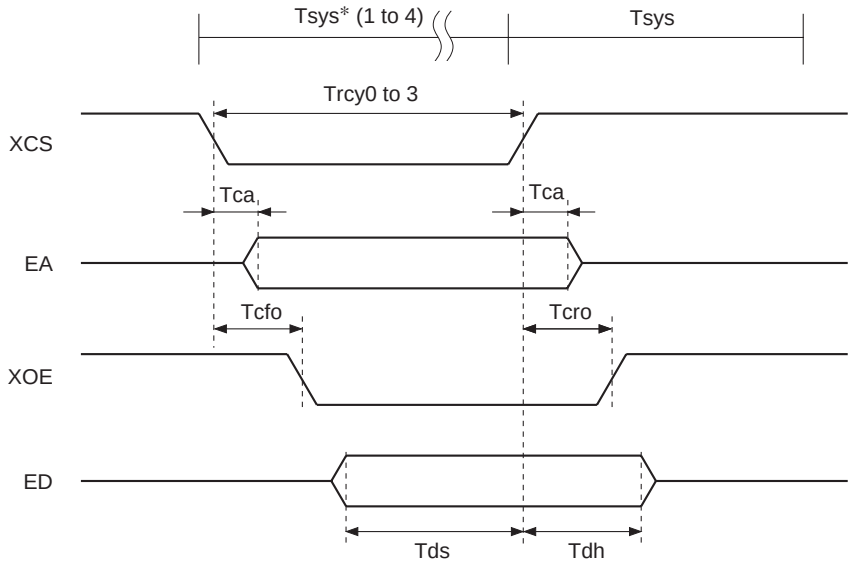
AC Characteristics

(1) External Memory Read Timing

(V_{DD} = 3.0 to 3.6V, CL = 40pF, Topr = –40 to +85°C, CPU clock = 18.4MIPS)

Item	Symbol	Min.	Typ.	Max.	Unit
Read cycle time (0WAIT)*1	Trcy0		54		ns
Read cycle time (1WAIT)*1	Trcy1		108		ns
Read cycle time (2WAIT)*1	Trcy2		162		ns
Read cycle time (3WAIT)*1	Trcy3		216		ns
Address delay time	Tca	0		4	ns
Read signal fall delay time	Tcfo	2		10	ns
Read signal rise delay time	Tcro	2		10	ns
Read data setup time	Tds	22			ns
Read data hold time	Tdh			0	ns

*1 0WAIT (normal), 1 to 3WAIT (settable according to the program)



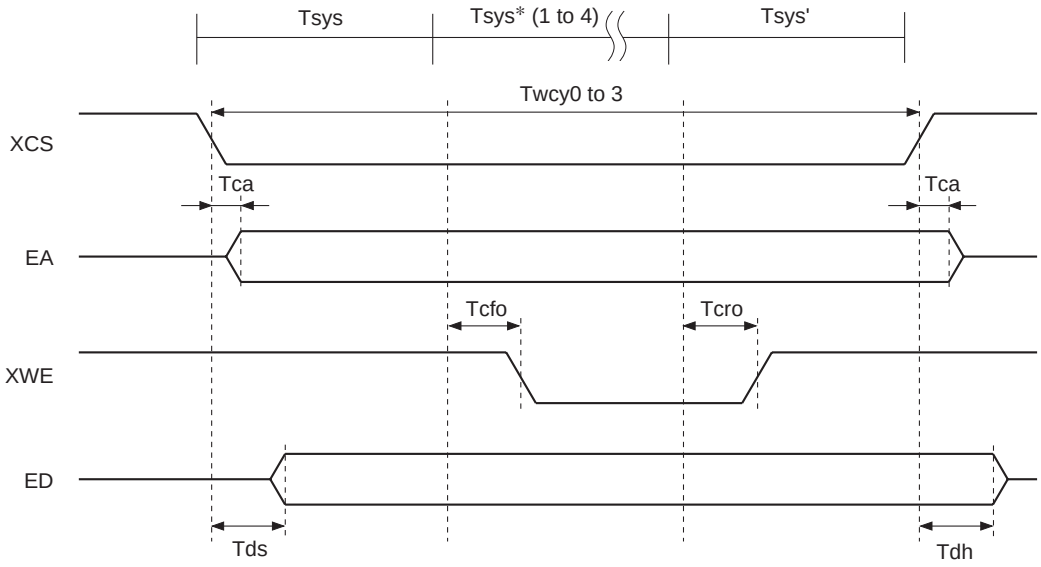
* Tsys: CPU clock cycle

(2) External Memory Write Timing

(V_{DD} = 3.0 to 3.6V, CL = 40pF, Topr = –40 to +85°C, CPU clock = 18.4MIPS)

Item	Symbol	Min.	Typ.	Max.	Unit
Write cycle time (0WAIT)*1	Twcy0		162		ns
Write cycle time (1WAIT)*1	Twcy1		216		ns
Write cycle time (2WAIT)*1	Twcy2		270		ns
Write cycle time (3WAIT)*1	Twcy3		324		ns
Address delay time	Tca	0		4	ns
Write signal fall delay time	Tcfo	2		6	ns
Write signal rise delay time	Tcro	2		8	ns
Write data setup time	Tds	2		15	ns
Write data hold time	Tdh	2		10	ns

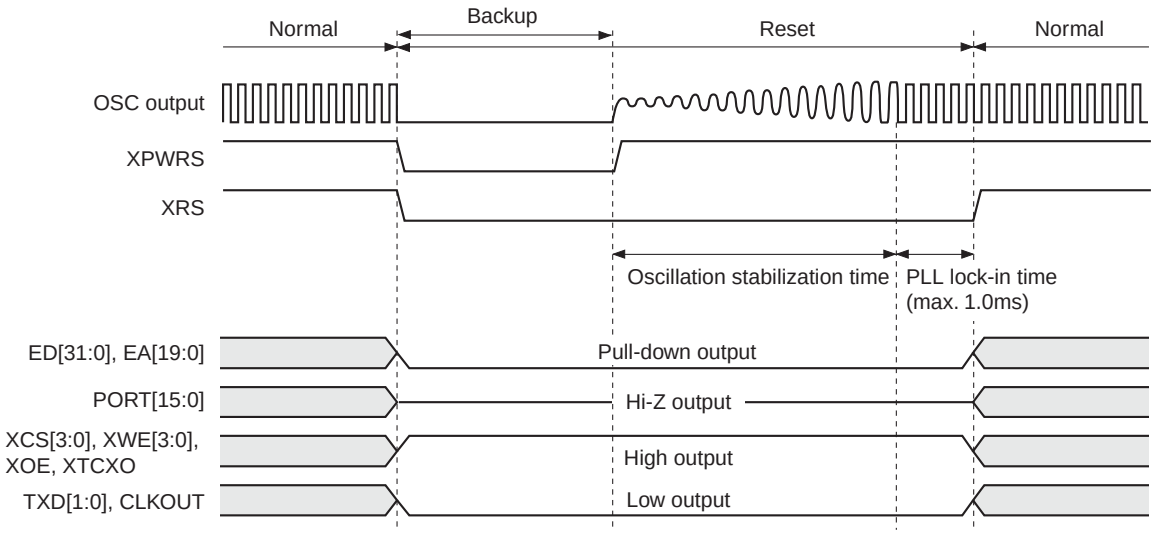
*1 0WAIT (normal), 1 to 3WAIT (settable according to the program)



* Tsys: CPU clock cycle

Backup Mode

When the power supply of the GPS receiver system is off (XPWRS = low: the external pull-down is necessary) and the reset state (XRS = low) is established, the device goes into the low power consumption state (backup mode) where the all oscillators except for the timer stop. The whole internal memory status at this time is retained and the Hot Start/Warm Start can be achieved. In order to cancel this mode, set the XRS pin to high after XPWRS is set to high and then the oscillation stabilization time and the PLL lock-in time are waited. (Normal operation / reset : V_{DD} = 3.0 to 3.6V, backup mode : V_{DD} = 2.0 to 3.6V)

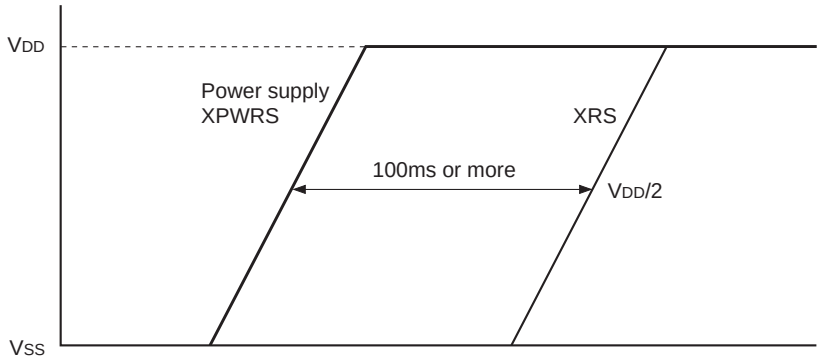


Initialization Setting

The device initialization is started by setting the reset pin (XRS) to low level. The timing should satisfy the conditions noted below.

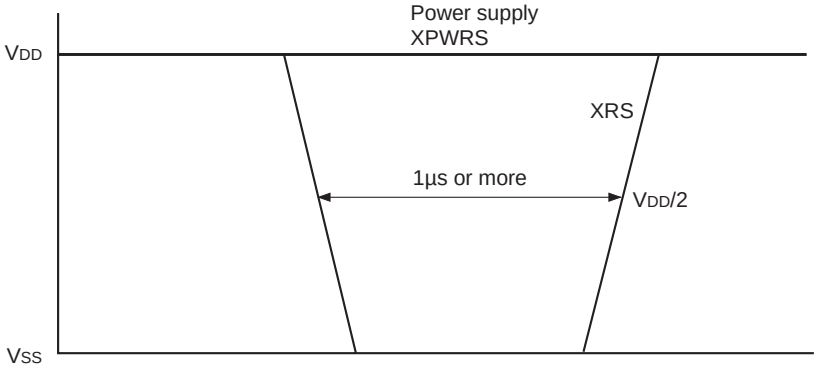
(1) During power-on (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

XPWRS should rise simultaneously with the power supply. XRS should rise 100ms or more after the power supply and XPWRS have risen.



(2) Initialization during operation (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

The internal registers can be initialized during operation by setting the XRS signal to low level for 100µs or more. Keep the XPWRS signal at high level at this time. (The internal memory value is held.)

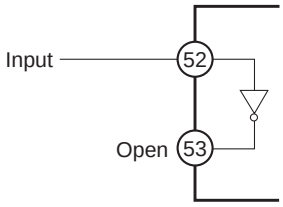


Application Notes

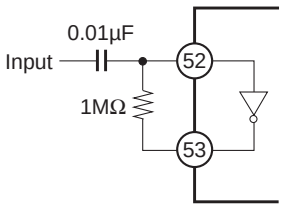
The constants shown in the circuits below are the examples, and do not guarantee the circuit operation.

(1) TCXO input

(a) When inputting the binary-converted signal
The TCXO input signal should be 18.414MHz ± 3ppm.



(b) When performing the self-oscillation with the TCXO and XTCXO pins
The TCXO input signal should be 18.414MHz ± 3ppm.
For inputting the signal which is not binary converted, the signal should go through the DC cut capacitor.

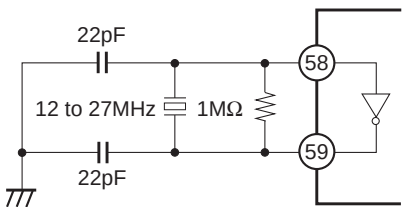


(2) CPU clock generation

(a) CPU clock selector
The CLKS2, CLKS1 and CLKS0 pins are used to select that the TCXO clock is used or that the self-oscillation is performed with the CLKI and CLKO pins. Set the CLKI pin to low when the TCXO clock is used. (CLKS[2:0] = 001: recommendation)

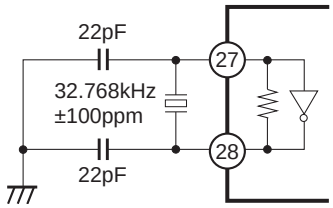
CLKS[2:0]	CLKI, CLKO	CPU frequency
001	—	TCXO × 1.0 (18.414MHz)
010	—	TCXO × 1.5 (27.671MHz)
101	18 to 27MHz	CLKI × 1.0 (18 to 27MHz)
110	12 to 18MHz	CLKI × 1.5 (18 to 27MHz)

(b) When performing the self-oscillation with the CLKI and CLKO pins
The crystal oscillator frequency should be within the values shown above.



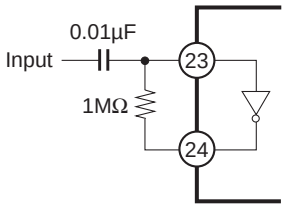
(3) Timer clock setting

When using the real-time clock (RTC) circuit in the device, connect the crystal oscillator of 32.768kHz ± 100ppm to the CCKI and CCKO pins. When using the external RTC circuit, set the CCKI pin to the low level. See the Port setting for the RTC internal/external selection.



(4) IF signal input

This device's IF signal supports only 1.023MHz. When the signal which is not binary-converted is input, the signal should go through the DC cut capacitor.



(5) Serial input/output communication system

See the corresponding data sheet for communication because the communication specification differs according to the communication format. See the Port setting for the communication format selection.
The transmission data (TXD0 and TXD1) amplitude is 0.4V or less for the low level and V_{DD} – 0.4V or more for the high level. When the LSI and others connected to this operate at 5V and the CMOS level input is used, convert 3V to 5V for input.

(6) Port setting

When the power turns on or initialization setting is performed by the reset input, the system starts operation according to the selected port setting. Perform initialization after the setting is changed because the setting can not be changed during operation.

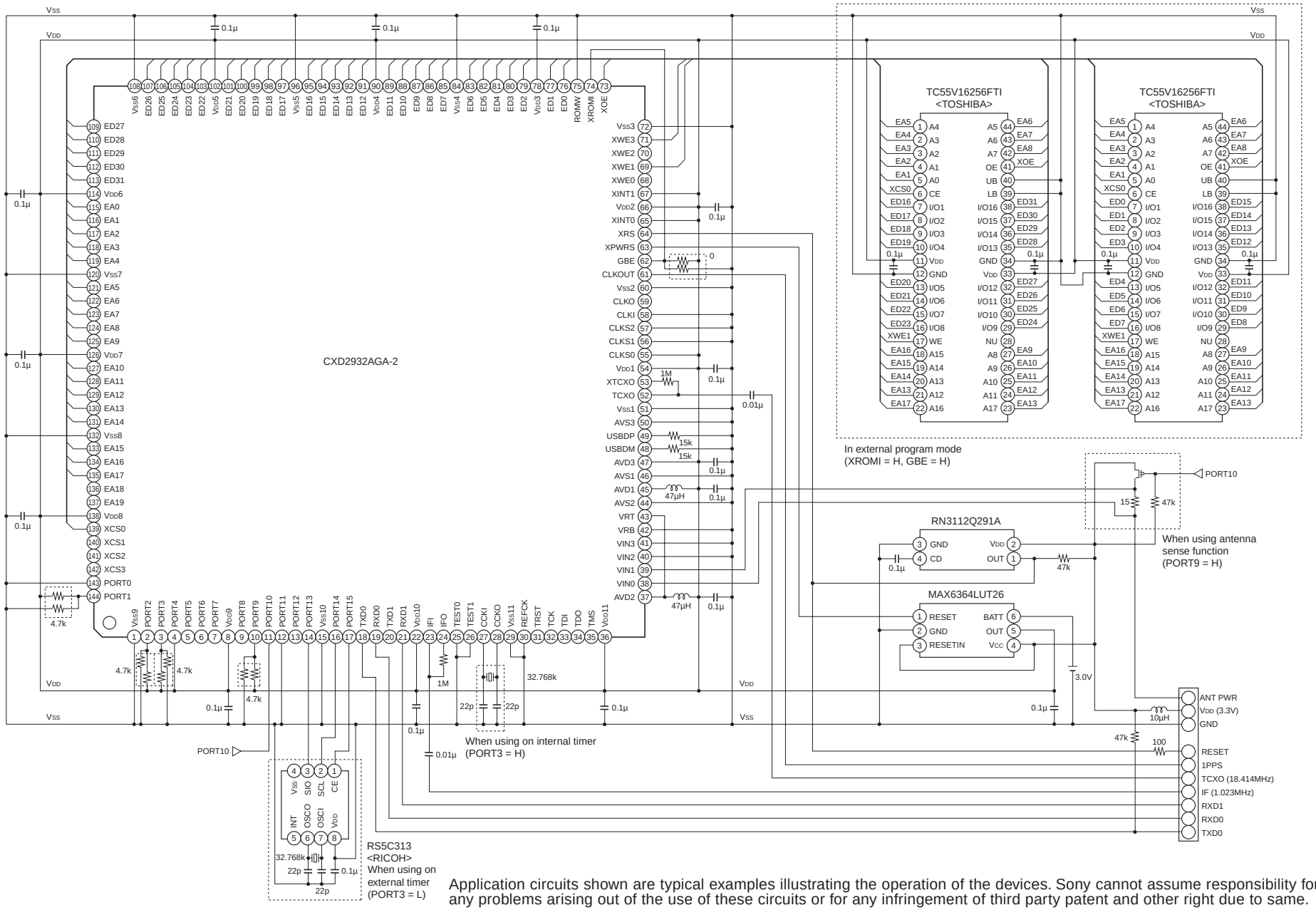
Port	I/O		Description
	For reset	For operation	
0	I	I	Test pin (Low = Normal mode)
1	I	I	Communication format selection PORT[2:1] = (00: Sony Binary, 01: NMEA4800, 10: NMEA9600, 11: Unused)
2	I	I	
3	I	I	RTC selection (High = Internal / Low = External)
4	I	I	Test pin (High = Normal mode)
5	I	I	Test pin (Low = Normal mode)
6	I	O	Unused
7	I	O	Unused
8	I	O	Unused
9	I	I	Antenna sense (Low = Disable / High = Enable)
10	I	O	Antenna shutdown (High = Cut)
11	I	I	Test pin (Low = Normal mode)
12	I	O	Unused
13	I	I/O	RTC SIO (Leave open when the internal RTC is selected.)
14	I	O	RTC SCL (Leave open when the internal RTC is selected.)
15	I	O	RTC CE (Leave open when the internal RTC is selected.)

(7) A/D setting

The antenna sense function can be realized by connecting the antenna power supply of the GPS receiver to the A/D channel pins shown below. See the Application Circuit for the resistance value and others. See the Port setting for the antenna sense function disable/enable selection.

VIN	I/O		Description
	For reset	For operation	
0	I	I	Antenna power supply (before current value detection resistor)
1	I	I	Antenna power supply (after current value detection resistor)
2	I	I	Test pin (Low level fixed)
3	I	I	Test pin (Low level fixed)

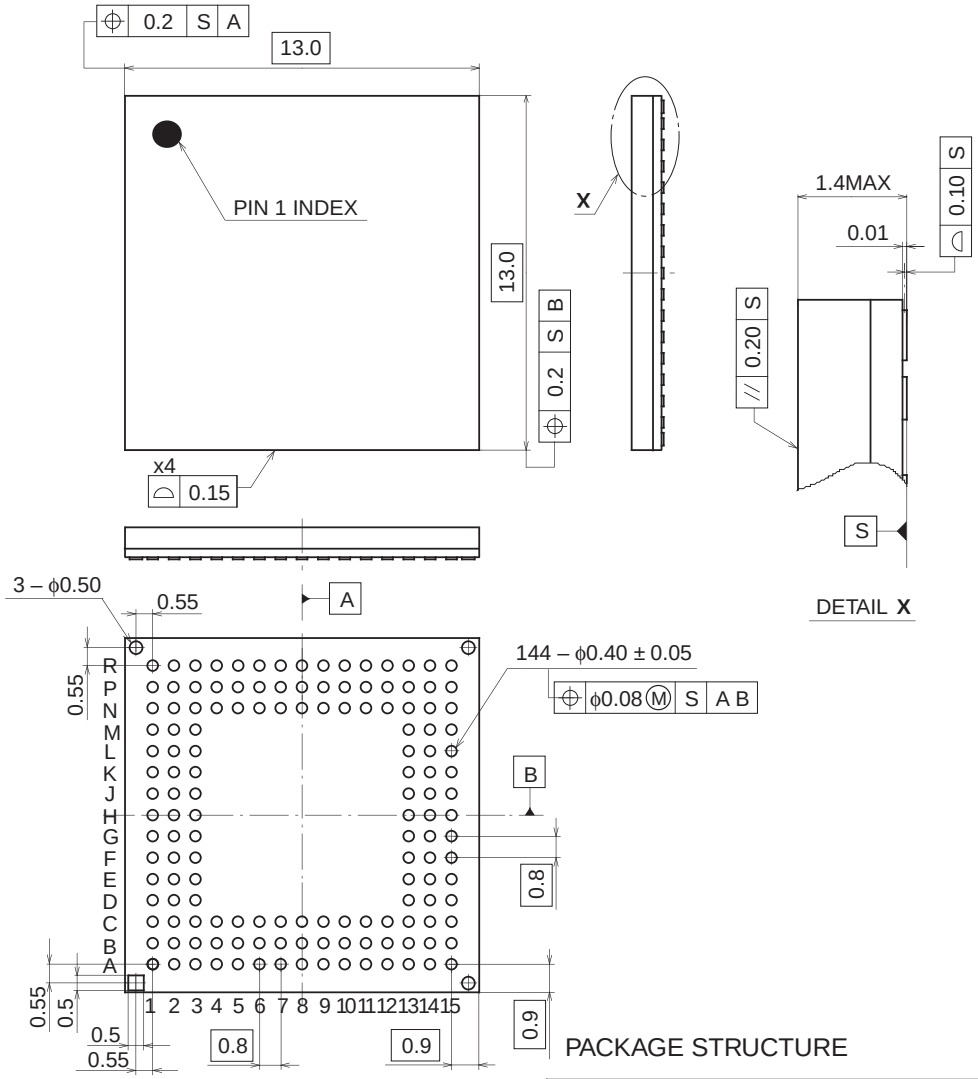
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

144PIN LFLGA



PACKAGE STRUCTURE

SONY CODE	LFLGA-144P-01
EIAJ CODE	P-LFLGA144-13x13-0.8
JEDEC CODE	————

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.5g