SONY

CXD2163BR

Signal Processor LSI for Single-Chip CCD Color Camera

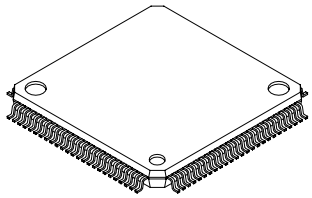
Description

The CXD2163BR is a signal processor LSI for Ye, Cy, Mg and G single-chip CCD color cameras. In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.

This chip also has a built-in microcontroller to realize basic camera functions without a microcomputer.

The CXD2163BR is a fully improved version and pin compatible with the CXD2163R by adding some functions and improving its performance.

100 pin LQFP (Plastic)



Features

- Single-chip CCD camera sync signal generation and luminance/chroma signal processing
- Supports NTSC/PAL modes
- Supports 360H/510H/720H/760H system CCD image sensors
- Y/C digital output pin (2 mode selection)
  — ITU—REC601 or 8-bit straight format
- Built-in 8-bit A/D converter
  — External 9/10-bit A/D converter can be selected
- Supports external sync functions (LL, VS, VBS, etc.)
  — Sync separation circuit, phase comparator
- AE/AWB detector
- Block control functions with a built-in microcontroller
  — AE/AWB/YC/CLAMP/SG control functions
- Peripheral IC communication control functions
  — TG, EVR, EEPROM communication control
- Serial communication function (2 mode selection)
  — Microcomputer or RS232C
- Defect compensation function

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0..5	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
	AV_{DD}	4.7 to 5.5	V
	AV_{DD}3 only	3.0 to 3.6	V
• Operating temperature			
	Topr	–20 to +75	°C

Applications

- Industrial CCD cameras (surveillance/FA/image input cameras)
- Multimedia CCD cameras (teleconferencing/personal computer cameras)

Applicable CCD Image Sensors*

Type 1/5 360H color CCDs
Type 1/3, Type 1/4, Type 1/6 510H color CCDs
Type 1/4 720H color CCD
Type 1/2, Type 1/3, Type 1/4 760H color CCDs

Supported Related LSIs

TG:	CXD2480R
AFD:	CXD2418R
AGC:	CXA2006Q
ADC:	CXD2311AR (10bit)
	CXD2312R (9bit)
EVR:	MB88347: 8 channels
	MB88346: 12 channels (Fujitsu Limited.)
EEPROM:	AK6420
	(Asahi Kasei Microsystems Co., Ltd.)

* Applicable CCD Image Sensors are applicable products as of preparing this data sheet.
They may be changed according to the version up and production stop of CCD image sensor.

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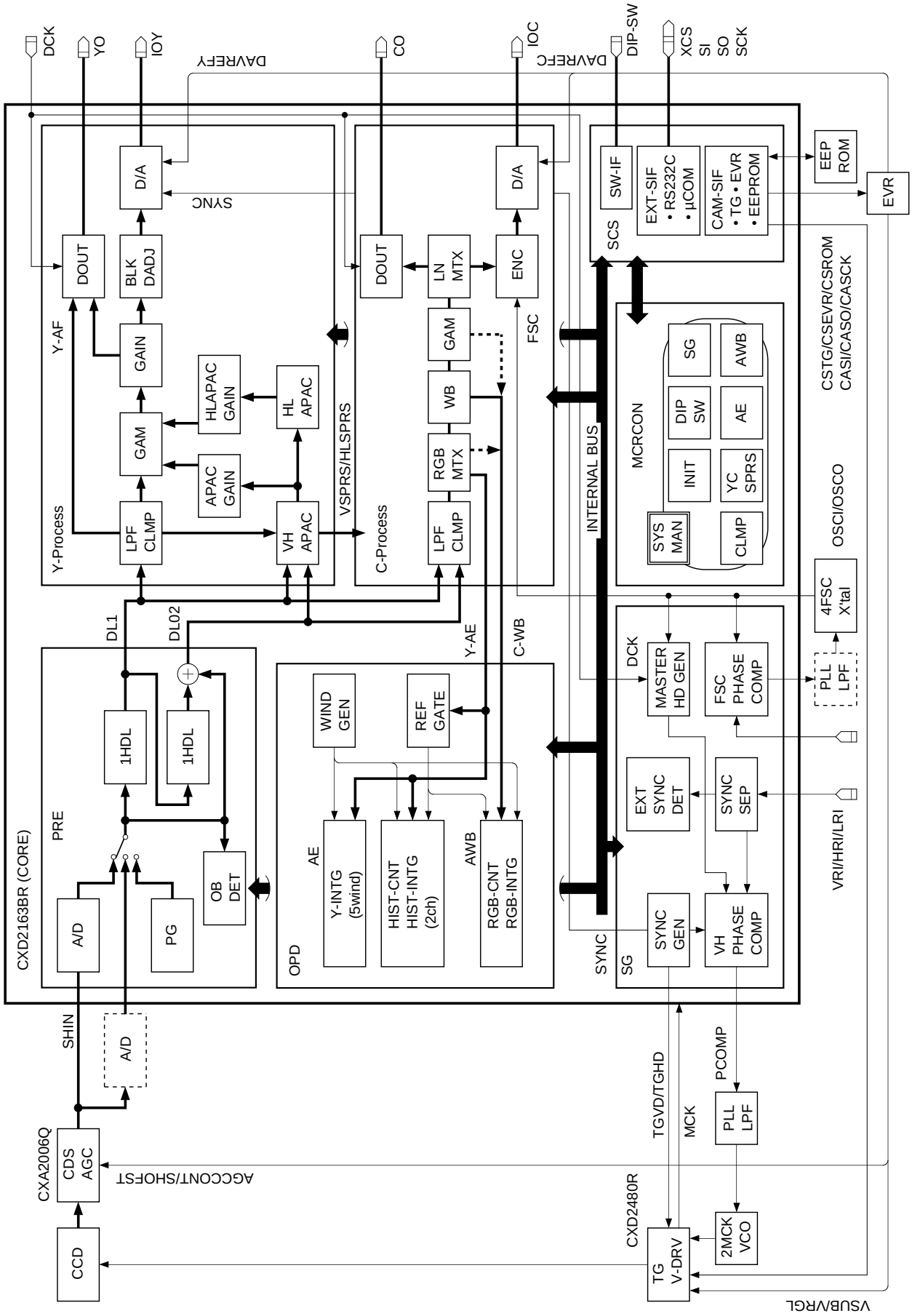
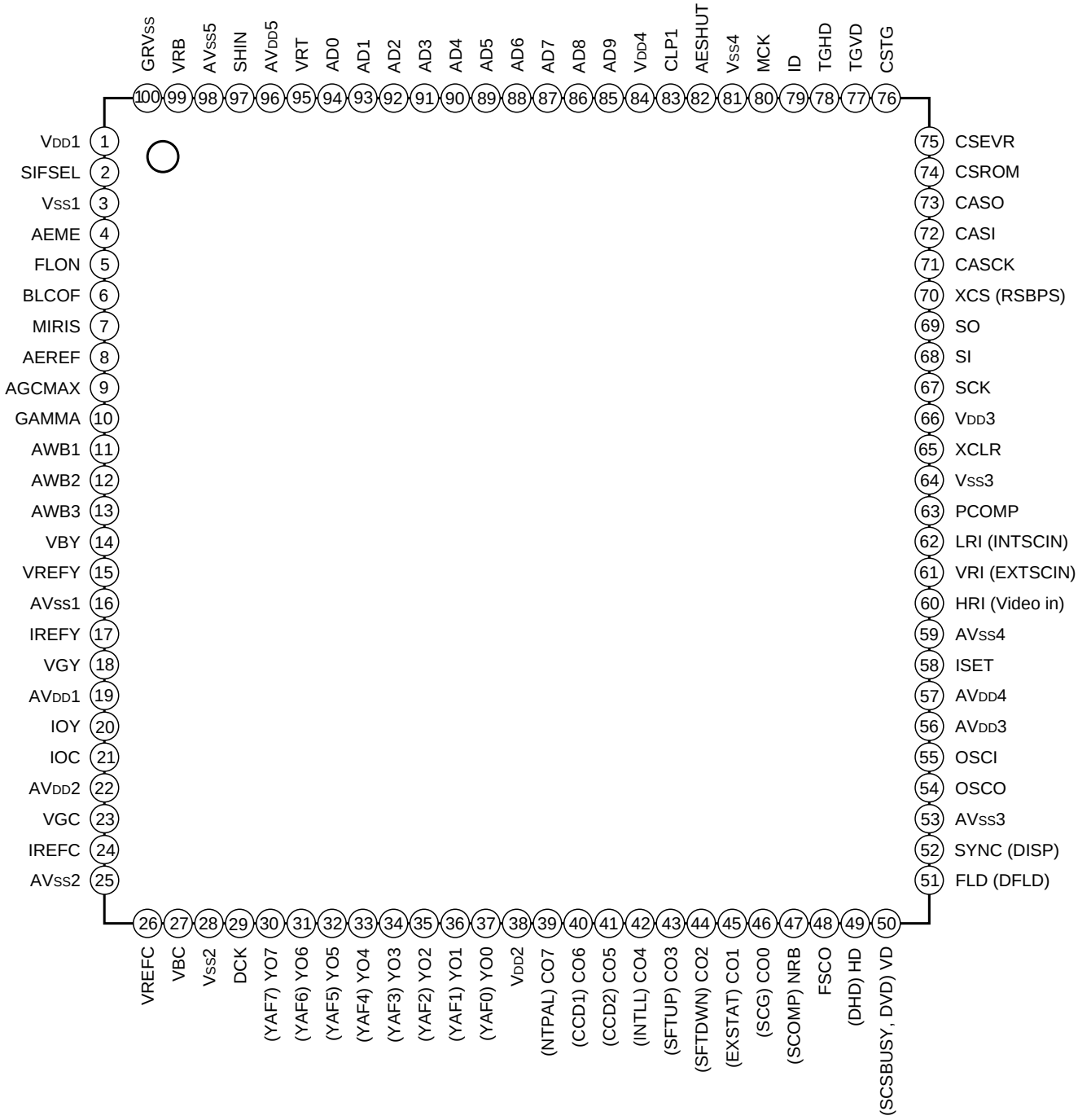
Block Diagram



Pin Configuration



Note) Symbols in parentheses are the signal names when the LSI is switched by the serial communication settings.
All pin symbols (pin names) for the CXD2163BR are the names next to the pin No. (outside the parentheses)

Pin Description

Pin No.	Symbol	I/O	Description	
1	$V_{DD}1$	—	Digital power supply (+3.3V)	
2	SIFSEL	I	Serial interface mode switching 0: microcomputer, 1: RS232C	
3	$V_{SS}1$	—	Digital GND	
4	AEME	I	AE mode switching 0: auto, 1: manual	
5	FLON	I	Flickerless mode (auto)/Shutter speed control (manual)	SW setting pin system
6	BLCOF	I	Backlight compensation off (auto)/Shutter speed control (manual)	
7	MIRIS	I	Iris mode switching (auto)/Shutter speed control (manual)	
8	AEREF	I	AE convergence level switching (auto)/Fixed gain mode selection (manual)	
9	AGCMAX	I	AGC maximum gain switching (auto)/Fixed gain mode selection (manual)	
10	GAMMA	I	Gamma correction 0: ON, 1: OFF	
11	AWB1	I	AWB mode switching 0: auto, 1: manual	
12	AWB2	I	ATW/push lock switching (auto)/Fixed WB mode selection (manual)	
13	AWB3	I	Push lock signal input (auto)/ Fixed WB mode selection (manual)	
14	VBY	I (A)	Capacitor connection pin (about 0.1µF) (for luminance signal D/A)	Luminance signal D/A
15	VREFY	I (A)	Reference voltage setting pin (for luminance signal D/A)	
16	$AV_{SS}1$	—	Analog GND (for luminance signal D/A)	
17	IREFY	O (A)	Reference current setting pin (for luminance signal D/A)	
18	VGY	I (A)	Capacitor connection pin (about 0.1µF) (for luminance signal D/A)	
19	$AV_{DD}1$	—	Analog power supply (for luminance signal D/A)	
20	IOY	O (A)	Luminance signal (current) output pin	
21	IOC	O (A)	Chroma signal (current) output pin	Chroma signal D/A
22	$AV_{DD}2$	—	Analog power supply (for chroma signal D/A)	
23	VGC	I (A)	Capacitor connection pin (about 0.1µF) (for chroma signal D/A)	
24	IREFC	O (A)	Reference current setting pin (for chroma signal D/A)	
25	$AV_{SS}2$	—	Analog GND (for chroma signal D/A)	
26	VREFC	I (A)	Reference voltage setting pin (for chroma signal D/A)	
27	VBC	I (A)	Capacitor connection pin (about 0.1µF) (for chroma signal D/A)	
28	$V_{SS}2$	—	Digital GND	
29	DCK	I/O	Clock I/O pin for digital output YO/CO *1	

*1 The I/O direction changes according to the serial data settings and CCD type.

Pin No.	Symbol	I/O	Description			
30	YO7	O	MSB*2		YAF7	MSB*2
31	YO6	O			YAF6	
32	YO5	O			YAF5	
33	YO4	O			YAF4	AF detection signal outputs
34	YO3	O	Luminance signal digital outputs		YAF3	(preset settings)
35	YO2	O			YAF2	
36	YO1	O			YAF1	
37	YO0	O	LSB		YAF0	LSB
38	$V_{DD}2$	—	Digital power supply (+3.3V)			
39	CO7	I/O	MSB*3	NTPAL	TV mode switching 0: NTSC, 1: PAL*3	Basic settings
40	CO6	I/O		CCD1	CCD type 0h: 360H, 1h: 510H*3	
41	CO5	I/O		CCD2	2h: 720H, 3h: 760H*3	
42	CO4	I/O	Chroma signal	INTLL	Line lock mode 0: OFF, 1: ON*3	External sync system
43	CO3	I/O	digital outputs	SFTUP	Phase shifter (UP) signal input*3	
44	CO2	I/O		SFTDWN	Phase shifter (DOWN) signal input*3	
45	CO1	O		EXSTAT	Extend sync mode identification output*3	
46	CO0	O	LSB	SCG	Subcarrier gate pulse output*3	
47	NRB	O	Color identification signal output *3	SCOMP	Subcarrier phase comparator output*3	
48	FSCO	O	Subcarrier output			Sync signal system
49	HD	O	Horizontal sync signal (HD) output *4, 5			
50	VD	O	Vertical sync signal (VD) output *4, 5	SCSBUSY	Serial BUSY signal output*4	
51	FLD	O	Field identification signal (FLD) output *4, 5			
52	SYNC	O	Composite sync signal output *4	DISP	OPD detection frame output*4	
53	$AV_{SS}3$	—	Analog GND (for 4fsc oscillator)			Oscillator
54	OSCO	O	4fsc oscillator output (for subcarrier generation)			
55	OSCI	I	4fsc oscillator input (for subcarrier generation)			
56	$AV_{DD}3$	—	Analog power supply (+3.3V, for 4fsc oscillator)			
57	$AV_{DD}4$	—	Analog power supply (+5V, for sync separation circuit)			Sync separator
58	ISET	I (A)	Current source input (for sync separation circuit)			
59	$AV_{SS}4$	—	Analog GND (for sync separation circuit)			
60	HRI	I (A)	External sync signal input (composite video signal input/H reset signal input)			

*2 The output signal contents change according to the serial data settings. The preset setting when cleared is YAF0 to 7 output.

*3 The functions of these pins change according to the serial data settings. The preset settings when cleared are basic settings/external sync system.

*4 The output contents change according to the serial data settings. The preset settings are HD, VD, FLD and SYNC output.

*5 The output change to sync signals (DFLD, DVD, DHD) for digital outputs according to the serial data settings.

Pin No.	Symbol	I/O	Description			
61	VRI	I	External sync signal input (external burst signal input/V reset signal input)			
62	LRI	I/O	External sync signal I/O (LALToutput/LALT reset signal input/internal subcarrier input)			
63	PCOMP	O	Phase comparator output for HPLL/VPLL			
64	$V_{SS}3$	—	Digital GND			
65	XCLR	I	Clear input pin			
66	$V_{DD}3$	—	Digital power supply			
67	SCK	I	Serial clock input for microcomputer communication (fixed to 1 during RS232C mode)			External communication system
68	SI	I	Serial data input for microcomputer/RS232C communication			
69	SO	O	Serial data output for microcomputer/RS232C communication			
70	XCS	I	Chip select input for microcomputer communication	RSBPS	RS232C BPS setting *6	
71	CASCK	O	Serial clock output for camera peripheral ICs (to TG, EVR, EEPROM)			Peripheral IC communication system
72	CASI	I	Serial data input for camera peripheral ICs (from EEPROM)			
73	CASO	O	Serial data output for camera peripheral ICs (to TG, EVR, EEPROM)			
74	CSROM	O	Chip select output for camera peripheral ICs (to EEPROM)			
75	CSEVR	O	Chip select output for camera peripheral ICs (to EVR)			
76	CSTG	O	Chip select output for camera peripheral ICs (to TG)			
77	TGVD	O	Vertical sync signal output for TG			TG system
78	TGHD	O	Horizontal sync signal output for TG			
79	ID	I	Line identification signal input			
80	MCK	I	CXD2163BR master clock input			
81	$V_{SS}4$	—	Digital GND			
82	AESHUT	I	1: Shutter speed manual & AGCamp auto mode (AEME pin = 0)			
83	CLP1	O	Analog optical black clamp pulse output			
84	$V_{DD}4$	—	Digital power supply (+3.3V)			

*6 Valid only during RS232C mode. RSBPS = 0: 4800bps, 1: 9600bps

Pin No.	Symbol	I/O	Description	
85	AD9	I	MSB*7	
86	AD8	I		
87	AD7	I		
88	AD6	I		
89	AD5	I		
90	AD4	I	Digital signal data inputs from external A/D	
91	AD3	I		
92	AD2	I		
93	AD1	I		
94	AD0	I	LSB	
95	VRT	I (A)	Reference top voltage input pin (for built-in A/D converter)*7	Built-in A/D
96	$AV_{DD}5$	—	Analog power supply (+5V, for built-in A/D converter)*7	
97	SHIN	I (A)	Analog signal input pin (for built-in A/D converter)*7	
98	$AV_{SS}5$	—	Analog GND (for built-in A/D converter)*7	
99	VRB	I (A)	Reference bottom voltage input pin (for built-in A/D converter)*7	
100	GRV_{SS}	—	Analog GND for noise guard (for built-in A/D converter)*7	

*7 AD0 to 9 (Pins 85 to 94) or the built-in A/D (Pins 95 to 100) are selected by the serial data settings. The preset setting when cleared is the built-in A/D.

I: Digital input
O: Digital output
I/O: Digital I/O
I (A): Analog input
O (A): Analog output

Electrical Characteristics

DC Characteristics

(Within recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}1, 2, 3, 4		3.0	3.3	3.6	V
	AV_{DD}1, 2	D/A output amplitude = 2Vp-p	4.7	5.0	5.5	V
	AV_{DD}3		3.0	3.3	5.5	V
	AV_{DD}4		4.7	5.0	5.5	V
	AV_{DD}5	A/D input amplitude = 2Vp-p	4.7	5.0	5.5	V
Output voltage1	$V_{OH}1$*1	I_{OH} = –1.2mA	V_{DD} – 0.8			V
	$V_{OL}1$*1	I_{OL} = 2.4mA			0.4	V
Output voltage2	$V_{OH}2$*2	I_{OH} = –2.4mA	V_{DD} – 0.8			V
	$V_{OL}2$*2	I_{OL} = 4.8mA			0.4	V
Input voltage1	$V_{IH}1$*3		$V_{DD} \times 0.7$			V
	V_{IL}*3				$V_{DD} \times 0.3$	V
Input voltage2	V_{T+}*4, 5		$V_{DD} \times 0.8$			V
	V_{T-}*4, 5				$V_{DD} \times 0.2$	V
Hysteresis 1	$V_{T+} – V_{T-}$*4			0.5		V
Hysteresis 2	$V_{T+} – V_{T-}$*5			0.6		V
Input leak current1	I_I1*3, 5	V_{IN} = V_{SS} or V_{DD}	–10		10	µA
Input leak current2	I_I2*4	V_{IN} = V_{SS} or V_{DD}	–40		40	µA
Input leak current3	I_{IH}*6	V_{IN} = V_{DD}	12	30	75	µA

*1 All output pins other than CASCK, CASO and DCK

*2 CASCK, CASO, DCK

*3 AD9 to 0, MCK, ID, VRI, DCK

*4 LRI, CO7 to 0, AEME, FLON, BLCOF, MIRIS, AEREF, AGCMAX, GAMMA, AWB1 to 3, SIFSEL

*5 XCS, SI, SCK, XCLR, CASI

*6 SIFSEL

I/O Pin Capacitance

(V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	PF

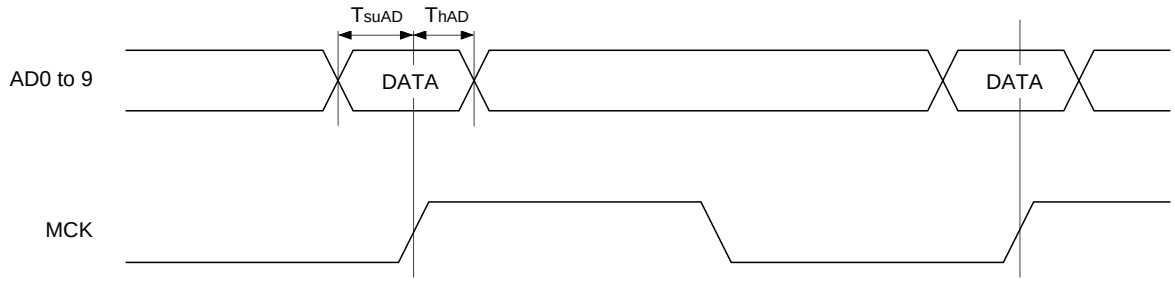
AC Characteristics

(Whithin recommended operating range, Load capacity of CL = 20pF)

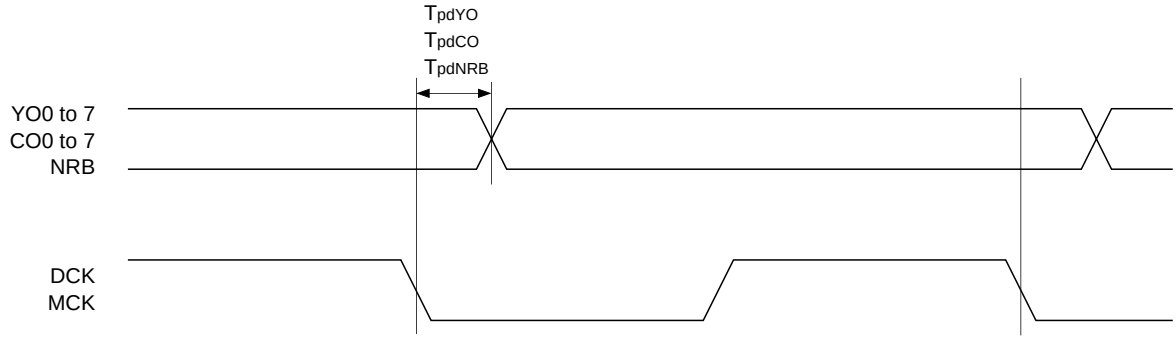
Classification	Item	Symbol	Min.	Typ.	Max.	Unit
AD input (AD0 to 9)	AD0 to 9 input set-up time, activated by the rising edge of MCK	T_{suAD}	20	—	—	ns
	AD0 to 9 input hold time, activated by the rising edge of MCK	T_{hAD}	0	—	—	ns
Digital output (YO0 to 7) (CO0 to 7)	YO0 to 7 output delay time, activated by the falling edge of DCK (DCK input mode)	T_{pdYO}		26		ns
	CO0 to 7 output delay time, activated by the falling edge of DCK (DCK input mode)	T_{pdCO}		26		ns
	NRB output delay time, activated by the falling edge of DCK (DCK input mode)	T_{pdNRB}		26		ns
	YO0 to 7 output delay time, activated by the falling edge of MCK (DCK output mode)	T_{pdYO}		15		ns
	CO0 to 7 output delay time, activated by the falling edge of MCK (DCK output mode)	T_{pdCO}		15		ns
	NRB output delay time, activated by the falling edge of MCK (DCK output mode)	T_{pdNRB}		15		ns
YAF output (YO0 to 7)	YO0 to 7 output delay time, activated by the rising edge of MCK	T_{pdYAF}		23		ns
CLEAR input (XCLR)	XCLR pulse width (Minimum low period for reset operation)	T_{wCLR}	500	—	—	ns
Sync pulse for S/H, TG	ID input set-up time, activated by the rising edge of MCK	T_{suID}	16	—	—	ns
	ID input hold time, activated by the rising edge of MCK	T_{hID}	6	—	—	ns
	TGVD, TGHD, CLP1 output delay time, activated by the rising edge of MCK	T_{pdTG}	6	12	28	ns
Sync pulse for video out	SYNC, FLD, VD and HD output delay time, activated by the rising edge of MCK	T_{pdSYNC}	10	20	46	ns
Serial communication	SCK input pulse width (High)	T_{wHSCK}	430	—	—	ns
	SCK input pulse width (Low)	T_{wLSCK}	430	—	—	ns
	XCE input set-up time, activated by the falling edge of SCK	T_{suXCE}	430	—	—	ns
	XCE input hold time, activated by the rising edge of SCK	T_{hXCE}	640	—	—	ns
	SI input set-up time, activated by the rising edge of SCK	T_{suSI}	140	—	—	ns
	SI input hold time, activated by the rising edge of SCK	T_{hSI}	140	—	—	ns
	SO output transition time (Hi-Z → Data active), activated by the falling edge of XCE	T_{zdSO}	70	—	200	ns
	SO transition time (Data active → Hi-Z), activated by the rising edge of XCE	T_{dzSO}	70	—	200	ns
	SO output delay time, activated by the falling edge of SCK	T_{pdSO}	70	—	240	ns

AC Characteristics Diagrams

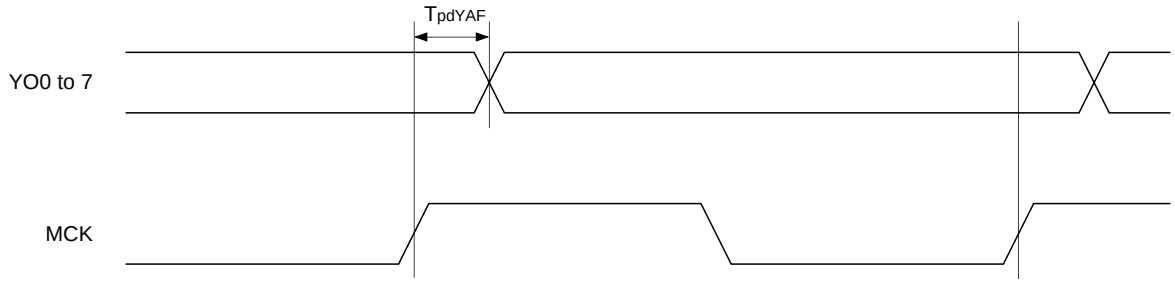
1. AD input



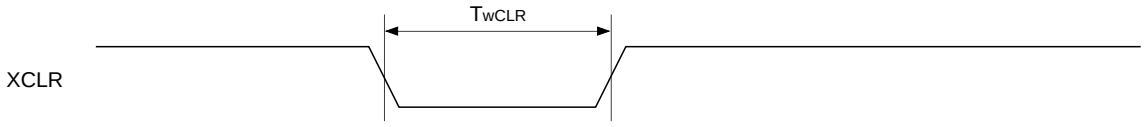
2. Digital output



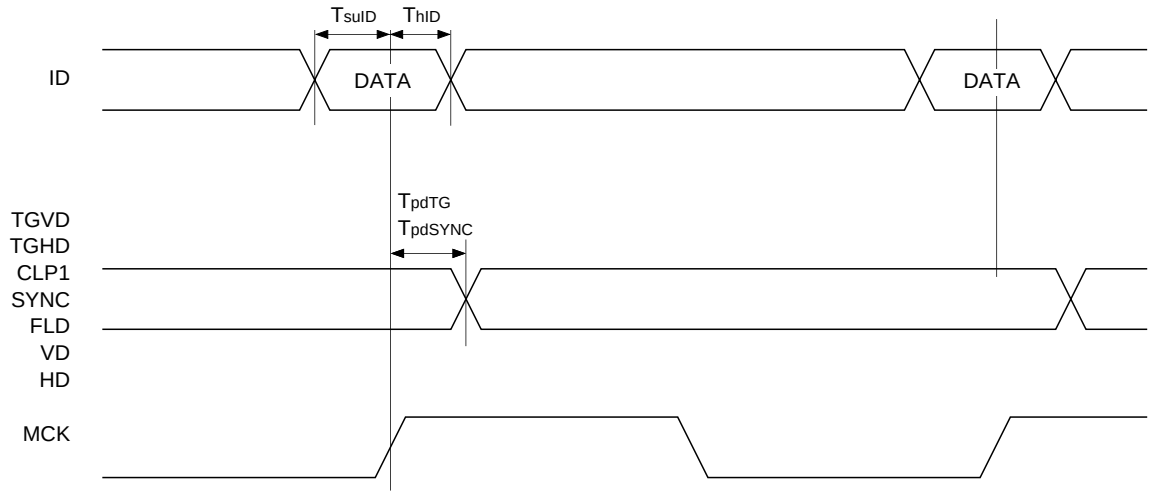
3. YAF output



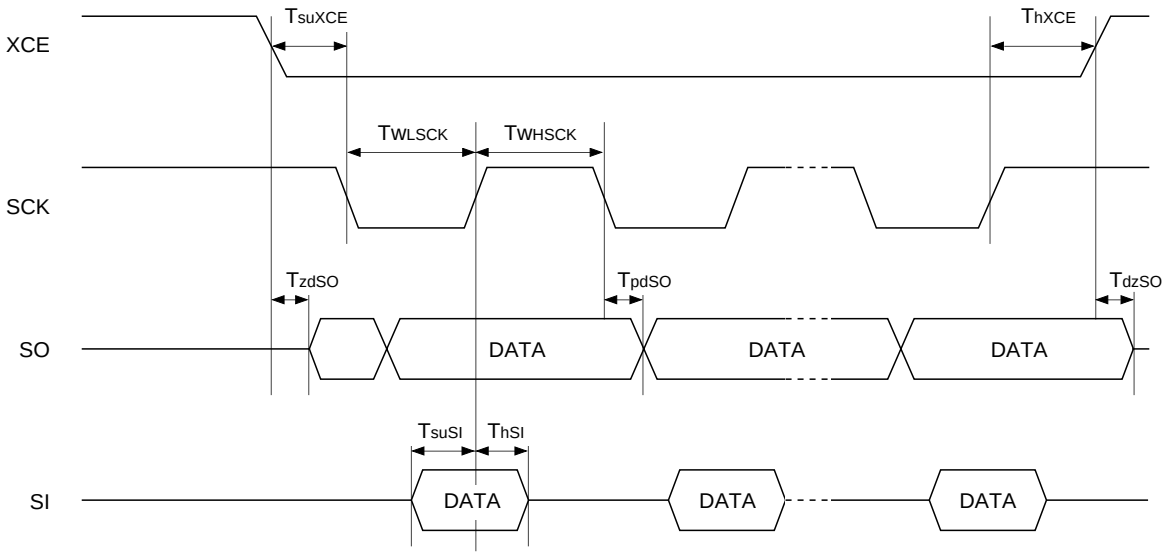
4. CLEAR input



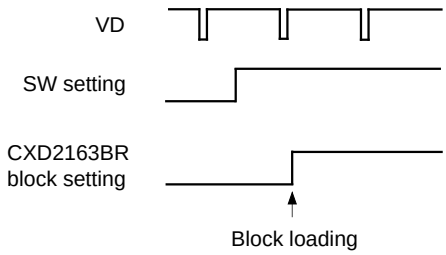
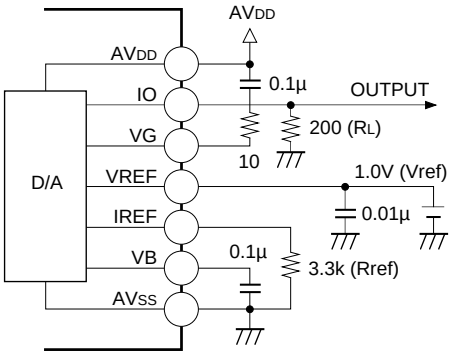
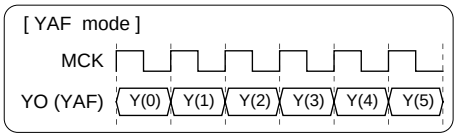
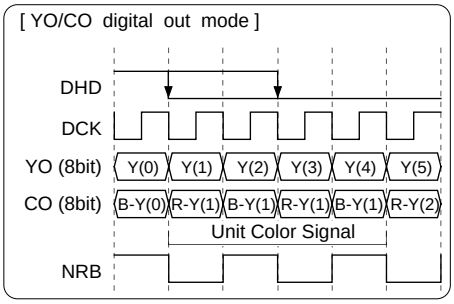
5. Sync pulse input/output

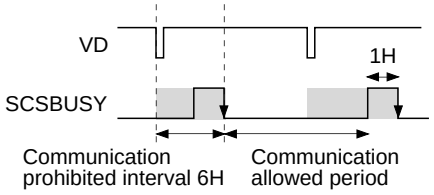


6. Serial communication (Microcomputer communication mode)

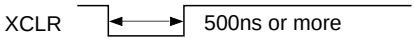
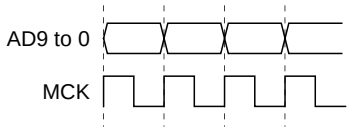


I/O Signals

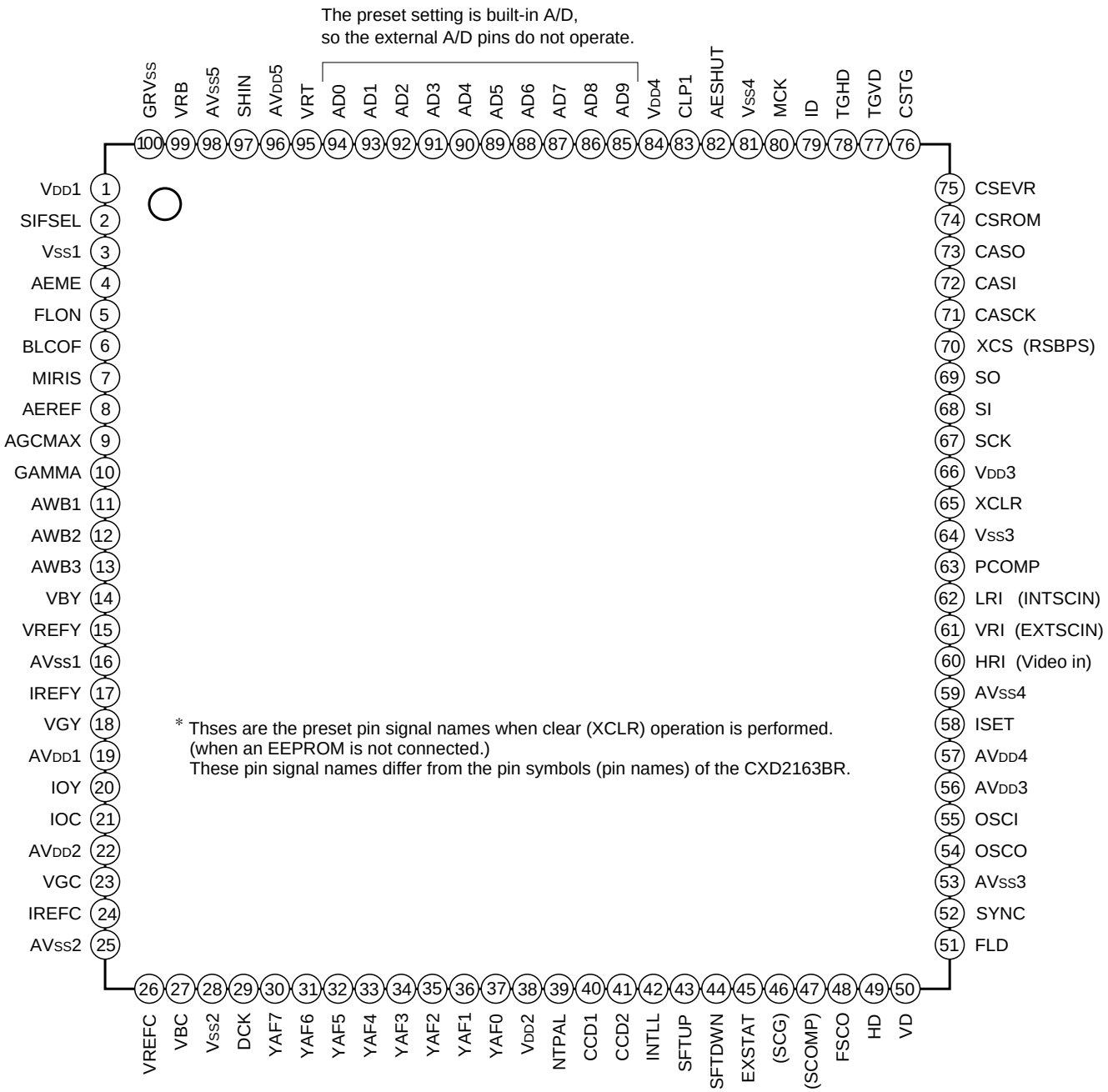
Symbol	Pin No.	Description
AEME FLON BLCOF MIRIS AEREF AGCMAX GAMMA AWB1 AWB2 AWB3	4 5 6 7 8 9 10 11 12 13	These are input pins for the SW setting. AE/AWB/gamma operation is switched by inputting high/low to these pins. The timing for loading the SW setting to each block is the V blanking following the field where the setting was input. 
VBY VREFY AVSS1 IREFY VGY AVDD1 IOY IOC AVDD2 VGC IREFC AVSS2 VREFC VBC	14 15 16 17 18 19 20 21 22 23 24 25 26 27	These pins form the peripheral circuits for the D/A converter that is used for luminance and chroma signal output. The setting voltage of Vref and the full-scale voltage (Vfs) of D/A are matched by setting the ratio of RL and Rref to 1:16. The calculation is shown below: Vfs = Vref × 16 × RL/Rref **Notes)** • IO = Vfs/RL should be 7mA or less. • RL should be 500Ω or less. (Recommended RL = 200Ω) • When Vfs is 2V, set the supply voltage (AVDD) to 5.0V. Also, when 0V ≤ Vfs < 2V, operation is possible with a supply voltage (AVDD) of 3.3V. 
YO0 to 7 CO0 to 7 NRB DCK (DHD)	30 to 37 39 to 46 47 29 (49)	YO/CO can be set to the following modes by the serial communication settings or the EEPROM setting values. CAT1 byte1 YDOUT = 0: YO = YAF mode 1: YO = Y digital out mode CAT1 byte1 UVDOUT = 0: CO = SW mode 1: CO = C digital out mode [YO = YAF mode (preset)] The Y-LPF processed luminance signal is output in sync with MCK (rise) for AF detection. The preset setting when cleared is YAF mode.  [YO = Y digital out mode] The Y-LPF/gamma/aperture correction/ blanking processed luminance signal is output in sync with DCK (fall). The following output formats can be selected. CAT1 byte 1 REC601 = 0: YO = 8-bit straight binary 1: YO = REC601  [CO = SW mode (preset)] These pins are the TV mode setting/CCD type setting/external sync system I/Os. The timing for loading the setting systems is the same as for Pins 4 to 13. The preset setting when cleared is SW mode. [CO = C digital out mode] The color difference signal immediately before the chroma encoder is output in sync with DCK (fall). NRB can be used as the chroma phase reference. Output starts from the B-Y phase in sync with the fall of DHD. The starting point is defined by the frequency ratio of MCK and DCK. The following output formats can be selected. CAT1 byte 1 REC601 = 0: CO = two's complement format 1: CO = REC601 (offset binary)

Symbol	Pin No.	Description
NRB DCK	47 29	[NRB output setting] Set (CAT1 byte 1 UVDOUT = 1) and (CAT9 byte 5 SCMPPIN = 1). [DCK I/O setting] The DCK pin is a normally input pin. However, in the following case only, MCK (13.5MHz) is output to the DCK pin. DCK output setting: When CCD type is set to 360H or 720H system, set (CAT1 byte 1 SG135 = 1).
FSCO	48	This pin outputs the subcarrier frequency signal. This pin outputs the OSCI/OSCO (Pins 54 and 55) oscillation cell output, divided by 4.
HD	49	This pin is the horizontal sync signal output. It is used to align the output and phase of the CXD2163BR's built-in Y, C-D/A. The output contents are switched by (CAT1 byte 14 HDPIN). To align the digital output pin YO/CO with the horizontal sync signal phase, switch this pin to DHD output. [DHD output setting] Set (CAT1 byte 1 DSYNC = 1).
VD	50	This pin is the vertical sync signal output. It is used to align the output and phase of the CXD2163BR's built-in Y, C-D/A. The output contents are switched by (CAT1 byte 14 VDPIN). When using an external microcomputer, the field cycle microcomputer interrupt signal (SCSBUSY) can be output from this pin. The CXD2163BR has a communication prohibited interval within the field which is convenient for synchronizing the start of microcomputer and CXD2163BR communication. Communication is allowed after the fall of SCSBUSY.  [SCSBUSY output setting] Set (CAT1 byte 13 VDBUSY = 1). VD phase is changed by the following settings. (linked with DHD) [DVD output setting] Set (CAT1 byte 1 DSYNC = 1).
FLD	51	This pin is the field identification signal output. The output contents are switched by (CAT1 byte 14 FLDPIN). FLD phase is changed by the following settings. (linked with DHD) [DFLD output setting] Set (CAT1 byte 1 DSYNC = 1).
SYNC	52	This pin is the composite sync signal output. The output contents are switched by (CAT1 byte 14 SYNCPIN). The OPD (AE/AWB) detection frame (DISP) can be output from this pin. This pin should be used for analog iris detection circuits, etc. [DISP output setting] Set (CAT1 byte 13 SYNDISP = 1). [Frame type selection] Select the AE/AWB frame according to the (CAT10 byte 3 OPDDISP) code.
OSCI OSCO	54 55	These pins are connected to the internal oscillation cell. Connect a 4fsc crystal vibrator to these pins.
HRI (Video in)	60	This pin is the external sync signal input. It is connected internally to the sync separation circuit (built-in clamp) and can be used to input the composite video signal (1Vp-p). When not using external sync, fix the HRI pin to 5.0V. Input the composite video signal or H reset signal according to the following conditions. Composite video signal input: When VS/VBS is locked during auto discrimination mode or when (CAT9 byte 1 SGMODE) is set to VS/VBS mode. (Care should be taken when using LL together with VS/VBS during auto mode.) H reset signal: When (CAT9 byte 1 SGMODE) is set to VRHR mode.

Symbol	Pin No.	Description
VRI (EXTSCIN)	61	This pin is the external sync signal input. When inputting an external burst signal, extract the burst with an external circuit, set the burst to the digital amplitude value (3.3Vp-p) and then input it to the VRI pin. The continuous subcarrier signal can be used as the input external burst signal, but the phase comparison period is only near the burst signal position (SCG (Pin 46)). When not using external sync, fix the VRI pin to 3.3V. Input the external burst signal or V reset signal according to the following conditions. External burst signal: When VBS is locked during auto discrimination mode or when (CAT9 byte 1 SGMODE) is set to VBS mode. (Care should be taken when using LL together with VS/VBS during auto mode.) V reset (V cycle) signal: When LL/VS is locked during auto discrimination mode or when (CAT9 byte 1 SGMODE) is set to LL/VRHR mode.
LRI (INTSCIN)	62	This pin is the external sync signal I/O. When VBS is locked, the FSCO (Pin 48) subcarrier output can be delayed with an external circuit and then re-input to the LRI pin for use in the chroma encoder in order to phase shift the subcarrier signal generated by the CXD2163BR. (In this mode, the LRI pin functions as the clock input pin for the chroma encoder block.) The LRI pin is normally the LALT signal output, but under the following conditions it functions as the LALT reset signal input or internal subcarrier input. LALT reset signal input: When (CAT9 byte 1 SGMODE) is set to VRHR mode. Internal subcarrier input: When (CAT9 byte 5 FSCPCMP = 1) is set with VBS locked during auto discrimination mode; or when (CAT9 byte 5 FSCPCMP = 1) is set with (CAT9 byte 1 SGMODE) is set to VBS mode.
PCOMP	63	This pin is the charge pump type phase comparator output for HPLL/VPLL. HPLL or VPLL phase comparison is selected according to the external sync mode of the SG block. The PCOMP output status can be classified into the following three states according to the SG mode. SG mode (including auto discrimination mode) No PCOMP output: VRHR PCOMP-V phase comparison output: LL PCOMP-H phase comparison output: INT, VS, VBS
EXSTAT (CO1)	45	This pin is the external sync mode identification output. It is normally low, but it goes high only when the external sync mode of the SG block is LL mode (including auto discrimination). This pin is convenient for switching the characteristics of the external PLL-LPF when using the PCOMP pin for both HPLL and VPLL. To use EXSTAT, set (CAT1 byte 1 UVDOUT = 0).
SCG (CO0)	46	This pin is the subcarrier gate pulse output. When the external sync mode of the SG block is VBS mode, this pin detects the externally input burst signal period and outputs a high pulse only during the burst period. The subcarrier phase comparator performs phase comparison only during this gate pulse period. To use SCG, set (CAT1 byte 1 UVDOUT = 0) and (CAT9 byte 5 FSCPCMP = 1).
SCOMP (NRB)	47	This pin is the subcarrier phase comparator output. It outputs the results of comparing the external burst input (VRI (Pin 61)) and the internal burst input (LRI (Pin 62)). The comparison interval is the SCG (Pin 46) pulse period. To use SCOMP, set (CAT1 byte 1 UVDOUT = 0) and (CAT9 byte 5 FSCPCMP = 1).

Symbol	Pin No.	Description
XCLR	65	This is the clear signal input pin. This clear operation initializes the entire chip and starts EEPROM loading operation. Input a low pulse. (This pin is active low.) Input clear signal during power on and initialize it. 
SIFSEL SCK SI SO XCS (RSBPS)	2 67 68 69 70	These pins are the microcomputer/RS232C serial communication I/Os. [When using microcomputer communication] Set the SIFSEL pin low. SI/SO data is transferred in sync with SCK only while XCS = low. [When using RS232C communication] Set the SIFSEL and SCK pins high. At this time, the XCS pin functions as the pin (RSBPS) which sets the RS232C transfer speed. RSBPS = 0: 4800 bps, 1: 9600 bps. (See the description of the serial communication method for other details.)
CASCK CASI CASO CSROM CSEVR CSTG	71 72 73 74 75 76	These pins are the serial communication I/Os for the camera peripheral ICs. The peripheral ICs where communication is performed are the TG, EVR and EEPROM. The TG and EVR communication timing is once per field during the V blanking. EEPROM read communication is performed for 3 consecutive fields only during the clear operation (XCLR). EEPROM write communication is performed once per field during the V blanking for AWB (push lock mode) and SG (external sync shifter).
TGVD TGHD ID MCK	77 78 79 80	These pins are I/Os for synchronization with the TG.
AESHUT	82	This is an input pin for the SW setting. AE operation is switched by inputting high/low to this pin. LNKAEOFF (Speccode54) = 0: AESHUT mode AEME pin = 0 & AESHUT pin = 0: AE full auto mode (Shutter & AGCamp out mode) AEME pin = 0 & AESHUT pin = 1: Shutter speed manual & AGCamp out mode AEME pin = 1 & AESHUT pin = X: Manual Exposure mode LNKAEOFF (speccode54) = 1: Low light suppress stop mode AESHUT = 0: Activate low light suppress function (AEME pin = X) AESHUT = 1: Stop low light suppress function (AEME pin = X)
CLP1	83	This pin is the clamp pulse output for DC fixing with a S/H IC.
AD0 to 9	85 to 94	These pins are digital data inputs for the external A/D. Input the A/D converted data output by the CCD in straight binary format to AD0 to 9. When using an external A/D, set (CAT1 byte 2 ADSEL = 0). When using an external 9-bit A/D, connect AD0 (Pin 94) to GND. 
VRT SHIN VRB GRVSS	95 97 99 100	These pins are analog inputs for the built-in A/D. The preset setting when cleared is the built-in A/D. GRVSS (Pin 100) is used to guard the built-in A/D from internal noise. Connect these pins to GND points with as little noise as possible.

Preset pin signal names when clear operation is performed

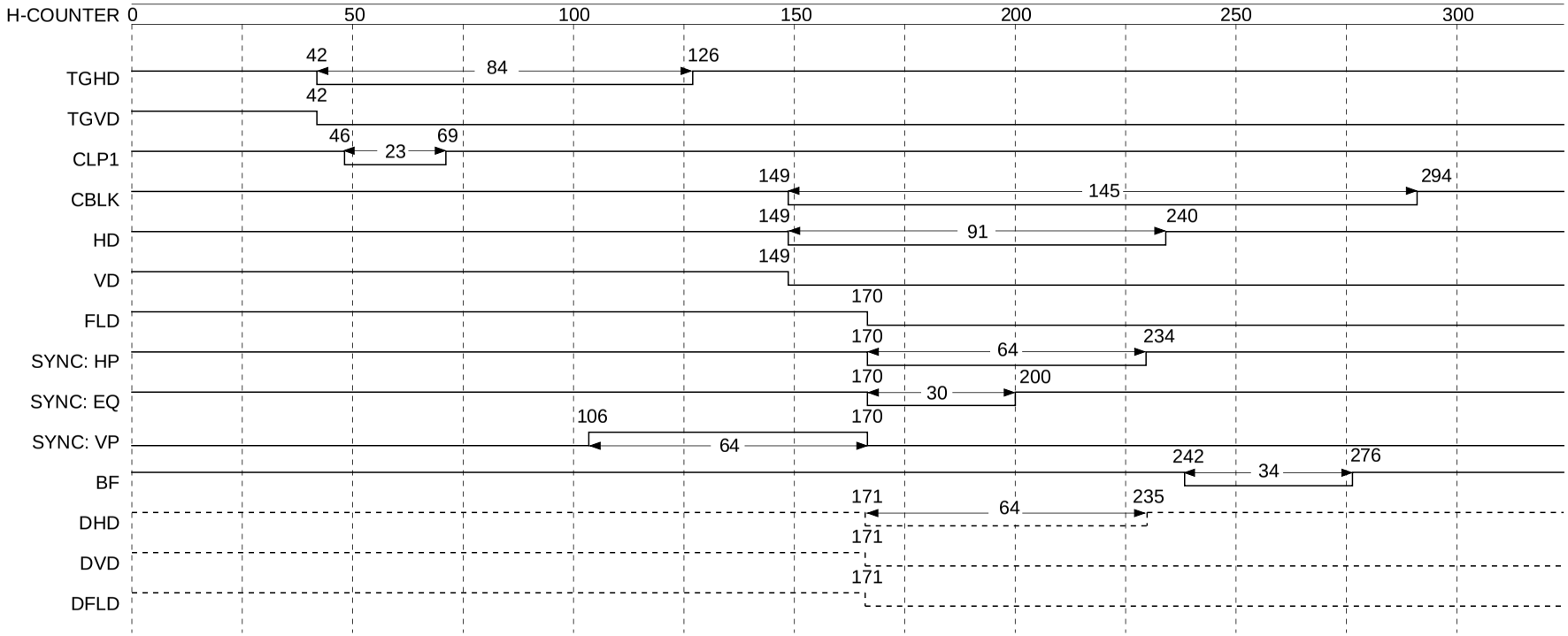


1) To perform pin settings other than those noted above, write the settings to the EEPROM or switch the setting using microcomputer/RS232C communication.

2) To operate SCG and SCOMP, switch the setting using the EEPROM or microcomputer/RS232C communication so that (CAT9 byte 5 FSCPCMP = 1).

(1) 360H NTSC Horizontal Timing Chart

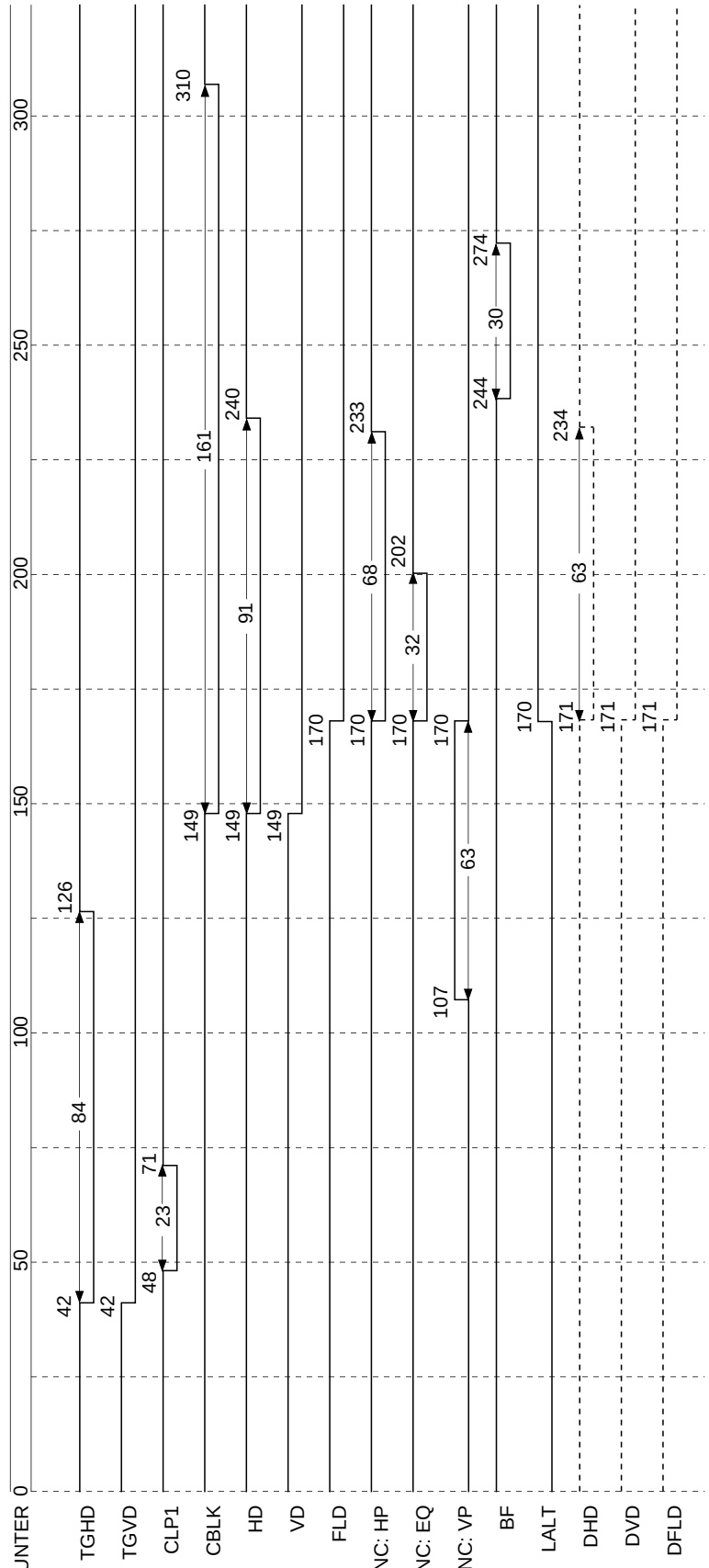
MCK: 858f_H (13.5MHz/74.07ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(2) 360H PAL Horizontal Timing Chart

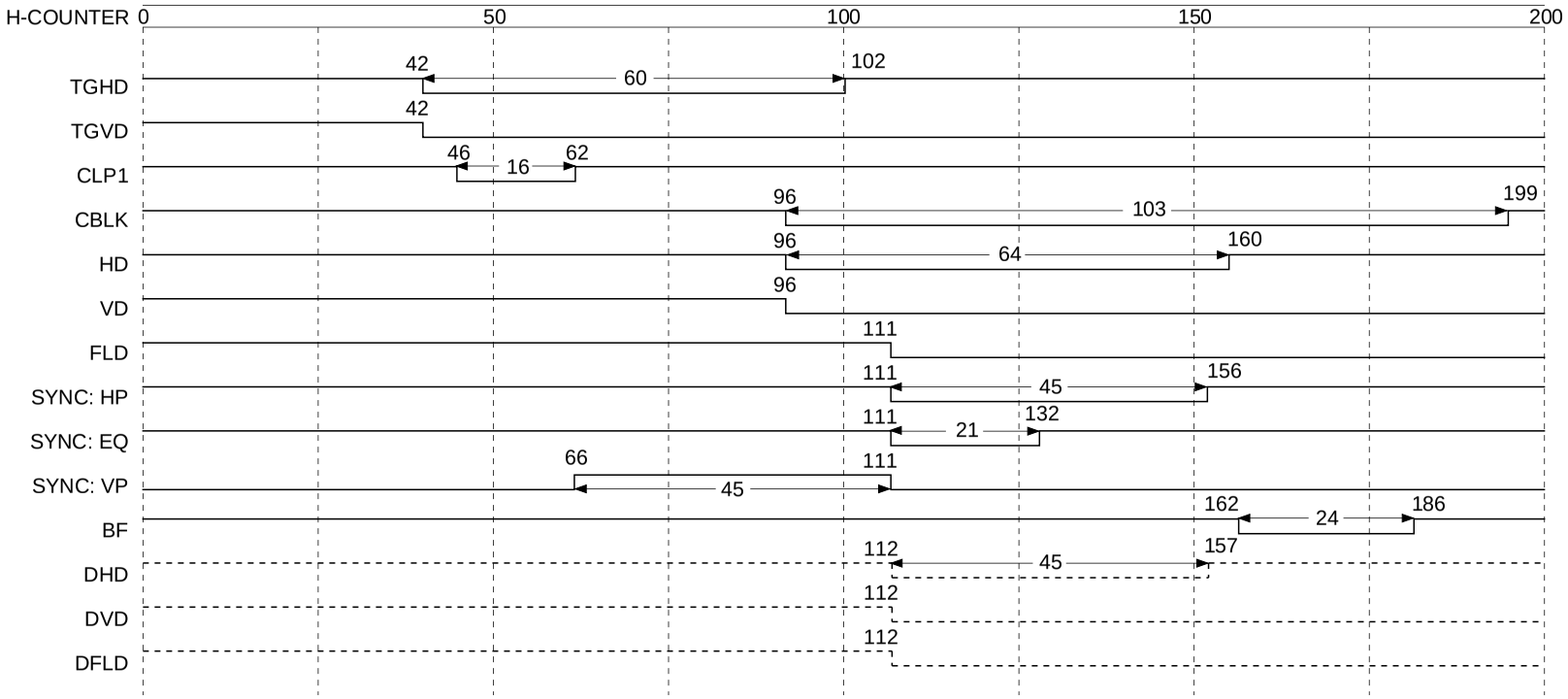
MCK: 864fH (13.5MHz/74.07ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(3) 510H NTSC Horizontal Timing Chart

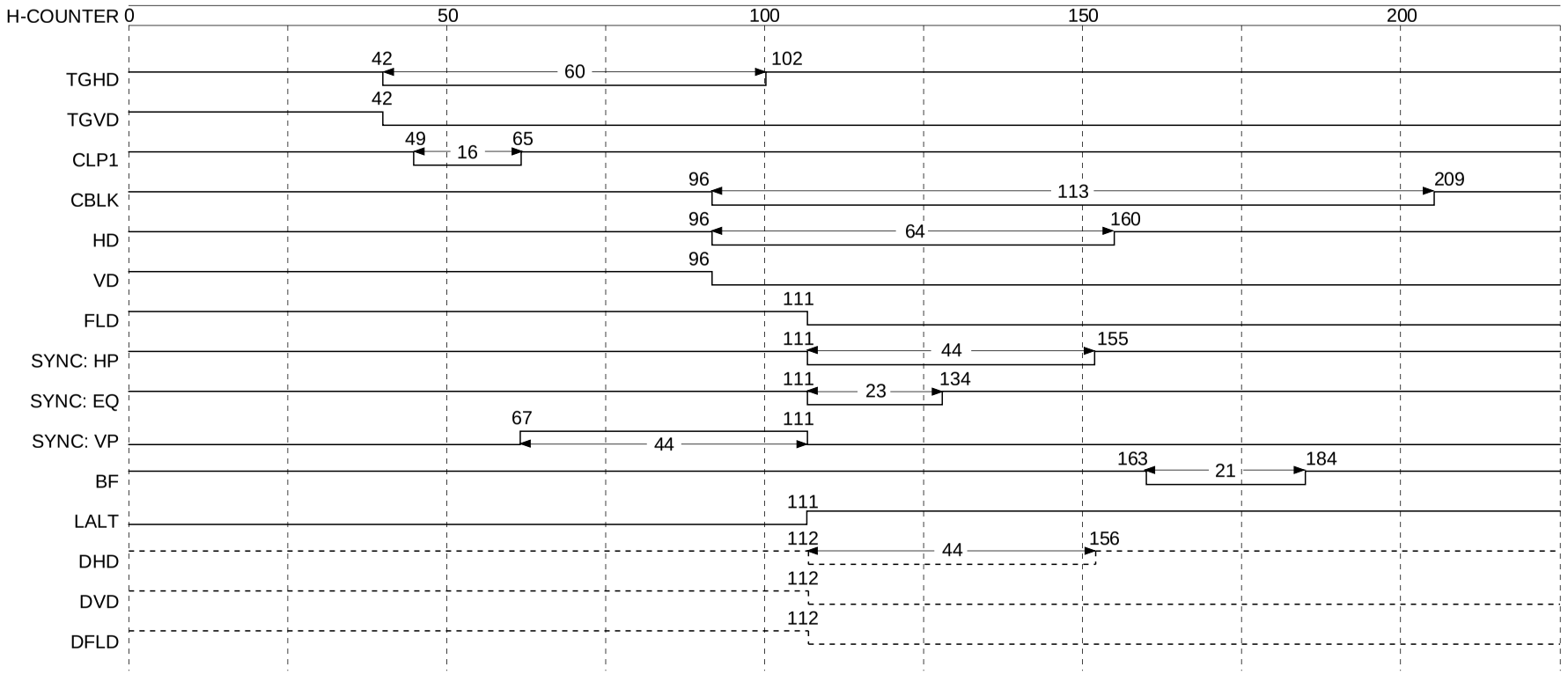
MCK: 606f_H (9.53496MHz/104.88ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(4) 510H PAL Horizontal Timing Chart

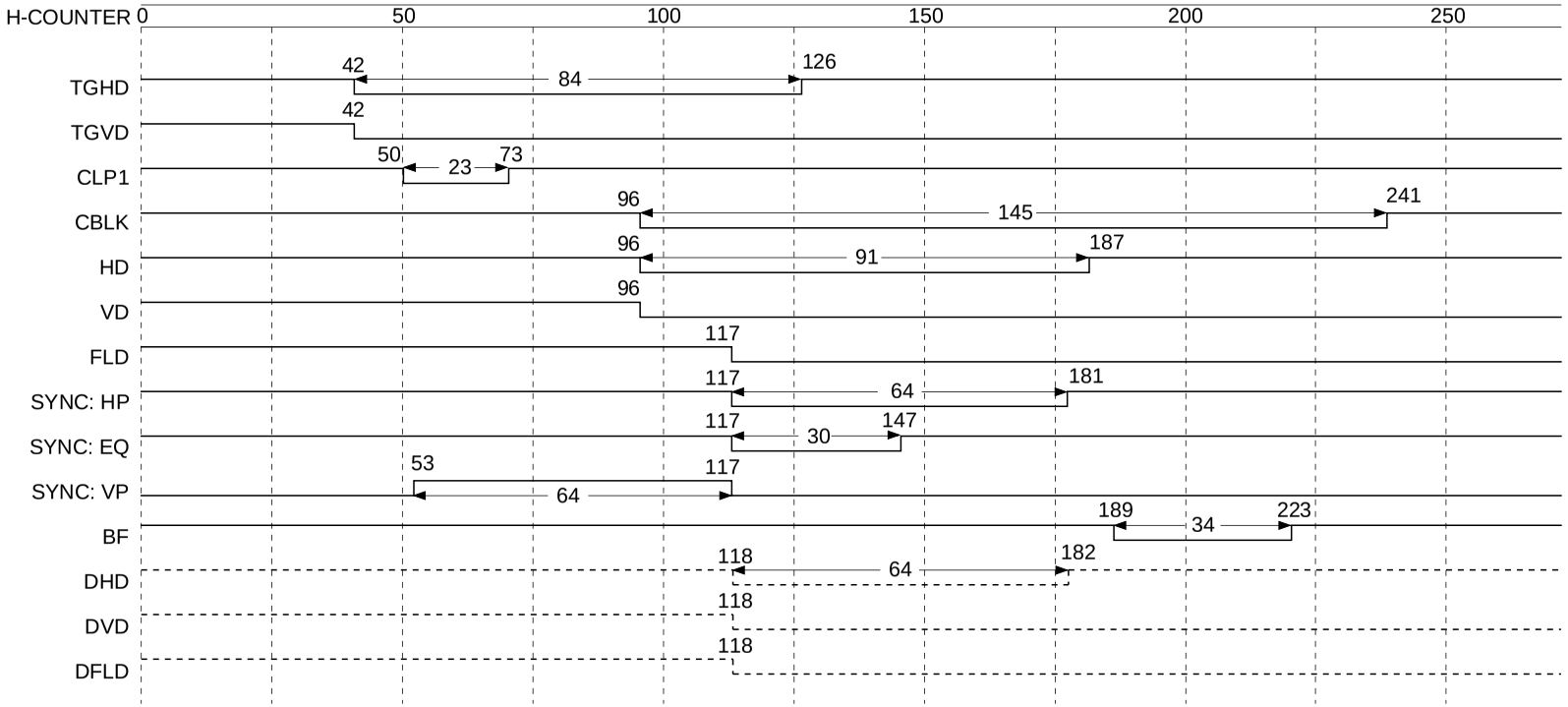
MCK: 606f_H (9.46875MHz/105.61ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(5) 720H NTSC Horizontal Timing Chart

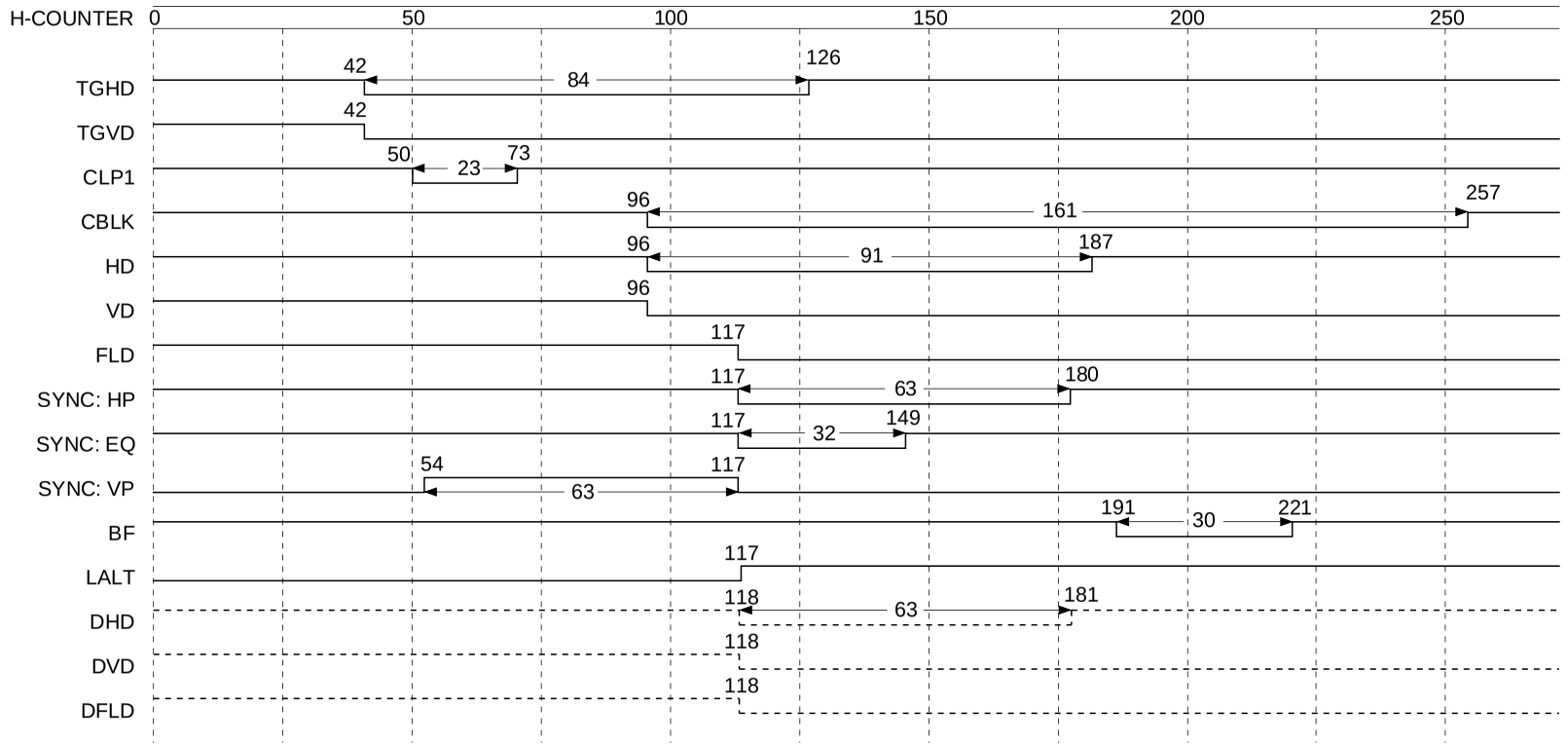
MCK: 858f_H (13.5MHz/74.07ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(6) 720H PAL Horizontal Timing Chart

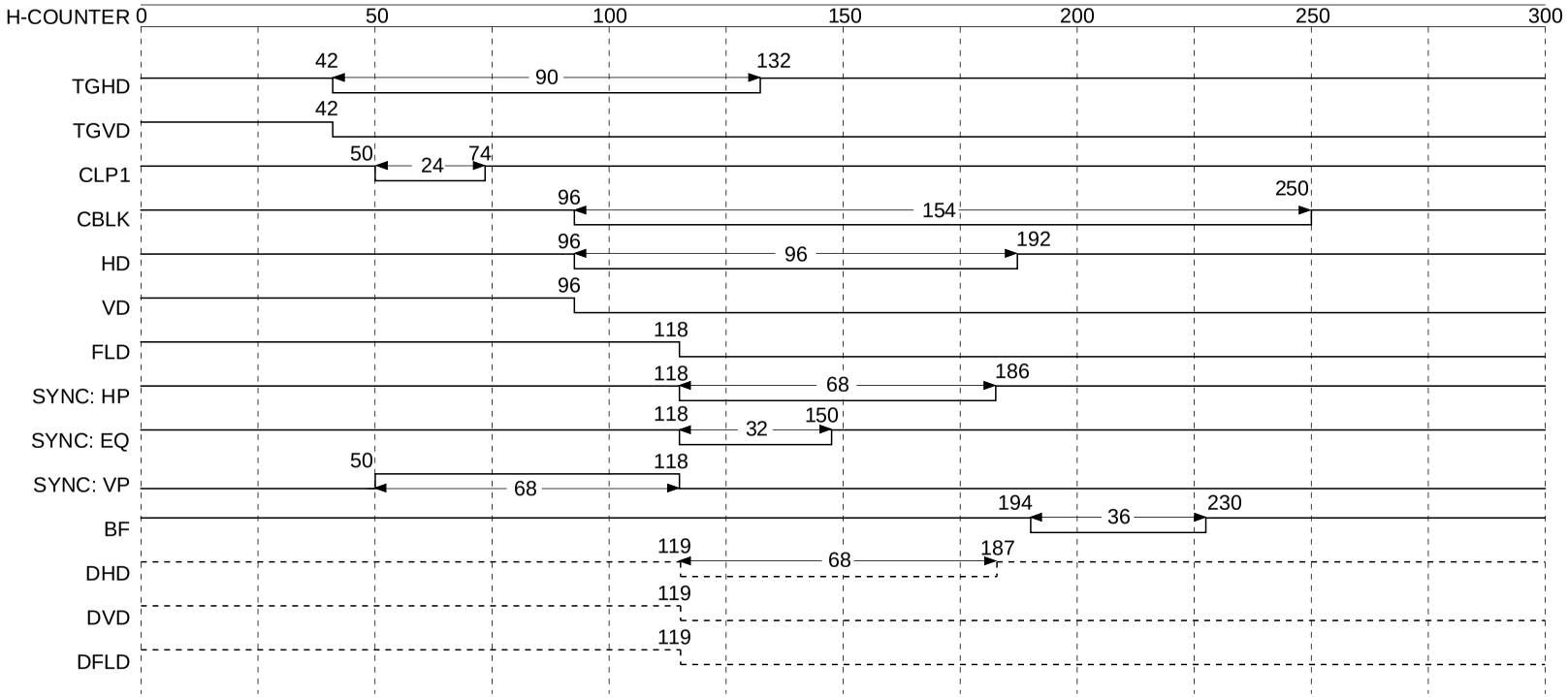
MCK: 864f_H (13.5MHz/74.07ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(7) 760H NTSC Horizontal Timing Chart

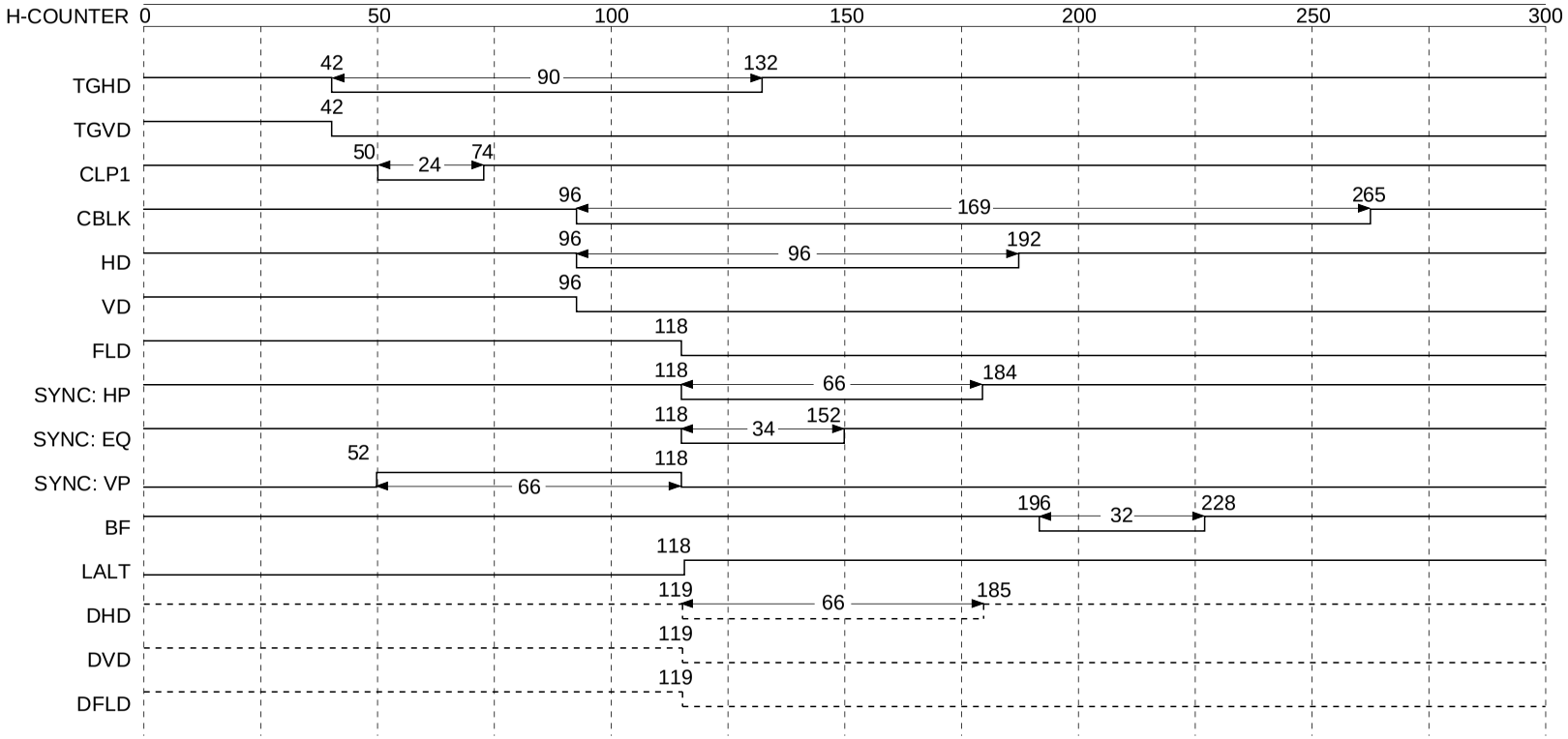
MCK: 910f_H (14.31818MHz/69.84ns)



Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

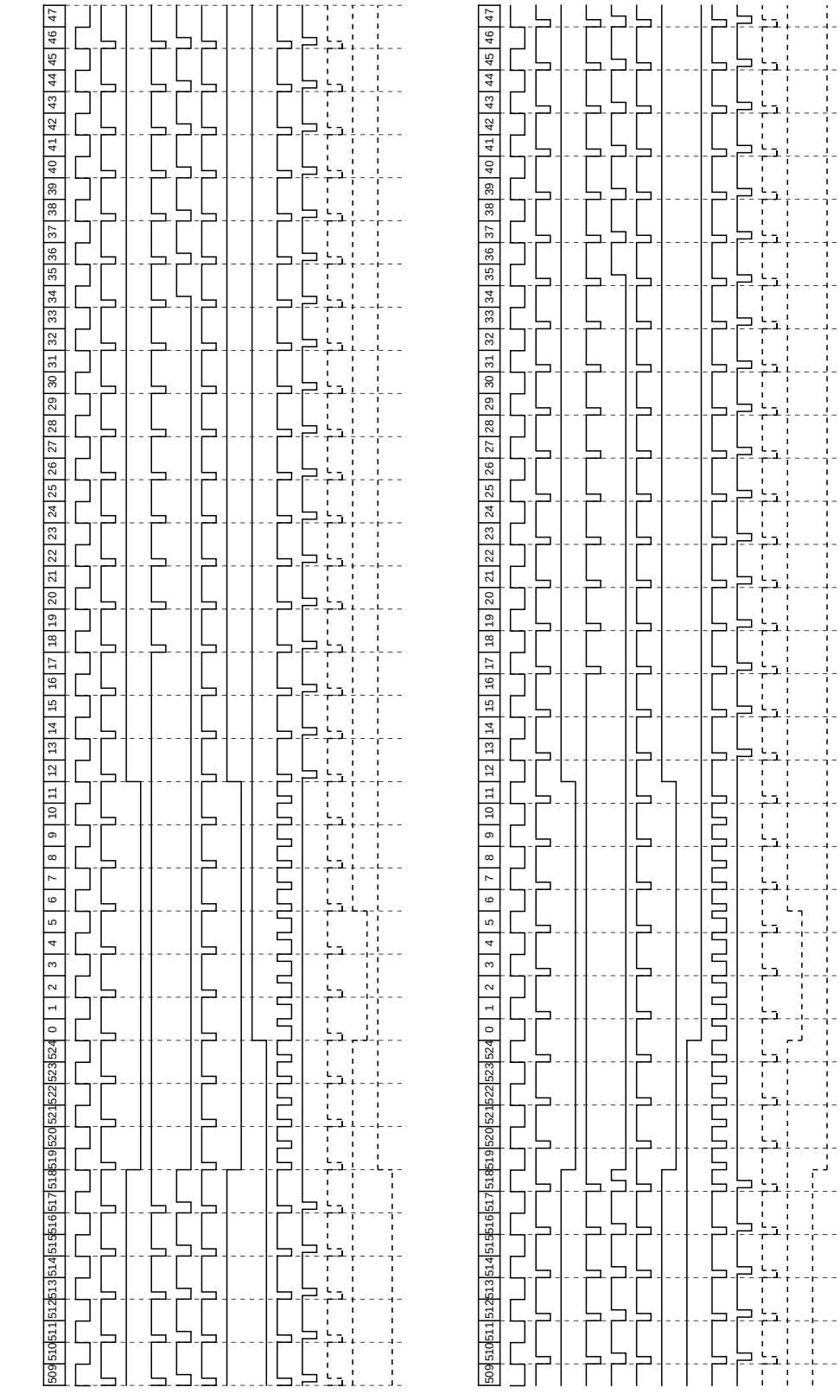
(8) 760H PAL Horizontal Timing Chart

MCK: 908f_H (14.1875MHz/70.48ns)



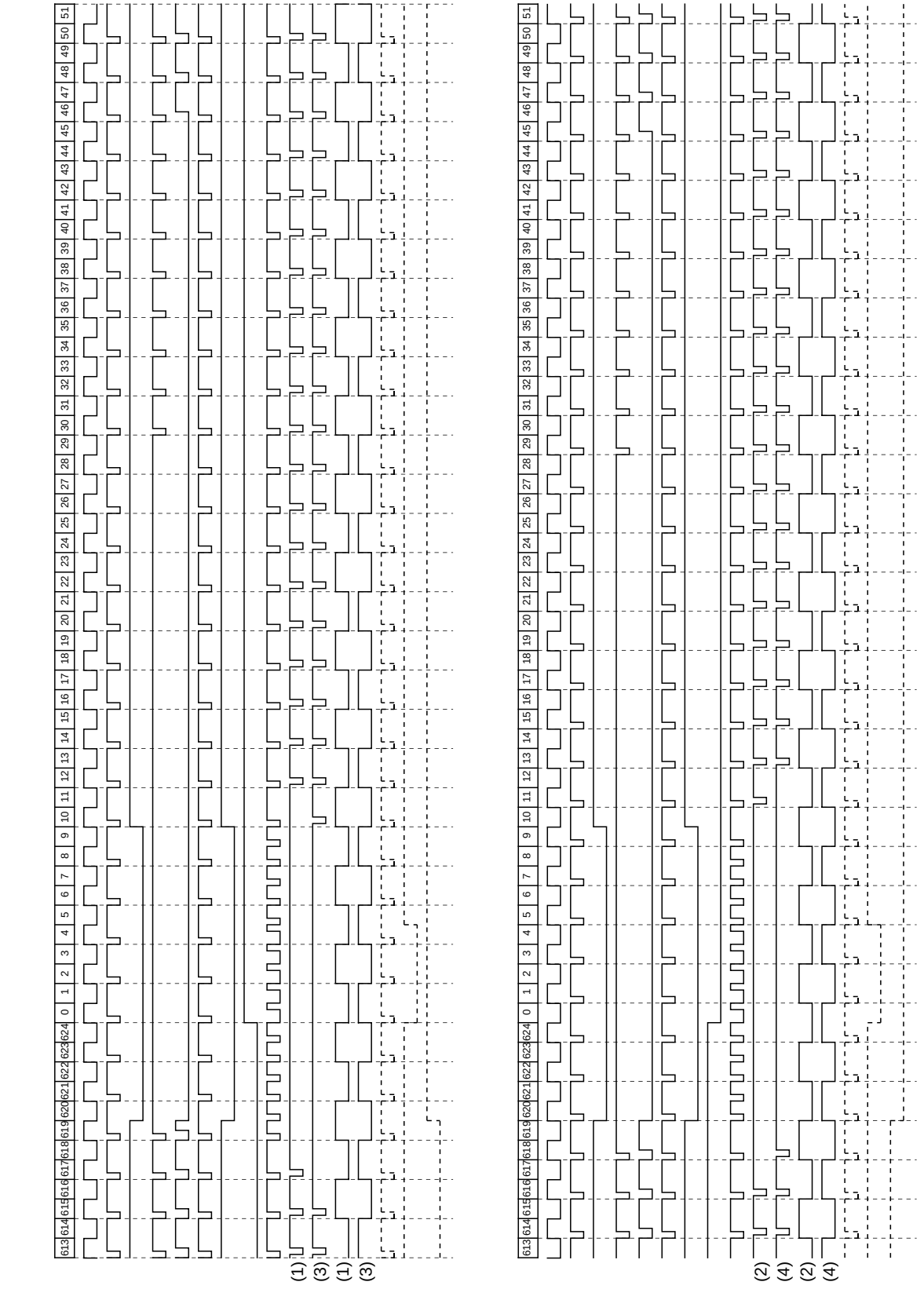
Note) The change of the signals of "DHD", "DVD", and "DFLD" becomes after approximately 3.5DCK from the above-mentioned timing.

(9) NTSC Vertical Timing Chart



Note) "HC" is an internal signal.

(10) PAL Vertical Timing Chart



Note) "HC" is an internal signal.

Microcomputer Communication

(1) The CXD2163BR's microcomputer interface circuit is designed as a serial interface with a general-purpose single-chip microcomputer.

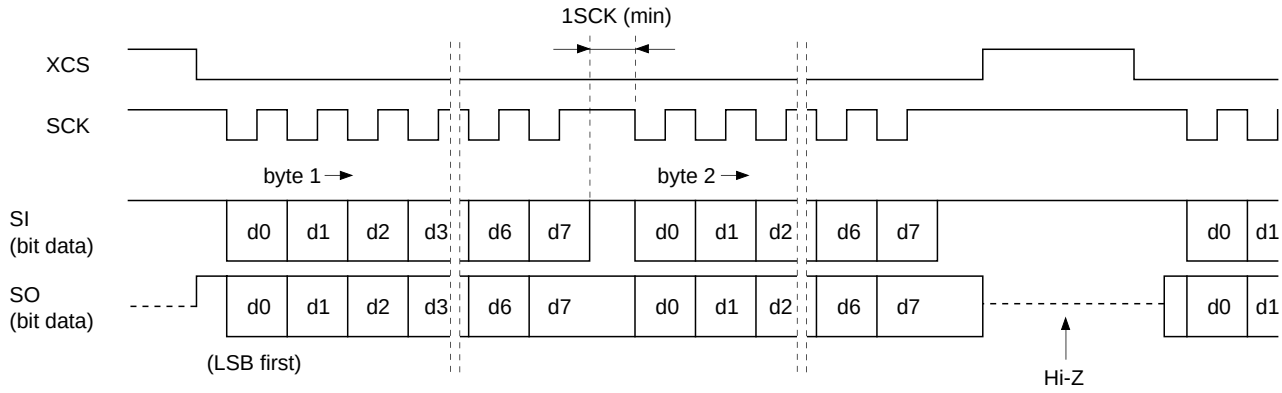
(2) The communication method is the full duplex sync method, and serial clock sync communication is performed in both directions between the CXD2163BR and microcomputer. The recommended communication speed is approximately 500K to 1Mbps.

(3) Connection between the CXD2163BR and microcomputer are following four lines.
Viewed from the CXD2163BR:
- XCS = CXD2163BR chip select input
- SCK = Clock input for serial transfer
- SI = CXD2163BR serial setting input (image parameters, etc.)
- SO = CXD2163BR serial data output (AE/AWB integral value, etc.)

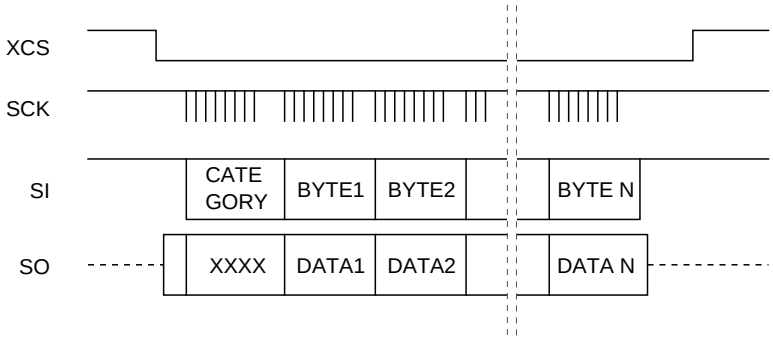
* When performing microcomputer communication, be sure to set the SIFSEL pin low.

(4) Communication timing
1. XCS is set low and the CXD2163BR's communication circuit is activated.
2. SI data is loaded in sync with the rise of SCK.
3. SO is output in sync with the fall of SCK.
4. Serial data is grouped in 8-bit units with the number of data set as desired.
   At least one SCK clock must be left open between 8-bit data units.
5. XCS is set high and communication ends.

* The communication data is LSB first.



(5) Communication format
The byte string transmitted from the microcomputer while XCS is low is treated as a single category.
Categories are classified by the number sent in the first byte.
Data output is synchronized with the input, and the data output contents are determined by the category.
(See the Communication Parameter Table for the byte data and data output contents. Note that the data output until the category is determined is "Don't care".)



RS232C Communication

(1) The CXD2163BR's RS232C interface circuit is designed for communication with the serial port of a personal computer. The CXD2163BR has a built-in I/O buffer (input 16 bytes, output 32 bytes).

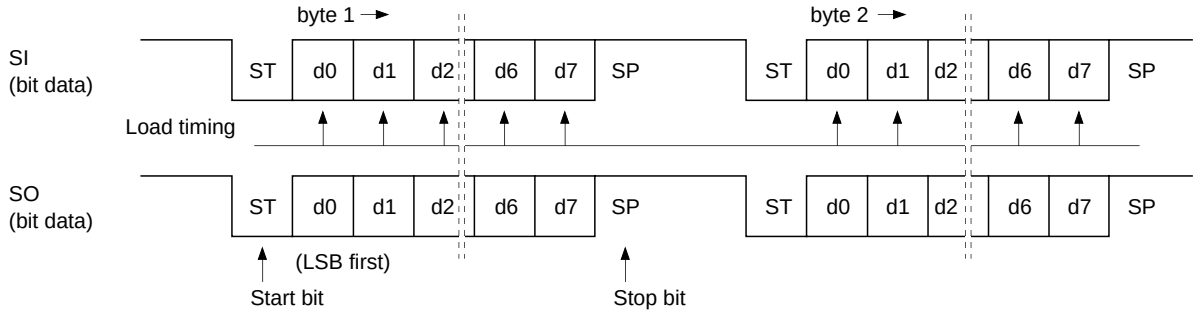
(2) The communication method is the full duplex start-stop sync method, and serial clock start-stop sync communication is performed in both directions between the CXD2163BR and personal computer.
The communication speed can be switched to 9600bps or 4800bps.
The communication settings are an 8-bit data length, no parity, one start bit, one stop bit and no flow control.

(3) Connection between CXD2163BR and personal computer are following two lines.
Viewed from the CXD2163BR:
- SI = CXD2163BR serial setting input (image parameters, etc.)
- SO = CXD2163BR serial data output (AE/AWB integral value, etc.)

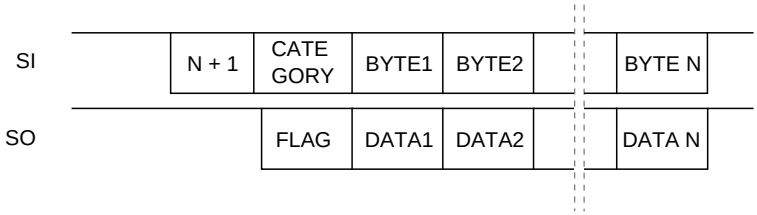
* When performing RS232C communication, be sure to set the SIFSEL and SCK pins high.
* The communication speed is 9600bps when XCS = high, and 4800bps when XCS = low.

(4) Communication timing
1. The CXD2163BR loads 8 bits of data at the timing determined by the communication speed after the fall of SI.
2. SO is output in sync with the SI data.
3. Serial data is grouped in 8-bit units with the number of data set as desired.

* The communication data is LSB first.



(5) Communication format
The CXD2163BR sends the number of bytes in the data string to be sent in the first byte in order to divide the data string (category). The data from the second byte onward has the same format as during microcomputer communication.
Also, the serial output is output in sync with the input like the microcomputer communication.
However, note that the CXD2163BR's internal status flag is output in the first of "Don't care" byte (the second input byte) during microcomputer communication. When d7 of this byte is 1, data is still remaining in the internal buffer and new communications are ignored.



Serial Communication Data

Classification of Serial Data

Category	I/O	Contents	
		Byte0	Byte1 to
CAT1: FIX	I	01h	Initially fixed parameters
	O	—	—
CAT2: FIELD	I	02h	Camera control parameters in field cycle
	O	—	—
CAT3: CLAMP	I	03h	Clamp control parameters
	O	—	OB integral data output
CAT4: DCREF	I	04h	DC setting (EVR-related) parameters
	O	—	—
CAT5: AE	I	05h	AE control parameters
	O	—	AE integral output
CAT6: AWB	I	06h	AWB control parameters
	O	—	AWB integral output
CAT7: FIXOPD	I	07h	Initially fixed parameters for OPD
	O	—	—
CAT8: MCRCON	I	08h	Control parameters for Microcontroller
	O	—	—
CAT9: SG	I	09h	SG control
	O	—	SG status output
CAT10: EXTCON	I	0Ah	External control parameters (for microcomputer)
	O	—	Y/C sampling data output

* "Block" and "Address" located at the upper right of the Serial Communication Data Table are as follows.

Block = This indicates the block which reflects that parameter.
(the destination block where parameter transmits)

Address = EEPROM write/read address
MSB represents most significant 8 bits and LSB represents least significant 8 bits.

Category 1: FIX [Initially fixed parameters]

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT1	LSB Category select code 01h: FIX MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	NTPAL	TV system mode 0: NTSC 1: PAL	SW	Common	01h MSB
	1	CCD1	LSB CCD mode 0h: 360H 1h: 510H 2h: 720H 3h: 760H	SW	Common	
	2	CCD2	MSB			
	3	YDOUT	Data selection for Y digital output 0: YAF out 1: Digital out	0	Y	
	4	UVDOUT	Data selection for C digital output 0: DIP SW 1: Digital out	0	Common	
	5	REC601	Format selection for digital output 0: linear 1: REC601	0	Common	
	6	DSYNC	Sync signal (HD pin) phase selection 0: for Analog 1: for Digital	0	SG	
	7	SG135	PLL reference selection 0: 4fsc ref. 1: 13.5MHz ref	0	SG	
2	0	ADSEL	A/D selection 0: Ext-A/D 1: Int-A/D	1	PRE	02h MSB
	1	ADINV	A/D clock phase selection 0: Forward 1: Reversed	0	PRE	
	2	ADDLY	10ns delay for A/D output 0: 0 delay 1: 10ns delay	0	PRE	
	3	DL1CK	1 CK delay for A/D output 0: 0 delay 1: 1CK delay	0	PRE	
	4	MMODE	SS-1M mode selection 0h: SS-1 mode 5h: SS-1M mode	0h	Common	
	5					
	6					
	7	NEGPOS	Negative/positive inversion 0: Positive 1: Negative	0	Y/C	
3	0	SETUP	LSB Setup level setting 0 IRE (0h) to 8.5 IRE (Fh)/ (4-bit step) MSB	Dh	Y	03h MSB
	1					
	2					
	3					
	4	WCLIP	LSB White clip level setting (Y-D/A max = 255dec) 0h: 142d 1h: 160d 2h: 178d 3h: 187d 4h: 196d 5h: 205d 6h: 214d 7h: 255d MSB	6h	Y	
	5					
	6					
	7	SUP601	Setup for digital output (REC601 mode) 0: setup off 1: setup on	0	Y	

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	SYNLV	LSB Sync signal amplitude adjustment (for fine adjustment) 2LSB × (0h) to 2LSB × (7h) Y-D/A 2LSB step	6h	Y	04h MSB
	1					
	2		MSB			
	3	SYNLVPM	Sync signal amplitude adjustment direction 0: Decrease 1: Increase	1	Y	
	4	YDLY	LSB Y signal delay adjustment (1 to 16 steps/1 (0h) to 16 (Fh) MCK step) 360H 510H 720H 760H NT 4h 2h 7h 7h PAL 0h 0h 3h 3h	SW	Y	
	5					
	6					
	7		MSB			
5	0	VHAPSL	LSB Aperture correction slice level setting Max (Fh) to Min (0h) = off	4h	Y	05h MSB
	1					
	2					
	3		MSB			
	4	VAPSL	LSB V-aperture slice level setting Max (7h) to Min (0h) = off	2h	Y	
	5					
	6		MSB			
	7	VAPLIM	V-aperture limiter switch 0: OFF 1: ON	0	Y	
6	0	HLAPSL	LSB High light aperture correction slice level adjustment	4h	Y	06h MSB
	1					
	2					
	3		MSB			
	4	HLAPPC	LSB High light aperture correction threshold level adjustment	3h	Y	
	5		MSB			
	6	HLAPDS	High light aperture correction detect point selection 0: det before γ 1: det after γ	0	Y	
	7	dummy				
7	0	HLAPPG	LSB High light aperture correction signal positive gain adjustment	3h	Y	07h MSB
	1		MSB			
	2	HLAPMG	LSB High light aperture correction signal negative gain adjustment	2h	Y	
	3		MSB			
	4	dummy				
	5					
	6					
	7					

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0 1 2 3 4 5 6 7	RMATY	LSB R signal primary color separation matrix coefficient R = Cr + <RMATY> × Yr + <RMATC> × Cb × 0.5 (7Fh) to × 0.0 (00h) to × –0.5 (80h) MSB (Data format = 2's)	32h	C	08h MSB
9	0 1 2 3 4 5 6 7	RMATC	LSB R signal primary color separation matrix coefficient R = Cr + <RMATY> × Yr + <RMATC> × Cb × 0.5 (7Fh) to × 0.0 (00h) to × –0.5 (80h) MSB (Data format = 2's)	F8h	C	09h MSB
10	0 1 2 3 4 5 6 7	BMATY	LSB B signal primary color separation matrix coefficient B = Cb + <BMATY> × Yb + <BMATC> × Cr × 0.5 (7Fh) to × 0.0 (00h) to × –0.5 (80h) (Data format = 2's) MSB	32h	C	0Ah MSB
11	0 1 2 3 4 5 6 7	BMATC	LSB B signal primary color separation matrix coefficient B = Cb + <BMATY> × Yb + <BMATC> × Cr × 0.5 (7Fh) to × 0.0 (00h) to × –0.5 (80h) (Data format = 2's) MSB	D3h	C	0Bh MSB

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	BSTLV	LSB Burst level adjustment Burst level = <BSTLVL> × 2 (LSB) NTSC: 0Ch PAL: 09h	SW	C	0Ch
	1					
	2					
	3					
	4		MSB			MSB
	5	CPHSEL	LSB Color identification signal reference phase selection 0h: 0 delay 1h: 1 delay 2h: 2 delay 3h: 3 delay	#2 1h	SG	
	6		MSB (1 delay = 1 MCK)			
	7	LIDSEL	Line identification signal reference phase selection 1: ID siginverse	0	C	
13	0	MODSW	Chroma encoder modulation switch ON/OFF 1: modulation (Color difference output)	0	C	0Dh MSB
	1	(Low)	"0" fixed	0		
	2	ENCSW	Encode clock switch 1: ENC CK OFF	0	C	
	3	SYNCSW	Sync ON/OFF for Y D/A converter 1: Sync OFF	0	Y	
	4	(Low)	"0" fixed	0		
	5	SYNDISP	SYNC pin output signal selection 0: Sync 1: Disp (OPD wind)	0	SG	
	6	VDBUSY	VD pin output signal selection 0: VD 1: SCSBUSY	0	SG	
	7	LALPIN	LRI pin input/output selection 0: LALT out 1: LALT in	0	SG	
14	0	SYNPIN	LSB Sync pin output signal selection 0h: Sync 1h: CBLK 2h: BF 3h: SCG	0h	SG	0Eh MSB
	1		MSB			
	2	FLDPIN	LSB FLD pin output signal selection 0h: FLD 1h: CBLK 2h: BF 3h: SCG	0h	SG	
	3		MSB			
	4	VDPIN	LSB VD pin output signal selection 0h: VD 1h: CBLK 2h: BF 3h: SCG	0h	SG	
	5		MSB			
	6	HDPIN	LSB HD pin output signal selection 0h: HD 1h: CBLK 2h: BF 3h: SCG	0h	SG	
	7		MSB			
15	0	BSTSW	Burst ON/OFF 0: ON 1: OFF	0	C	5Fh MSB
	1	YLPFSW	Y-LPF ON/OFF 0: ON 1: OFF	0	Y	
	2	VALIMVTH	V-aperture limiter Aperture threshould level	1h	Y	
	3					
	4	VALIMHTH	V-aperture limiter High light threshould level	2h	Y	
	5					
	6	VLMVTHSW	V-aperture limiter Aperture detection 0: ON 1: OFF	0	Y	
	7	VLMHTHSW	V-aperture limiter High light detection 0: ON 1: OFF	0	Y	

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

#2: Initial value = 0h only NTSC 360H-CCD mode.

Category 2: FIELD [Camera control parameters in field cycle]

		Serial input				
Byte	bit	Name	Description	**#1**	Block	Address
0	0	CAT2	LSB Category selection code 02h: FIELD MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	YGAIN	LSB Luminance signal gain adjustment × 2 (FFh) to × 0 (00h) MSB	86h	Y	0Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
2	0	HAPGL	LSB H-aperture correction (low band) gain adjustment MSB 0h: × 0 1h: × 0.5 2h: × 1 3h: × 2	2h	Y	10h MSB
	1					
	2	HAPGH	LSB H-aperture correction (high band) gain adjustment MSB 0h: × 0 1h: × 1 2h: × 2 3h: × 4	2h	Y	
	3					
	4	VAPG	LSB V-aperture correction gain control × 1 (Fh) to × 0 (0h) MSB	Ah	Y	
	5					
	6					
	7					
3	0	VHAPG	LSB V-aperture correction gain adjustment × 2 (Fh) to × 0 (0h) MSB	6h	Y	11h MSB
	1					
	2					
	3					
	4	HLAPG	LSB High light aperture correction gain adjustment MSB	2h	Y	
	5					
	6	dummy				
	7					

#1: Initial setting value with Power-on

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	CSVLV	LSB Chroma suppress (V-aperture correction) level selection MSB	0h	C	12h MSB
	1					
	2	CSVTH	LSB Chroma suppress (V-aperture correction) threshold level selection MSB	1h	Y	
	3					
	4	CSHLV	LSB Chroma suppress (luminance) level selection MSB	0h	C	
	5					
	6	CSHTH	LSB Chroma suppress (luminance) threshold level selection MSB	2h	Y	
	7					
5	0	YGAM	LSB Y gamma level adjustment High γ (Fh) to Low γ (0h)	4h	Y	13h MSB
	1					
	2		MSB			
	3	YSGAMLV	Y gamma: low level signal compression level selection	0	Y	
	4	YKNE	LSB Y knee level adjustment MSB	0h	Y	
	5					
	6					
	7	YSGAMSW	Y gamma: low level signal compression function switch ON/OFF 1: compression ON	0	Y	
6	0	CGAM	LSB Chroma gamma level adjustment High γ (7h) to Low γ (0h)	4h	C	14h MSB
	1					
	2		MSB			
	3	CKNCLOP0	Chroma knee clip level 0 selection	1	C	
	4	CKNE	LSB Chroma knee level adjustment MSB	7h	C	
	5					
	6					
	7	CKNCLIP1	Chroma knee clip level 1 selection	1	C	
7	0	RBQUAD	LSB Quadrant selection for independent adjustment of linear matrix 0: OFF 1st quadrant (bit 0) 2nd quadrant (bit 1) 1: ON 3rd quadrant (bit 2) 4th quadrant (bit 3) MSB	Fh	C	
	1					
	2					
	3					
	4	CONGAIN	Gain coefficient selection for linear matrix adjustment 0: OFF 1: gain set	1	C	
	5	CONHUE	Hue coefficient selection for linear matrix adjustment 0: OFF 1: hue set	1	C	
	6	dummy				
	7					

#1: Initial setting value with Power-on

		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	RYGAIN	LSB Linear matrix coefficient (R-Y GAIN) × –1 (80h) to × 0 (00h) to × 1 (7Fh) R-Y = <RYGAIN> × {R-G + <BYHUE> × B-G} MSB (Data format = 2's)	20h	C	4Fh 51h 53h 55h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	BYGAIN	LSB Linear matrix coefficient (B-Y GAIN) × –1 (80h) to × 0 (00h) to × 1 (7Fh) B-Y = <BYGAIN> × {B-G + <RYHUE> × R-G} (Data format = 2's) MSB	11h	C	50h 52h 54h 56h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	RYHUE	LSB Linear matrix coefficient (R-Y HUE) × –1 (80h) to × 0 (00h) to × 1 (7Fh) B-Y = <BYGAIN> × {B-G + <RYHUE> × R-G} MSB (Data format = 2's)	D0h	C	57h 59h 5Bh 5Dh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	BYHUE	LSB Linear matrix coefficient (B-Y HUE) × –1 (80h) to × 0 (00h) to × 1 (7Fh) R-Y = <RYGAIN> × {R-G + <BYHUE> × B-G} MSB (Data format = 2's)	F8h	C	58h 5Ah 5Ch 5Eh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 3: CLAMP [Clamp control parameters]

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0	CAT3	LSB Category selection code 03h: CLAMP MSB				0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
1	0	BLACK1L	LSB Black level adjustment for digital clamp (S1) LSB 8 bits (Integral part = 7 bits + decimal part = 2 bits) MSB (Data format = BIN)	00h	Y/C	15h MSB	0	OB1L	LSB OB integral level output for digital clamp (S1) LSB 8 bits (Integral part = 7 bits + decimal part = 5 bits) MSB (Data format = BIN)	PRE
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
2	0	BLACK2L	LSB Black level adjustment for digital clamp (S2) LSB 8 bits (Integral part = 7 bits + decimal part = 2 bits) MSB (Data format = BIN)	00h	Y/C	16h MSB	0	OB1M	LSB OB integral level output for digital clamp (S1) MSB 4 bits (Integral part = 7 bits + decimal part = 5 bits) MSB (Data format = BIN)	PRE
	1						1			
	2						2			
	3						3			
	4						4	OB2M	LSB OB integral level output for digital clamp (S2) MSB 4 bits (Integral part = 7 bits + decimal part = 5 bits) MSB (Data format = BIN)	PRE
	5						5			
	6						6			
	7						7			
3	0	BLACK1M	BLACK1 MSB 1 bit	0	Y/C	17h MSB	0	OB2L	LSB OB integral level output for digital clamp (S2) LSB 8 bits (Integral part = 7 bits + decimal part = 5 bits) MSB (Data format = BIN)	PRE
	1	BLACK2M	BLACK2 MSB 1 bit	0	Y/C		1			
	2	dummy					2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
4	0	SHOFST	LSB Offset voltage adjustment for S/H IC (FFh) to (00h) MSB (Data format = BIN)	3Dh	EVR ch7	18h MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
5	0	EVRUSR	LSB EVR voltage adjustment for USR setting (FFh) to (00h) MSB (Data format = BIN)	89h	EVR ch8	19h MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
6	0	CLIPS1BL	LSB Complementary color pixel clip level S1B LSB 8 bits MSB (Data format = BIN)	FFh	C	60h MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
7	0	CLIPS1RL	LSB Complementary color pixel clip level S1R LSB 8 bits MSB (Data format = BIN)	FFh	C	61h MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
8	0	CLIPS2BL	LSB Complementary color pixel clip level S2B LSB 8 bits MSB (Data format = BIN)	FFh	C	62h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	CLIPS2RL	LSB Complementary color pixel clip level S2R LSB 8 bits MSB (Data format = BIN)	FFh	C	63h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	CLIPS1BM	LSB Complementary color pixel clip level MSB S1B MSB 2 bits (Data format = BIN)	3h	C	64h MSB
	1					
	2	CLIPS1RM	LSB Complementary color pixel clip level MSB S1R MSB 2 bits (Data format = BIN)	3h		
	3					
	4	CLIPS2BM	LSB Complementary color pixel clip level MSB S2B MSB 2 bits (Data format = BIN)	3h		
	5					
	6	CLIPS2RM	LSB Complementary color pixel clip level MSB S2R MSB 2 bits (Data format = BIN)	3h		
	7					

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
11	0	HLEDDL1	High light edge color compensation (DL1 H-edge detection) 1: ON	0	C	65h MSB
	1	HLEDDL2	High light edge color compensation (DL2 H-edge detection) 1: ON	0	C	
	2	HLEDV	High light edge color compensation (V-edge detection) 1: ON	0	C	
	3	(Low)	"0": fixed	0		
	4	HLEPASE	High light edge color compensation (Detection phase setting)	1h	C	
	5					
	6	dummy				
	7					
12	0	HLEDLVL	High light edge color compensation (Detection level LSB)	00h	PRE	66h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	HLEDLVM	High light edge color compensation (Detection level MSB)	1h	PRE	67h MSB
	1					
	2	dummy				
	3					
	4	HLEWID	High light edge color compensation (Detection signal width)	5h	C	
	5					
	6					
	7	(Low)	"0" fixed	0		

#1: Initial setting value with Power-on

Category 4: DCREF [DC setting (EVR-related) parameters]

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
0	0 1 2 3 4 5 6 7	CAT4	LSB Category selection code 04h: DCREF MSB			
1	0 1 2 3 4 5 6 7	DAVRFY	LSB Reference voltage adjustment for Y-D/A conveter MSB	70h	EVR ch3	1Ch MSB
2	0 1 2 3 4 5 6 7	DAVRFC	LSB Reference voltage adjustment for C-D/A converter MSB	66h	EVR ch4	1Dh MSB
3	0 1 2 3 4 5 6 7	VSUB	LSB VSUB voltage adjustment for CCD MSB	80h	EVR ch5	1Eh MSB

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
4	0	VRGL	LSB VRGL voltage adjustment for CCD MSB	80h	EVR ch6	1Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
5	0	EVR12CH	EVR 8ch/12ch selection 0: 8ch 1: 12ch	0	SCS	60h LSB
	1	dummy				
	2					
	3					
	4					
	5					
	6					
	7					
6	0	EVRUSR9	LSB EVR user voltage setting (EVR channel 9 output) (00h to FFh) MSB	00h	EVR ch9	61h LSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
7	0	EVRUSR10	LSB EVR user voltage setting (EVR channel 10 output) (00h to FFh) MSB	00h	EVR ch10	62h LSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
8	0	EVRUSR11	LSB EVR user voltage setting (EVR channel 11 output) (00h to FFh)	00h	EVR ch11	63h LSB
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
9	0	EVRUSR12	LSB EVR user voltage setting (EVR channel 12 output) (00h to FFh)	00h	EVR ch12	64h LSB
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Category 5: AE [AE control parameters/AE integral output]

Serial input							Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0	CAT5	LSB Category selection code 05h: AE MSB				0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
1	0	AGCCNT	LSB Voltage control data for AGC-amp GAIN MSB	1Eh	EVR ch2	20h MSB	0	INTEG0L	LSB WIND0 Y integral data output LSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
2	0	IRISV	LSB Voltage control data for mechanical IRIS MSB	FFh	EVR ch1	21h MSB	0	INTEG0M	LSB WIND0 Y integral data output MSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
3	0	TGSHTM	Shutter speed data (MSB)	0	TG	—	0	INTEG1L	LSB WIND1 Y integral data output LSB 8 bits MSB (Data format = BIN)	OPD
	1	TGSHTHL	Shutter speed 0: high 1: low	0	TG		1			
	2	TGSHTON	Shutter SW 0: OFF 1: ON	0	TG		2			
	3	(Low)	"0" fixed	0	TG		3			
	4	TGNTPAL	TV mode for TG	SW	TG		4			
	5	TGCCD1	CCD mode for TG1	SW	TG		5			
	6	TGCCD2	CCD mode for TG2	SW	TG		6			
	7	(High)	"1" fixed	1	TG		7			

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
4	0	TGSHTL	LSB Shutter speed Data (LSB) MSB	00h		—	0	INTEG1M	LSB WIND1 Y integral data output MSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
5	0	HREF1HL	HIST reference (channel 1) control	0	OPD	—	0	INTEG2L	LSB WIND2 Y integral data output LSB 8 bits MSB (Data format = BIN)	OPD
	1	HREF2HL	HIST reference (channel 2) control	0	OPD	—	1			
	2	dummy	0: REF ≤ YAE 1: REF ≥ YAE			—	2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
6	0	HREF1	LSB HIST reference (channel 1) setting MSB	00h	OPD	—	0	INTEG2M	LSB WIND2 Y integral data output MSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
7	0	HREF2	LSB HIST reference (channel 2) setting MSB	00h	OPD	—	0	INTEG3L	LSB WIND3 Y integral data output LSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
8	0	dummy					0	INTG3M	LSB WIND3 Y integral data output MSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
9	0	dummy					0	INTG4L	LSB WIND4 Y integral data output LSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
10	0	dummy					0	INTG4M	LSB WIND4 Y integral data output MSB 8 bits MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
11	0	dummy					0	INTGH1L	LSB HIST1 integral data output LSB 8 bits (AGCCNT: AECO = 001 mode) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
12	0	dummy					0	INTGH1M	LSB HIST1 integral data output MSB 8 bits (IRISV: AECO = 001 mode) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
13	0	dummy					0	INTGH2L	LSB HIST2 integral data output LSB 8 bits (TGSHT1: AECO = 001 mode) (AEYMIN: AEMAXMIN = 1) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
14	0	dummy					0	INTGH2M	LSB HIST2 integral data output MSB 8 bits (TGSHT2: AECO = 001 mode) (AEYMAX: AEMAXMIN = 1) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
15	0	dummy					0	HSTCNT1L	LSB HIST1 count data output LSB 8 bits (AESC1: AECO = 001 mode) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
16	0	dummy					0	HSTCNT1M	LSB HIST1 count data output MSB 8 bits (AESC2: AECO = 001 mode)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7		MSB (Data format = BIN)	
17	0	dummy					0	HSTCNT2L	LSB HIST2 count data output LSB 8 bits	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7		MSB (Data format = BIN)	
18	0	dummy					0	HSTCNT2M	LSB HIST2 count data output MSB 8 bits	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7		MSB (Data format = BIN)	

#1: Initial setting value with Power-on

Category 6: AWB [AWB control parameters/AWB integral output]

Serial input							Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0	CAT6	LSB Category selection code 06h: AWB MSB				0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
1	0	WBR	LSB WB-amp gain adjustment (RED channel) MSB	3Ah	C	22h MSB	0	AWBCNTL	LSB WB integral counter data output LSB 8 bits (AJSTAD: AWBCO = 011) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
2	0	WBG	LSB WB-amp gain adjustment (GREEN channel) MSB	26h	C	23h MSB	0	AWBCNTM	LSB WB integral counter data output MSB 8 bits (AJSTAD: AWBCO = 011) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
3	0	WBB	LSB WB-amp gain adjustment (BLUE channel) MSB	48h	C	24h MSB	0	INTGRL	LSB R integral data output (R-G intg or R intg) LSB 8 bits (AJSTR: AWBCO = 011) (Data format = 2's or BIN) MSB	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
4	0	WBYREFH	LSB Y threshold level setting for WB intg. (Top reference) MSB	D0h	OPD		0	INTGR	LSB R integral data output (R-G intg or R intg) mid 8 bits (AJSTR: AWBCO = 011) (Data format = 2's or BIN) MSB	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
5	0	WBYREFL	LSB Y threshold level setting for WB intg. (Bottom reference) MSB	04h	OPD		0	INTGRM	LSB R integral data output (R-G intg or R intg) MSB 8 bits (Data format = 2's or BIN) MSB	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
6	0	dummy					0	INTGGL	LSB G integral data output (G intg) LSB 8 bits (AJSTG: AWBCO = 011) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
7	0	dummy					0	INTGG	LSB G integral data output (G intg) mid 8 bits (AJSTG: AWBCO = 011) MSB (Data format = BIN)	OPD
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
8	0	dummy					0	INTGGM	LSB	OPD
	1						1			
	2						2			
	3						3		G integral data output (G intg) MSB 8 bits	
	4						4			
	5						5			
	6						6			
	7						7		MSB (Data format = BIN)	
9	0	dummy					0	INTGBL	LSB	OPD
	1						1			
	2						2			
	3						3		B integral data output (B-G intg or B intg) LSB 8 bits (AJSTB: AWBCO = 011)	
	4						4			
	5						5			
	6						6			
	7						7		(Data format = 2's or BIN) MSB	
10	0	dummy					0	INTGB	LSB	OPD
	1						1			
	2						2			
	3						3		B integral data output (B-G intg or B intg) mid 8 bits (AJSTB: AWBCO = 011)	
	4						4			
	5						5			
	6						6			
	7						7		(Data format = 2's or BIN) MSB	
11	0	dummy					0	INTGBM	LSB	OPD
	1						1			
	2						2			
	3						3		B integral data output (B-G intg or B intg) MSB 8 bits	
	4						4			
	5						5			
	6						6			
	7						7		(Data format = 2's or BIN) MSB	

#1: Initial setting value with Power-on

Category 7: FIXOPD [Initially fixed parameters for OPD]

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
0	0	CAT7	LSB Category selection code 07h: FIXOPD MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	AWBWSEL	AWB detection window selection 0: all wind 1: without wind0	0	OPD	25h MSB
	1	AWBGAM	AWB integral data selection 0: before γ 1: after γ	0	C	
	2	AWBBFSEL	AWB control selection 0: Feedback 1: Feedforward	0	OPD	
	3	AWBDPSEL	AWB integral mode selection 0: R-G/B-G 1: RGB	0	OPD	
	4	AEMAXMIN	AE output selection 0: HIST2 1: MAXMIN	0	OPD	
	5	AWMSPOT	AWB detection window selection 2 0: AWBWSEL select 1: AEW4	0	OPD	
	6	dummy				
	7					
2	0	CNTOFST	LSB Horizontal count start offset of AE/AWB detection window (COUNTER OFFSET) <CNTOFST> × 4MCK 360H 510H 720H 760H NT 14h 15h 1Ch 1Bh PAL 16h 16h 1Eh 1Dh MSB	SW	OPD	26h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3	0	CNTWID	LSB Horizontal unit width data of AE/AWB detection window (COUNTER WIDTH) <CNTWID> × 4MCK 360H 510H 720H 760H NT 05h 08h 0Bh 0Ch PAL 05h 08h 0Bh 0Ch MSB	SW	OPD	27h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

Serial input						
Byte	bit	Name	Description	#1	Block	Address
4	0	W4STAH	LSB Horizontal start data of WIND4 (WIND4 START H) Start position = W4STAH × CNTWID × 4MCK MSB	5h	OPD	28h
	1					
	2					
	3					
	4	W4WIDH	LSB Horizontal width data of WIND4 (WIND4 WIDTH H) Horizontal width = W4WIDH × CNTWID × 4MCK MSB	5h	OPD	MSB
	5					
	6					
	7					
5	0	W4STAV	LSB Vertical start data of WIND4 (WIND4 START V) Start position = W4STAV × 15 line (NTSC), 18 line (PAL) MSB	4h	OPD	29h
	1					
	2					
	3					
	4	W4WIDV	LSB Vertical width data of WIND4 (WIND4 WIDTH V) Start width = W4WIDV × 15 line (NTSC), 18 line (PAL) MSB	7h	OPD	MSB
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 8: MCRCON [Control parameters for microcontroller]

Serial input						
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT8	LSB Category selection code 08h: MCRCON			
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
1	0	AWBCO	LSB AWB co.process mode selection 000: copro non act 001: AWB monitor 010: AWB average 011: adjust out	0h	MCR	
	1					
	2		MSB			
	3	MCRAWB	Microcontroller AWB 0: ON 1: OFF	0	MCR	
	4	AECO	LSB AE co.process mode selection 000: copro non act 001: AE monitor 010: AE average 011: adjust AGC MIN	0h	MCR	
	5					
	6		MSB			
	7	MCRAE	Microcontroller AE 0: ON 1: OFF	0	MCR	
2	0	MCREXT	0: Microcontroller 1: External microcomputer	0	MCR	
	1	MCRSPRS	Microcontroller FIELD control switch 0: ON 1: OFF	0	MCR	
	2	MCRSG	Microcontroller SG control switch 0: ON 1: OFF	0	MCR	
	3	MCRDIP	Microcontroller DIP switch scan 0: ON 1: OFF	0	MCR	
	4	MCRCLP	Microcontroller CLAMP control switch 0: ON 1: OFF	0	MCR	
	5	(Low)	"0" fixed	0	MCR	
	6	MCRGAM	Microcontroller GAMMA control switch 0: ON 1: OFF	0	MCR	
	7	dummy				
3	0	ENTPAL	TV system mode 0: NTSC 1: PAL (MCRDIP = 1)	SW	MCR	
	1	ECCD1	LSB CCD mode 0h: 360H 1h: 510H 2h: 720H 3h: 760H (MCRDIP = 1)	SW	MCR	
	2	ECCD2	MSB			
	3	AESHUT	AE shutter manual 0: auto 1: Shutter manual (MCRDIP = 1)	0	MCR	
	4	(Low)	"0" fixed	0h		
	5					
	6	GAMMA	Gamma switch 0: ON 1: OFF (MCRDIP = 1)	0	MCR	
	7	AEME	AE/ME selection 0: auto 1: manual (MCRDIP = 1)	0	MCR	

#1: Initial setting value with Power-on

The "SW" mark of #1, it is meant to change by DIP-SW setting.

Serial input						
Byte	bit	Name	Description	#1	Block	Address
4	0	FLON	Flikerless mode switch 0: OFF 1: ON (MCRDIP = 1)	0	MCR	
	1	BLCOF	Back light compensation switch 0: ON 1: OFF (MCRDIP = 1)	0	MCR	
	2	MIRIS	IRIS mode selection 0: E-IRIS 1: Mecha-IRIS (MCRDIP = 1)	0	MCR	
	3	AEREF	AE convergence level selection 0: preset 1: eeprom (MCRDIP = 1)	0	MCR	
	4	AGCMAX	AGC max gain selection 0: Low (eeprom) 1: High (eeprom)(MCRDIP = 1)	0	MCR	
	5	AWB1	LSB AWB mode selection (MCRDIP = 1)	0	MCR	
	6	AWB2	0h: ATW 1h: MWB-Adjust 2h: Push Lock 3h: User	0	MCR	
	7	AWB3	4h: Indoor 5h: FL 6h: MWB-Lock/HOLD 7h: Outdoor MSB	0	MCR	
5	0	E2WR	EEPROM WRITE 1byte 0: OFF 1: WRITE	0	SCS	
	1	E2WEN	EEPROM WRITE enalbe 0: OFF 1: SEND	0	SCS	
	2	E2RLSB	EEPROM READ data 0: MSB 1: LSB	0	SCS	
	3	E2RSW	EEPROM READ mode hold switch 0: OFF 1: ON	0	SCS	
	4	E2RAL1	EEPROM READ-1 0: OFF 1: READ	0	SCS	
	5	E2RAL2	EEPROM READ-2 0: OFF 1: READ	0	SCS	
	6	E2RAL3	EEPROM READ-3 0: OFF 1: READ	0	SCS	
	7	E2RAL4	EEPROM READ-4 0: OFF 1: READ	0	SCS	
6	0	E2CODE	LSB	00h	EEP ROM	
	1					
	2					
	3		EEPROM read/write code			
	4					
	5					
	6					
	7		MSB			
7	0	E2ADRS	LSB	00h	EEP ROM	
	1					
	2					
	3		EEPROM write address			
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
8	0	E2DATA	LSB EEPROM write data (MSB) MSB	00h	EEP ROM	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	SPCODE	LSB Microcontroller spec code (See spec code table (1) to (6).) MSB	00h	MCR	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	SPCDAT	LSB Microcontroller spec data (See spec code table (1) to (6).) MSB	00h	MCR	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	EAGC	LSB External microcomputer AGC data MSB	00h	MCR	
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
12	0	E2DATAL	LSB EEPROM write data (LSB) MSB	00h	EEP ROM	
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 9: SG [SG control/SG status output]

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0	CAT9	LSB Category selection code 09h: SG MSB				0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
1	0	SGMODE	SG mode 0h:INT 1h:LL 2h:VSL 3h:VBSLHP 4h:VBSLHR 5h:VRHR 7h:AUTO	7h	SG	2Ah MSB	0	SGSTAT	SG status output 0h:INT 1h:LL 2h:VSL 3h:VBSLHP 4h:VBSLHR 5h:VRHR 6h:SG135	SG
	1						1			
	2						2			
	3	dummy					3	HDET	External sync signal detection flag (detect = "1")	
	4						4	VDET		
	5	(Low)	"0" fixed	0			5	SCDET		
	6	(Low)	"0" fixed	0			6	(Low)	"0" fixed	
	7	PALSEQ	PAL field sequence on	0	SG		7			
2	0	SFTHL	LSB In case of H-PLL: H-Phase adjustment In case of H-RESET: Counter load value setting LSB 8 bits MSB	00h	SG	2Bh MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
3	0	SFTVL	LSB In case of V-PLL: V-Phase adjustment In case of V-RESET: Counter load value setting LSB 8 bits MSB	02h	SG	2Ch MSB	0	—	Unfixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
4	0	SFTHM	SFTH MSB 2 bits	0h	SG	2Dh MSB	0	—	Unifixed data output	
	1						1			
	2	SFTVM	SFTV MSB 2 bits	0h	SG		2			
	3						3			
	4	dummy					4			
	5						5			
	6						6			
	7						7			
5	0	SFTFSC	LSB Subcarrier PLL phase shifting 0 deg (0h) to 315 deg (7h) MSB	0h	SG	2Eh MSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3	FSCPCMP	Subcarrier phase comparator ON	0	SG		3			
	4	FSCPSEL	Subcarrier output phase selection	0h	SG		4			
	5						5			
	6	SCMPPIN	SCOMP pin selection	0	SG		6			
	7	INVPCMP	Phase comparator input change (ref/vari)	1	SG		7			
6	0	WBSTAHL	Wide Burst Horizontal start position LSB 8 bits	00h	SG	65h LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
7	0	WBSTOHL	Wide Burst Horizontal start position LSB 8 bits	00h	SG	66h LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
8	0	WBSTAHM	LSB Wide Burst Horizontal start position MSB 2 bits	0h	SG	67h LSB	0	—	Unifixed data output	
	1		MSB				1			
	2	WBSTOHM	LSB Wide Burst Horizontal start position MSB 2 bits	0h	SG		2			
	3		MSB				3			
	4	WBSTON	Wide Burst mode 1: ON	0	SG		4			
	5	4FHSEL	LSB 4Fsc frequency divider HD output pin selection	0h	SG		5			
	6		MSB				6			
	7	4FHOUT	4Fsc frequency divider HD output	0	SG		7			
9	0	DEF1HL	LSB Blemish compensation 1 Horizontal position setting LSB 8 bits	0h	SG	68h LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7		MSB				7			
10	0	DEF1VL	LSB Blemish compensation 1 Vertical position setting LSB 8 bits	0h	SG	69h LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7		MSB				7			
11	0	DEF1HM	LSB Blemish compensation 1 Horizontal position setting MSB 2 bits	0h	SG	6Ah LSB	0	—	Unifixed data output	
	1		MSB				1			
	2	DEF1VM	LSB Blemish compensation 1 Vertical position setting MSB 2 bits	0h	SG		2			
	3		MSB				3			
	4	DEF1L	Blemish 1: continuous 2 pixels	0	SG		4			
	5	dummy					5			
	6						6			
	7	DEFMK	Blemish 1, 2 marker 1: ON	0	SG		7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
12	0	DEF2HL	LSB Blemish compensation 2 Horizontal position setting LSB 8 bits MSB	00h	SG	6Bh LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
13	0	DEF2VL	LSB Blemish compensation 2 Vertical position setting LSB 8 bits MSB	00h	SG	6Ch LSB	0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
14	0	DEF2HM	LSB Blemish compensation 2 MSB Horizontal position setting MSB 2 bits	0h	SG	6Dh LSB	0	—	Unifixed data output	
	1						1			
	2	DEF2VM	LSB Blemish compensation 2 MSB Vertical position setting MSB 2 bits	0h	SG		2			
	3						3			
	4	DEF2L	Blemish compensation 2: continuous 2 pixels	0	SG		4			
	5	dummy					5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

Category 10: EXTCON [External control parameters/Sampling data output]

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
0	0	CAT10	LSB Category selection code 0Ah: EXTCON MSB				0	—	Unifixed data output	
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
1	0	(Low)	"0" fixed	00h			0	AJSTY	LSB Sampling data output for Y signal adjustment MSB (Data format = BIN)	Y
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7						7			
2	0	ADJSTH	LSB Horizontal position setting for camera adjustment pulse (Adjust pulse H) MSB	00h	SG		0	AJSTRY	LSB Sampling data output for R-Y signal adjustment MSB (Data format = 2's)	C
	1						1			
	2						2			
	3						3			
	4						4			
	5						5			
	6						6			
	7	ADJSTVL	Vertical phase adj. (LSB)	0	SG		7			
3	0	ADJSTVM	Vertical position setting (MSB) (Adjust pulse V)	0h	SG		0	AJSTBY	LSB Sampling data output for B-Y signal adjustment MSB (Data format = 2's)	C
	1						1			
	2	DISPMIX	Wind display 0: OFF 1: ON	0	Y		2			
	3	OPDADJ	OPD adjustment mode switch	0	OPD		3			
	4	OPDDISP	LSB OPD window display selection **#2** MSB	5h or 0h **#3**	OPD		4			
	5						5			
	6						6			
	7						7			

#1: Initial setting value with Power-on

#2: 1h: AEW0 2h: AEW1 3h: AEW2 4h: AEW3 5h: AEW4 6h: AWBW 7h: HISTW
9h: HIST1 integral pixel Ah: HIST2 integral pixel Bh: AWB integral pixel

#3: Setting value differs according to mode during initial setting with power-on.
SS-1M mode: 5h SS-1 mode: 0h

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
4	0	PGON	Test pattern signal on/off	0	SG		0	—	Unifixed data output	
	1	PGMIXAL	TP signal full display	0	SG		1			
	2	PGLIDSEL	Signal phase selection by line	0	SG		2			
	3	PGBIDSEL	Color identification signal phase selection	0	SG		3			
	4	PGCOLSEL	Color bar/monochrome output selection	0	SG		4			
	5	PGCOL	LSB	0h	SG		5			
	6		Monochrome selection				6			
	7		MSB				7			
5	0	PGHV	H/V switch	0	SG		0	—	Unifixed data output	
	1	PGRSTR	Raster setting	0	SG		1			
	2	PGPTSEL	TP signal pattern selection	0	SG		2			
	3						3			
	4	PGSIDSEL	Serial data display	0	SG		4			
	5	PGSIDAL	Serial data normal display	0	SG		5			
	6	PGGAIN	TP signal level selection MIN (0h) to MAX (3h)	0	SG		6			
	7						7			
6	0	PGDCRS2	LSB	00h	SG		0	—	Unifixed data output	
	1						1			
	2						2			
	3		Serial setting data RS2				3			
	4						4			
	5						5			
	6						6			
	7		MSB (Data format = BIN)				7			
7	0	PGDCRS1	LSB	00h	SG		0	—	Unifixed data output	
	1						1			
	2						2			
	3		Serial setting data RS1				3			
	4						4			
	5						5			
	6						6			
	7		MSB				7			

#1: Initial setting value with Power-on

		Serial input					Serial output			
Byte	bit	Name	Description	#1	Block	Address	bit	Name	Description	Block
8	0	PGDCBS2	LSB	00h	SG		0	—	Unfixed data output	
	1						1			
	2						2			
	3		Serial setting data BS2				3			
	4						4			
	5						5			
	6						6			
	7		MSB				7			
9	0	PGDCBS1	LSB	00h	SG		0	—	Unifixed data output	
	1						1			
	2						2			
	3		Serial setting data BS1				3			
	4						4			
	5						5			
	6						6			
	7		MSB				7			

#1: Initial setting value with Power-on

Spec code: AE (CAT8 byte9 code = 0Xhex)

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
01	0	AESPED	LSB AE speed (01h to FFh) MSB	08h		2Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
02	0	AEUSR	LSB AE USR level setting (00h to 0Ch) MSB	04h		30h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
03	0	AGCMAXL	LSB AE AGC-amp max gain at low mode (00h to FFh) MSB	BBh		31h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
04	0	AGCMIN	LSB AE AGC-amp min gain (00h to FFh) MSB	11h		32h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
05	0 1 2 3 4 5 6 7	SHTLIM	LSB AE shutter limit 00h: 1/500 04h: 1/10000 01h: 1/1000 05h: 1/20000 02h: 1/2000 06h: 1/50000 03h: 1/5000 07h: 1/100000 MSB	07h		33h MSB
06	0 1 2 3 4 5 6 7	AGCMAXH	LSB AE AGC-amp max gain at high mode (00h to FFh) MSB	EEh		34h MSB
07	0 1 2 3 4 5 6 7	AEBLLV	LSB AE Back Light Level (00h to FFh) MSB	0Ch		35h MSB
08	0 1 2 3 4 5 6 7	HISTOFF	LSB AE HISTOGRAM function switch (00h: ON 01h: OFF) MSB	00h		36h MSB

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
09	0	W0WEIT	LSB AE wind0 weight (00h to 0Fh) MSB	01h		37h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
0A	0	W1WEIT	LSB AE wind1 weight (00h to 0Fh) MSB	01h		38h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
0B	0	W2WEIT	LSB AE wind2 weight (00h to 0Fh) MSB	03h		39h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
0C	0	W3WEIT	LSB AE wind3 weight (00h to 0Fh) MSB	03h		3Ah MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
0D	0	OFFIRISV	LSB IRISV output voltage setting during MIRIS OFF (00h to FFh) MSB	66h		4Eh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Spec code: AWB (CAT8 byte9 code = 1Xhex)

Serial input						
Byte	bit	Name	Description	#1	Block	Address
11	0	AWBSPED	LSB AWB speed (01h to 0Eh)	02h		3Bh
	1					
	2					
	3		MSB			MSB
	4	AWBAJST5	Offset of Frameless area (ATW mode: G-Mg direction)			
	5					
	6	AWBAJST6	Offset of Frameless area (ATW mode: Color temperature direction)			
	7					
12	0	AWBFRAM	LSB AWB vector frame 00h: Typical Frame 04h: Wide Frame 12h: Frame less	00h		3Ch
	1					
	2					
	3					
	4					MSB
	5					
	6					
	7		MSB			
13	0	WBRSFT	LSB WB R shift (80h to 00h to 7Fh: 2's)	03h		3Dh
	1					
	2					
	3					
	4					MSB
	5					
	6					
	7		MSB			
14	0	WBBSFT	LSB WB B shift (80h to 00h to 7Fh: 2's)	01h		3Eh
	1					
	2					
	3					
	4					MSB
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
15	0	WBUSRR	LSB WB USR preset R gain (00h to FFh) MSB	4Ch		3Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
16	0	WBUSRB	LSB WB USR preset B gain (00h to FFh) MSB	2Ch		40h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
17	0	AWBPRER	LSB AWB PRE white balance R (00h to FFh) MSB	37h		41h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
18	0	AWBPREB	LSB AWB PRE white balance B (00h to FFh) MSB	39h		42h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Spec code: FIXOPD (CAT8 byte9 code = 2Xhex)

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
21	0	SPCNTWID	LSB H COUNTER width (00h to 0Fh) MSB	08h		43h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
22	0	SPW4STAH	LSB Wind4 H START (00h to 0Fh) MSB	05h		44h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
23	0	SPW4WIDH	LSB Wind4 H WIDTH (00h to 0Fh) MSB	05h		45h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
24	0	SPW4STAV	LSB Wind4 V START (00h to 0Fh) MSB	04h		46h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Byte	bit	Name	Description	#1	Block	Address
25	0	SPW4WIDV	LSB Wind4 V WIDTH (00h to 0Fh)	07h		47h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Note) Microcontroller calculates OPD detection area from Spec code: FIXOPD. It is set to the same value with CAT7: FIXOPD by power-on initial operation.
But when CAT7: FIXOPD is set again after power-on initial operation, the same value must be communication set to the same value for Spec code: FIXOPD to make microcontroller know its setting value.

Spec code: SPRS (CAT8 byte9 code = 3Xhex)

Serial input						
Byte	bit	Name	Description	**#1**	Block	Address
31	0	CSPRSSTA	LSB Chroma suppress start level (00h to FFh) MSB	52h		48h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
32	0	CSPRSEND	LSB Chroma suppress end level (00h to FFh) MSB	80h		49h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
33	0	CSPRSLV	LSB Chroma suppress level (00h to FFh: × 0 to × 1.0) MSB	8Ah		4Ah MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
34	0	ASPRSSTA	LSB Apcom suppress start level (00h to FFh) MSB	3Dh		4Bh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
35	0	ASPRSEND	LSB Apcom suppress end level (00h to FFh) MSB	80h		4Ch MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
36	0	ASPRSLV	LSB Apcom suppress level (00h to FFh: × 0 to × 1.0) MSB	00h		4Dh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
37	0	RYGAIN1	LSB R-Y Gain 1/4 MSB	20h		4Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
38	0	BYGAIN1	LSB B-Y Gain 1/4 MSB	11h		50h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
39	0	RYGAIN2	LSB R-Y Gain 2/4 MSB	20h		51h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3A	0	BYGAIN2	LSB B-Y Gain 2/4 MSB	11h		52h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3B	0	RYGAIN3	LSB R-Y Gain 3/4 MSB	20h		53h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3C	0	BYGAIN3	LSB B-Y Gain 3/4 MSB	11h		54h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
3D	0	RYGAIN4	LSB R-Y Gain 4/4 MSB	20h		55h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3E	0	BYGAIN4	LSB B-Y Gain 4/4 MSB	11h		56h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Chroma: HUE initial value (CAT2)

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
	0	RYHUE1	LSB	D0h		57h
	1					
	2					
	3		R-Y Hue 1/4			MSB
	4					
	5					
	6					
	7		MSB			
	0	BYHUE1	LSB	F8h		58h
	1					
	2					
	3		B-Y Hue 1/4			MSB
	4					
	5					
	6					
	7		MSB			
	0	RYHUE2	LSB	D0h		59h
	1					
	2					
	3		R-Y Hue 2/4			MSB
	4					
	5					
	6					
	7		MSB			
	0	BYHUE2	LSB	F8h		5Ah
	1					
	2					
	3		B-Y Hue 2/4			MSB
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
	0	RYHUE3	LSB R-Y Hue 3/4 MSB	D0h		5Bh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	BYHUE3	LSB B-Y Hue 3/4 MSB	F8h		5Ch MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	RYHUE4	LSB R-Y Hue 4/4 MSB	D0h		5Dh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	0	BYHUE4	LSB B-Y Hue 4/4 MSB	F8h		5Eh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Spec code: SG (CAT8 byte9 code = 4Xhex)

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
41	0	PRSETVL	LSB	90h		6Ah
	1					
	2					
	3		Preset V Shifter LSB (00h to FFh)			MSB
	4					
	5					
	6					
	7		MSB			
42	0	PRSETVM	LSB	00h		6Bh
	1					
	2					
	3		Preset V Shifter MSB (00h to 03h)			MSB
	4					
	5					
	6					
	7		MSB			
43	0	PRSETHL	LSB	06h		68h
	1					
	2					
	3		Preset H Shifter LSB (00h to FFh)			MSB
	4					
	5					
	6					
	7		MSB			
44	0	PRSETHM	LSB	01h		69h
	1					
	2					
	3		Preset H Shifter MSB (00h to 03h)			MSB
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Spec code: MCR (CAT8 byte9 code = 5Xhex)

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
51	0	AWBTRIG	Push lock selection 0: push period 1: trigger starting	0		6Ch MSB
	1	MWBLOCK	Hold/Lock selection 0: hold 1: MWBLOCK	0		
	2	AWBSEPOF	Integral mode by luminance ON/OFF 0: ON 1: OFF	0		
	3	INTLOWLV	Integral lower limit level selection by luminance 0: 04h 1: 0h	0		
	4	AWBHLCUT	Integral high luminance minimum area by luminance 0: 2 blocks 1: 16 blocks 2: 36 blocks 3: 64 blocks	0h		
	5					
	6	LSHTLIM	FLON mode 0: shutter fixed 1: low-speed shutter limiter	0		
	7	SPMMODE	MCR mode selection 0h: SS-1 mode 1h: SS-1M mode	0		
52	0	KEYINFLD	LSB	1Eh		6Dh MSB
	1		Key initial period processing field (00h to FFh)			
	2					
	3					
	4					
	5					
	6					
	7		MSB			
53	0	KEYINCNT	LSB	2h		6Eh MSB
	1		Key initial period processing count (0h to Fh)			
	2					
	3		MSB			
	4	KEYRPFLD	LSB	5h		
	5		Key continuous period processing interval (0h to Fh)			
	6					
	7		MSB			
54	0	LNKAEOFF	Link AE off 0: AESHUT mode 1: Low light suppress mode	0		6Eh LSB
	1	dummy				
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Spec code: AWBM (CAT8 byte9 code = 6Xhex)

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
61	0	AWBWRSFT	LSB ATW/Push-lock convergence point shift (R-Y direction) (80h to 00h to 7Fh: 2's) MSB	00h		6Fh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
62	0	AWBWBSFT	LSB ATW/Push-lock convergence point shift (B-Y direction) (80h to 00h to 7Fh: 2's) MSB	00h		70h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
63	0	PRSETMWR	LSB MWB preset gain (R gain) (00h to FFh) MSB	37h		71h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
64	0	PRSETMWB	LSB MWB preset gain (B gain) (00h to FFh) MSB	39h		72h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
65	0	PRERBL	LSB ATW operation frame data (adjustment data) (R-B)/G LSB 8 bits (00h to FFh: 2's) MSB	00h		73h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
66	0	PRERBM	LSB ATW operation frame data (adjustment data) (R-B)/G MSB 8 bits (80h to FFh: 2's minus range) MSB	E6h		74h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
67	0	PRERBGL	LSB ATW operation frame data (adjustment data) (R + B – 2G)/G LSB 8 bits (00h to FFh: 2's) MSB	00h		75h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
68	0	PRERBGM	LSB ATW operation frame data (adjustment data) (R + B – 2G)/G MSB 8 bits (00h to 7Fh: 2's plus range) MSB	0Bh		76h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Serial input						
Code	bit	Name	Description	#1	Block	Address
69	0	PRE2R	LSB ATW high color temperature R gain (approx. 9500K) (00h to FFh) MSB	60h		77h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6A	0	PRE2B	LSB ATW high color temperature B gain (approx. 9500K) (00h to FFh) MSB	20h		78h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6B	0	AWBAJST1	LSB ATW gain limiter Upper limit offset (00h to FFh) MSB	18h		79h MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6C	0	AWBAJST2	LSB ATW gain limiter Lower limit offset (00h to FFh) MSB	18h		7Ah MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Spec code: AWBM (CAT8 byte9 code = 6Xhex, 70hex)

Serial input						
Code	bit	Name	Description	**#1**	Block	Address
6D	0	BLOGAIN	LSB MWB lower limit B gain (00h to FFh) MSB	28h		7Bh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6E	0	INTSLICE	LSB Luminance specific integral slice level (00h to FFh) MSB	80h		7Ch MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6F	0	AWBAJST3	LSB ATW operation frame offset (R-B)/G (80h to 00h to 7Fh: 2's) MSB	00h		7Dh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					
70	0	AWBAJST4	LSB ATW operation frame offset (R + B – 2G)/G (80h to 00h to 7Fh: 2's) MSB	00h		7Eh MSB
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

EEPROM Map (1)

EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
00	SS-1/SS-1M ROM Code = 9D			CXD2163R CXD2163BR Area		Not occupied				
01	CAT1 FIX	1	NTPAL, CCD, YDOUT, , ,							
02		2	ADSEL, ADINV, ADDLY, , ,							
03		3	SETUP, WCLIP, SUP601							
04		4	SYNLV, SYNLVPM, YDLY							
05		5	VHAPSL, VAPSL, VAPLIM							
06		6	HLAPSL, HLAPPC, , ,							
07		7	HLAPPG, HLAPMG							
08		8	RMATY							
09		9	RMATC							
0A		10	BMATY							
0B		11	BMATC							
0C		12	BSTLV, CPHSEL, LIDSEL							
0D		13	MODSW, ENCSW, , ,							
0E		14	SYNPIN, FLDPIN, , ,							
0F	CAT2 FIELD	1	YGAIN							
10		2	HAPGL, HAPGH, VAPG							
11		3	VHAPG, HLAPG							
12		4	CSVLV, CSVTH, , ,							
13		5	YGAM, YSGAMLV, , ,							
14		6	CGAM, CKNCLIP0							

EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
15	CAT3 CLAMP	1	BLACK1L	CXD2163R CXD2163BR Area		Not occupied				
16		2	BLACK2L							
17		3	BLACK1M, BLACK2M							
18		4	SHOFST							
19		5	EVRUSR ch8							
1A	Not occupied									
1B										
1C	CAT4 DCREF	1	DAVREFY	CXD2163R CXD2163BR Area						
1D		2	DAVREFC							
1E		3	VSUB							
1F		4	VRGL							
20	CAT5 AE	1	AGCCNT							
21		2	IRISV							
22	CAT6 AWB	1	WBR			CAT6 AWB	1	WBR (Same as MSB)	CXD2163R CXD2163BR Area	
23		2	WBG				2	WBG (Same as MSB)		
24		3	WBB				3	WBB (Same as MSB)		
25	CAT7 FIXOPD	1	AWBWSEL, AWBGAM, , ,			Not occupied				
26		2	CNTOFST							
27		3	CNTWID							
28		4	W4STAH, W4WIDH							
29		5	W4STAV, W4WIDV							

EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
2A	CAT9 SG	1	SGMODE, PALSEQ	CXD2163R CXD2163BR Area		Not occupied				
2B		2	SFTHL			CAT9 SG	2	SFTHL (Same as MSB)	CXD2163R CXD2163BR Area	
2C		3	SFTVL				3	SFTVL (Same as MSB)		
2D		4	SFTHM, SFTVM				4	SFTHM, , , (Same as MSB)		
2E		5	SFTSFC, FSCPCMP, , ,			Not occupied				
2F	SPEC AE	code 01	AESPED							
30		code 02	AEUSR							
31		code 03	AGCMAXL							
32		code 04	AGCMIN							
33		code 05	SHTLIM							
34		code 06	AGCMAXH							
35		code 07	AEBLLV							
36		code 08	HISTOFF							
37		code 09	W0WEIT							
38		code 0A	W1WEIT							
39		code 0B	W2WEIT							
3A		code 0C	W3EWIT							
3B	SPEC AWB	code 11	AWBSPED, AWBAJST5, 6							
3C		code 12	AWBFRAM							
3D		code 13	WBRSFT							
3E		code 14	WBBSFT							
3F		code 15	WBUSRR							

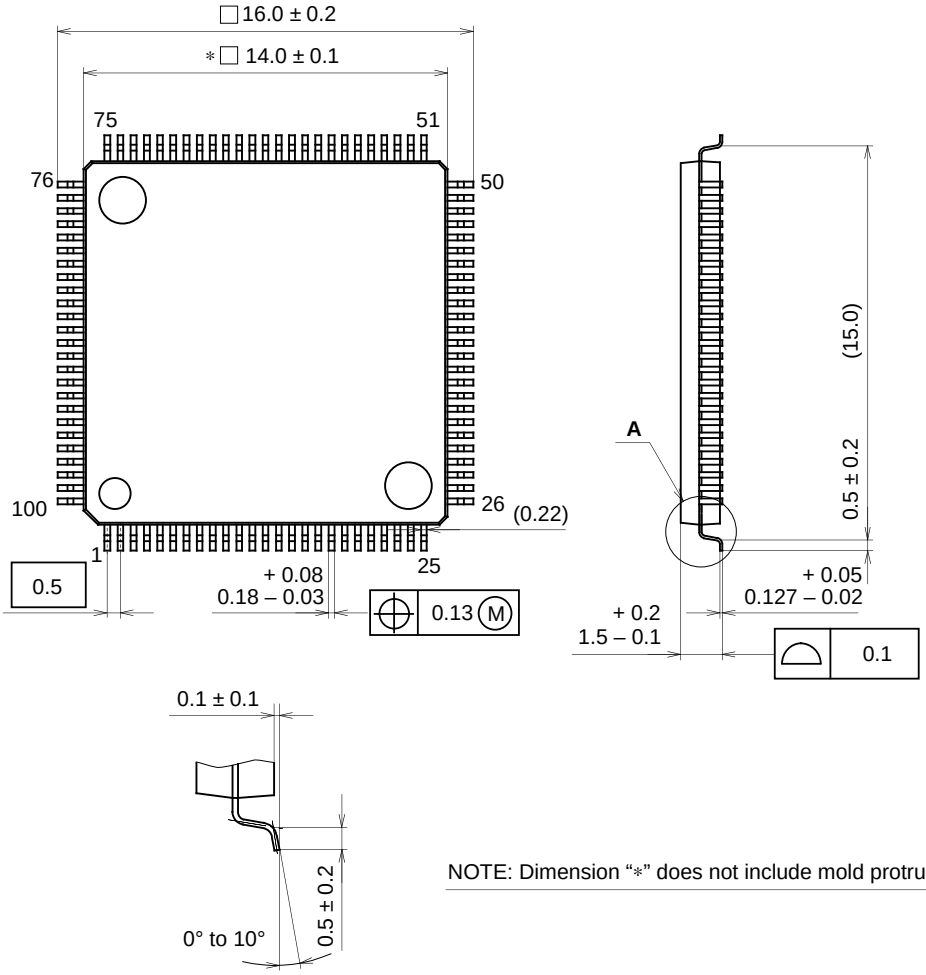
EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
40	SPEC AWB	code 16	WBUSRB	CXD2163R CXD2163BR Area		Not occupied				
41		code 17	AWBPRER							
42		code 18	AWBPREB							
43	SPEC FIXOPD	code 21	SPCNTWID							
44		code 22	SPW4STAH							
45		code 23	SPW4WIDH							
46		code 24	SPW4STAV							
47		code 25	SPW4WIDV							
48	SPEC SPRS	code 31	CSPRSSTA							
49		code 32	CSPRSEND							
4A		code 33	CSPRSLV							
4B		code 34	ASPRSSTA							
4C		code 35	ASPRSEND							
4D		code 36	ASPRSLV							
4E	SPEC AE	code 0D	OFFIRISV	2163BR						
4F	SPEC SPRS	code 37	RYGAIN1	CXD2163R CXD2163BR Area						
50		code 38	BYGAIN1							
51		code 39	RYGAIN2							
52		code 3A	BYGAIN2							
53		code 3B	RYGAIN3							
54		code 3C	BYGAIN3							
55		code 3D	RYGAIN4							
56		code 3E	BYGAIN4							

EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
57	CAT2 FIELD	10	RYHUE1	CXD2163R CXD2163BR Area		Not occupied				
58		11	BYHUE1							
59		10	RYHUE2							
5A		11	BYHUE2							
5B		10	RYHUE3							
5C		11	BYHUE3							
5D		10	RYHUE4							
5E		11	BYHUE4							
5F	CAT1	15	BSTSW, YLPFSW, , ,	2163BR						
60	CAT3 CLAMP	6	CLIPS1BL	CXD2163BR Area		CAT4 DCREF	5	EVR12CH	CXD2163BR Area	
61		7	CLIPS1RL				6	EVRUSR9		
62		8	CLIPS2BL				7	EVRUSR10		
63		9	CLIPS2RL				8	EVRUSR11		
64		10	CLIPS1BM, CLIPS1RM, , ,				9	EVRUSR12		
65		11	HLEDDL1, HLEDDL02, , ,			CAT9 SG	6	WBSTAHL		
66		12	HLEDLVL				7	WBSTOHL		
67		13	HLEDLVM, HLEWID, , ,				8	WBSTAHM, WBSTOHM, , ,		
68	SPEC SG	code 41	PRESETVL				9	DEF1HL		
69		code 42	PRESETVM				10	DEF1VL		
6A		code 43	PRESETHL				11	DEF1HM, DEF1VM, , ,		
6B		code 44	PRESETHM				12	DEF2HL		

EEPROM										
Address	MSB 8bit					LSB 8bit				
	Serial Communication		Parameter Name	CXD2163BR Area	Note	Serial Communication		Parameter Name	CXD2163BR Area	Note
	Category	Byte				Category	Byte			
6C	SPEC MCR	code 51	AWBTRIG, MWBLOCK, , ,	CXD2163BR Area		CAT9 SG	13	DEF2VL	CXD2163BR Area	
6D		code 52	KEYINFLD				14	DEF2HM, DEF2VM, , ,		
6E		code 53	KEYINCNT, KEYRPFLD			SPEC MCR	code 54	LNKAEOFF		
6F	SPEC AWB	code 61	AWBWRSFT			Not occupied				
70		code 62	AWBWBSFT							
71		code 63	PRSETMWR							
72		code 64	PRSETMWB							
73		code 65	PRERBL							
74		code 66	PRERBM							
75		code 67	PRERBGL							
76		code 68	PRERBGM							
77		code 69	PRE2R							
78		code 6A	PRE2B							
79		code 6B	AWBAJST1							
7A		code 6C	AWBAJST2							
7B		code 6D	BLOGAIN							
7C		code 6E	INTSLICE							
7D		code 6F	AWBAJST3							
7E		code 70	AWBAJST4							
7F	CXD2163BR Work Area (There is no necessary of the initial value writing.)								2163BR	

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g