SONY

CXB1457R

EGA/VGA/WVGA/SVGA 24-bit Transmitter

Description

The CXB1457R is a transmitter chip for data transmission based on GVIF (Gigabit Video Interface) technology.

This IC supports 24-bit color data transmission with EGA/VGA/WVGA/SVGA resolution.

Features

- 1 chip transmitter for serial transmission of 24-bit color EGA/VGA/WVGA/SVGA picture
- On-chip PLL synthesizer
- On-chip differential cable driver
- On-chip FIFO circuit
- CMOS logic interface
- +3.3V single power supply
- Low power consumption
- Lead-free 48-pin plastic LQFP package (7mm × 7mm)

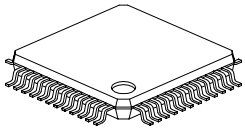
Application

GVIF (Gigabit Video Interface)

Structure

Bi-CMOS IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}, $V_{CC}A$	–0.3 to +4.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	333	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}, $V_{CC}A$	3.135 to 3.465	V
• Operating temperature	Topr	–40 to +85	°C

Block Diagram & Pin Configuration

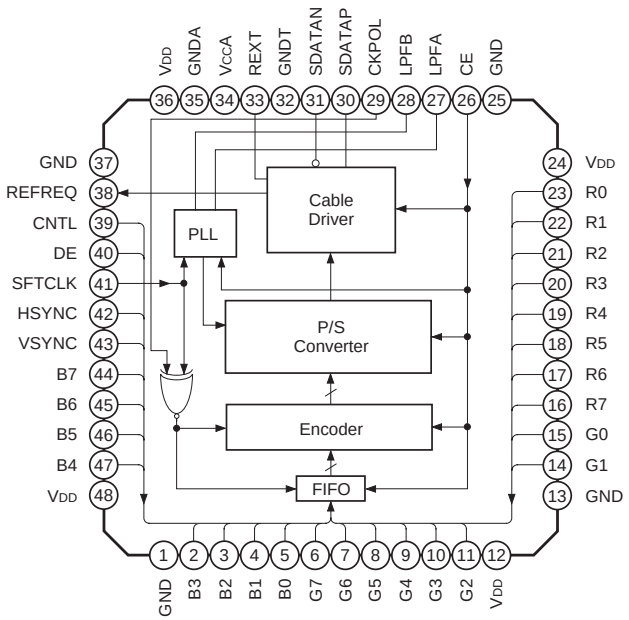


Fig. 1. Block Diagram & Pin Configuration

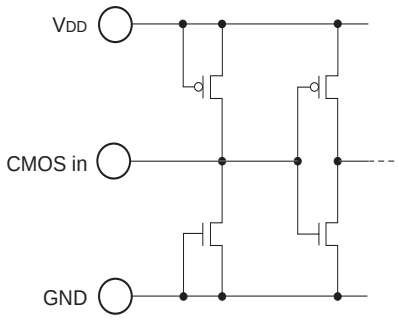
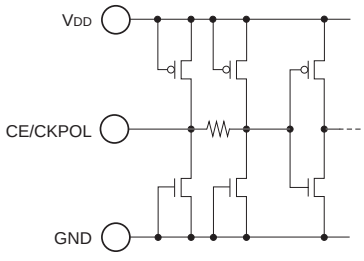
E04Y33A52

Pin Description

Table 1. Power Supply/GND

Symbol	Pin No.	Description
V_{DD}	12, 24, 36, 48	Logic positive power supply. Connects to 3.3V ± 5%.
GND	1, 13, 25, 37	Logic GND. Connects to 0V.
$V_{CC}A$	34	Analog positive power supply. Connects to 3.3V ± 5%.
GNDA	35	Analog GND. Connects to 0V.
GNDT	32	Transmission GND. Connects to 0V.

Table 2. Digital Signals

Symbol	Pin No.	Type	Description	Equivalent circuit
SFTCLK	41	CMOS in 1	Shift clock input for the data fetch at rising or falling edge	
RED (7 to 0)	16, 17, 18, 19, 20, 21, 22, 23	CMOS in 1	Pixel data inputs 1 pixel/shift-clock input	
GRN (7 to 0)	6, 7, 8, 9, 10, 11, 14, 15			
BLU (7 to 0)	44, 45, 46, 47, 2, 3, 4, 5			
HSYNC	42	CMOS in 1	Hsync data input	
VSYNC	43	CMOS in 1	Vsync data input	
CNTL	39	CMOS in 1	Control data input (reserved pin) When not used, connect to GND.	
DE	40	CMOS in 1	Display enable data input	
CE	26	CMOS in 2	Chip enable input	
CKPOL	29	CMOS in 2	SFTCLK fetching edge polarity control input	

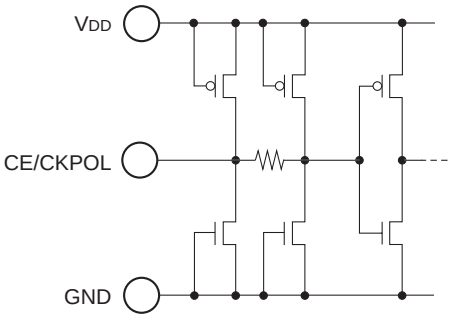
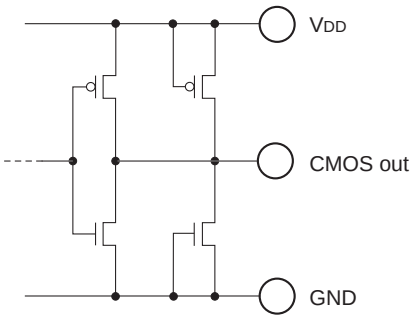
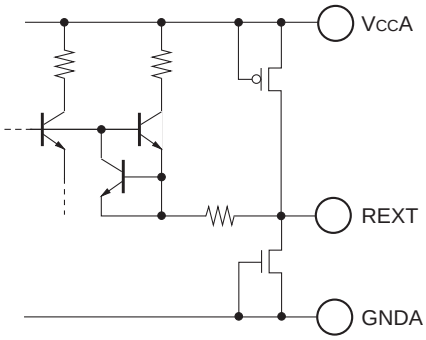
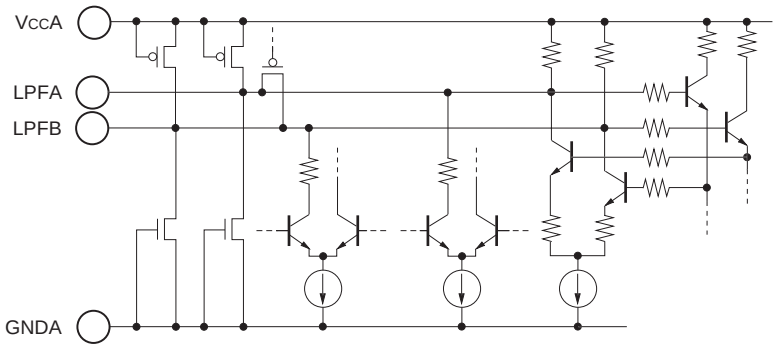
Symbol	Pin No.	Type	Description	Equivalent circuit
SDATAP/N	30, 31	Tx	Serial data output and Refclk request input Data rate of SDATAP/N output 8MHz-clock input to SFTCLK: 240Mbps 16MHz-clock input to SFTCLK: 480Mbps 25MHz-clock input to SFTCLK: 750Mbps 33MHz-clock input to SFTCLK: 990Mbps 40MHz-clock input to SFTCLK: 1200Mbps	
REFREQ	38	CMOS out	Refclk request detection flag	

Table 3. Others

Symbol	Pin No.	Description	Equivalent circuit
REXT	33	SDATAP/N output current trimming. Connects to the external resistor.	
LPFA/B	27, 28	External loop filter	

Electrical characteristics

Table 4. Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{CC}	–0.3	—	+4.0	V	
CMOS DC input voltage	V_I_C	–0.5	—	+4.0	V	
CMOS High level output current	I_{OH}_C	–10	—	0	mA	
CMOS Low level output current	I_{OL}_C	0	—	+10	mA	
Serial data output pin voltage	Vsdout	V_{CC} – 1.2	—	V_{CC} + 0.5	V	
Storage temperature	Tstg	–65	—	+150	°C	

Table 5. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{CC}	3.135	3.3	3.465	V	
Ambient temperature	Ta	–40	—	+85	°C	

Table 6. DC Characteristics (Under the recommended conditions. See Table 5.)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
SFTCLK/Pixel/Sync/Cntl/DE High level input voltage		V_{IH}_C1	V_{DD} – 1.0	—	V_{DD}	V	
SFTCLK/Pixel/Sync/Cntl/DE Low level input voltage		V_{IL}_C1	0	—	0.8	V	
SFTCLK/Pixel/Sync/Cntl/DE High level input current		I_{IH}_C1	—	—	1.0	µA	$V_{IN} = V_{DD}$
SFTCLK/Pixel/Sync/Cntl/DE Low level input current		I_{IL}_C1	–1.0	—	—	µA	$V_{IN} = 0$
CE and CKPOL High level input voltage		V_{IH}_C2	V_{DD} – 0.5	—	V_{DD}	V	
CE and CKPOL Low level input voltage		V_{IL}_C2	0	—	0.5	V	
CE and CKPOL High level input current		I_{IH}_C2	—	—	1.0	µA	$V_{IN} = V_{DD}$
CE and CKPOL Low level input current		I_{IL}_C2	–1.0	—	—	µA	$V_{IN} = 0$
CMOS High level output voltage		V_{OH}_C	2.4	—	—	V	I_{OH} = –2mA
CMOS Low level output voltage		V_{OL}_C	—	—	0.4	V	I_{OL} = 2mA
SDATA High level output current		I_{OH}_SD	–0.1	—	+0.5	mA	REXT = 4.7kΩ
SDATA Low level output current		I_{OL}_SD	14.0	—	18.0	mA	
SDATA High level input voltage		V_{IH}_SD	V_{CC} – 0.50	—	—	V	Common mode voltage
SDATA Low level input voltage		V_{IL}_SD	—	—	V_{CC} – 0.74	V	
Supply current	Worst case	I_{CC}	—	70	95	mA	C_L = 10pF, f = 40MHz
			—	60	—	mA	C_L = 10pF, f = 8MHz
	16 gray scale		—	60	85	mA	C_L = 10pF, f = 40MHz
			—	55	—	mA	C_L = 10pF, f = 8MHz

Table 7. AC Characteristics (Under the recommended conditions. See Table 5.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SFTCLK frequency	Fsftclk	7.6	—	16	MHz	For EGA panel
		23.75	25.0	26.25	MHz	For VGA panel
		31.35	33.0	34.65	MHz	For WVGA panel
		38.0	40.0	42	MHz	For SVGA panel
SFTCLK duty factor	Dsftclk	40	—	60	%	Vth = V_{DD}/2
Pixel/Sync/Cntl/DE setup time1 to SFTCLK	Tsetup1	2.0	—	—	ns	Vth = 1.4V Tir≤5.0ns, Tif≤5.0ns
Pixel/Sync/Cntl/DE hold time1 to SFTCLK	Thold1	6.0	—	—	ns	Vth = 1.4V Tir≤5.0ns, Tif≤5.0ns
Pixel/Sync/Cntl/DE setup time2 to SFTCLK	Tsetup2	4.0	—	—	ns	Vth = 1.4V 5.0ns<Tir≤8.5ns 5.0ns<Tif≤8.5ns Fsftclk≤34.65MHz
Pixel/Sync/Cntl/DE hold time2 to SFTCLK	Thold2	8.0	—	—	ns	Vth = 1.4V 5.0ns<Tir≤8.5ns 5.0ns<Tif≤8.5ns Fsftclk≤34.65MHz
CMOS input rise time1	Tir1	—	—	5.0	ns	20 to 80%
CMOS input fall time1	Tif1	—	—	5.0	ns	20 to 80%
CMOS input rise time2	Tir2	—	—	8.5	ns	20 to 80% Fsftclk≤34.65MHz
CMOS input fall time2	Tif2	—	—	8.5	ns	20 to 80% Fsftclk≤34.65MHz
SDATA rise time	Trsd	—	270	—	ps	20 to 80%, C_L = 2pF
SDATA fall time	Tfsd	—	270	—	ps	20 to 80%, C_L = 2pF
CLOCK mode assert time	TAclk	—	36	—	ns	
CLOCK mode deassert time	TDclk	—	180	—	ns	
PLL lock-in time	Tlockin	—	350	—	µs	

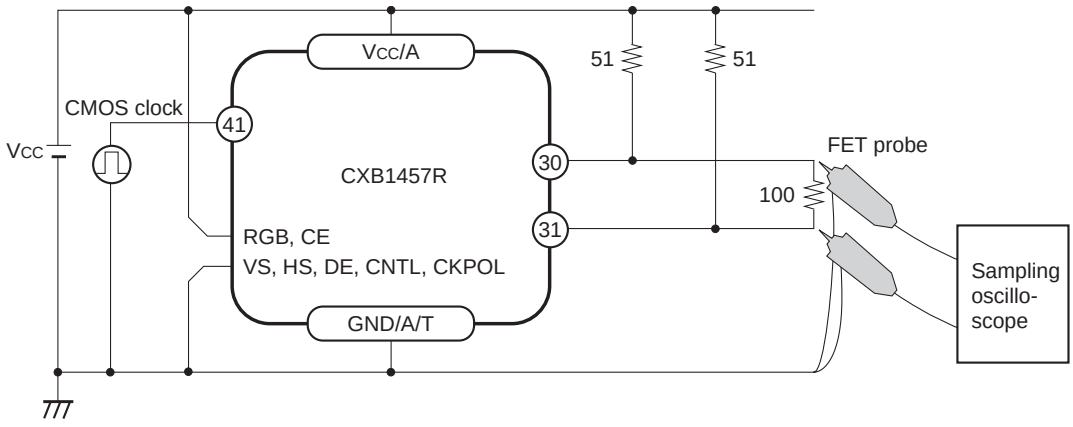
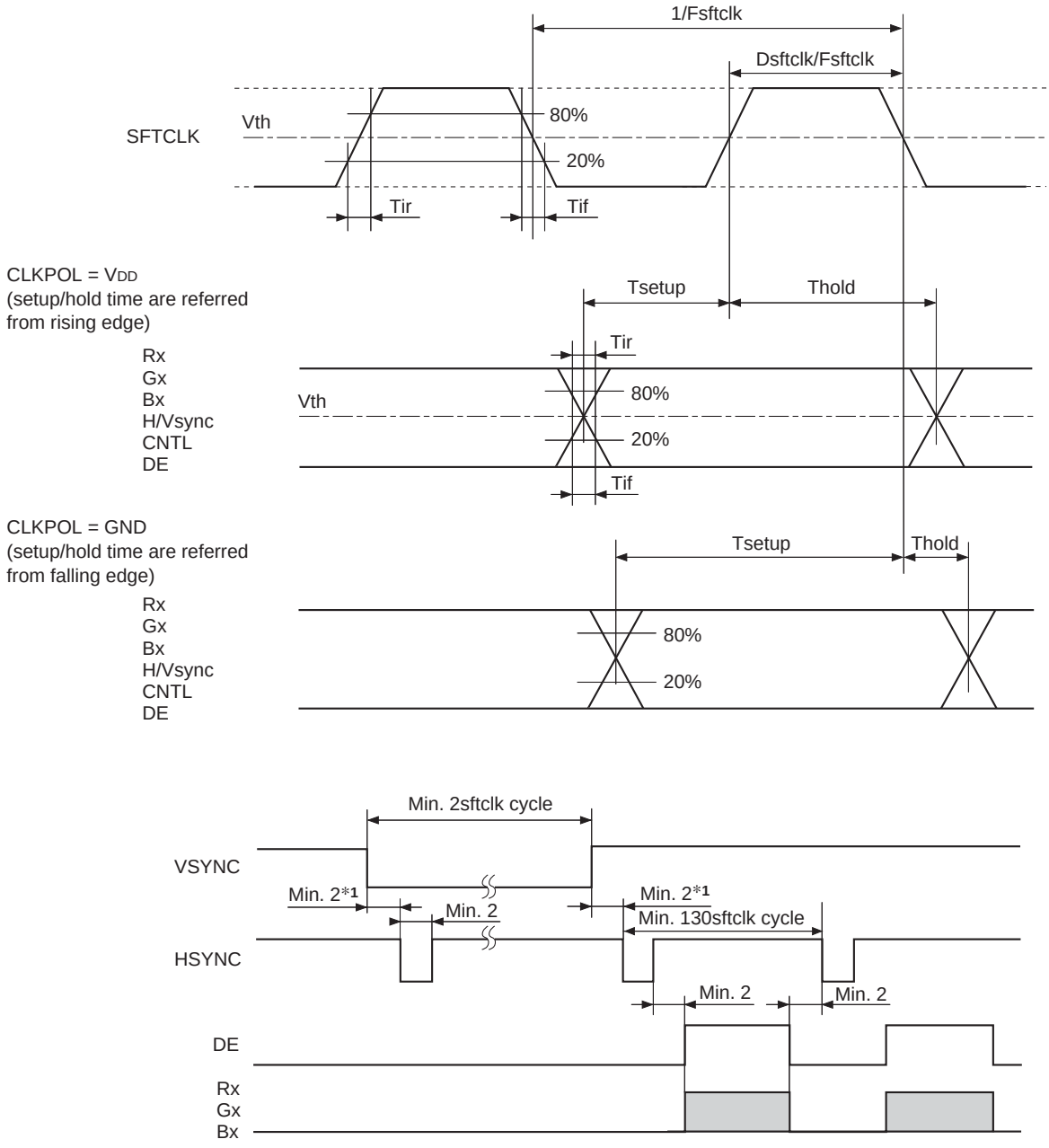


Fig. 2. SDATA Waveform Measurement

Timing Chart



*1 The edge of VSYNC and HSYNC must be apart by 2 shift-clock cycles or more. When they cannot be apart by 2 shift-clock cycles, overlap these edges. It is prohibited for correct transmission that these edges are apart by 1 shift-clock cycle.

Fig. 3. CMOS Input Timing

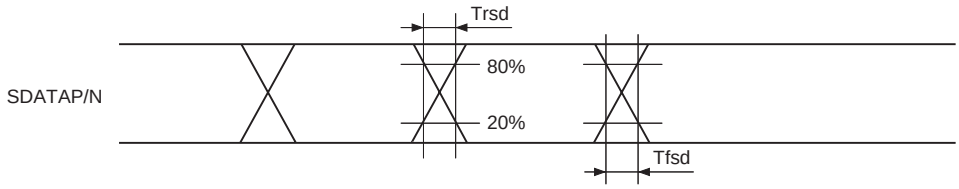


Fig. 4. Serial Data Output Timing

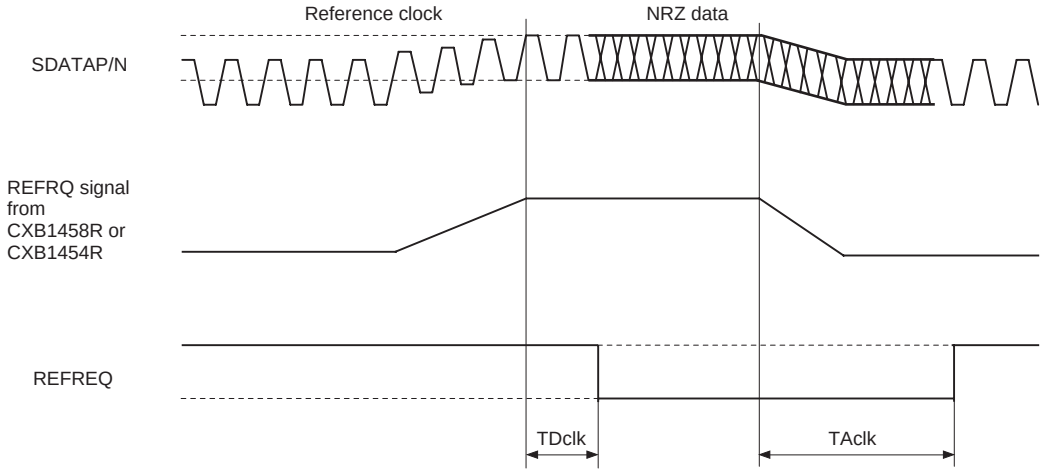


Fig. 5. Refclk Request Timing

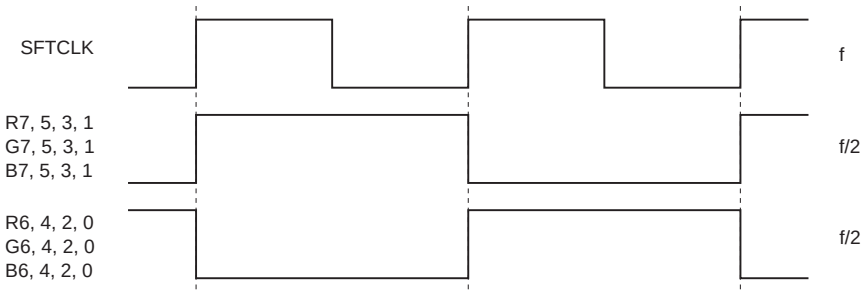


Fig. 6. Worst Case Test Pattern

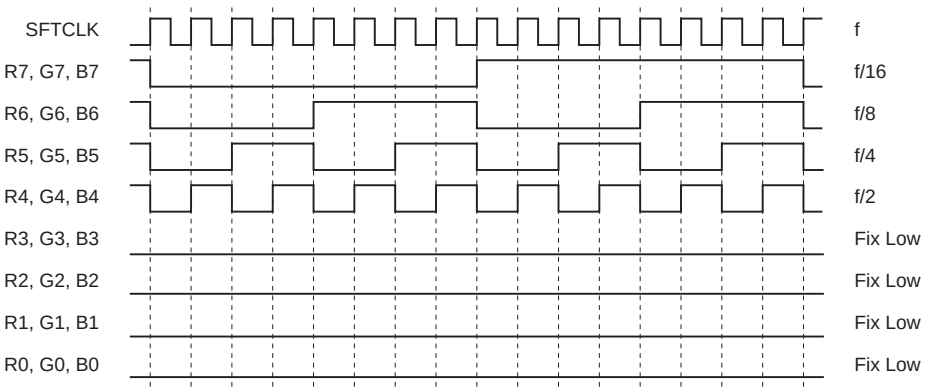


Fig. 7. 16 Gray Scale Test Pattern

CE Pin Control

The CE pin should be controlled as follows.
When the power is turned on or SFTCLK stops, or when the SFTCLK input signal falls into the disorder while the SFTCLK frequency is varied, the CE pin should be set to Low level and the CE pin should be set to High level after the SFTCLK frequency stabilizes. (See Fig. 8 and Fig. 9.)

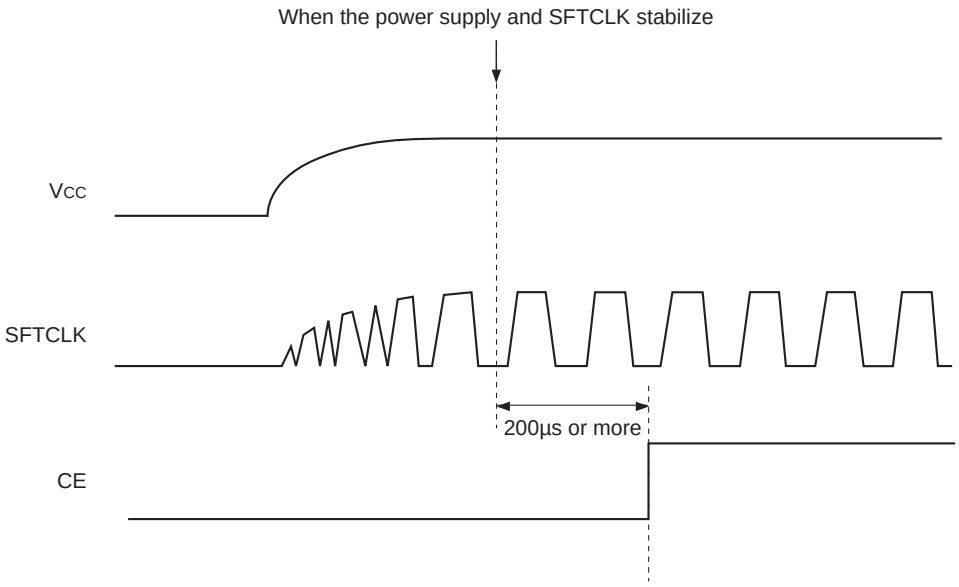
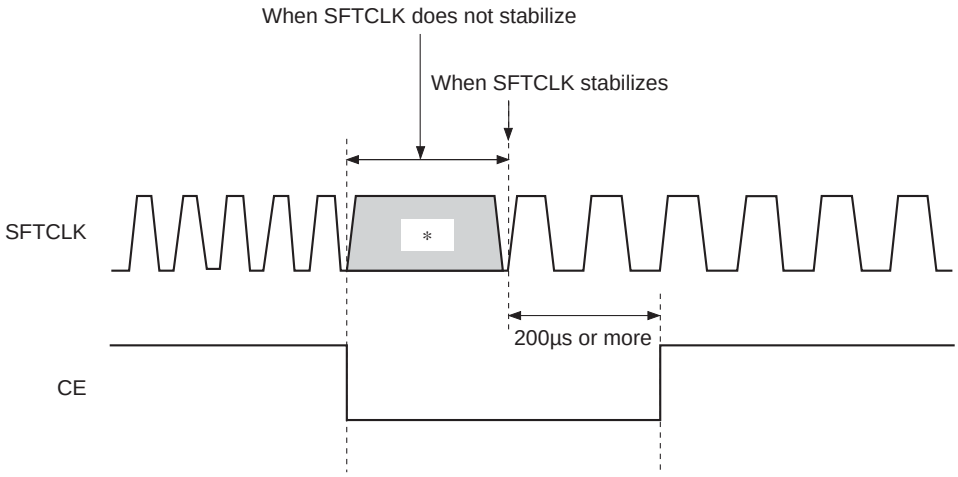


Fig. 8. CE Timing when Power Supply is Turned On



* When SFTCLK stops or the frequency of 7.6MHz or less and 42MHz or more are input.

Fig. 9. CE Timing when SFTCLK Input Signal is Not Stabilized

CKPOL Pin Control

The CKPOL pin selects the SFTCLK data sampling trigger edge. (See Table 8.)

Table 8. SFTCLK Polarity

CKPOL	SFTCLK data sampling trigger
L	Falling edge
H	Rising edge

Applications

The CXB1457R GVIF transmitter is applied to the digital RGB signal transmission for car navigation system etc. with the CXB1458R GVIF receiver.

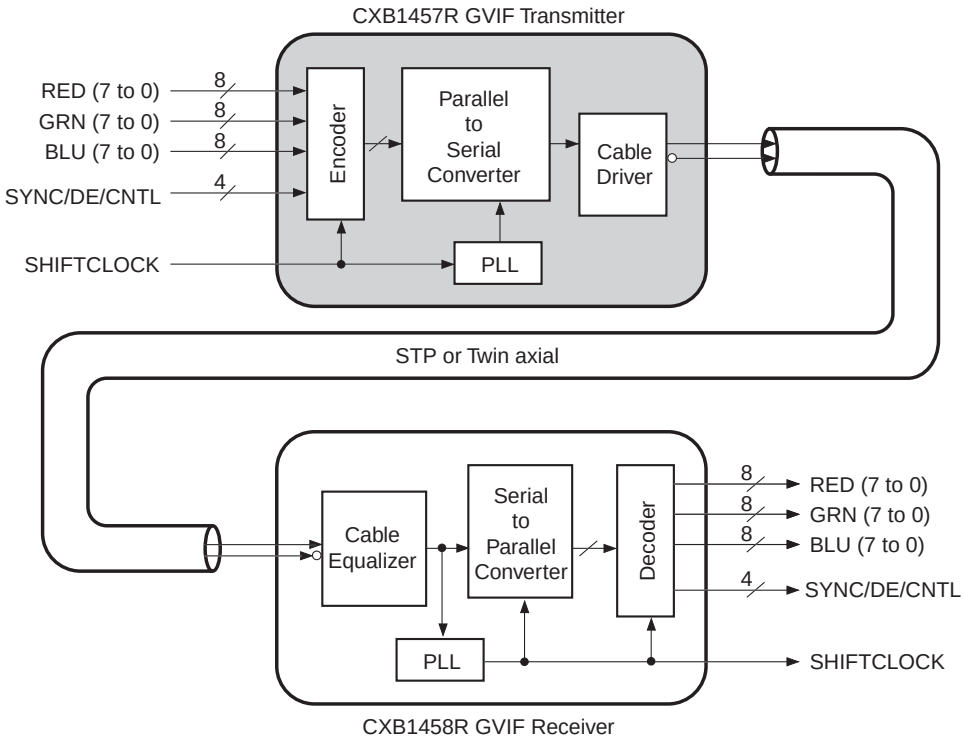
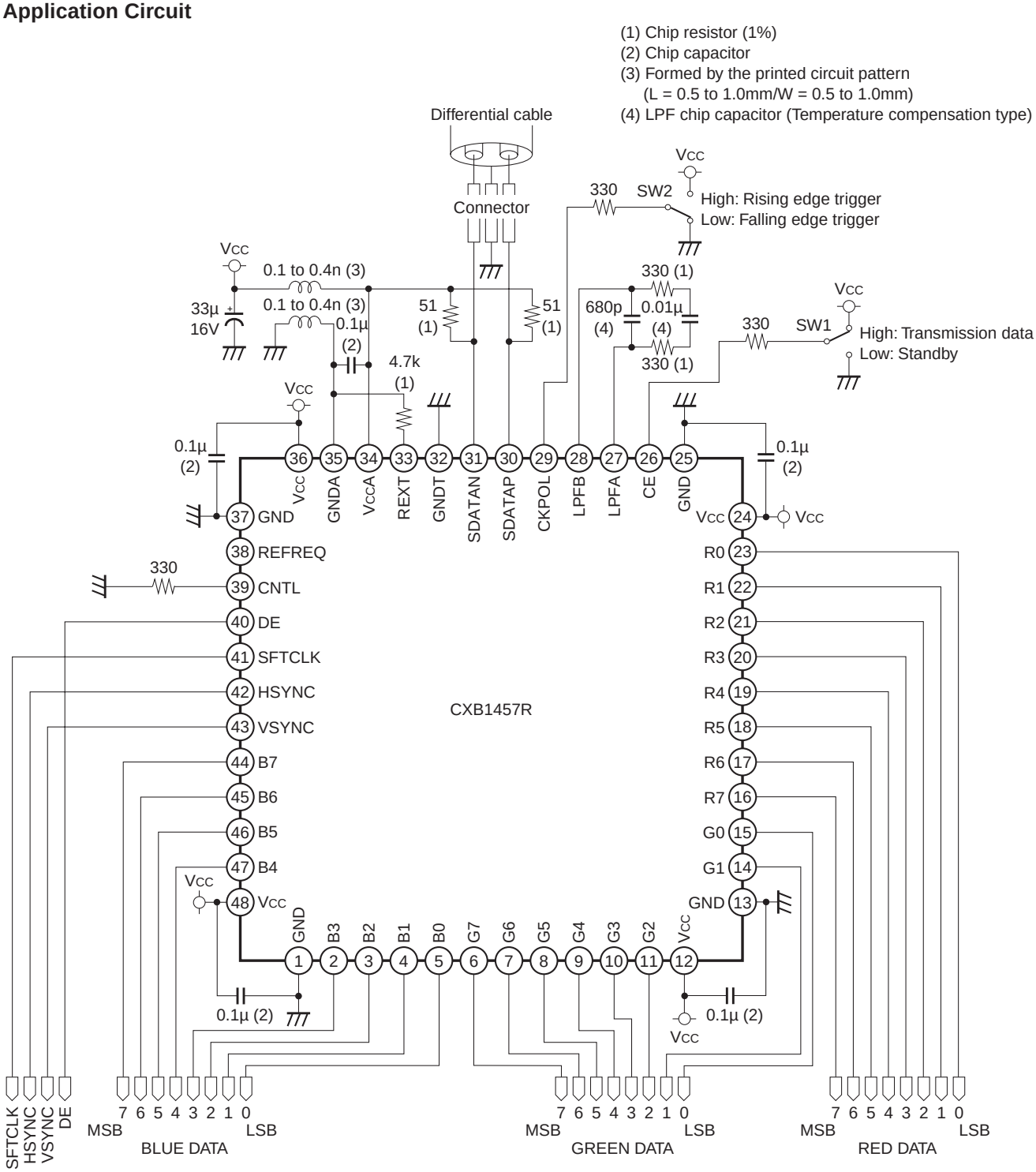


Fig. 10. Block Diagram of GVIF Transceiver Chip Set

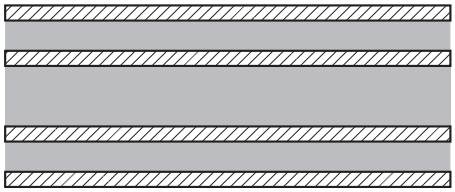
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Fig. 11. Example of Application Circuit

Recommended Printed Circuit Board Structure



L1: Cu plating (18µm) + solder coat
I1: Glass fabric base epoxy core (0.3mm)
L2: Cu plating (36µm)
I2: Glass fabric base epoxy core (0.8mm)
L3: Cu plating (36µm)
I3: Glass fabric base epoxy core (0.3mm)
L4: Cu plating (18µm) + solder coat

Fig. 12. Recommended Printed Circuit Board Pattern Structure

Recommended Printed Circuit Board Pattern

Example of power supply and special signal routing

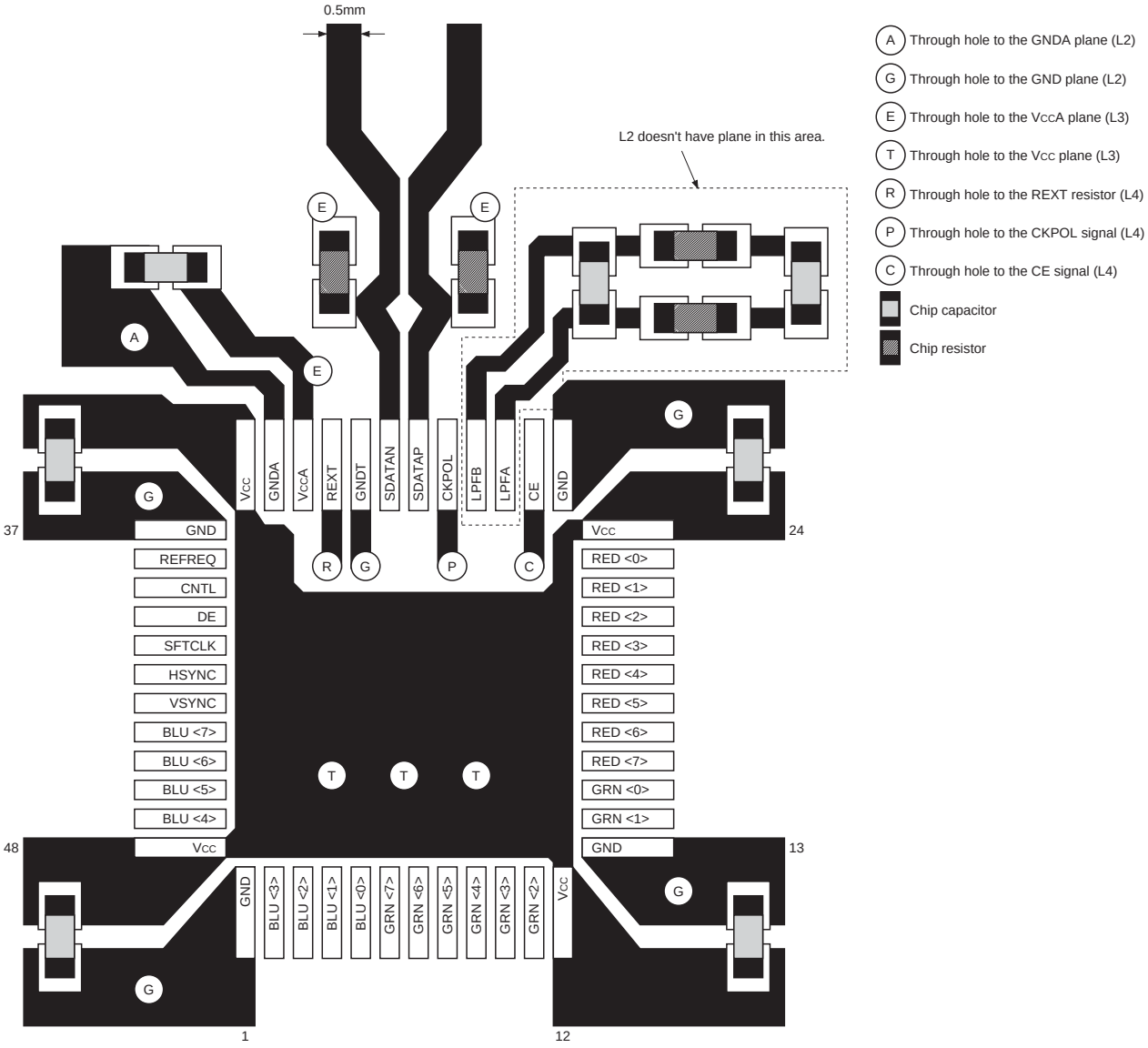


Fig. 13. Recommended Printed Circuit Board Pattern

Micro Strip Line

The CXB1457R/CXB1458R transmit maximum 1.2Gbps high-speed digital signal, so it is necessary to connect from the LSI transmission signal pins SDATAP/N to the footprint of the connector using micro strip line with the characteristic impedance 50Ω. The optimal line can be made by forming the pattern with 0.5mm width on L1 under the recommended circuit board structure. The length of the lines should be identical and through hole should not be used. L2 is recommended as the whole ground plane.

Terminators

Terminators (51Ω resistor) should be located as close to the LSI as possible.

Filter Devices and Reference Resistors

Capacitors and resistors which are connected to LPFA/B and REXT are PLL loop filters and reference resistors. Locate them close to the LSI. The L2 GND plane under these elements and lines should be removed for decreasing the parasitic capacitance.

Bypass Capacitors

Locate the 0.1µF chip capacitor as close to the pins as possible as shown in the recommended circuit.

Notes on Transmission System Configuration

The GVIF system uses terminators at both the transmitter and receiver ends, a built-in cable equalizer and a small amplitude differential transmission signal in order to solve the problems of high-speed data transmission such as signal reflection and attenuation of signal level and EMI.
In order to solve these problems completely, however, some care should be taken about the entire transmission system shown in the figure below.

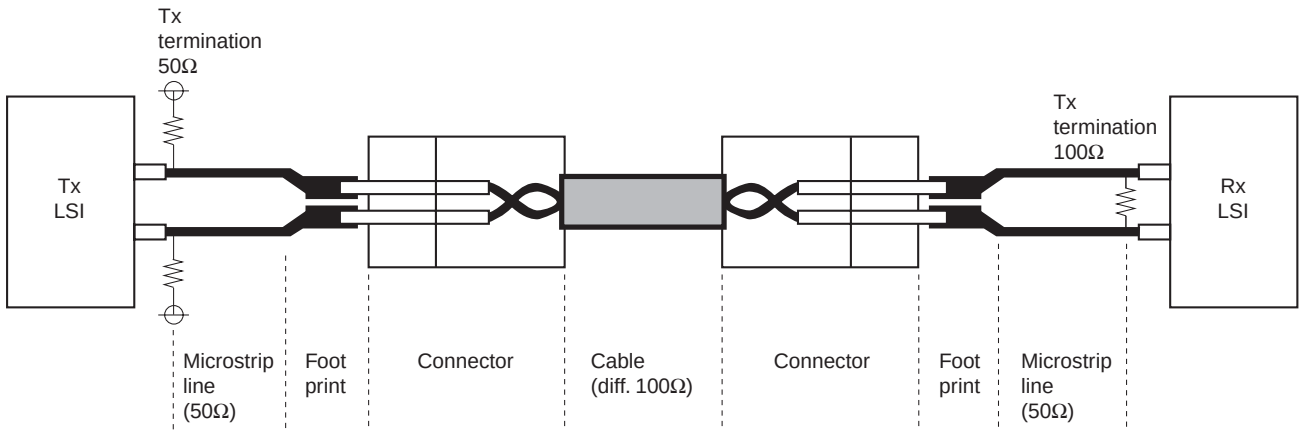


Fig. 14. Example of Transmission System Configuration

The following four items should be required for transmission system.

- Good impedance matching (less reflection)
  Differential impedance should be fit to the recommended template on the next page.
- Cable loss should be small and the loss curve should be smooth
  Maximum cable-loss should be less than 15dB at 1GHz (conforming to $\sqrt{f}$ atttenuation).
  See the next page.
- Skew of POS/NEG (differential serial data) should be small
  24% or less of 1-bit time in SVGA or 30% or less of 1-bit time in EGA, VGA and WVGA is recommended.
  1250ps @EGA (8MHz) 400ps @VGA (25MHz)
  303ps @WVGA (33MHz) 200ps @SVGA (40MHz)
- Good EMI characteristics

In order to satisfy these items, the followings are effective.

- Use the differential cable which provides high accuracy impedance, low loss and low skew matching.
  A shielded twisted pair (STP) cable is recommended.
- Use low reflectance connectors.
- Take care for the connector pin assignment.
  Select pins which do not cause interference with other signals and make both positive and negative signals equal length wiring on the board.
- Use a double shielded structure cable.

Recommended Transmission Path: Differential Impedance Template

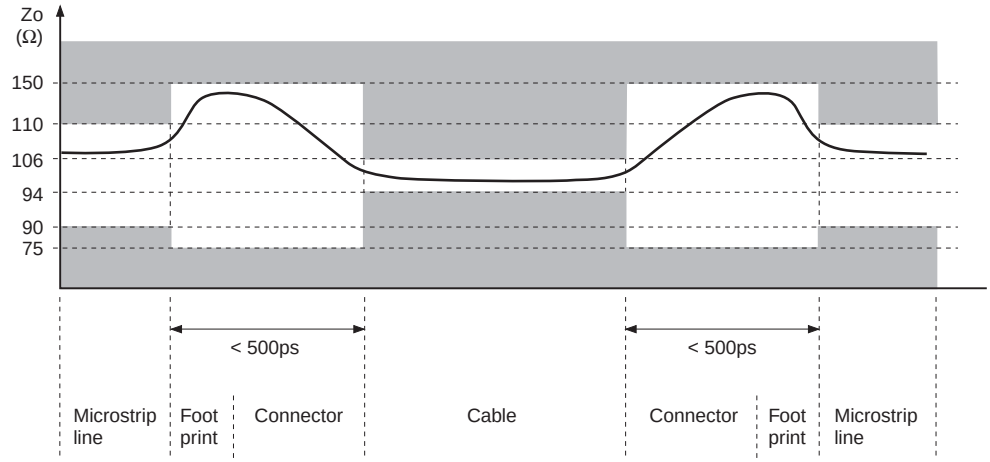


Fig. 15. Recommended Transmission Path: Example of Differential Impedance Template

Recommended Transmission Path: Attenuation Characteristics

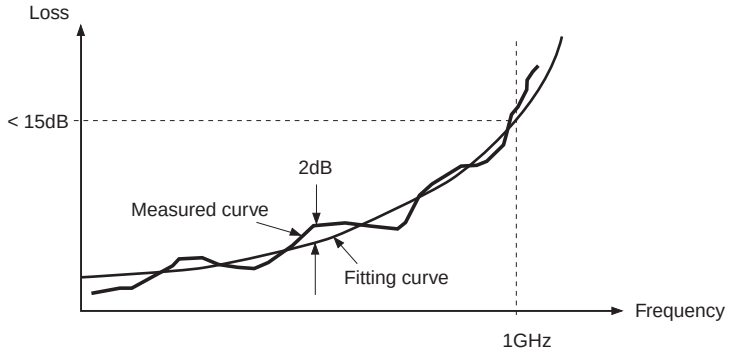


Fig. 16. Recommended Transmission Path: Example of Attenuation Characteristics

Example of Representative Characteristics

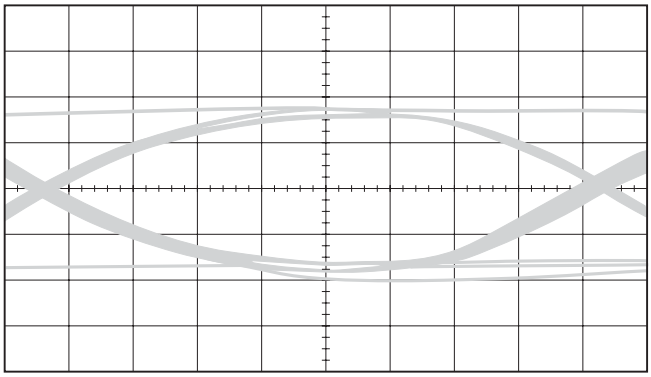
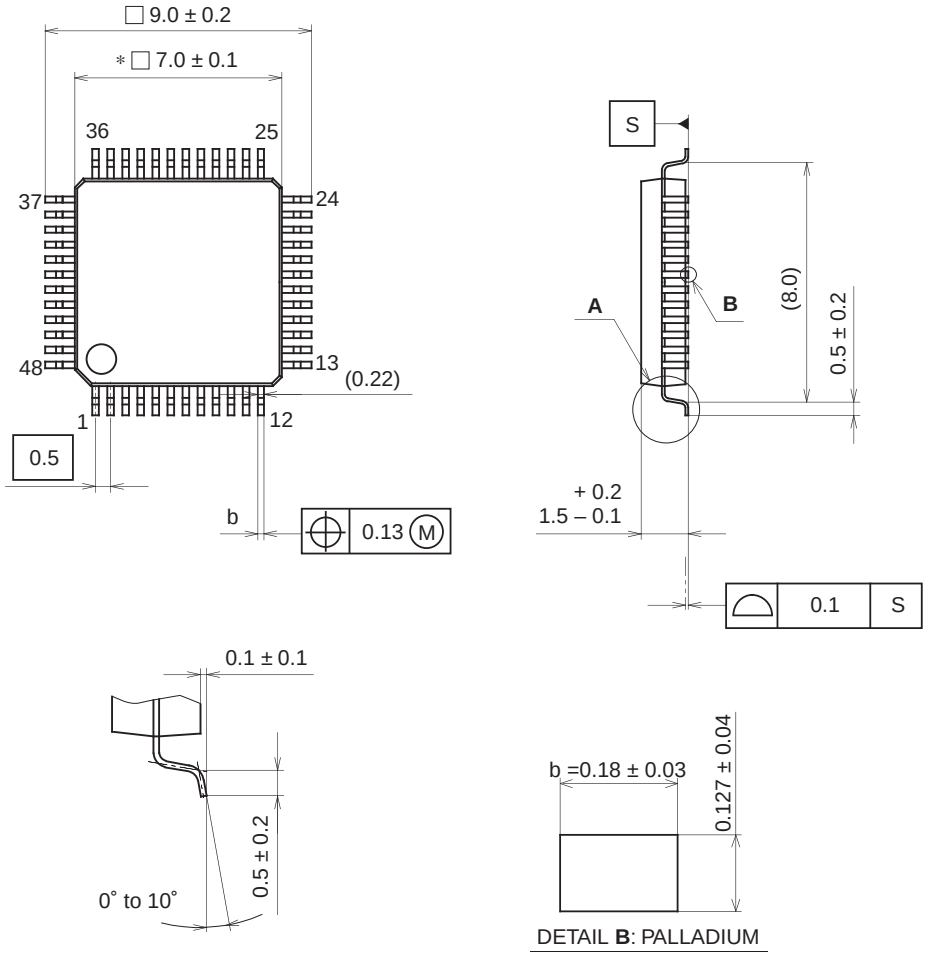


Fig. 17. 1.2Gbps SDATA Output Waveform (SFTCLK: 40MHz)

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g