SONY

CXA3304N

IF IC for ETC

Description

The CXA3304N is an IF signal processing IC for the ETC car-mounted system which employs the newest bipolar process.

Features

- Low current consumption 7.8 mA (typ. at V_{CC}=3.0 V)
- Small package 16-pin SSOP
- 40 MHz IF amplifier
- RSSI function
- RSSI buffer
- Peak hold circuit for carrier detection
- Comparator for carrier detection
- Comparator for data output waveform shaping
- Sleep mode supported

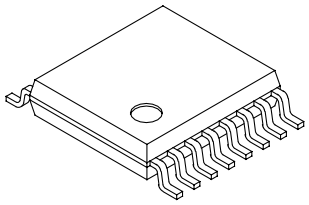
Application

ETC car-mounted system

Structure

Bipolar silicon monolithic IC

16 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

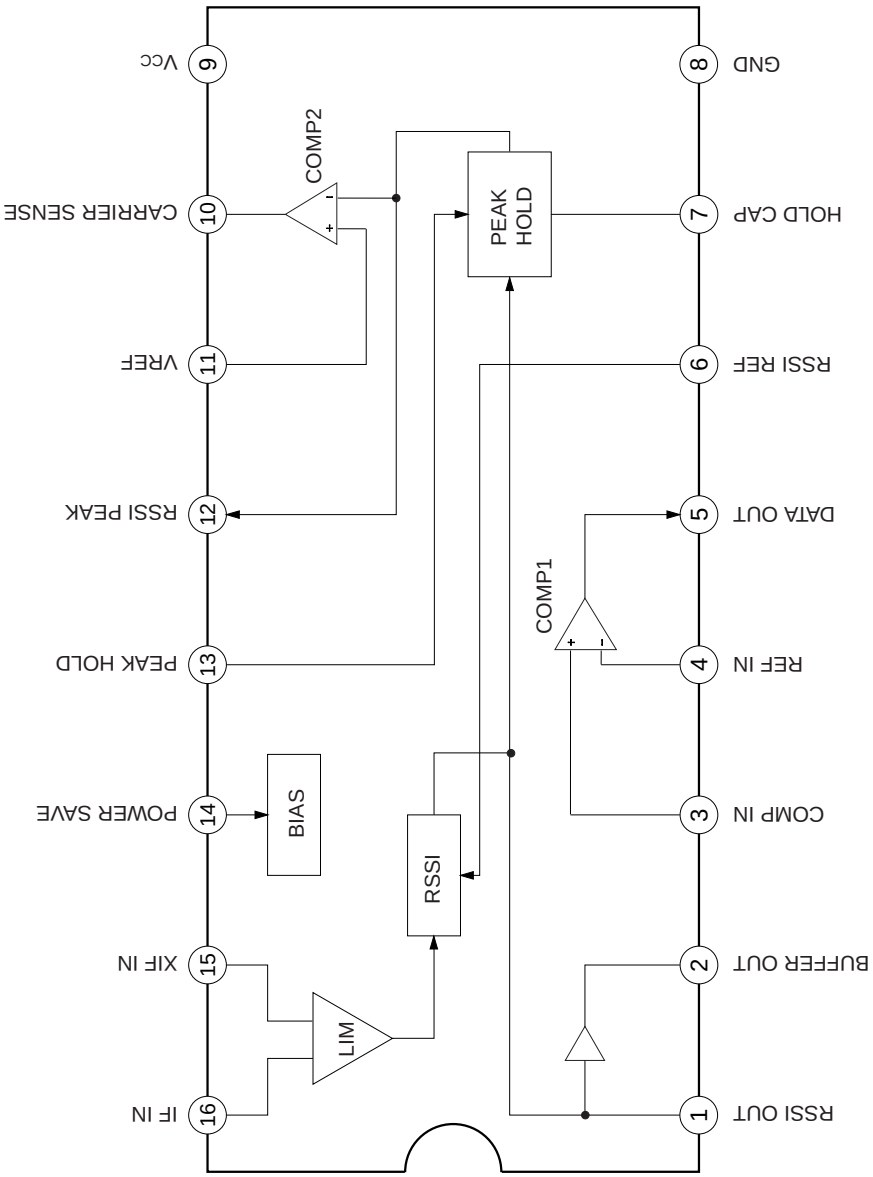
• Supply voltage	V_{CC}	14.0	V
• Operating temperature	Topr	–30 to +100	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	300	mW

Operating Condition

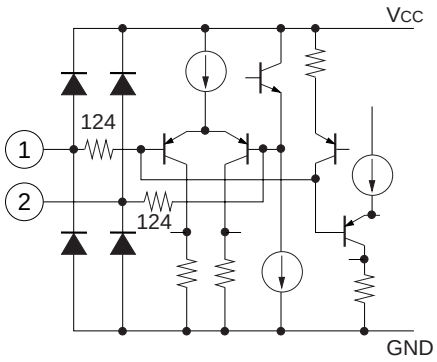
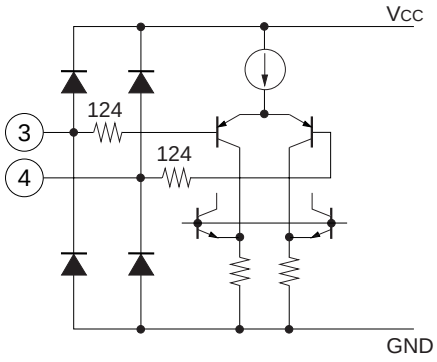
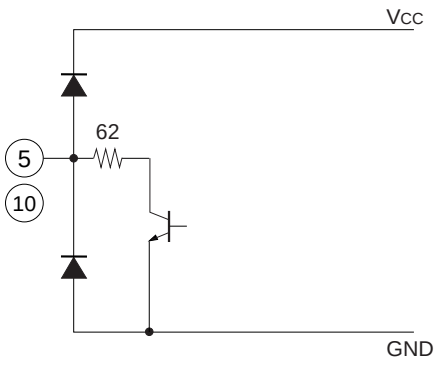
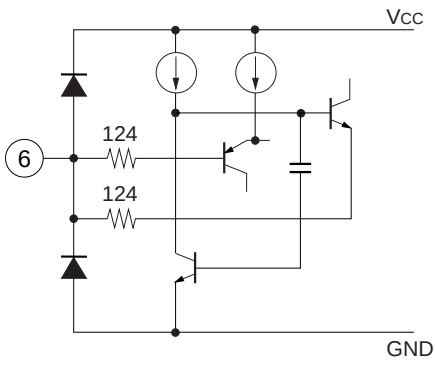
Supply voltage	V_{CC}	2.5 to 5.5	V

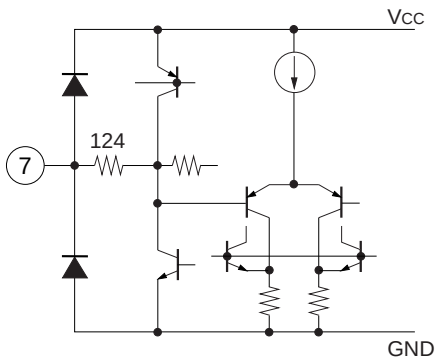
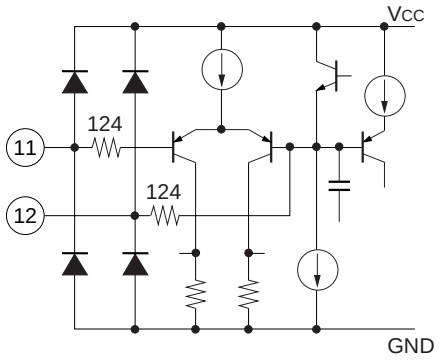
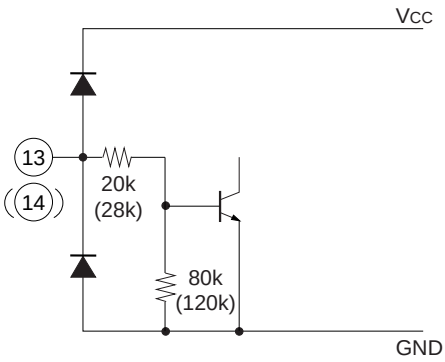
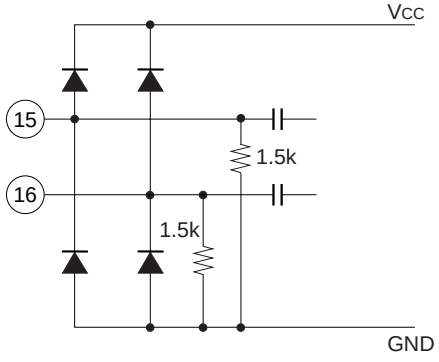
E98X40-TE

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	RSSI OUT	—		RSSI output and RSSI buffer input. The current output is converted to the voltage and it undergoes the waveform shaping by the external resistor and capacitor. The input/output voltage range is between 0.2 V to 1.4 V.
2	BUFFER OUT	—		Buffer output which outputs the RSSI voltage.
3	COMP IN	—		Comparator input.
4	REF IN	—		Comparator reference voltage input.
5 10	DATA OUT CARRIER SENSE	—		Comparator output. Open collector.
6	RSSI REF	0.2 V		Connects the resistor which determines the output current characteristics for the RSSI circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	HOLD CAP	—		Connects the external capacitor which determines the peak hold time constant. The bias current of the internal buffer circuit flows even in hold mode.
8	GND	—		Ground.
9	Vcc	—		Vcc.
11	VREF	—		Input of voltage which is the threshold value of the carrier sense comparator.
12	RSSI PEAK	—		RSSI peak voltage output. This is also connected to the input pin for the carrier sense comparator.
13	PEAK HOLD	—		Peak hold circuit control. Peak hold for low; reset operation for high.
14	POWER SAVE	—		Power saving control. Sleep mode for low; IC operation for high.
15 16	XIF IN IF IN	0 V		IF signal input. It is input with DC coupled. Input the IF signal via a matching circuit.

Electrical Characteristics (V_{CC}=3 V, Ta=25 °C)

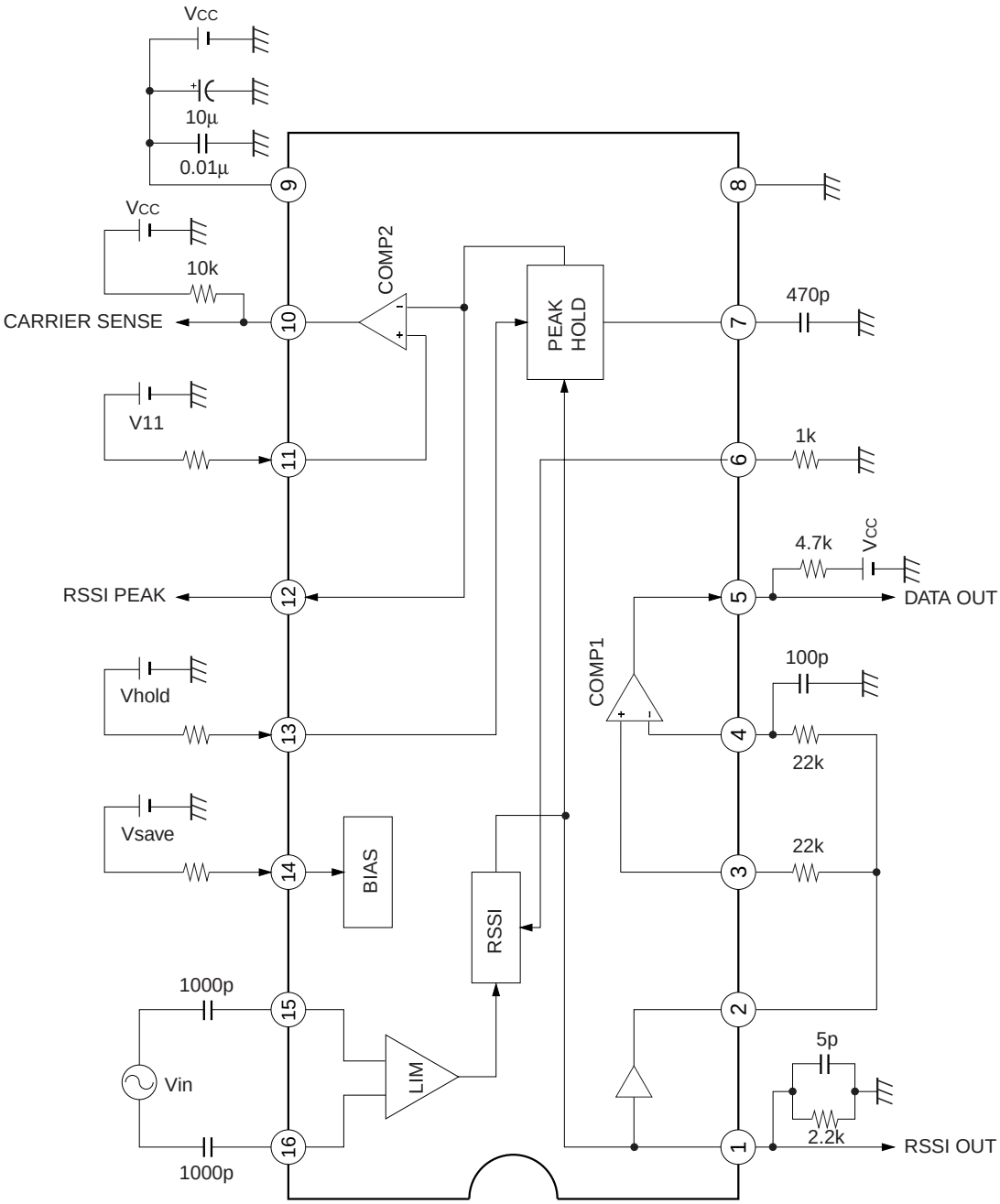
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Vin=0 V, Pin 9 current	5.5	7.8	10	mA
Current consumption	I_{CCS}	V14=0 V, Pin 9 current	—	33	100	µA
Logic input voltage high level	Vth	—	1	—	V_{CC}	V
Logic input voltage low level	Vtl	—	0	—	0.35	V
IF limiter input resistance	Rif	DC voltage	1.2	1.5	1.8	kΩ
Comparator 1 output saturation voltage	Vst1	I5=640 µA, V3=0.16 V, V4=0.2 V	—	0.15	0.4	V
Comparator 1 output leak current	Icl1	V5=3 V, V3=0.24 V, V4=0.2 V	—	0	5	µA
Comparator 1 output current	Io1	V5=0.4 V, V3=0.16 V, V4=0.2 V	640	—	—	µA
Comparator 2 output saturation voltage	Vst2	I10=300 µA, V11=0.2 V, V7=0.24 V	—	0.1	0.4	V
Comparator 2 output leak current	Icl2	V10=3 V, V11=0.2 V, V7=0.16 V	—	0	5	µA
Comparator 2 output current	Io2	V10=0.4 V, V11=0.2 V, V7=0.24 V	300	—	—	µA
RSSI output voltage 1	Vr1	Vin=–67 dBm, 40 MHz	0.2	0.35	0.5	V
RSSI output voltage 2	Vr2	Vin=–47 dBm, 40 MHz	0.61	0.81	1.01	V
RSSI output voltage 3	Vr3	Vin=–17 dBm, 40 MHz	1.1	1.35	1.655	V
RSSI buffer output current +	Irs +	V1=1.4 V, V2=0.2 V	100	—	—	µA
RSSI buffer output current –	Irs –	V1=0 V, V2=1.4 V	100	130	—	µA
Peak hold leak current	Ipl	V13=0 V, V1=0.2 V, V7=1.4 V Pin 7 current	—	0.05	5	µA
Peak hold charge current	Ipc	V13=0 V, V7=0.2 V, V1=1.4 V Pin 7 current	100	220	—	µA
Peak hold discharge current	Ipd	V7=1.4 V Pin 7 current	100	180	—	µA
Pin 11 input current	I11	V11=0, V7=1.4 V	—	0.5	50	µA
Pin 13 input current	I13	—	—	17	50	µA
Pin 14 input current	I14	V14= 1 V	—	11	50	µA

Unless otherwise specified, V14=3 V, V13=3 V and V11=3 V.

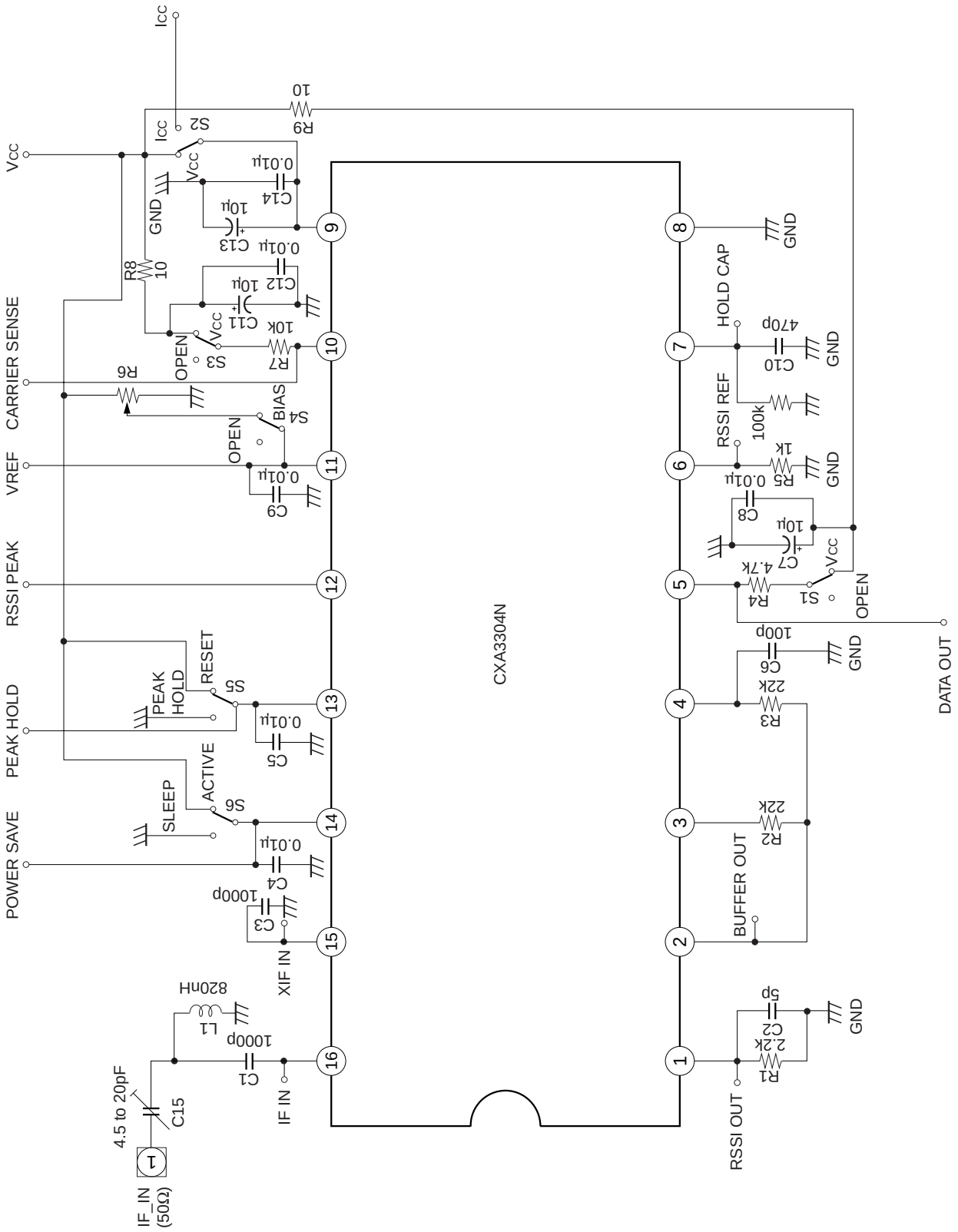
Pin condition Example) V13 : Pin 13 voltage, I5 : Pin 5 current

The external constant is the value shown in the Application Circuit.

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1) Power supply

This IC has a built-in regulator and is designed for stable operation over a wide range of supply voltages from 2.5 to 5.5 V. Wiring to the power supply pin should be decoupled as close to the pin as possible. In addition, the Pin 9 power supply line and the power supply line connected to the comparator output pull-up resistor should be separated as necessary. The IC can also be set to sleep mode to reduce power consumption by controlling Pin 14.

Pin 14 voltage	HI	LOW
Function	IC operation mode	Sleep mode

2) Limiter amplifier

This is a differential input type limiter amplifier. The input impedance is approximately 700 Ω. Input the IF signal via a matching circuit.

3) RSSI circuit

This circuit outputs a current corresponding to the amplitude of the IF signal input to the limiter amplifier. If the IF signal is the ASK signal, demodulated output is obtained. Connect a resistor to Pin 1 to convert the voltage. Adjusting this resistance value also changes the RSSI output voltage, but the value should be set so that the output voltage is smaller than the supply voltage –1.1 V. The output current includes a component twice the IF signal frequency. Adjust the value of the Pin 1 external capacitor as necessary. Connect a resistor to Pin 6 for determining the temperature characteristics of the RSSI circuit output current.

Pin 2 is the RSSI circuit buffer output. The output range is from approximately 0.2 V to the supply voltage - 1.1 V.

4) COMP1 circuit

This is the comparator circuit for shaping the ASK demodulation signal waveform. The output is an open collector. Connect this circuit to the power supply, etc., via a pull-up resistor. Set the connected power supply to the Pin 9 potential or lower.

5) Peak hold circuit

This circuit holds the Pin 1 RSSI output voltage peak. Peak hold operation and reset operation are switched with Pin 13.

Peak hold operation

The input RSSI voltage is held by the Pin 7 capacitor. The held voltage passes through the buffer circuit and is output to Pin 12. The response characteristics during peak hold operation are determined by the peak hold charge and leak currents, which are determined inside the IC, and the Pin 7 capacitance value.
The held voltage fluctuates according to the peak hold leak current. This fluctuation becomes larger as the capacitor value is set smaller. Adjust the reset operation interval and the capacitor value as necessary. In addition, the hold time can also be shortened by connecting a resistor between Pin 7 and GND.

Reset operation

The charge held by the Pin 7 capacitor is discharged according to the peak hold discharge current which is determined inside the IC. The discharge time changes according to the capacitor value.

Pin 13 voltage	HI	LOW
Function	Reset	Peak hold

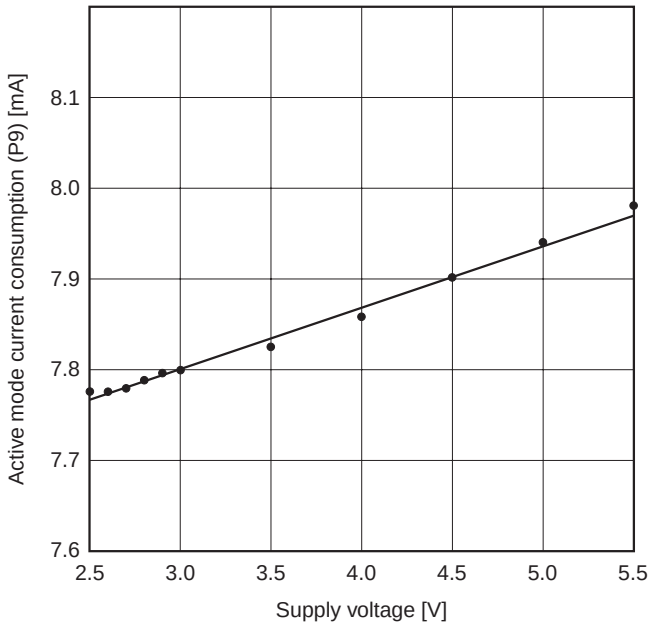
6) COMP2 circuit

This is the carrier sense comparator circuit. The input pin is connected internally to the RSSI PEAK output (Pin 12). Apply the voltage to be used as the threshold value to Pin 11. The comparator output is an open collector output, and should be connected to the power supply, etc., via a pull-up resistor. Set the connected power supply to the Pin 9 potential or lower.

Example Representative Characteristics

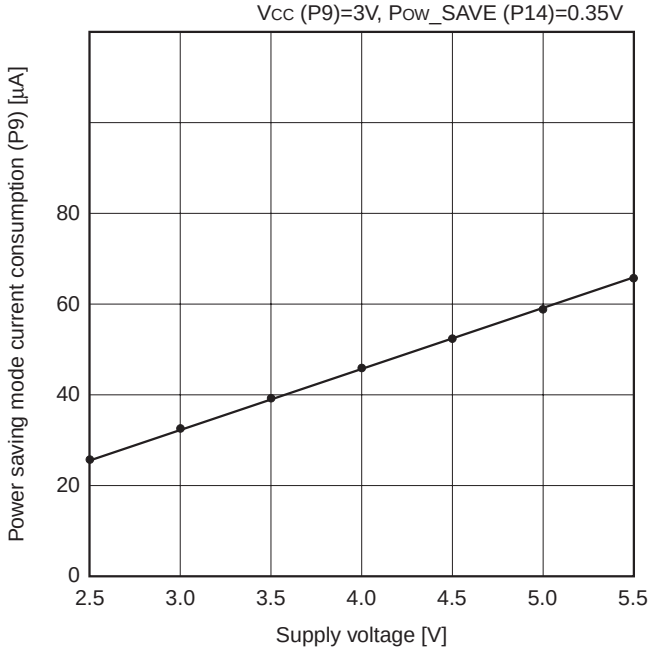
Active mode current consumption (P9)

VCC (P9)=3V, POW_SAVE (P14)=1V

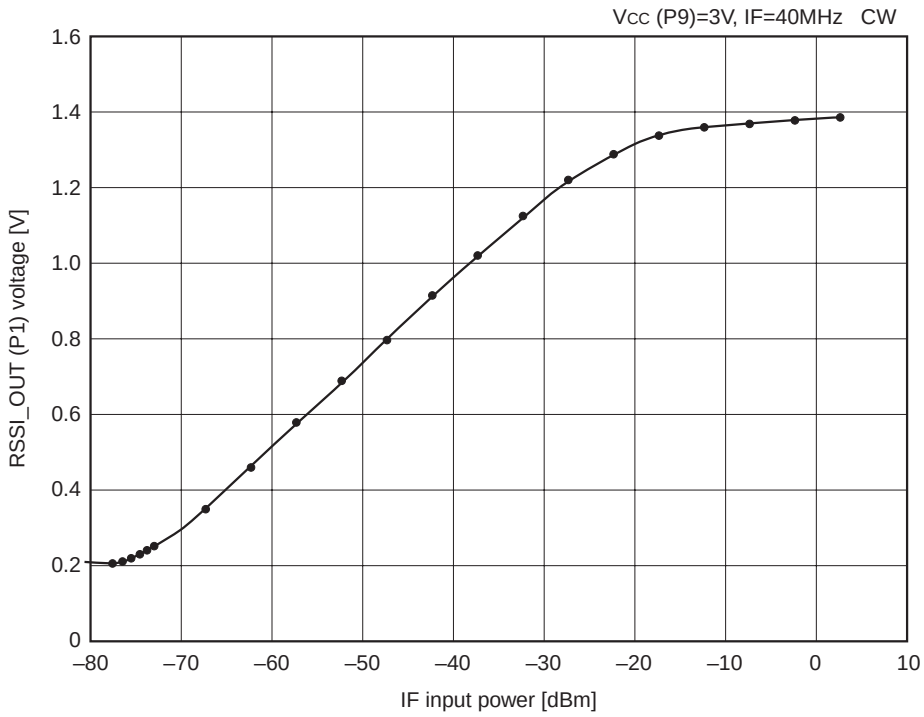


Power saving mode current consumption (P9)

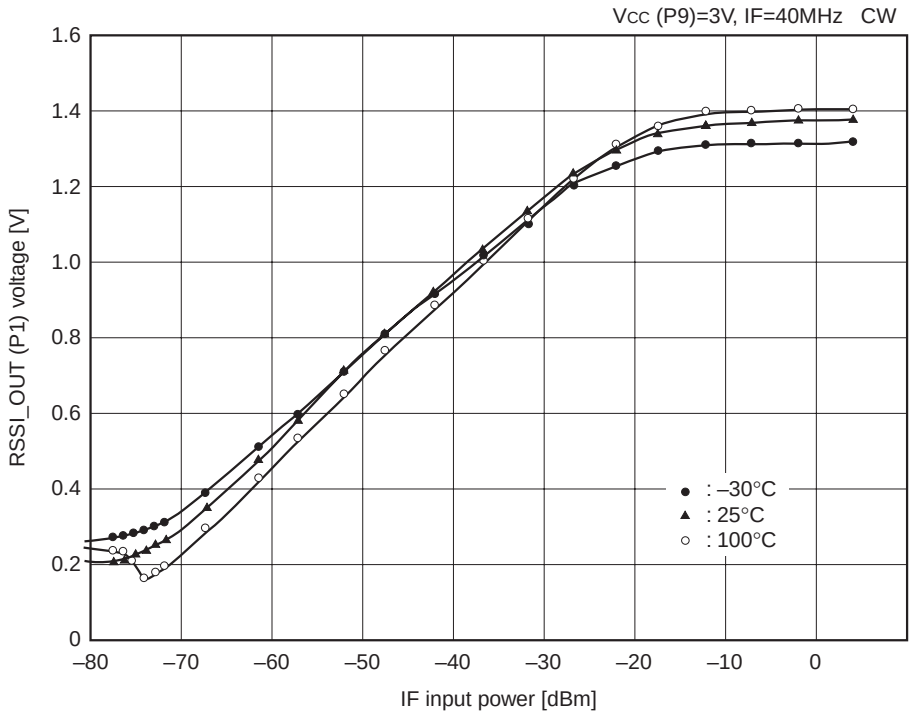
VCC (P9)=3V, POW_SAVE (P14)=0.35V



RSSI output characteristics

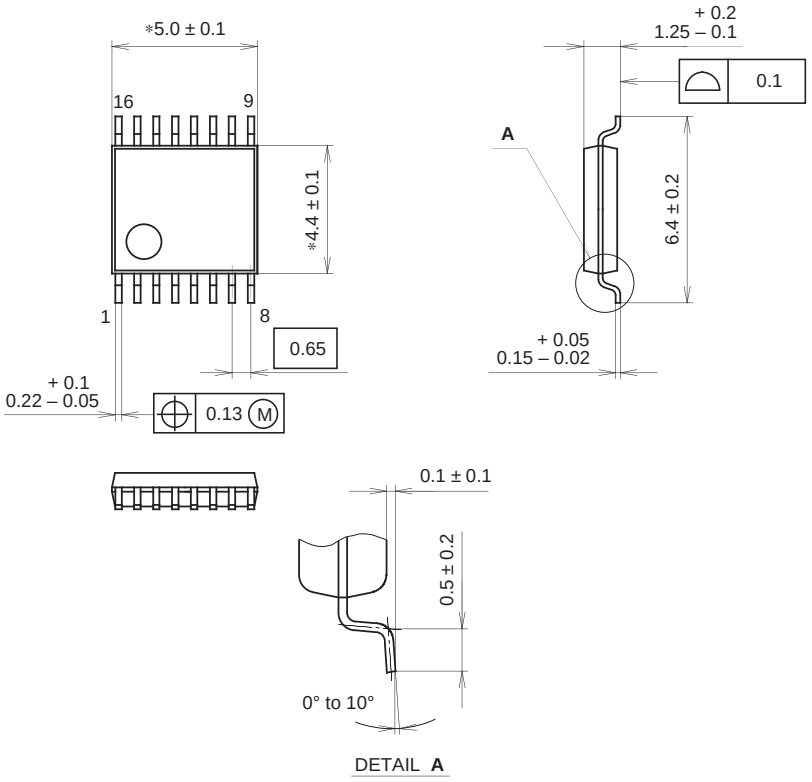


RSSI output temperature characteristics



Package Outline Unit : mm

16PIN SSOP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).