SONY

CXA1387S

Aperture Compensation for TV

Description

The CXA1387S is a bipolar IC for aperture compensation designed to improve TV picture quality.

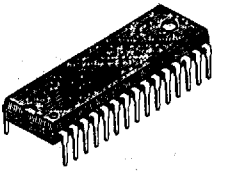
Features

- Aperture compensation using built-in delay line.
- Luminance signal coring function.
- VM (velocity modulation) signal output.
- Tracking delay for luminance signal output, VM output and Chroma signal output.
- Chroma signal image interval gain control (excluding burst signal interval).

Applications

Improvement of picture quality for TV, monitor, etc.

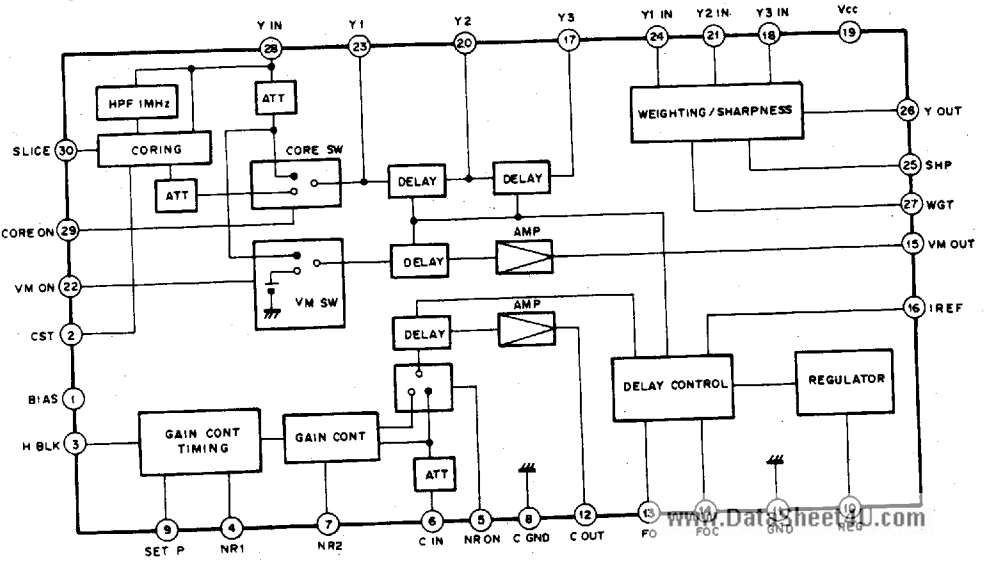
30pin SDIP (Plastic)



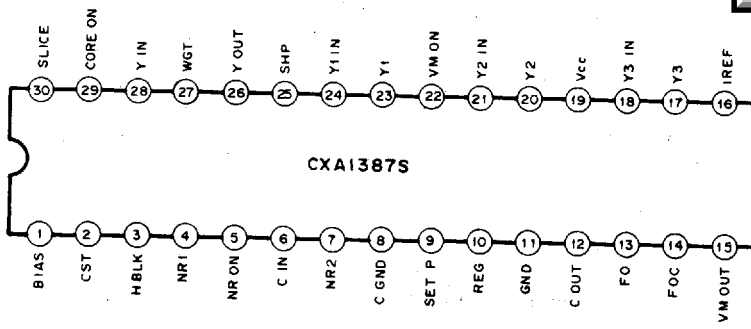
Structure

Bipolar silicon monolithic IC

Block Diagram



Pin Configuration



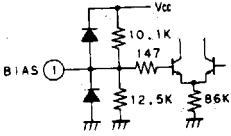
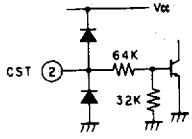
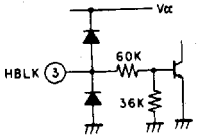
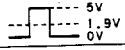
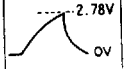
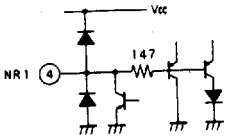
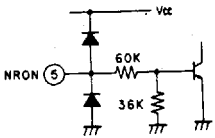
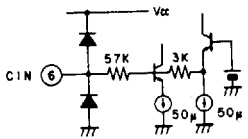
Absolute Maximum Ratings(Ta=25°C)

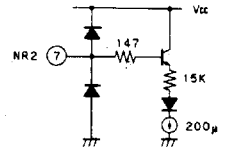
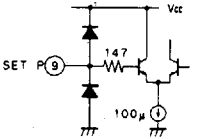
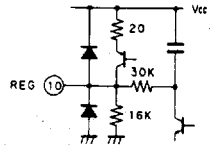
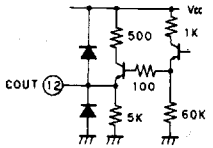
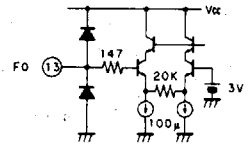
• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.35	W
• Voltage impressed to pin		−0.3 to V_{CC}+0.3	V

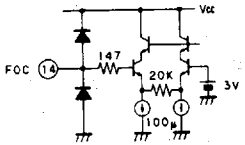
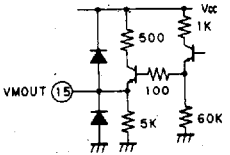
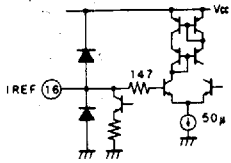
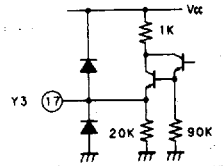
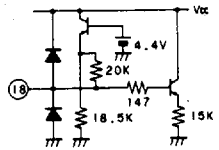
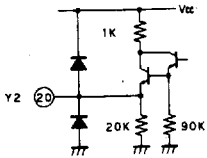
Operating Conditions

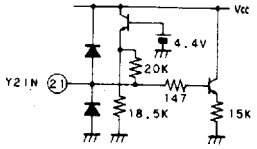
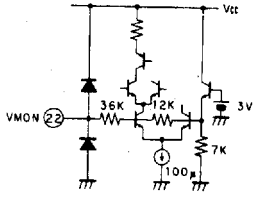
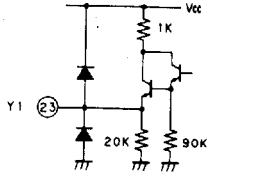
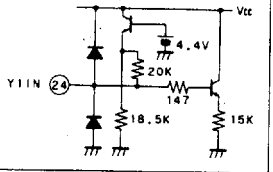
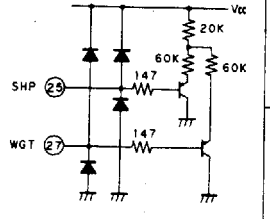
• Supply voltage	V_{CC}	8.5 to 9.5	V

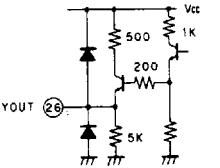
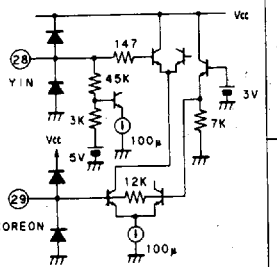
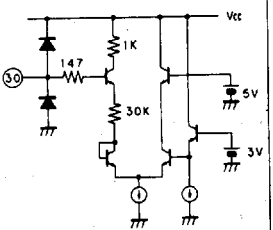
Pin Description

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
1	BIAS	5V		Bias pin used inside the IC. Connect capacitor between this and GND.
2	CST			Connect to GND.
3	HBLK			H Blanking pulse input pin. Provides the timing for gain control when CNR is ON through this HBLK pulse. 
4	NR1			Connect 5.6kΩ±1% resistance to V_{CC} and 4700pF±5% capacitor to GND.
5	NRON			Chroma signal gain control ON/OFF switchover pin. At L : Gain control OFF At H : Gain control ON
6	CIN	3V		Chroma signal input pin. Chroma signal input dynamic range within 500mVp-p. When low-frequency Y signal included, within 2Vp-p. (Max)

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
7	NR2	2 to 7V*		Gain control voltage when CNR SW is ON. 7V (Typ.) at 0dB. 2V at less than −26dB.
8	CGND			GND pin.
9	SET P			Control pin that determines the timing of periods where gain control is applied and where it is not when chroma signal gain control is ON. When this pin's voltage is set to 2.87V, gain control is not applied for approx. The 10 μsec period from the rising edge of HBLK pulse (Pin 3 input). The input of the burst signal period in the period where gain control is not applied enables color control.
10	REG	8V		Built-in constant voltage supply output pin. Connect capacitor between this and GND.
11	GND			GND pin.
12	COUT	4.4V		Chroma signal output pin.
13	FO	2 to 4V*		Delay control pin of built-in delay line. Controls Y, VM, and C signal at the same time. Raising control voltage reduces delay.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
14	FOC	2 to 4V*		Delay control pin of built-in delay line. Controls only C signal independently. Delay of Y and VM signal does not change. Control characteristics is the same as FO.
15	YMOUT	4.6V		Y signal output pin for VM control.
16	IREF	6.7V		External resistance pin for internal reference current. Connect 6.8kΩ±1% resistance between this pin and REG (Pin 10). Also, connect to GND with capacitor. See Application Circuit (P.18).
17	Y3	3.65V		Output pin for Y signal passed through 2 delay lines. Attenuated by −24.5dB compared with input.
18	Y3IN	3.7V		Input pin of signal for aperture control. Pin 17 signal (Y3) is coupled through a capacitor and input.
19	V_{CC}	9.0V*		Supply pin.
20	Y2	3.65V		Output pin of Y signal passed through one delay line. Attenuated by −24.5dB compared with input.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
21	Y2IN	3.7V		Input pin of signal for aperture control. Pin 20 signal (Y2) is coupled through a capacitor and input.
22	YMON	2.3V		VM output switchover control pin. At L : VM signal (Y signal) output. At H : No output (DC).
23	Y1	3.65V		Attenuates input Y signal by −24.5dB before output.
24	Y1IN	3.7V		Input pin of signal for aperture control. Pin 23 signal (Y1) is coupled through capacitor and input.
25	SHP	3 to 5V*		Controls preshoot and overshoot magnitude of Y output signal. At 3V : Sharpness flat } At 5V : Sharpness maximum.
27	WGT	0 to 6V*		Controls the ratio of preshoot and overshoot of Y output signal. At 0V : Only preshoot At 3V : Preshoot, Overshoot At 5V : Only overshoot.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
26	YOUT	5.0V		Y signal output pin.
28	YIN	5V		Y signal input pin. Input dynamic range at 2Vp-p (Max.)
29	COREON	2.3V		Y signal coring ON/OFF switchover pin. At L : Coring OFF At H : Coring ON
30	SLICE	1 to 6.5V*		Core level control pin when coring is ON. When voltage is set to 6.5V, controls −3dB (Typ.) at 4.5MHz.

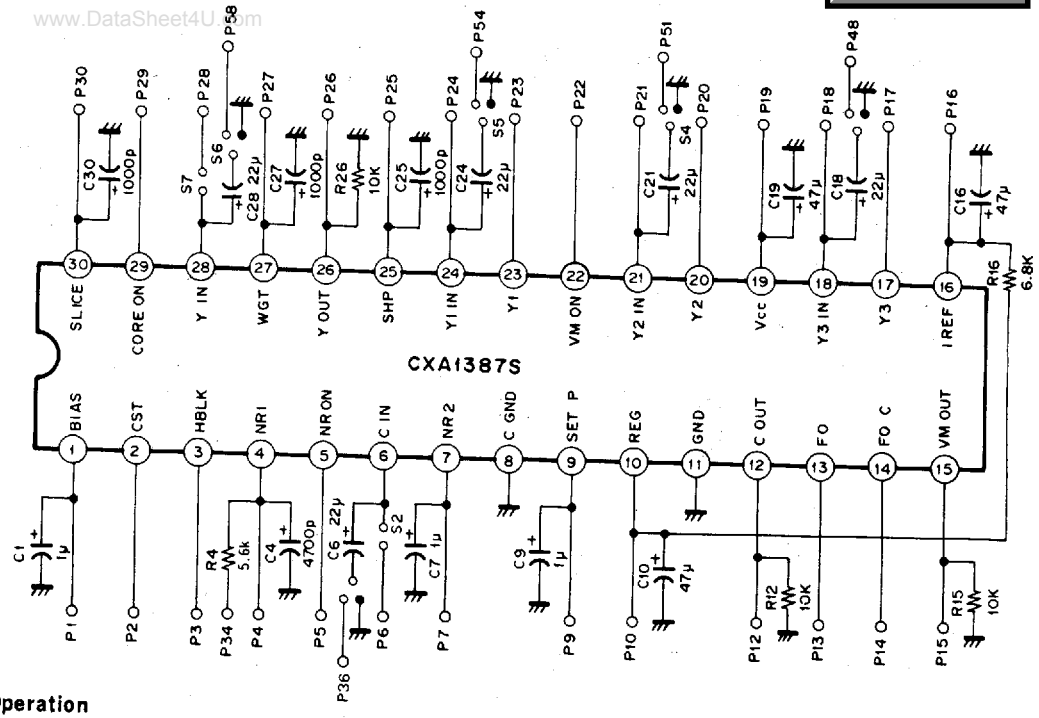
* : External applied voltage

Electrical Characteristics (T_a=25°C, V_{CC}=9.0V, See Electrical Characteristics Test Circuit, P.11)

No.	Item	Symbol	Bias condition	Switch set ON	Input point and input signal	Test point	Test contents Standard value	Min.	Typ.	Max.	Unit
1	Consumption current	I_{CC}	P13, P14, P25, P27 } 3V P19……9V			P19		20	30	40	mA
2	Constant voltage output	V_{REG1}				P10		7.70	8.00	8.30	V
3	Constat voltage output supply voltage characteris tics	dV					Output voltage fluctuation at REG (Pin 10) when 9.5V or 8.5V is applied to V_{CC} (Pin 19). Ref. voltage at 9.0V)	−10	0	10	mV
4	Chroma level	CG		S1	3.58MHz 500mVp-p Sine wave at Pin 36.	P12	Gain tested.	−3.0	−1.5	0.0	dB
5	Y output level	YG	P13,P14 P25, P27 } 3V P19……9V P22……GND P29……GND	S6	1MHz 2.0Vp-p Sine wave at Pin 58.	P26	Signal output from Y2 (Pin 20) is input to Y2 IN and the gain from Y out (Pin 26) output is tested.	−2.0	−0.5	1.0	dB
6	Y signal frequency characteris tics.	Yf			8MHz 2.0Vp-p Sine wave at Pin 58.		Gain difference between f=1MHz and F=8MHz. (Sharpness center)	−6.0	−3.0	0.0	dB
7	VM output level	VMG			1MHz 2.0Vp-p Sine wave at Pin 58.	P15	Gain tested.	−2.0	−1.0	0.0	dB
8	Y coring	COR	P13,P14 P25, P27 } 3V P22……3V P29……3V P19……9V		4.5MHz 400mVp-p Sine wave at Pin 58.	P23	Output gain difference when the voltage at Pin 30 is varied from 1V to 6.5V.	−10.0	−6.0	−2.0	dB
9	Maximum delay time	DL_{max}	P13……2V P14,P25 P27 } 3V P22……GND P29……GND P19……9V		1MH 2Vp-p Sine wave at Pin 58.	P20	Output delay time in relation to the input. Difference in delay time Input P58 — AC 0 Output P20 — AC 0	220	270		ns
10	Minimum delay time	DL_{min}	P13……4V P14,P25 P27 } 3V P22……GND P29……GND P19……9V						120	160	ns
11	Aperture level	AP1	P13, P14 P27 } 3V P25……5V P22……GND P29……GND P19……9V	S3, S4, S5	P54 : Y1 P51 : Y2 P48 : Y3	P26	Input Y1, Y2, Y3 Output V1, V2, V3, V4 100mVpp 15.75kHz duty 50%	430	530	630	mV
12	Maximum preshoot	PR_{max}	P13, P14…3V P27……0V P25……5V P22……GND P29……GND P19……9V				Output V1, V3	900	1000	1100	mV
13	Maximum overshoot	OV_{max}	P13, P14…3V P27……6V P25……5V P22……GND P29……GND P19……9V				Output V2, V4	950	1100	1200	mV

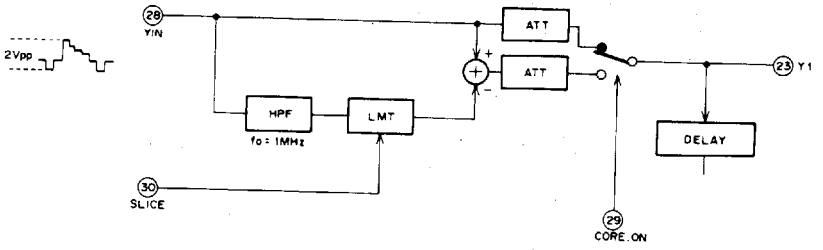
No.	Item	Symbol	Bias condition	Switch set ON	Input point and input signal	Test point	Test contents Standard value	Min.	Typ.	Max.	Unit
14	VM switch threshold level	V_{VM}					Threshold level when VM is ON/OFF. At L : VM ON At H : VM OFF	2.0	2.2	2.4	V
15	Coring switch threshold level	V_{COR}					Threshold level when coring is ON/OFF. AT L : Coring OFF AT H : Coring ON	2.0	2.2	2.4	V
16	CNR switch threshold level	V_{CNR}					Threshold level when CNR is ON/OFF. At L : CNR OFF At H : CNR ON	1.5	2.0	2.5	V
17	CNR ON time	T_{CNR}	P13, P14, P25, P27 } 3V P22,P29···GND P19, P34···9V P9·····2.78V		P3 5μ 3V OV f=15.75kHz	P4	Input signal 5μsec P3 3V OV f=15.75kHz Output waveforms P4 t ● t time is tested. ※ Time here is when CNR is ON and when gain control of the chroma signal is not applied.	9.7	10.0	10.3	μs
18	CNR offset	CNOS				P12	Input signal 5μsec P3 H.BLK 3V OV f=15.75kHz Output waveforms P12 C.OUT V ● Test electric potential gradient V. ※ Offset voltage when gain control is applied in the chroma signal and when it is not with CNR ON.	0	150	600	mV
19	Chroma gain control	CNR	P13, P14, P25, P27 } 3V P19,P34···9V P5·····3V P7·····2V	S1	P36 3.58MHz 500mVp-p		Gain between input and output is tested.			−26	dB

Electrical Characteristics Test Circuit

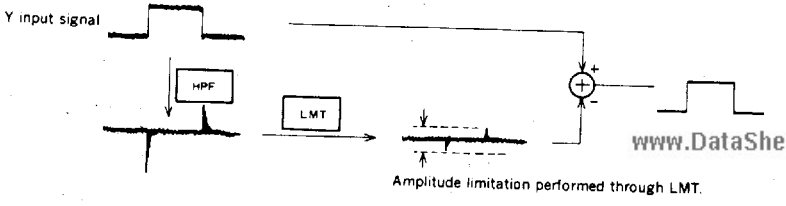


Operation

1. Y coring



As shown in the above diagram, Y signal is passed through HPF, amplitude limitation is performed and the result substracted from the original signal to execute Y signal coring.



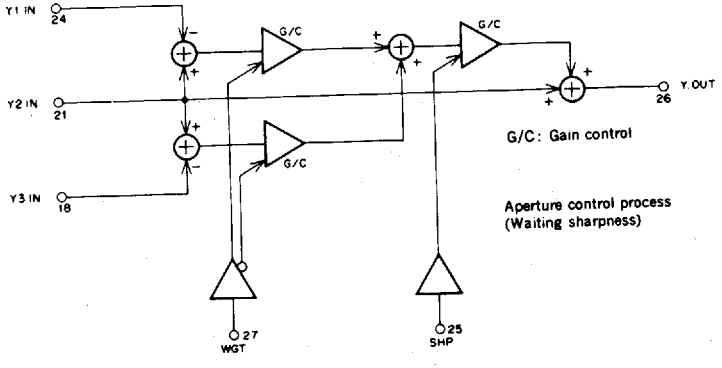
Cut off frequency of the HPF (high pass filter) used for coring stands at approx. 1MHz (Typ.). The amplitude limiting range of the limiter stands within 0 to 400mV (Typ.). Control is performed through Pin 30 (SLICE).

- Raising the voltage of Pin 30 (SLICE) raises the limiter level and coring effect is more amply expressed.
- Coring is controlled through Pin 29. At L level, coring is OFF and at H, it is ON. At this threshold level, this pin is biased.

2. Aperture control

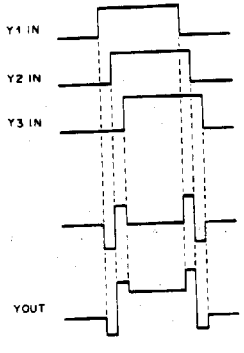
Y signal is attenuated by approx. −24.5dB passing through the coring (process) circuit to be output from Pin 23 as Y1 output. Y1 output passes through one built-in delay line to be output as Y2 output from Pin 20. Then Y2 output passes through still another delay line to be output as Y3 output from Pin 17. (See Block Diagram, P.4)

These three outputs (Y1, Y2, and Y3) are input to Pins 24 (Y1IN), 21 (Y2IN), and Pin 18 (Y3IN) through capacity coupling to start aperture control process.



Aperture control process controls preshoot/overshoot ratio through WGT pin (Pin 27) and sharpness level through SHP pin (Pin 25) respectively. This control process is indicated on the above diagram.

The basic principle of delay line aperture control is shown on the below diagram.

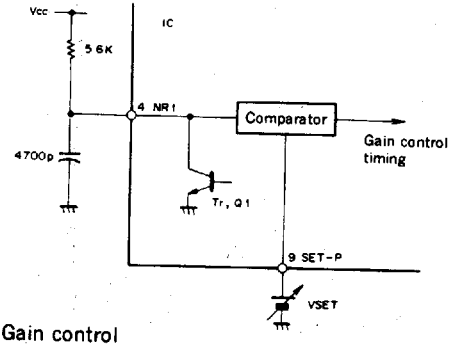


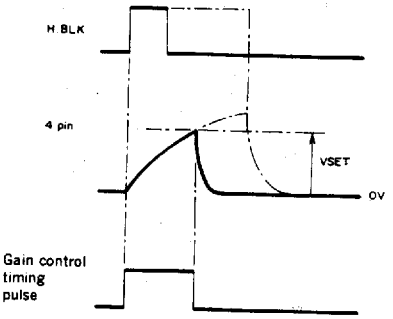
3. Chroma signal gain control

When CNR is ON, chroma signal gain control in executed at a timing other than that of burst signal. As a result, chroma signal is restrained and pales. In signals with numerous noise components, this gain control pales color to reduce conspicuous color noise and evenly distribute CNR (chroma noise reduction) effects.

(1) Timing

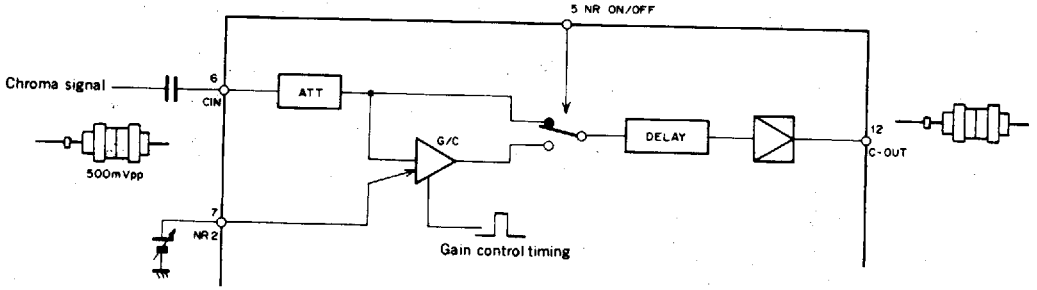
When CNR is ON, gain control is executed in the image section only (With the exception of burst section). The timing is, therefore, formed by using H. BLK pulse input from Pin 3.
Simultaneously with the input of H. BLK pulse Tr. Q1 turns OFF and Pin 4 (NR1) voltage rises. Tr. Q1 turns ON again when H. BLK pulse turns to L level and Pin 4 voltage reaches the voltage set at Pin 9 (SET-P). Gain control timing pulse is emitted during the period when H. BLK pulse is input (When it turns to H level) until Pin 4 voltage reaches the voltage set at Pin 9. During this period gain control is not performed.

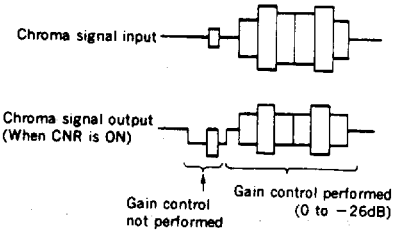




(2) Gain control

When CNR is ON, gain control is performed according to the timing set in (1). The amount of gain control is set at Pin 7 (NR2).
Control range stands within 0dB to −26dB. (See Pin Description, P.5 ~)

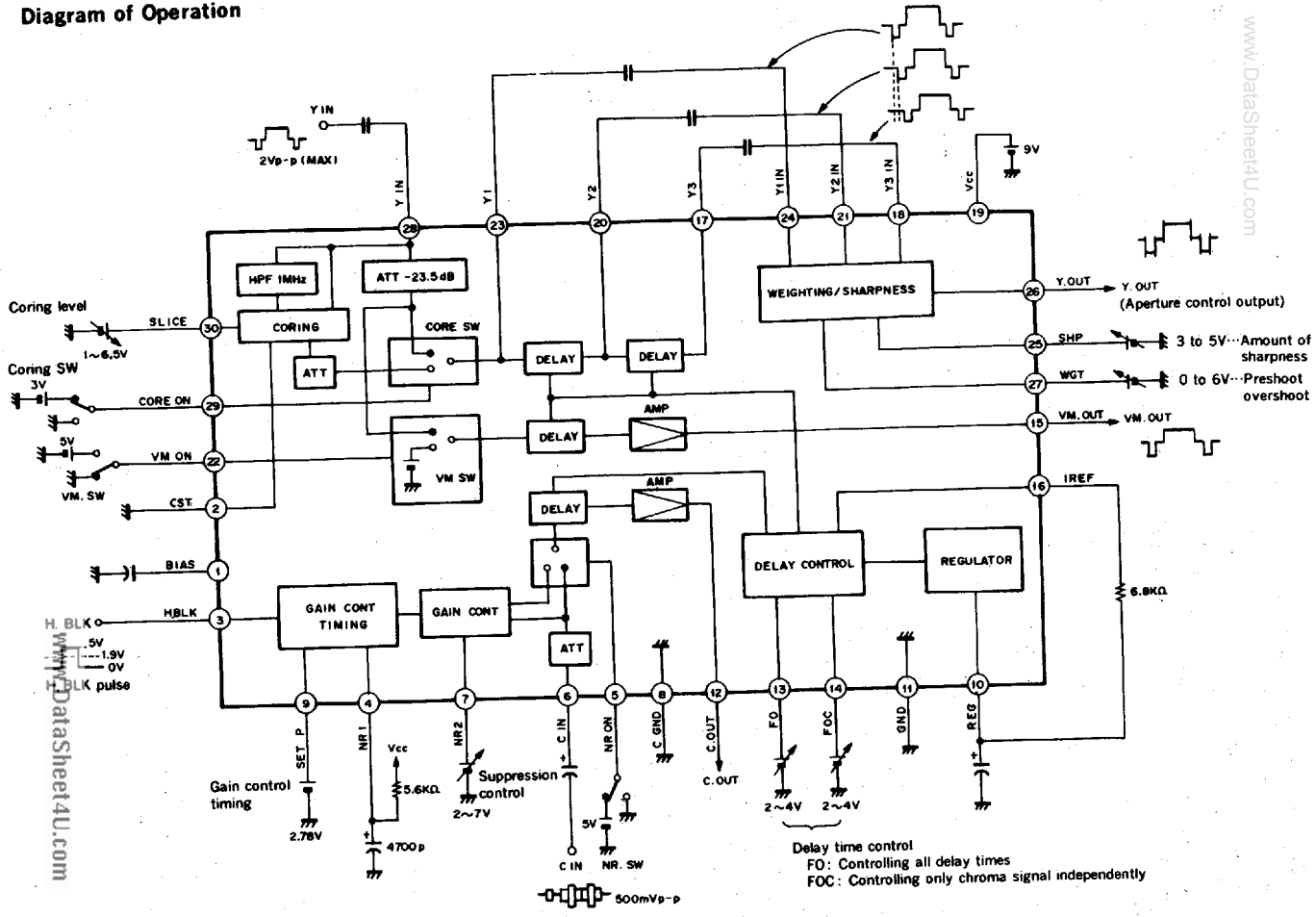




4. VM output

CXA1387S features a VM (velocity modulation) signal output. (Pin 15)
Basically, it is similar to Y input. Since Y output is contour accentuated by means of the built-in delay line. VM output has the same delay time as Y output. Changing the delay time of Y output delay (that is, changing Y output peak frequency). means simultaneously changing VM output delay time. This goes the same with C output, except that C output, can be canged independently.

Diagram of Operation



Notes on Operation

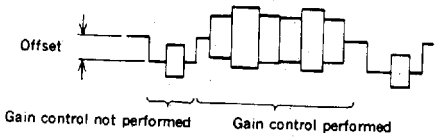
Consider the following points during usage.

1. Oscillation

   Output stage (YOUT, VMOUT, and COUT) in this IC is an emitter follower. When loads concerned with capacity are involved oscillation may occur. Use a buffer. Connect a by-pass capacitor to each of pins, FO (Pin 13) and FOC (Pin 14), that control the delay time of the built-in delay line.

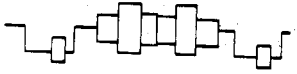
2. Offset of chroma signal when CNR is ON

   There is an offset between where image signals are gain controlled and burst signal not gain controlled. (See Fig. below.)

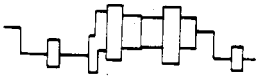


(This offset is specified in Item, No.18, Electrical Characteristics.)

When the changing offset applies to the image chroma signal, the TV screen is adversely affected. Adjust Pin 9 (SET. P) voltage, controlling Pin 9 voltage so that it does not apply to the image.



〈Good example〉



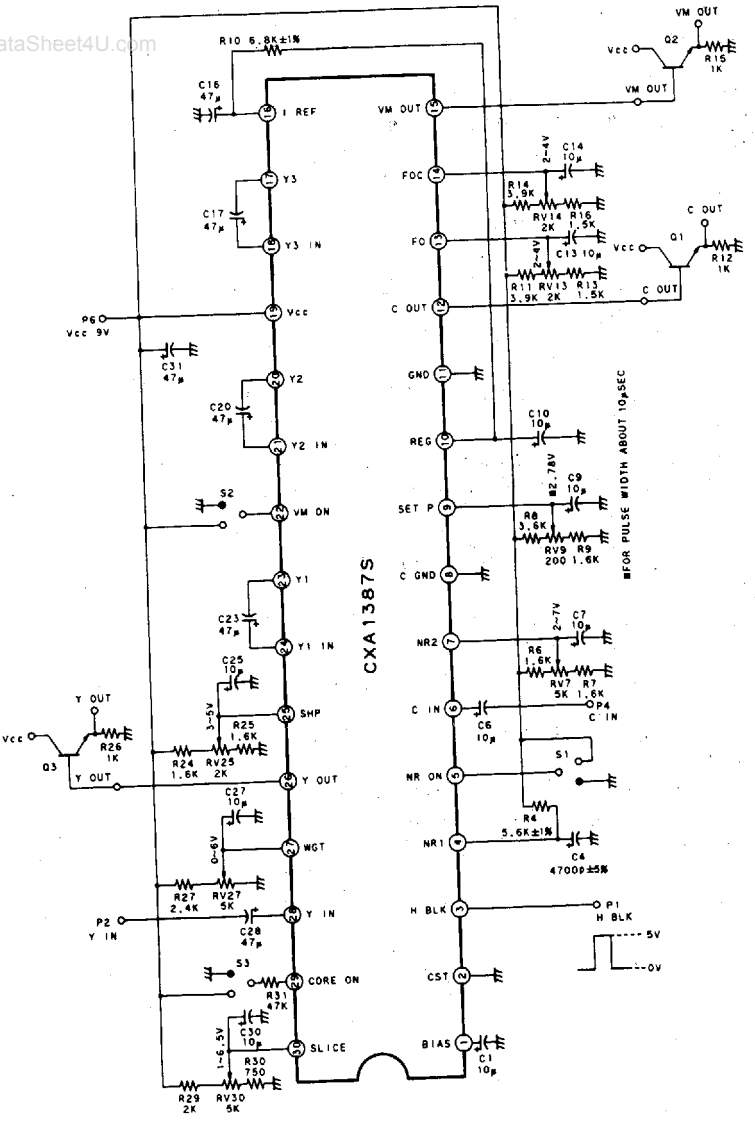
〈Bad example〉

3. Input signal dynamic range

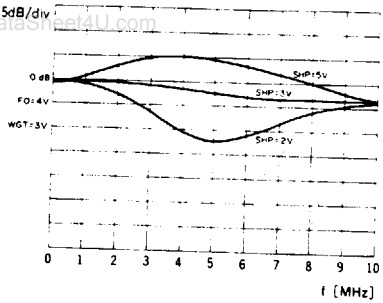
   i) The max. input dynamic range of Y signal stands at 2Vp-p. This is the value from Sync to White peak. When the input signal exceeds 2Vp-p, it may be clipped and distorted.

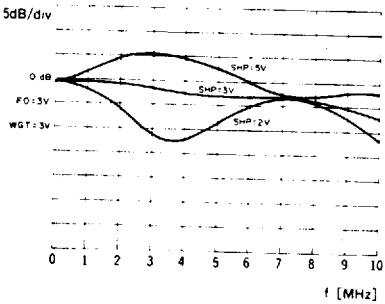
   ii) The max. input dynamic range in the chroma signal stands at 500mVp-p (Max.). This is when the chroma signal is at burst signal. When a low frequency Y signal is mixed with the chroma input signal (CIN), this input dynamic range may reach a max. of 2Vp-p.

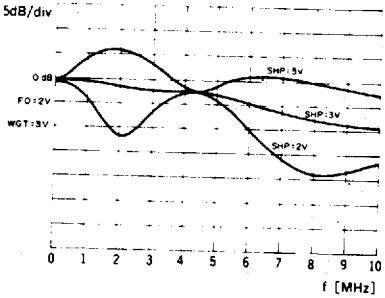
Application Circuit



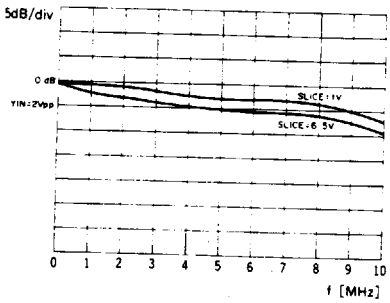
1. Sharpness characteristics

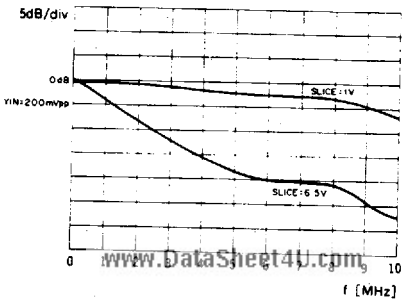






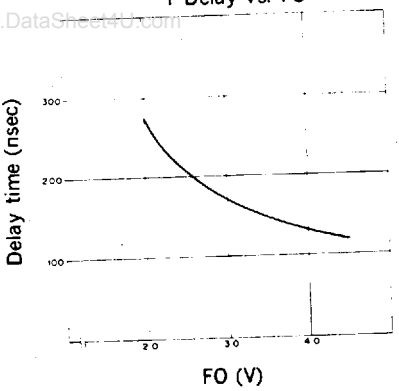
2. Coring characteristics



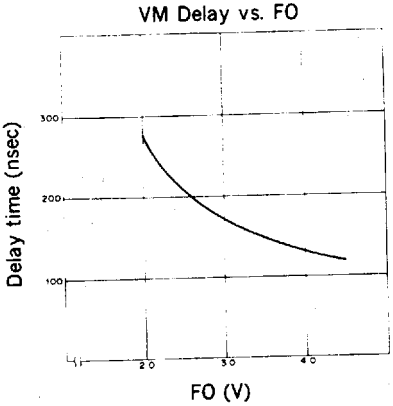


3. Delay characteristics

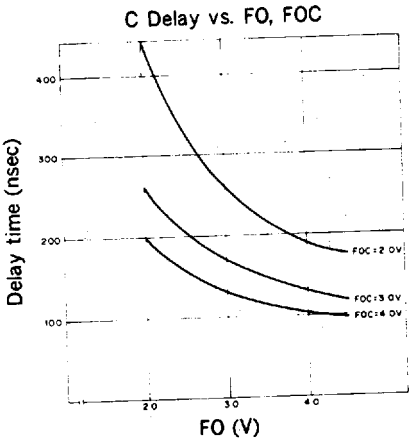
Y Delay vs. FO



VM Delay vs. FO

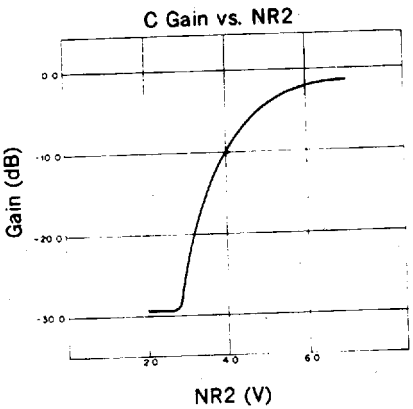


C Delay vs. FO, FOC



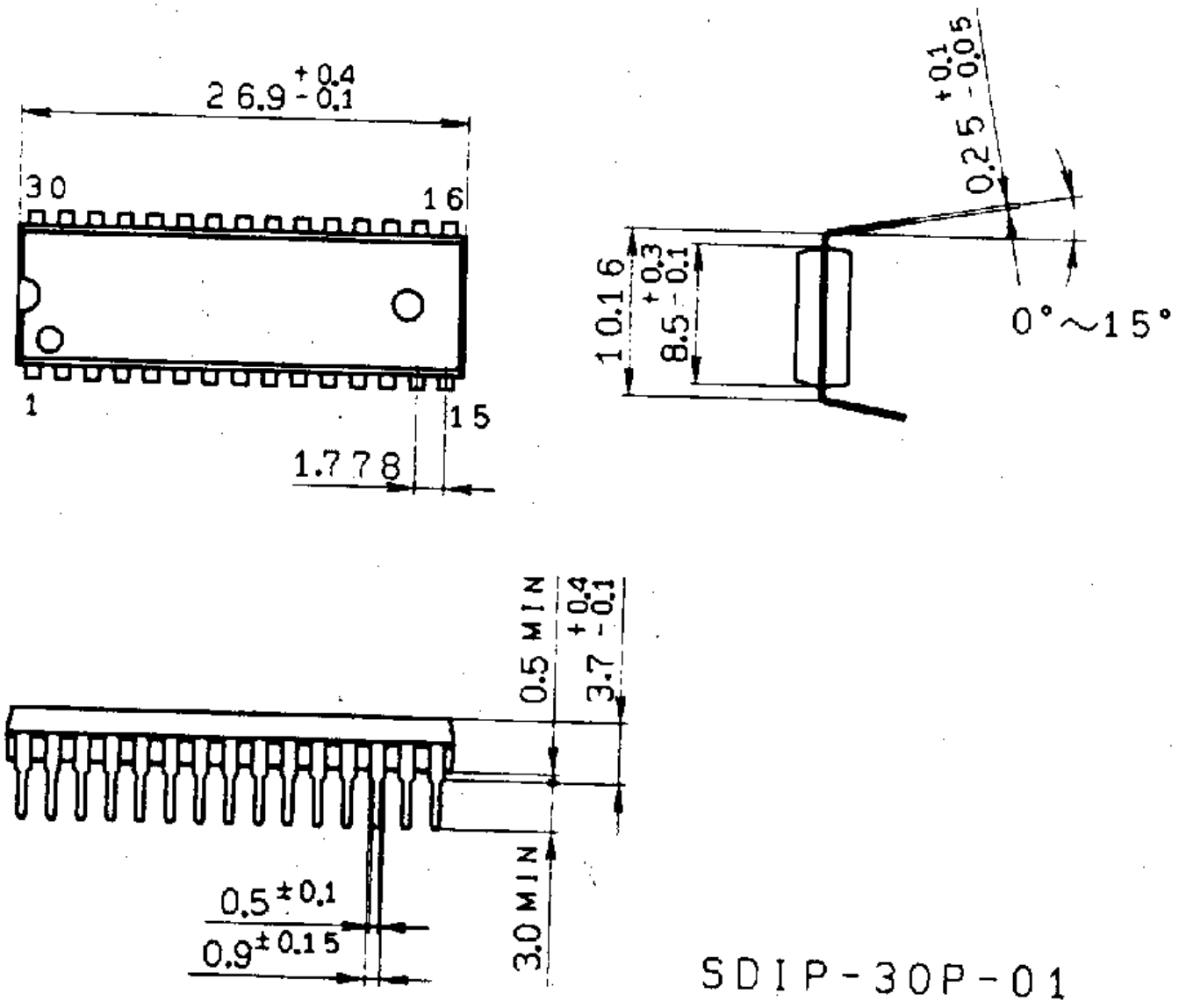
4. Chroma signal gain control characteristics

C Gain vs. NR2



Package Outline Unit : mm

30pin SDIP (Plastic) 400mil 1.8g



SDIP-30P-01