CX25898/9
Video Encoder with Adaptive Flicker Filtering and HDTV Output

Data Sheet

102759A
February 2006

CONEXANT

Ordering Information

Model Number	Package	Operating Temperature

Revision History

Revision	Date	Description
A	February 14, 2006	Initial Release

Information in this document is provided in connection with Conexant Systems, Inc. ("Conexant") products. These materials are provided by Conexant as a service to its customers and may be used for informational purposes only. Conexant assumes no responsibility for errors or omissions in these materials. Conexant may make changes to this document at any time, without notice. Conexant advises all customers to ensure that they have the latest version of this document and to verify, before placing orders, that information being relied on is current and complete. Conexant makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Conexant's Terms and Conditions of Sale for such products, Conexant assumes no liability whatsoever.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF CONEXANT PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. CONEXANT FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. CONEXANT SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

Conexant products are not intended for use in medical, lifesaving or life sustaining applications. Conexant customers using or selling Conexant products for use in such applications do so at their own risk and agree to fully indemnify Conexant for any damages resulting from such improper use or sale.

The following are trademarks of Conexant Systems, Inc.: Conexant® and the Conexant C symbol. Product names or services listed in this publication are for identification purposes only, and may be trademarks of third parties. Third-party brands and names are the property of their respective owners. Macrovision® is a registered traademark of Macrovision Corporation.

For additional disclaimer information, please consult Conexant's Legal Information posted at www.conexant.com which is incorporated by reference.

Reader Response: Conexant strives to produce quality documentation and welcomes your feedback. Please send comments and suggestions to conexant.tech.pubs@conexant.com. For technical questions, contact your local Conexant sales office or field applications engineer.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

CX25898/9

Video Encoder with Adaptive Flicker Filtering and HDTV Output

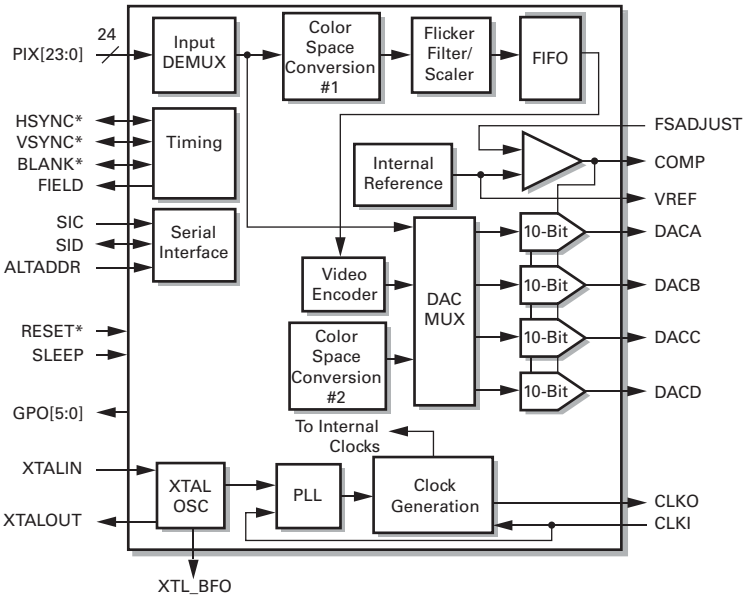
Conexant's CX25898/9 is specifically designed to meet TV out system requirements for the next-generation desktop PCs, notebook PCs, game consoles, portable media players, progressive DVD players, and set-top boxes. With software-forward compatibility to the CX25870/1/2/3/4/5, manufacturers can quickly bring to market new solutions that require adaptive flicker filtering, ATSC High-Definition Television (HDTV) outputs, and standard TV out active VGA resolutions from 320 x 200 (minimum) to 1024 x 768 (maximum).

Adaptive flicker filtering is a Conexant technology in which the encoder looks at the characteristics of the video content on a pixel-by-pixel basis and automatically determines the optimal amount of flicker filtering required. If an end-user wants to work on a spreadsheet while watching a DVD movie in a window, both the text-intensive application requiring a lot of flicker filtering, and the DVD movie requiring very little flicker filtering can look their best.

The CX25898/9 also provides an analog RGB or YP_RP_B HDTV output. The CX25898/9 is compliant with the EIA770-3 and SMPTE 274M/293M/296M standards and supports all major ATSC HDTV resolutions including 480p, 625p (576p), 720p, and 1080i.

All worldwide standard definition composite outputs are supported, including NTSC-M (N. America, Taiwan), NTSC-J (Japan), NTSC 4.43, PAL-B,D,G,H,I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay), PAL-Nc (Argentina), PAL-60 (China) and SECAM. For enhanced TV viewing, S-video (SVHS) can be transmitted as well. The CX25898 and CX25899 are functionally identical, except the CX25899 can output standard definition video with Macrovision® Level 7.1.L1 copy protection capability, and HDTV with Macrovision 525p (480p) copy protection for progressive scan outputs.

Functional Block Diagram



Distinguishing Features

- 4 high-performance, 10-bit DACs
- HDTV output mode
  - Compliant with EIA770-3 and SMPTE274M (1080i), SMPTE296M (720p), ITU-R.BT1358 (625p and 525p) and ITU-R.BT.709-4 (1035i and CIF 30/ PsF and 60/ I) standards
  - Automatic trilevel sync and broad pulse generation
  - Direct YP_RP_B or RGB HDTV outputs from progressive RGB or YCrCb graphics video in 1080i, 720p, 480p ATSC and ITU-R.BT.1358 625p and 525p resolutions
  - Support for Japan D1 (525i), D2 (D1+525p), D3 (D2+750p), D4 (D3+1125i) HDTV formats
- Software and register compatible with the CX25870/1/2/3/4/5
- Worldwide standard-definition TV support: NTSC-M, J, 4.43, PAL-B, D, G, H, I, M, N, Nc, 60, and SECAM
- Adaptive flicker filtering for enhanced image quality (patents pending), and peaking filters for text sharpness
- Programmable overscan compensation from 0% to 25%
- Programmable power management
- Wide-Screen Signaling (WSS) and CGMS support for variable clock rates
  - Adheres to EIAJ CPR-1204 and 1204-1, 1204-2, and EN300 294 standards
- 3.3 V operation with scalable low-voltage graphics controller interface
- Colorstream™ (EIA 770.2) and Super Colorstream™ component video outputs
- Component $YC_R C_B$ analog outputs
- Luma and chroma comb filtering

(Continued on next page)

(Continued from previous page)

- SCART RGB or Y/C output for Europe
  - 4th DAC is NTSC/PAL composite
  - EN50-049 and IEC 933-1 compliant
- S-Video output (simultaneous with composite or 2nd S-Video NTSC, PAL or SECAM)
- Simultaneous component YC_RC_B and Composite output
- Accepts many different input data formats:
  - 15/16/24-bit RGB multiplexed or nonmultiplexed
  - 16-bit 4:2:2 and 24-bit 4:4:4 YCrCb multiplexed or nonmultiplexed
  - Flexible pixel ordering with various alternate formats
- 48 autoconfiguration modes
- CCIR601/ITU-R BT.601 (i.e., 720 x 480i for 525/60 video systems and 720 x 576i for 625/50 video systems) and CCIR656/ITU-R.BT.601 syncless compatible input modes
- Closed captioning encoding (NTSC/PAL)
- Six general-purpose output ports (GPO[0]–GPO[5])
- VGA RGB or YUV outputs
- Macrovision 7.1.L1 and 525p (480p) DVD 1.03 Macrovision Copy Protection (CX25899 only)
- 80-pin TQFP package

Contents

Figures 7

Tables 11

1 Functional Description 13

1.1 Pin Descriptions 13

1.1.1 Data and Pin Assignments 17

1.2 Device Block Diagram 19

1.3 Flicker Filter 20

1.4 Device Description 21

1.4.1 Overview 21

1.4.2 Low-Voltage Digital Graphics Interface 22

1.4.3 Reset 24

1.4.4 Device Initialization 25

1.4.5 Clocking Generation and Reference Crystal 25

1.4.6 3:2 Clocking Mode for Higher Input Resolutions 28

1.4.7 Master, Pseudo-Master, and Slave Interfaces 30

1.4.8 Autoconfiguration and Interface Bits 34

1.4.9 Adaptations for Clock-Limited Master Devices 38

1.4.10 Input Formats 40

1.4.11 Input Pixel Timing 40

1.4.12 YCrCb Inputs 40

1.4.13 RGB Inputs 42

1.4.14 Input Pixel Vertical Sync 44

1.4.15 Input Pixel Blanking 45

1.4.16 Overscan Compensation 46

1.4.18 Adaptive Flicker Filter 51

1.4.19 VGA Registers Involved in the TV Out Process 55

1.4.20 Output Modes 58

1.4.21 Analog Horizontal Sync 59

1.4.22 Analog Vertical Sync 59

1.4.23 Analog Video Blanking 59

1.4.24 Video Output Standards Supported 60

1.4.25 Subcarrier Generation 69

1.4.26 Subcarrier Phase Reset/Offset 69

1.4.27 Burst Generation 70

1.4.28 Video Amplitude Scaling and SINX/X Compensation 70

1.4.29 Chrominance Disable 70
1.4.30 FIELD Pin Output. 70
1.4.31 Buffered Crystal Clock Output 72
1.4.32 Noninterlaced Output. 73
1.4.33 Closed Captioning 73
1.4.34 Wide Screen Signaling—Standard-Definition TV 77
1.4.35 Wide Screen Signaling—High-Definition TV 86
1.4.36 Chrominance and Luminance Processing 95
1.4.37 Color Bar and Blue Field Generation 97
1.4.38 CCIR656 Mode Operation. 99
1.4.39 CCIR601 Mode Operation for DVD Playback. 102
1.4.40 SECAM Output 106
1.4.41 Elimination of Dot Crawl in Composite NTSC Output. 114
1.4.42 Macrovision Copy Protection 117
1.4.43 HDTV Output Mode 118
1.4.44 SCART Output. 119
1.4.45 Y CR CB 480i (YUV) Standard-Definition Component Video Outputs 123
1.4.46 VGA(RGB)—DAC Output Operation 127
1.4.47 TV DAC Detection Procedures 130
1.4.48 Sleep/Power Management. 133

2 Internal Registers 135

2.1 Register Map Overview 135
2.2 Reading Registers 138
2.3 Writing Registers 141

3 Parametric Information 161

3.1 DC Electrical Parameters 161
3.2 AC Electrical Parameters 164
3.3 Power Consumption Results 168
3.4 Timing Diagrams 169
3.5 Mechanical Specifications 181

A Approved Crystal Vendors Appendix 183

B Autoconfiguration Mode Register Values and Details Appendix. 187

Figures

Figure 1. Pinout Diagram for CX25898/9 13
Figure 2. Encoder Block Diagram. 19
Figure 3. Flicker Filter Block Diagram 20
Figure 4. Sample Schematic 23
Figure 5. Single-Ended Oscillator Biasing Circuit 27
Figure 6. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input/ NTSC Output 28
Figure 7. Operating the Encoder in Master Interface 30
Figure 8. Operating the Encoder in Pseudo-Master Interface (Default Interface at Power-Up) 31
Figure 9. Operating the Encoder in Slave Interface 32
Figure 10. Slave Interface without a BLANK* Signal (Input or Output) 36
Figure 11. Slave Interface with a BLANK* Input to the CX25898/9. 37
Figure 12. Decimation Filter Response at Sampling Frequency (Fs) of 27 MHz 41
Figure 13. Horizontal Timing Register Relationship 43
Figure 14. Vertical Timing Register Relationship 44
Figure 15. Windows Desktop TV Out Image from Encoder without Overscan Compensation 48
Figure 16. Windows Desktop TV Out Image from CX25898/9 with Overscan Compensation 48
Figure 17. Flicker Filter and Video Adjustment Control Diagram 54
Figure 18. Horizontal Timing Relationship—Generic GPU 57
Figure 19. Vertical Timing Relationship—Generic GPU 57
Figure 20. Important Bit Settings for Generation of Standard-Definition Video Outputs. 60
Figure 21. Interlaced 525-Line (NTSC) Video Timing 61
Figure 22. Interlaced 525-Line (PAL-M) Video Timing 62
Figure 23. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 1–4) 63
Figure 24. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 5–8) 64
Figure 25. Interlaced 625-Line (PAL-N) Video Timing (Fields 1–4) 65
Figure 26. Interlaced 625-Line (PAL-N) Video Timing (Fields 5–8) 66
Figure 27. Noninterlaced 262-Line (NTSC) Video Timing 67
Figure 28. Noninterlaced 262-Line (PAL-M) Video Timing 67
Figure 29. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, Nc) Video Timing 67
Figure 30. Interlaced 625-Line (SECAM-B, D, G, K, K1, L, M) Video Timing (Fields 1-4) 68

Figure 31. FIELD Pin Output Timing Diagram: NTSC-M, J, 4.43, PAL-M, 60 71
Figure 32. FIELD Pin Output Timing Diagram (PAL-B, D, G, H, I, N, Nc) 71
Figure 33. EIA-608B (CEA-608B)-Compliant Line 21 Waveform (NTSC) 73
Figure 34. CEA 805A-TYPEA-Compliant HDTV 1080i, 720p Waveform 76
Figure 35. Horizontal Timing for PAL Output-Line 23 that Contains WSS Data 77
Figure 36. WSS PAL Composite Signal 80
Figure 37. Typical WSS NTSC Analog Waveform Compatible to EIAJ CPR-1204 and IEC 61880-1 82
Figure 38. CX25898/9 WSS NTSC Line 20 Analog Waveform; WSSDAT = FC F0 1 hex 85
Figure 39. Typical WSS 480p (525p) Luma Analog Waveform 86
Figure 40. Typical WSS 720p (750p) Luma Analog Waveform 89
Figure 41. Typical WSS 1080i (1125i) Luma Analog Waveform 92
Figure 42. Digital Luminance Upsampling Filter 95
Figure 43. Text Sharpness (Luminance Upsampling) Filter with Peaking Options 95
Figure 44. Close-Up of Text Sharpness (Luminance Upsampling) Filter with Peaking and Reduction Options 96
Figure 45. Zoom-In of Text Sharpness (Luminance Peaking) Filter Options 96
Figure 46. Digital Chrominance Standard Bandwidth Filter (CHROMA_BW = 0—Default) 96
Figure 47. Digital Chrominance Wide Bandwidth Filter (CHROMA_BW = 1) 97
Figure 48. Composite and S-Video Analog Voltage Levels (SDTV Color Bars) 98
Figure 49. CX25898/9 Connection to CCIR656-Compatible Master Device 100
Figure 50. DVD Playback Utilizing Graphics Controller for Color-Space and Progressive Scan Conversion 104
Figure 51. SECAM High Frequency Pre-emphasis Filter 106
Figure 52. NTSC Composite Output: Standard 75 Percent Color Bars With Dot Crawl Artifact 114
Figure 53. CX25898/9 Driving a Type I SCART Connector (EN 50-049 and IEC 933-1 Compliant) 122
Figure 54. CX25898/9 Driving a Type II SCART Connector (Y/C and BBC SCART Compliant) 122
Figure 55. Y PR PB Component Video Signals using 100/0/100/0 Color Bars as the Digital Input Signal (Courtesy– EIA-770.2-A standard, page 8 and EIA-770.1 standard) 124
Figure 56. Filterless DAC Outputs for VGA (RGB) DAC Output with Sync Buffers . . . 129
Figure 57. Timing Details for All Interfaces 169
Figure 58. Master Interface Timing Relationship/Noninterlaced RGB/YCrCb Input . . 170
Figure 59. Pseudo-Master Interface Timing Relationship—Active Line/Noninterlaced RGB Input 171
Figure 60. Pseudo-Master Timing Relationship Blank Line/Noninterlaced RGB/YCrCb Input 172
Figure 61. Slave Interface Timing Relationship/Noninterlaced RGB/YCrCb Input . . . 173
Figure 62. Slave Interface Timing Relationship/Interlaced Multiplexed RGB Input (FLD_MODE = 10—Default) 174
Figure 63. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 01) 175
Figure 64. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 00) 176

Figure 65. HDTV Output Horizontal Timing Details: 1080i 177
Figure 66. HDTV Output Horizontal Timing Details: 720p 178
Figure 67. HDTV Output Horizontal Timing Details: 480p 179
Figure 68. HDTV Output Vertical Timing Details: 480p 179
Figure 69. HDTV Output Horizontal Timing Details: 576p (625p) 180
Figure 70. HDTV Output Vertical Timing Details: (576p (625p) 180
Figure 71. 80-Pin TQFP Package Diagram 181

Tables

Table 1. Pin Descriptions . . . 14
Table 2. Data and Pin Assignments for Multiplexed Input Formats . . . 17
Table 3. Data and Pin Assignments for Nonmultiplexed Input Formats . . . 18
Table 4. Autoconfiguration Solutions that Utilize 3:2 Clocking Mode . . . 29
Table 5. Master Interface without a BLANK* Signal (Input or Output) . . . 34
Table 6. Master Interface with a BLANK* Input to the CX25898/9 . . . 35
Table 7. Pseudo-Master Interface without a BLANK* Signal (Input or Output) to the CX25898/9 (Default at Power-Up) . . . 35
Table 8. Pseudo-Master Interface with a BLANK* Input to the CX25898/9 . . . 35
Table 9. Adjustment to the Encoder's MSC Registers . . . 38
Table 10. Adjustment to the PLL_INT and PLL_FRACT Registers . . . 39
Table 12. Optimal Adaptive and Standard Flicker Filter Settings for Common PC Applications and Resolutions . . . 53
Table 13. VGA/CRTC Registers Involved in TV Out Process . . . 56
Table 14. Switching Conexant Encoder into PAL WSS Output Operation . . . 81
Table 15. Serial Writes Required to Switch Conexant Encoder into NTSC WSS Output Operation . . . 84
Table 16. Serial Writes Required to Switch Conexant Encoder into HDTV 480p (525p) WSS Output Operation . . . 88
Table 17. Serial Writes Required to Switch Conexant Encoder into HDTV 720p (750p) WSS Output Operation . . . 91
Table 18. Switching Conexant Encoder into HDTV 1080i (1125i) WSS Output Operation . . . 94
Table 19. Composite and Luminance Color Bar Amplitudes . . . 98
Table 20. Composite and Chrominance Color Bar Magnitudes . . . 99
Table 21. CCIR656 "XY" Events . . . 100
Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out . . . 107
Table 23. Vital SECAM Bit Settings–Register 0xA2 . . . 111
Table 24. SECAM Specific Registers within the Conexant VGA Encoder . . . 113
Table 25. Source Code for Elimination of Dot Crawl in NTSC Composite Video . . . 115
Table 26. Serial Writes Required to Switch CX25898/9 into SCART Output Operation 119
Table 27. Default SCART Outgoing Signal Assignments . . . 120
Table 28. CX25898/9 SCART Outputs for Different SCART Standards . . . 121
Table 29. Common Registers Required to Switch CX25898/9 into EIA-770.2-A- or EIA-770.1-Compliant Component Video Outputs . . . 125
Table 30. Unique Registers Required to Switch CX25898/9 into EIA-770.2-A- Compliant Component Video Outputs . . . 125
Table 31. Serial Writes Required to Remove Bilevel Syncs from all VGA/DAC Outputs . . . 127
Table 32. Serial Writes Required to Switch CX25898/9 into VGA/DAC Output Operation . . . 127
Table 33. Standard DAC Detection Algorithm for the CX25898/9 . . . 130
Table 34. Legacy DAC Detection Algorithm . . . 132

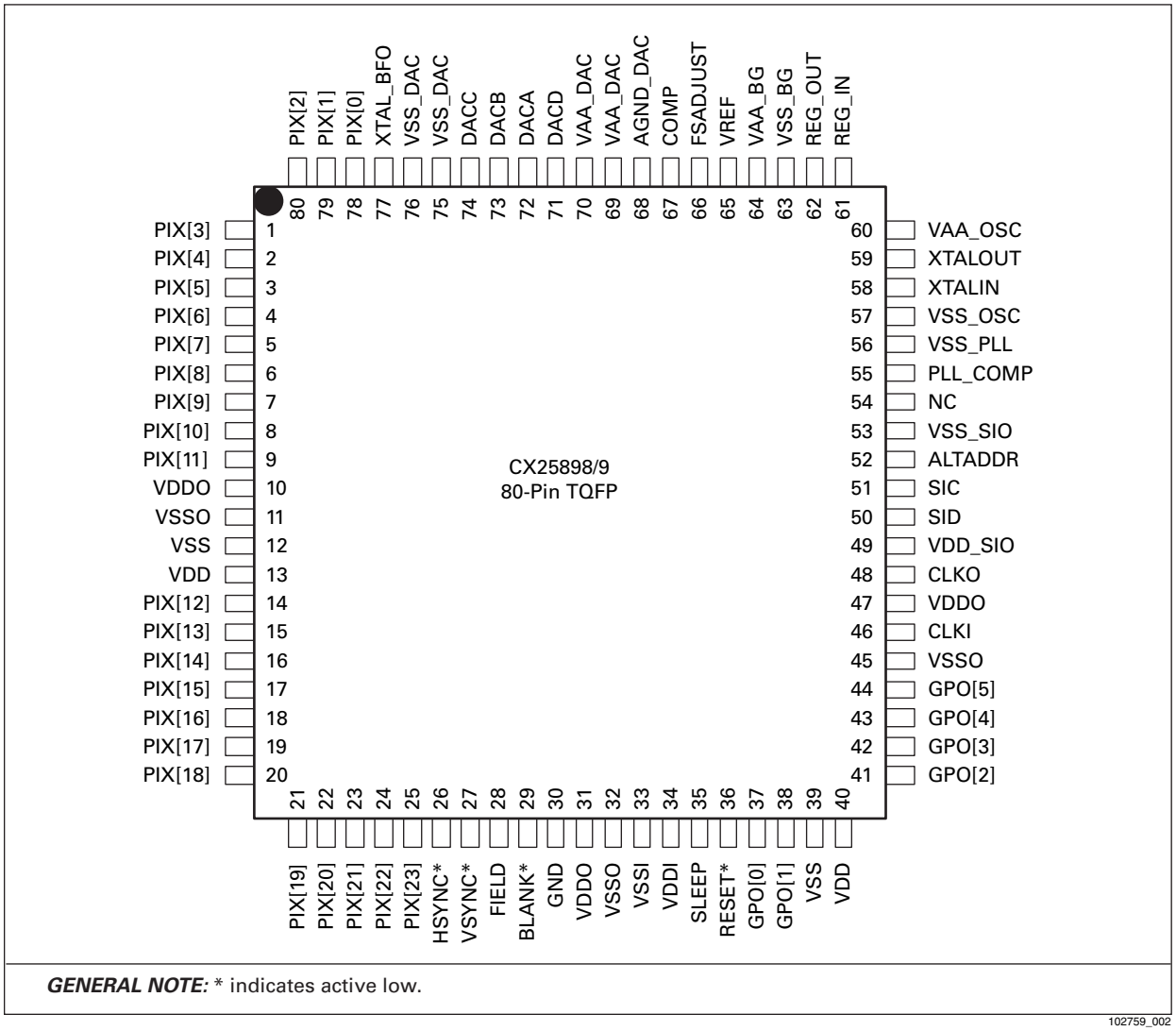
Table 35. ESTATUS[1:0] Read-Back Bit Map for Legacy Algorithm 133
Table 36. Register Bit Map for CX25898/9 135
Table 37. Bit Map for Read-Only Registers 139
Table 38. Data Details for All Read-Only Registers 140
Table 39. Programming Details for All Read/Write Registers 141
Table 40. DC Recommended Operating Condition 161
Table 41. DC Absolute Maximum Ratings 162
Table 42. DC Characteristics for CX25898/9. 163
Table 43. AC Characteristics for CX25898/9. 164
Table 44. CX25898/9 Operating Current, Operating Voltage, and Power-Related Results under Different Testing Conditions 168
Table 45. CX25898/9 Register Values for Autoconfiguration Modes 0–4 187
Table 46. CX25898/9 Register Values for Autoconfiguration Modes 5–10 190
Table 47. CX25898/9 Register Values for Autoconfiguration Modes 11–15 193
Table 48. CX25898/9 Register Values for Autoconfiguration Modes 16–21 196
Table 49. CX25898/9 Register Values for Autoconfiguration Modes 22–26 199
Table 50. CX25898/9 Register Values for Autoconfiguration Modes 27–30 202
Table 51. CX25898/9 Register Values for Autoconfiguration Modes 31–36 205
Table 52. CX25898/9 Register Values for Autoconfiguration Modes 37–42 208
Table 53. CX25898/9 Register Values for Autoconfiguration Modes 43–47 211

1 Functional Description

1.1 Pin Descriptions

Figure 1 shows the pinout diagram. Table 1 provides the pin description.

Figure 1. Pinout Diagram for CX25898/9



GENERAL NOTE: * indicates active low.

102759_002

***Table 1. Pin Descriptions** (1 of 3)*

Pin Name	I/O	Pin #	Description
AGND_DAC	—	68	Analog circuit GND. Connect all analog and digital ground pins together on the same PCB plane to prevent latchup.
ALTADDR	I	52	Alternate slave address input (TTL compatible). A logical 0 configures the device to respond to a serial write address of 0x88. A logical 1 configures the device to respond to a serial write address of 0x8A. In addition, serial reads to address 0x89 (ALTADDR = 0) or 0x8B (ALTADDR = 1) are possible with this pin.
BLANK*	I/O	29	Digital composite blanking control (TTL compatible) pin. This can be generated by the encoder or supplied from the graphics controller. If internal blanking is used, this pin can be used to indicate the control character clock edge. If unused, BLANK* should be tied high through a 10 kΩ pullup resistor.
CLKI	I	46	Pixel clock input (TTL compatible). Use this as either the encoder's main clock (slave interface) or as a delayed version of the CLKO signal (same frequency) synchronized with the pixel data input. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins.
CLKO	O	48	Pixel clock output (TTL compatible). In master or pseudo-master interface, this signal is used by the encoder to tell the master the frequency at which data should be transferred. This pin is three-stated if the CLKI pin provides the encoder clock. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins.
COMP	O	67	Compensation pin.Decouple to VAA 0.1 μF ceramic capacitor to bypass this pin to VAA. The capacitor must be as close to the pin as possible to keep lead lengths to a minimum.
DACA	O	72	DACA Analog output. Attach a 75 Ω termination resistor, 1% tolerance, with short traces between this pin and ground. If unused, leave this pin as a no connect.
DACB	O	73	DACB Analog output. Attach a 75 Ω termination resistor, 1% tolerance, with short traces between this pin and ground. If unused, leave this pin as a no connect.
DACC	O	74	DACC Analog output. Attach a 75 Ω termination resistor, 1% tolerance, with short traces between this pin and ground. If unused, leave this pin as a no connect.
DACD	O	71	DACD Analog output. Attach a 75 Ω termination resistor, 1% tolerance, with short traces between this pin and ground. If unused, leave this pin as a no connect.
FIELD	O	28	Field control output (TTL compatible). FIELD transitions after the rising edge of CLKI, two clock cycles following falling HSYNC*. It is a logical 0 during odd fields and is a logical 1 during even fields. If unused, FIELD should be left as a no connect. The polarity of the FIELD signal can be adjusted with the FIELDI bit.
FSADJUST	I	66	Full-scale adjust control pin. A resistor (RSET) with a value of 402 Ω (±1%) connected between this pin and GND controls the full-scale output current on the analog outputs.
GND	—	30	Analog circuit GND. Connect all analog and digital ground pins together on the same PCB plane to prevent latchup.

***Table 1. Pin Descriptions** (2 of 3)*

Pin Name	I/O	Pin #	Description
GPO [0:5]	O	37, 38, 41, 42, 43, 44	General-purpose output pin #0–#5. User can select high or low output level through the GPO[0:5] bit. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins. If unused, tie this pin to GND through a 47 kΩ resistor in series.
HSYNC*	I/O	26	Horizontal sync input/output (TTL compatible). As an output (timing master operation), HSYNC* is output following the rising edge of CLKO. As an input (timing slave operation), HSYNC* is clocked on the rising edge of CLKI. The polarity of the HSYNC* signal can be adjusted with the HSYNCI bit.
NC	—	54	No-connect pin
PIX[0:23]	I	1–9, 14–20, 21–25, 78–80	Pixel input pin #0–#23. The input data is sampled on the rising edge for nonmultiplex modes and both the rising and falling edges of CLKI for multiplexed modes. A higher bit index corresponds to a greater bit significance. Note: 1. Ground all unused pixel input pins. 2. One can remap the order of the pins by setting the register bit PIX_REVERSE (0x24, bit 0). Current Pin → Re-mapped Function PIX[23] → PIX[0] PIX[22] → PIX[1]
PLL_COMP	—	55	PLL compensation pin. Use a 1.0 μF ceramic capacitor to decouple this pin to GND. This pin also provides compensation for stable operation of the internal PLL regulator.
REG_IN	—	61	Pass transistor emitter voltage. Tie this pin to emitter of 2N3904 (or similar) NPN transistor.
REG_OUT	—	62	Pass transistor base voltage. Tie this pin to base of 2N3904 (or similar) NPN transistor.
RESET*	I	36	Reset control input (TTL compatible). A logical 0 applied for a minimum of 1 μs resets and disables video timing (horizontal, vertical, subcarrier counters) to the start of VSYNC of the first field. The serial interface registers are also reset to their default values. The hardware RESET* pulse must match the digital I/O voltage levels.
SIC	I	51	Serial interface clock input (TTL compatible). Data is latched into the device via this pin coupled with the SID pin. Maximum serial transfer rate is 400 kHz. Minimum serial transfer rate is 100 kHz. The high voltage level to the SIC pin must match the voltage level of pin 49 = VDD_SIO.
SID	I/O	50	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this pin coupled with the SIC pin. Maximum serial transfer rate is 400 kHz. Minimum serial transfer rate is 100 kHz. The high voltage level to/ from the SID pin must match the voltage level of pin 49 = VDD_SIO.

***Table 1. Pin Descriptions** (3 of 3)*

Pin Name	I/O	Pin #	Description
SLEEP	I	35	Power-down control input (TTL compatible). A logical 1 configures the device for power-down mode. A logical 0 configures the device for normal operation.
VAA_BG	—	64	Video DAC bandgap power. Connect all VAA pins and VDD together on the same PCB plane to prevent latchup.
VAA_DAC	—	69, 70	DAC Analog power. Connect all VAA pins and VDDI together on the same PCB plane to prevent latchup.
VAA_OSC	—	60	Crystal oscillator supply pin. Tie this pin to the VAA power supply.
VDD	—	13, 40	Digital power for core logic 1.2 V. Connect all VDD pins together on the same PCB plane to prevent latchup.
VDDI	—	34	Digital power output supply. This pin should be tied to 3.3 V. Connect all VAA pins and all VDD supply pins be connected together on the same PCB plane to prevent latchup.
VDD_SIO	—	49	Serial interface supply pin. Tie this pin only to 3.3 V.
VDDO	—	10, 31, 47	Digital input supply pins. Tie these pins to the I/O power supply. Could be varied from 1.1 V to 3.45 V.
VREF	O	65	Voltage reference pin. Use a 0.1 μF ceramic capacitor to decouple this pin to GND. Place the decoupling capacitor as close to the pin as possible to keep lead lengths to an absolute minimum.
VSS_BG	—	63	Video DAC bandgap ground. All analog and digital ground pins must be connected together on the same PCB plane to prevent latchup.
VSS_DAC	—	75, 76	Common DAC Analog ground pins. Connect VSS pins together on the same PCB plane to prevent latchup.
VSS	—	12, 39	Digital ground for core logic. Connect all VSS pins together on the same PCB plane to prevent latchup.
VSS_OSC	—	57	Crystal oscillator ground pin. Connect all analog and digital ground pins together on the same PCB plane to prevent latchup.
VSS_PLL	—	56	PLL ground pin. Tie this pin to the ground plane.
VSS_SIO	—	53	Serial interface ground pin. Digital ground for syncs and timing pins. Connect all analog and digital ground pins together on same PCB plane to prevent latchup.
VSSI	—	33	Digital output ground pins. Tie all these pins to ground. Connect all analog and digital ground pins together on the same PCB plane to prevent latchup. Note: Ground all unused pixel input pins.
VSSO	—	11, 32, 45	Digital input ground pins. Tie all these pins to ground. Connect all analog and digital ground pins together on the same PCB plane to prevent latchup. Note: Ground all unused pixel input pins.
VSYNC*	I/O	27	Vertical sync input/output (TTL compatible). As an output (timing master operation), VSYNC* is output following the rising edge of CLKO. As an input (timing slave operation), VSYNC* is clocked on the rising edge of CLKI. The polarity of the VSYNC* signal can be adjusted with the VSYNCI bit.
XTAL_BFO	O	77	Buffered crystal output.
XTALIN	I	58	Connect a 13.5000 MHz crystal between these pins. The pixel clock output (CLKO) is derived from these pins in conjunction with an internal PLL. XTALIN can be driven from an external clock oscillator as a CMOS input pin. Internally, this is a CMOS inverter tying XTALOUT to XTALIN. If a single-ended oscillator is utilized, this must drive XTALIN, and the biasing circuit must be integrated for XTALOUT.
XTALOUT	O	59	

1.1.1 Data and Pin Assignments

Tables 2 and 3 present data and pin assignments for multiplexed and nonmultiplexed input formats.

Table 2. Data and Pin Assignments for Multiplexed Input Formats

Pin	24-Bit RGB Mode	15/16-Bit RGB Mode	16-Bit YCrCb Mode	24-Bit YCrCb Mode	Alternate 24-Bit RGB Mode	Alternate 16-Bit YCrCb Mode	Alternate 24-Bit YCrCb Mode
IN_MODE[3:0]	**0000**	**0010/0001**	**0101**	**0100**	**1000**	**0110**	**1100**
Rising Edge of CLKI							
PIX[11]	G4	G2	Cr7/Cb7	Cr7	G3	—	Y3
PIX[10]	G3	G1	Cr6/Cb6	Cr6	G2	—	Y2
PIX[9]	G2	G0	Cr5/Cb5	Cr5	G1	—	Y1
PIX[8]	B7	B4	Cr4/Cb4	Cr4	G0	—	Y0
PIX[7]	B6	B3	Cr3/Cb3	Cr3	B7	Cr7/Cb7	Cb7
PIX[6]	B5	B2	Cr2/Cb2	Cr2	B6	Cr6/Cb6	Cb6
PIX[5]	B4	B1	Cr1/Cb1	Cr1	B5	Cr5/Cb5	Cb5
PIX[4]	B3	B0	Cr0/Cb0	Cr0	B4	Cr4/Cb4	Cb4
PIX[3]	G0	—	—	Cb7	B3	Cr3/Cb3	Cb3
PIX[2]	B2	—	—	Cb6	B2	Cr2/Cb2	Cb2
PIX[1]	B1	—	—	Cb5	B1	Cr1/Cb1	Cb1
PIX[0]	B0	—	—	Cb4	B0	Cr0/Cb0	Cb0
Falling Edge of CLKI							
PIX[11]	R7	R4	Y7	Y7	R7	—	Cr7
PIX[10]	R6	R3	Y6	Y6	R6	—	Cr6
PIX[9]	R5	R2	Y5	Y5	R5	—	Cr5
PIX[8]	R4	R1	Y4	Y4	R4	—	Cr4
PIX[7]	R3	R0	Y3	Y3	R3	Y7	Cr3
PIX[6]	G7	G5[(1)]	Y2	Y2	R2	Y6	Cr2
PIX[5]	G6	G4	Y1	Y1	R1	Y5	Cr1
PIX[4]	G5	G3	Y0	Y0	R0	Y4	Cr0
PIX[3]	R2	—	—	Cb3	G7	Y3	Y7
PIX[2]	R1	—	—	Cb2	G6	Y2	Y6
PIX[1]	R0	—	—	Cb1	G5	Y1	Y5
PIX[0]	G1	—	—	Cb0	G4	Y0	Y4

FOOTNOTE:
(1) G5 is ignored in 15-bit RGB Multiplexed Input Mode.

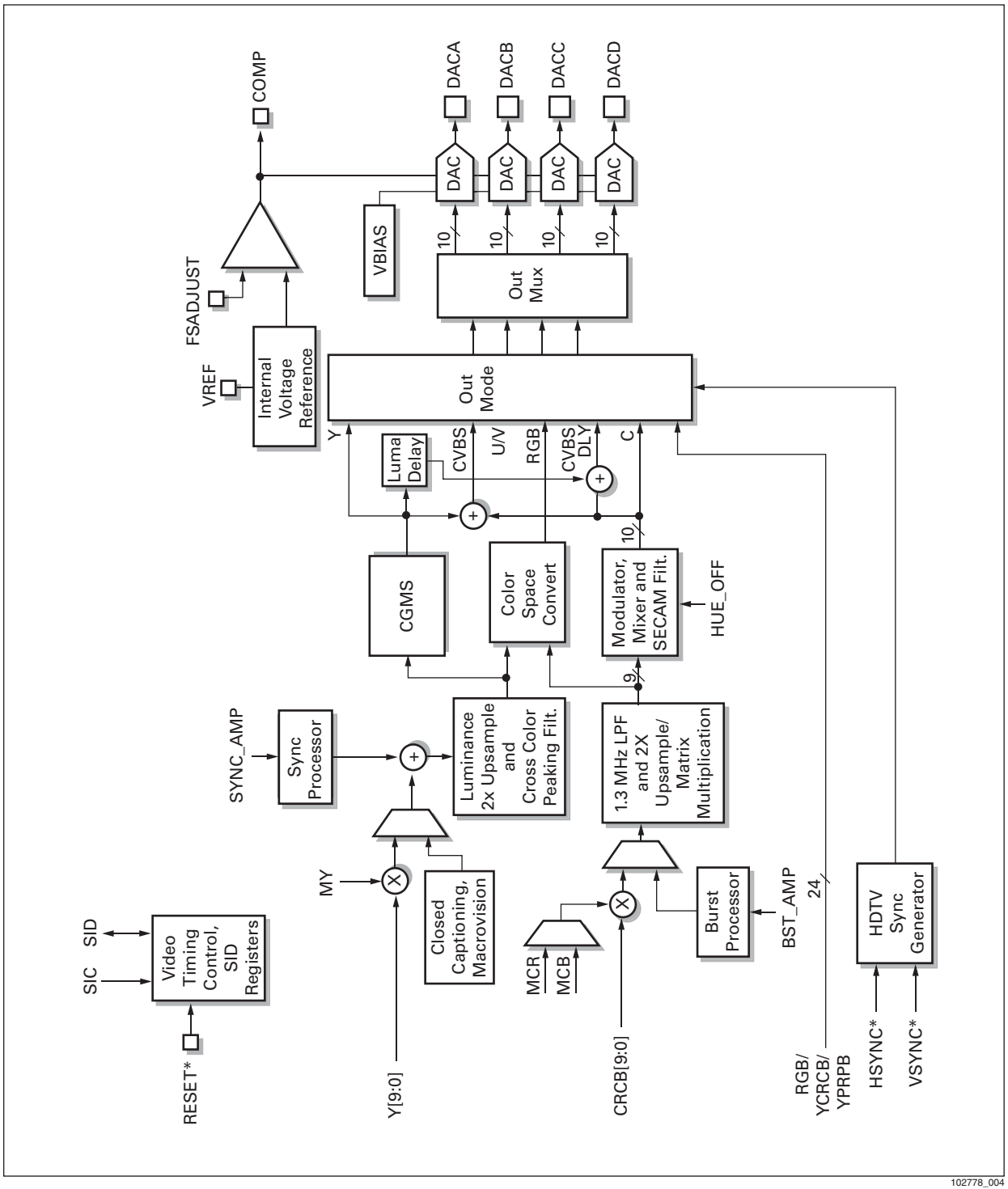
Table 3. Data and Pin Assignments for Nonmultiplexed Input Formats

Pin	16-Bit Nonmux RGB	16-Bit Nonmux YCrCb	24-Bit Nonmux RGB	24-Bit Nonmux YCrCb	Alternate 24-Bit Nonmux RGB	Alternate 24-Bit Nonmux YCrCb
IN_MODE[3:0]	**1010**	**1110**	**0011**	**0111**	**1011**	**1111**
PIX[23]	—	—	B7	Cb7	R7	Cr7
PIX[22]	—	—	B6	Cb6	R6	Cr6
PIX[21]	—	—	B5	Cb5	R5	Cr5
PIX[20]	—	—	B4	Cb4	R4	Cr4
PIX[19]	R4	Y7	B3	Cb2	R3	Cr3
PIX[18]	R3	Y6	B2	Cb2	R2	Cr2
PIX[17]	R2	Y5	B1	Cb1	R1	Cr1
PIX[16]	R1	Y4	B0	Cb0	R0	Cr0
PIX[15]	R0	Y3	G7	Cr7	G7	Y7
PIX[14]	G5	Y2	G6	Cr6	G6	Y6
PIX[13]	G4	Y1	G5	Cr5	G5	Y5
PIX[12]	G3	Y0	G4	Cr4	G4	Y4
PIX[11]	G2	Cr7/Cb7	G3	Cr3	G3	Y3
PIX[10]	G1	Cr6/Cb6	G2	Cr2	G2	Y2
PIX[9]	G0	Cr5/Cb5	G1	Cr1	G1	Y1
PIX[8]	B4	Cr4/Cb4	G0	Cr0	G0	Y0
PIX[7]	B3	Cr3/Cb3	R7	Y7	B7	Cb7
PIX[6]	B2	Cr2/Cb2	R6	Y6	B6	Cb6
PIX[5]	B1	Cr1/Cb1	R5	Y5	B5	Cb5
PIX[4]	B0	Cr0/Cb0	R4	Y4	B4	Cb4
PIX[3]	—	—	R3	Y3	B3	Cb3
PIX[2]	—	—	R2	Y2	B2	Cb2
PIX[1]	—	—	R1	Y1	B1	Cb1
PIX[0]	—	—	R0	Y0	B0	Cb0

1.2 Device Block Diagram

Figure 2 shows a block diagram of the encoder core.

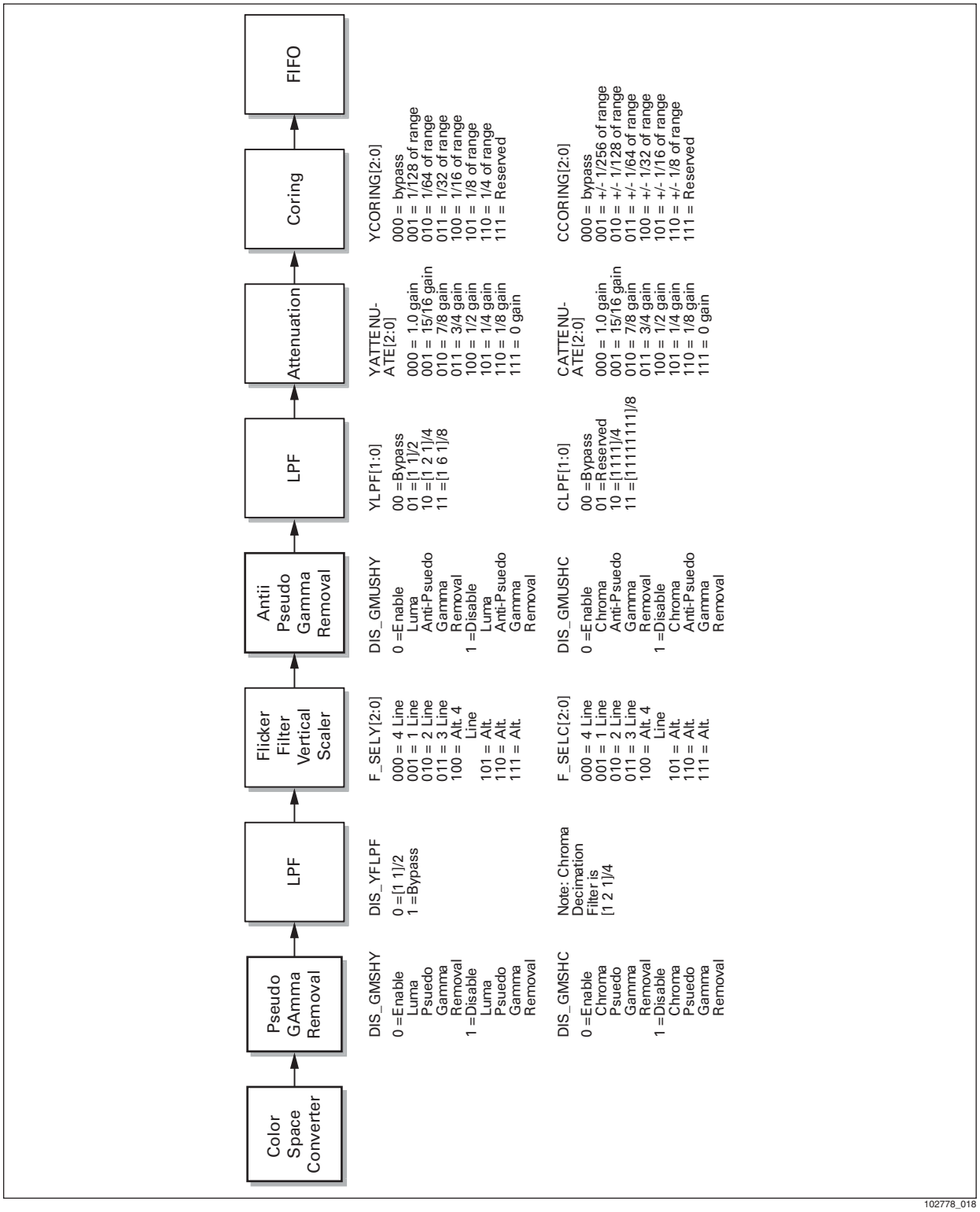
Figure 2. Encoder Block Diagram



1.3 Flicker Filter

Figure 3 shows the flicker filter data path.

Figure 3. Flicker Filter Block Diagram



1.4 Device Description

1.4.1 Overview

The CX25898/9 is a video encoder designed for TV output of interlaced and noninterlaced input graphics data. Common applications requiring flicker-filtered TV output include:

- desktop/portable PCs with TV out
- high-definition TVs
- DVD players and set-top boxes
- graphic cards with TV out
- game consoles
- set-top boxes

It incorporates normal and adaptive filtering technology for flicker removal and flexible amounts of overscan compensation for high-quality display of noninterlaced images on an interlaced TV. The CX25898/9 accomplishes this by minimizing the flicker and controlling the amount of overscan so that the entire image is viewable.

The CX25898/9 consists of a Color Space Converter/Flicker Filter engine followed by a digital video encoder. The Color Space Converter/Flicker Filter contains:

- A timing converter
- Various horizontal video processing functions
- Flicker filter and vertical scaler for overscan compensation

The output of this engine feeds into a FIFO for synchronization with the digital video encoder.

The CX25898/9 provides composite (CVBS), S-Video, Component (YC_RC_B or YUV), R/G/B/PAL Euro SCART, VGA R/G/B, or 3-signal analog RGB or YP_BP_R HDTV output. While the encoder is in HDTV output mode, the device will automatically insert trilevel synchronization pulses and vertical synchronizing “broad pulses.” The CX25898/9 is compliant with EIA770-3, SMPTE 274M/293M/296M and supports the most popular ATSC HDTV resolutions including 480p, 625p (576p), 720p, and 1080i. Finally, this encoder (CX25899 only) supports both standard-definition Macrovision® (version 7.1.L1) and high-definition Macrovision (525p copy protection for progressive scan).

1.4.2 Low-Voltage Digital Graphics Interface

The CX25898/9 can receive or transmit signals from/to a graphics controller at any voltage level from 3.3 V (maximum) to 1.1 V (minimum). The most common lower voltage levels are 2.5 V, 1.8 V, 1.5 V, 1.3 V, and 1.1 V. The default input/output voltage preferred amplitude swing for the graphics interface signals (defined as PIX[23:0], HSYNC*, VSYNC*, CLKI, SLEEP, BLANK*, RESET*, CLKO). This level matches the first and second generation Conexant VGA to TV encoders (Bt868/869 and CX25870/1/2/3/4/5 respectively) and ensures backwards compatibility.

For a 3.3 V digital interface, no special configuration steps are necessary. If this is done on power-up, the encoder will automatically expect 3.3 V signal interface.

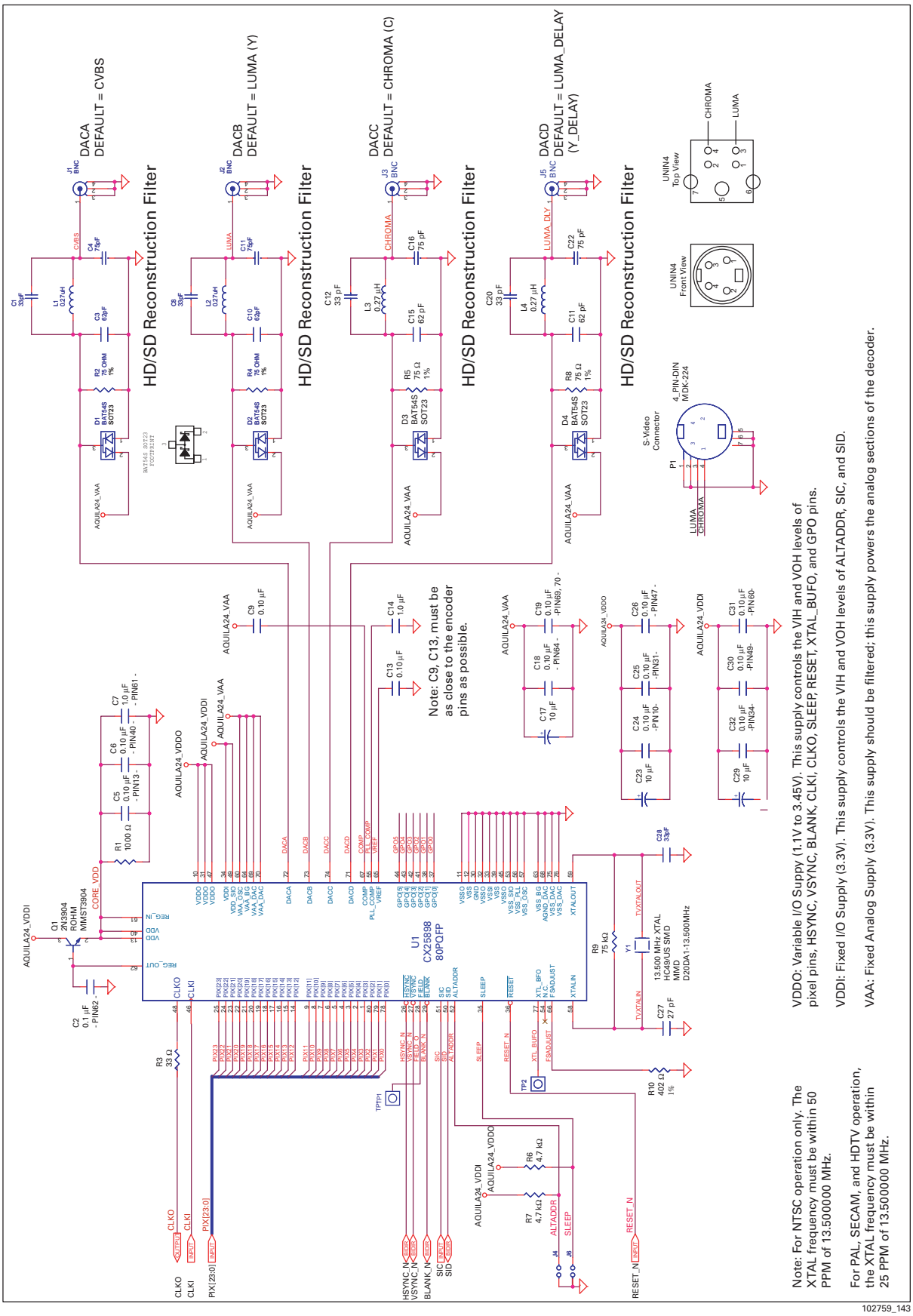
For a 1.5 V or sub 3.3 V digital interface, several special configuration steps are necessary. First, connect the VDDO (pins 10, 31, and 47) power supply pins to the lower supply voltage (1.5 V or other). Second, make sure the graphics controller is configured to send and accept signals at the lower supply voltage.

Adjusting the VDDO pins appropriately controls the input (or output) voltage levels for the PIX[23:0], CLKI, SLEEP, RESET*, FIELD and HSYNC*/VSYNC*, BLANK*, and the GPO [5:0] (in slave interface; EN_BLANKO = 0) digital graphics-related pins.

The REG_IN, REG_OUT pins are associated with the encoder's core voltage and have no influence on the graphics interface nor the serial interface peak-to-peak voltage levels.

NOTE: For a 3.3 V digital interface, refer to the CX25898/9 sample schematic in Figure 4.

Figure 4. Sample Schematic



1.4.3 Reset

There are four reset events possible with this device:

First, if the RESET* pin is held low (between 0.8 V and GND –0.5 V) for a minimum of 1 μs, a timing reset and a software reset are performed. This is called a hardware RESET* event. If the RESET* pin is continually held low, the encoder's SIC and SID lines remain high, allowing other devices on the serial bus to receive commands while the CX25898/9 is in its reset state. No serial communication (reads or writes) with the encoder is possible while its RESET* line is held low. In addition, active video from all DACs will completely disappear, and a 27.000 MHz signal will be sent from CLKO while the RESET* line is held down.

Second, a timing reset can be generated by setting the TIMING_RST register bit. In this case, the subcarrier phase is set to zero, and the horizontal and vertical counters are configured to the beginning of VSYNC* of Field 1 (both counters equal to zero).

The third reset event is a software reset. By setting SRESET bit to 1, all registers are configured internally to their default state. The SRESET bit will be cleared back to zero automatically. A software reset, which can be generated by setting the SRESET register bit, initializes all the serial interface registers to their default state. As a result, all digital output control pins are three-stated. Registers 0x38 and 0x76 to 0xB4 inclusive are then initialized to autoconfiguration mode 0 (see the Auto Configuration section values). The EN_OUT bit must be set to enable the digital outputs.

The final reset event is a power-on reset occurring immediately after correct VDD, VAA, and ground are first applied to the device. A power-on reset is generated on power-up. The power-on reset generates the same type of reset as the RESET* pin. A time delay circuit is triggered after the supply voltage reaches a value sufficiently high enough for the circuit to operate and then generates the power-on reset. As such, the device may not initialize to the default state unless the power supply ramp rate is sufficiently fast enough. A hardware/pin reset is recommended if the default state is required. This event happens automatically regardless of the type of master device connected to the DENC.

If the CX25898/9 is in the master interface (i.e., encoder sends the syncs to the data master) then after a power-on or pin reset, the encoder and the flicker filter start at line 1, pixel 1 of their respective timing generation. For the encoder this means the odd field is always the first field after a power-on reset, pin reset, or timing reset.

In slave timing interface (encoder is either pseudo-master or pure slave), even though the input is receiving progressive frames that have no field associated with it, the input timing generator keeps track of the frames received. As a result, after every second frame received, a frame sync is sent to the encoder section so that the input and encoder remain synchronized. The frame sync forces the encoder to the beginning of the odd field.

A power-on reset, pin reset, or timing reset (register 0x6C, bit 7) causes the input timing generator to send the encoder a frame synchronization pulse setting the encoder to the beginning of the odd field. The first HSYNC*/VSYNC* combination then corresponds to the encoder even field. Then, the second HSYNC*/VSYNC* combination again causes a frame synchronization pulse, and the encoder will start the odd field, and so on and so forth.

1.4.4 Device Initialization

After a non-timing reset event, the CX25898/9 will be configured in autoconfiguration mode 0, pseudo master interface, active video turned off. The device must be programmed through the serial interface to activate a video output (i.e., set EACTIVE bit to 1), and configure the CLKO, HSYNC*, VSYNC*, and FIELD outputs to match the desired interface. The easiest method for accomplishing the initialization phase is to use an appropriate autoconfiguration mode from Appendix B, and switch the interface bits appropriately. (For information on autoconfiguration and interface bits see to Section 1.4.8.)

1.4.5 Clocking Generation and Reference Crystal

Two timing generators control the operation of the encoder. The first generator controls the input timing and processing of image data through the flicker filter and overscan compensation sections to the internal FIFO, which bridges the input and output sections. The output encoder timing block generates the signals for the proper encoding of the video into NTSC, PAL, or SECAM and extracts the processed input pixels from the internal FIFO. The timing generators can receive a clock from either an external crystal oscillator and internal PLL (master, pseudo-master, or slave interface), or from the CLKI pin (slave interface only). The preferred clock source for the timing generation is the internal PLL which uses the XTALIN pin as its reference. The PLL has a main output clock, F_{CLK}, which is defined by the equation that follows later. There is also a secondary output with a different divide ratio so that it is exactly two thirds the frequency of F_{CLK}. Alternately, the pin CLKI can be used as the clock source for the timing generators. Conexant recommends that the encoding clock be generated by an external crystal residing between XTALIN and XTALOUT or a clock oscillator chip driving XTALIN (bias circuit connected to XTALOUT). Register bit EN_XCLK selects the clock source.

Besides the registers that set the various parameters in both the vertical and horizontal direction, the following register bits are used to set the type of video input format.

DIV2—Setting this bit to 1 will change the input from a progressive scan format to an interlaced video format, such as CCIR601. The one exception is for HDTV interlaced format; this bit should remain zero.

DIV2_LATCH—When it is 0, the input data will latch only on the rising edge of clock, as with CCIR601. When it is set to 1, the input data will latch on both edges of the clock, which is useful for a format like interlaced RGB. This bit is only active when DIV2 = 1.

MODE2X—Use this bit for VGA controllers that can only send data on one edge of the input clock. The encoder will only latch pixel data on CLKI's rising edge.

PLL_32CLK—This bit puts the encoder into a clocking mode where the input timing generator still receives the main clock from the PLL, but the output timing now uses the secondary clock. The name derives from the fact that for every three clocks at the input, there are two clocks at the output. This mode is used for standard TV out with all 1024x768 inputs and some 800x600 inputs.

PIX_DOUBLE—This will cause a duplication of each input pixel. This mode is useful for low-resolution formats like 320x240.

EN_XCLK—If set to a logical 0, the internal clock source is selected via the crystal attached to XTALIN/XTALOUT. When the EN_XCLK bit is set to 1, the clock frequency received at the CLKI pin is utilized as the main pixel/encoder clock.

BY_PLL—Setting this bit is not recommended for normal use but only for debug or testing purposes. BY_PLL will bypass the PLL and use the reference clock at the XTALIN pin as the encoder clock source. This bit has a lower precedence than EN_XCLK.

A crystal must be present between XTALIN and XTALOUT pins if the internal clock source is selected. In this case, the CX25898/9's CLK frequency is synthesized by its PLL such that the pixel clock frequency equals

F_{CLK} = Fxtal * {PLL_INT[5:0] + (PLL_FRACT[15:0]/2^{16})}/6

The PLL_LOCK bit is set when the PLL is stable.

When the encoder is the clock master, a delayed version of the clock output from the pin CLKO is returned to the pin CLKI and synchronized with the pixel data. The frequency of this clock is F_{CLK}, except for these two cases:

1. PIX_DOUBLE = 1
2. DIV2 = 1 and DIV2_LATCH = 1.

In these two cases CLKO frequency = $\frac{1}{2}$ F_{CLK}.

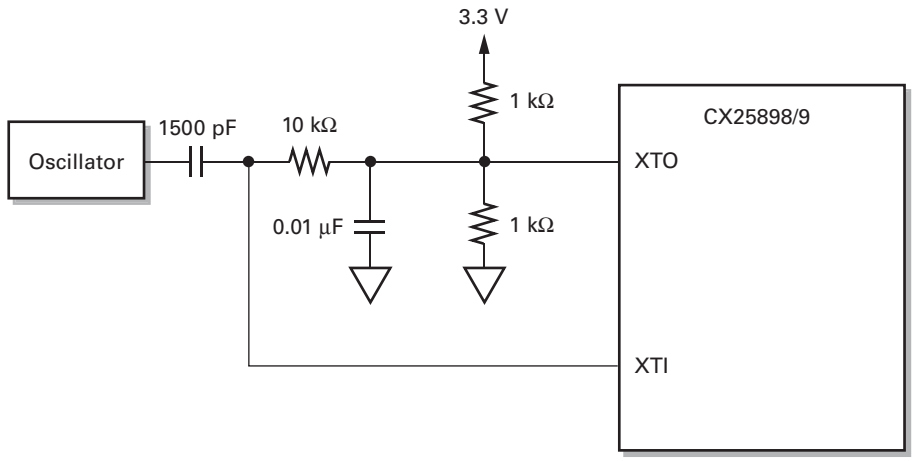
The frequency of the video output clock is determined by the mode of operation set by the bits MODE2X and PLL_32CLK. This frequency is used in the SINX/X correction equation detailed in later sections. The following table shows how this clock is derived from the PLL. As mentioned previously, the main PLL output = F_{CLK} and the secondary PLL output = $\frac{2}{3}$ F_{CLK}.

MODE2X	PLL_32CLK	Video Output Clock Frequency
0	0	Main PLL output
0	1	Secondary PLL output
1	0	1/2 main PLL output
1	1	1/2 secondary PLL output

The crystal must be chosen so that the precise line rate for the video standards required can be achieved. This is done to maintain the subcarrier relationship to the line rate and thereby achieve the precise subcarrier frequency required. The crystal oscillator is designed to oscillate from 10 MHz through 25 MHz. A 13.5000 MHz crystal meets the requirements for NTSC, PAL, SECAM, Component YCRCB, SCART, and HDTV video standards. The crystal must be within 50 ppm of the maximum desired clock rate for NTSC operation, and 25 ppm for any other standard or HDTV video format, across the temperature range (0° to 70° C). If the CX25898/9 is to provide all video outputs selectable through software, the customer must use a crystal with a maximum tolerance across the temperature range of 25 ppm. If a crystal is used, the designer must ensure that the crystal operates with an external load capacitance equal to its specified data sheet listed value (usually C_L). In addition, the external load capacitors used in the crystal circuit must have their ground connections very close to the encoder. Appendix A contains a list of previously tested and recommended crystal vendors.

Optionally, an externally generated 13.5000 MHz clock source may be supplied to the CX25898/9 instead of a crystal. This single-ended clock source can be derived from an external oscillator or dedicated clock generation chip. If an external clock source is used, it should have CMOS label specifications. This 13.5000 MHz clock should be connected to the encoder's XTALIN and XTALOUT pins using the biasing circuit shown in Figure 5. Again, the external source must exhibit ±25 ppm or better frequency tolerance.

Figure 5. Single-Ended Oscillator Biasing Circuit



GENERAL NOTE:

If current through 1 kΩ resistors is deemed to be excessive, substitute a 2 kΩ resistor for each 1 kΩ and retest crystal oscillation and device operation.

102759_020

When the PLL_INPUT register bit is set to a logical 1, CLKI is selected as the reference for PLL after it is divided by two. This is a special mode for slave interface with PLL_32CLK = 1. In this mode, set PLL_INT = 12 DEC and PLL_FRACT = 0

If the external clock source is selected (EN_XCLK=1), a clock signal of the desired pixel clock rate must be present at the CLKI pin. The clock must meet the same requirements as above. It is highly recommended that the internal clock be used in order to ensure the output video remains within the specifications defined by the relevant video standard. Any aberration in the source clock is reflected in the color subcarrier frequency of the output video and detracts from the quality of the image on the television.

If the DIV2 register bit is set, this internal clock is divided by two before driving the first timing generator. This is required for interlaced input to interlaced output mode (i.e., CCIR601/DVD and CCIR656 applications).

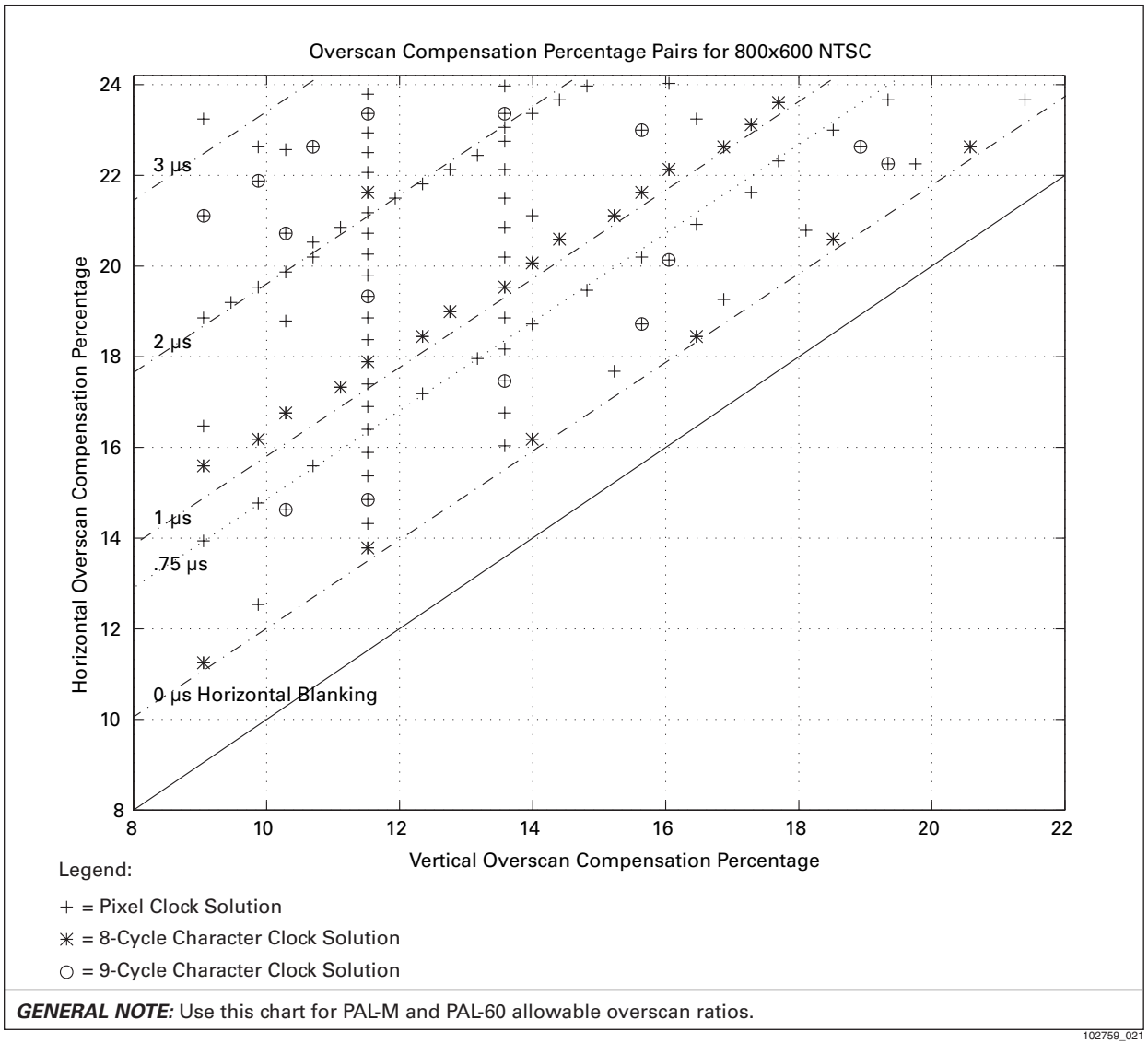
The CLKI pin is the clock used for synchronizing pixel inputs (PIX[23:0]) with the timing input signals (HSYNC*, VSYNC*, and BLANK*) and normally is a delayed version of the CLKO pin. It can be directly connected to CLKO if desired. Data is registered with this input and re-synchronized to the internal clock. In a multiplexed input mode, both edges of the CLKI input are used. If the MODE2X register bit is set, the internal clock is divided by two, allowing a 2x external clock, and data to be provided on the rising edge only. For proper encoder operation, regardless of the interface chosen, a single-ended oscillator must drive the XTALIN pin (and biasing circuit used, see Figure 5) or a crystal must be present between the XTALIN/XTALOUT ports.

1.4.6 3:2 Clocking Mode for Higher Input Resolutions

All graphics controllers require some finite time for resetting their internal counters to zero, clearing register flags, and any other event that needs to be performed on a line-by-line basis. The sum of time these incidents take are the graphics controller's total horizontal blanking time. The amount of horizontal blanking time varies from one master device to another but it is never less than 0 µs and usually does not exceed 4 µs per digital line.

Figure 6 illustrates that when higher active resolutions (i.e., 800x600 or greater), are generated by data master devices that require more horizontal blanking time than the CX25898/9 allows for in standard clocking mode for dual display of certain overscan compensation percentage pairs, a problem can result. For the 800x600 NTSC example, a graphics controller may require a minimum total of 1.25 µs of Horizontal Blanking time per line while clocking a frame with an active resolution of 800x600 to the encoder. If this were the case, the entire set of overscan compensation solutions charted at the 1 µs diagonal plot line (denoted with a dot-dash-dot) and below are made unavailable to the designer. The result is a more limited set of overscan pairs to choose from, and correspondingly less size control for the picture when displayed on a television.

Figure 6. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input/NTSC Output



GENERAL NOTE: Use this chart for PAL-M and PAL-60 allowable overscan ratios.

102759_021

Since the CX25898/9 contains its unique 3:2 Clocking Mode, the designer does not face this constraint any longer. By choosing an appropriate autoconfiguration mode, which sets the PLL_32CLK bit to 1, and altering the values for various timing registers within the controller and encoder (e.g., H_CLKI = HTOTAL, VLINES_I = VTOTAL, H_BLANKI, V_BLANKI, etc.), the encoder switches into the 3:2 Clock mode. While in this operational state, additional solutions in the overscan-compensation-pairs domain for higher resolutions now exist. In addition, the encoder now allows the data master (e.g., graphics controller) to send digital data to it at a faster rate than is clocked out of the encoder. Specifically, the CX25898/9 begins to transfer pixels out at a rate of [2/3] that of the CLKI input frequency. In other words, the pixel input frequency clocks in data at a ratio of [3:2] or 1½ times faster than the CX25898/9 outputs the analog pixel data. In this mode, the encoder's expansive on-chip FIFO bridges the frequency difference that now exists between the digital-timing input and mixed-signal encoder output blocks of the CX25898/9. The result is a much closer match in the available overscan percentages in the horizontal and vertical direction for the higher resolutions. This ensures the TV out picture appears more orthogonal where the amount of blanking is nearly equal on all sides of the image.

Since the horizontal blanking time only becomes a critical issue at higher resolutions, the user should use the 3:2 Clocking Mode only when necessary at the 800x600, between 800x600 and 1024x768, and always at the 1024x768 active resolution. For software programming ease, most of the autoconfiguration modes for 800x600 and all for the 1024x768 resolution are 3:2 mode solutions already. The specific modes that use the 3:2 clock feature are summarized in Table 4.

Table 4. Autoconfiguration Solutions that Utilize 3:2 Clocking Mode

Autoconfiguration Mode #	Active Resolution	Type of Digital Input	Overscan Ratio	Video Output Type
10	1024x768	RGB	Standard	NTSC
11	1024x768	RGB	Standard	PAL-BDGHI
14	1024x768	YCrCb	Standard	NTSC
15	1024x768	YCrCb	Standard	PAL-BDGHI
18	800x600	RGB	Lower	NTSC
22	800x600	YCrCb	Lower	NTSC
26	1024x768	RGB	Lower	NTSC
27	800x600	RGB	Lower	PAL-60
30	1024x768	YCrCb	Lower	NTSC
34	800x600	RGB	Higher	NTSC
40	800x600	RGB	Alternate	NTSC
42	1024x768	RGB	Higher	NTSC
43	1024x768	RGB	Higher	PAL-BDGHI

If the desired overscan ratio is not available, contact your local PAE directly.

1.4.7 Master, Pseudo-Master, and Slave Interfaces

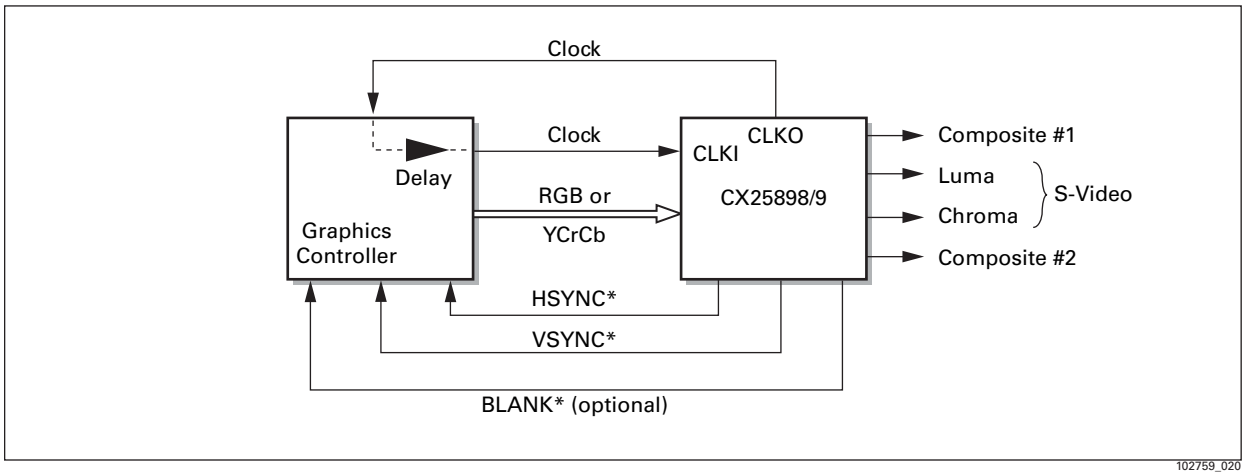
Like its predecessors, the Bt868/869 and the CX25870/1/2/3/4/5, the CX25898/9 encoders can be operated in three possible interfaces. These connection types are named master, pseudo-master, and slave. The clocking ability of the master device and direction of the timing signals dictate what particular interface is used between the Conexant encoder and graphics controller/data master device.

1.4.7.1 Master Interface

In master interface, CLKO, HSYNC*, VSYNC*, and BLANK*, are generated by the encoder as outputs. These signals' leading edges denote when a new clock period, new line, and new frame starts, respectively. Because the encoder transmits the clock and timing signals, this interface is also referred to as clocking master/timing master.

An illustration of the master interface is shown in Figure 7 using the graphics controller as the master device and S-Video and two Composite ports as the video outputs.

Figure 7. Operating the Encoder in Master Interface



A minimum of 9 inputs (CLKI and 8 lines for pixel data PIX[7:0]) and 3 outputs (HSYNC*, VSYNC*, and CLKO) are required for this configuration. The amount of inputs could grow as high as 26 if the 24-bit RGB nonmultiplexed mode with a blank * signal is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

Master interface can only exist if the graphics controller can accept the encoder's reference clock and send back a version of that clock at the same frequency with the pixel data transitions synchronized to CLKI's rising and falling edges. This is accomplished via the VGA encoder's clock output (CLKO) and clock input (CLKI) ports.

1.4.7.2 Reason for BLANK*

If the graphics controller possesses pixel-based resolution (i.e., pixels are only a single pixel clock wide) then the encoder does not have to transmit or receive the BLANK* signal. However, for graphics controllers that are character clock based, a BLANK* signal is necessary.

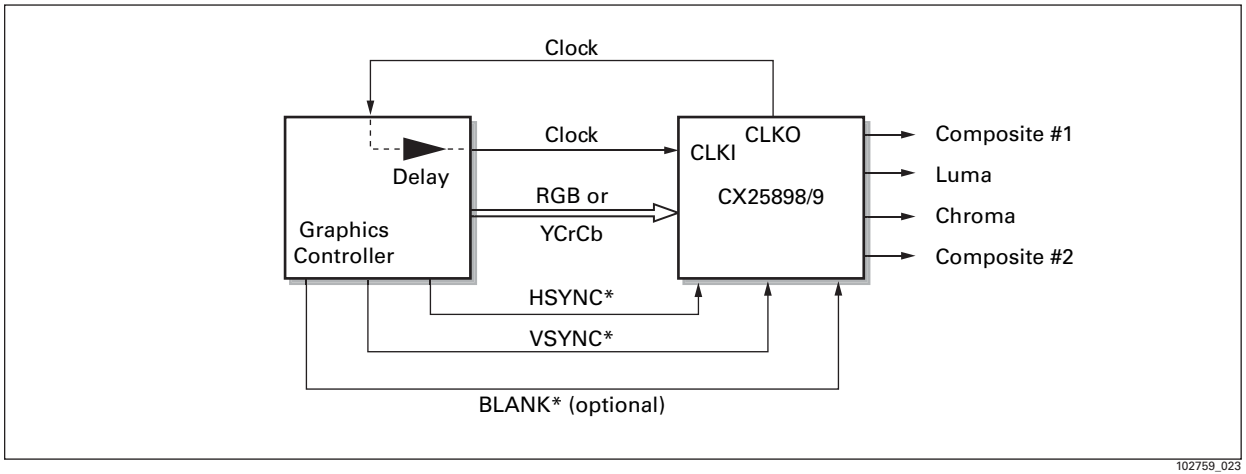
The BLANK line is necessary because a character clock is actually 8 or 9 pixel clocks in duration. This causes several pixel clocks to elapse, resulting in an erroneous delay prior to the next HSYNC* being observed by the encoder and the next line starting. The only method of compensating for this delay is for character clock based controllers to use the BLANK* signal. This signal is required in the physical interface to indicate the exact location of the first active pixel on each line.

1.4.7.3 Pseudo-Master Interface

In pseudo-master interface, the encoder generates a clock reference signal, CLKO as an output. This signal's purpose is to inform the graphics controller the exact frequency at which the data must be sent to the encoder. Timing signals—HSYNC*, VSYNC*, and BLANK*—are received by the encoder as inputs. The leading edges of these signals denote when a new clock period, new line, and new frame starts, respectively. Because this connection scheme shares mastering responsibilities, the interface is also named clocking master/timing slave.

Figure 8 provides an illustration of the pseudo-master interface using the graphics controller as the timing master device.

Figure 8. Operating the Encoder in Pseudo-Master Interface (Default Interface at Power-Up)



A minimum of 11 inputs (CLKI, HSYNC*, VSYNC*, and 8 lines for pixel data PIX[7:0]) and 1 output (CLKO) are required for this configuration. The amount of inputs could grow as high as 28 if the 24-bit RGB nonmultiplexed mode is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

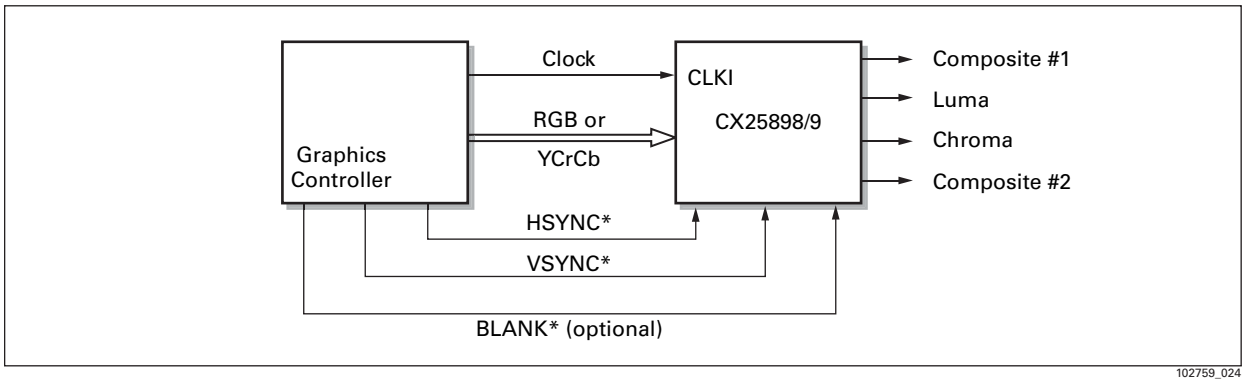
Pseudo-master interface can only exist if the graphics controller can accept the encoder's reference clock and send back a version of that clock at the same frequency with the pixel data transitions synchronized to CLKI's rising and falling edges. This is accomplished via the VGA encoder's clock output (CLKO) and clock input (CLKI) ports.

1.4.7.4 Slave Interface

In slave interface, no output signals are generated by the encoder. The CX25898/9 relies strictly on the graphics controller to send clock and timing signals to trigger when a new clock period, new line, and new frame starts. Because no frequency reference signal is used (CLKO), the master device must pre-program the encoder with an appropriate register set so the encoder expects data at the specific digital pixel rate prior to actually receiving the data. In addition, the timing signals must be shaped so they adhere to the appropriate slave interface timing diagrams illustrated in Section 3.4. Due to the added complexity of this interface, Conexant recommends its use only as a final option.

The slave interface is illustrated in Figure 9 using the graphics controller as the master device and S-Video and two Composite ports as the video outputs.

Figure 9. Operating the Encoder in Slave Interface



A minimum of 11 inputs (CLKI, HSYNC*, VSYNC*, and PIX[7:0]) are required for this configuration. The amount of inputs will increase to 15 (without BLANK*) or 28 (with BLANK*) if 24-bit nonmultiplexed RGB mode is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

It is highly recommended that the device operate in master or pseudo-master interface to ensure that the input and output video streams remain synchronized. If either the master device, supplying the HSYNC* and VSYNC* inputs, or the encoder, which receives the data, is not correctly programmed, the output image will lose lock with the input. By running the CX25898/9 in either clock master interface, any timing errors that occur can be absorbed to some extent by the expansive on-board FIFO, and synchronization problems do not occur.

1.4.7.5 Slave Interface Without a Crystal

Since PAL and SECAM televisions are especially strict in terms of accepting color subcarrier frequencies with more than 25 ppm error (i.e., Fsc ± 338 Hz using a crystal of 13.500 MHz), it is critical that the data master maintain a very high level of accuracy and frequency consistency within the incoming pixel clock in slave interface. In numerical terms, this means that the incoming clock (tied to CLKI) should always remain within a window of {ideal CLKI} ± 25 ppm. As an example, for 640x480 PAL autoconfiguration mode #1, CLKI would have to reside in the range [29.499670 MHz < ideal CLKI = 29.500008 MHz < 29.500746 MHz]. NTSC televisions have slightly more tolerance in terms of the color subcarrier frequency deviation. Most consumer NTSC sets can accept pixel clock rates with up to 50 ppm error (i.e., Fsc ± 675 Hz using a crystal of 13.500 MHz) while still maintaining color within the picture. However, it is still important that the data master maintain a high level of accuracy for the incoming clock for this SDTV format as well. In numerical terms, for 640x480 NTSC autoconfiguration mode #0, the pixel clock (CLKI) would have to reside in the range [28.195118 MHz < ideal CLKI = 28.195793 MHz < 28.196468 MHz].

Tight control of the incoming digital clock ensures that the CX25898/9 generates an analog Fsc (color subcarrier) of 4.433618 MHz ± 338 Hz for PAL-BGHI or 4.250000 / 4.406250 MHz ± 338 Hz for SECAM or 3.579545 MHz ± 675 Hz for NTSC. Actual testing has found that excursions outside this range eventually result in a loss of color for PAL, SECAM, and NTSC consumer televisions.

Often, the only reason that slave interface is used is because the data master or GPU driving the encoder is clock-limited and cannot receive and process the incoming clock from the DENC (i.e., CLKO). As a result, the GPU must use its own internal PLL and transmit the pixel clock frequency needed by the encoder for that autoconfiguration or other TV Out mode. Unfortunately, because the encoder's PLL (m/n) ratio and resolution far exceeds the PLL capability of most GPUs, pixel clock frequency mismatches commonly occur in between what the GPU sends versus what the DENC needs for that particular mode. This mismatch often causes color to be lost in an otherwise stable and synchronized TV out picture because the color subcarrier frequency is skewed by an amount proportional to the difference in frequencies.

Fortunately, color can be re-established so long as the GPU can generate a pixel clock (CLKI) frequency within ± 1 MHz. of the CLKI frequency normally needed by the encoder to support the desired autoconfiguration or other valid custom mode. If this can be done, extra registers (MSC[31:0], PLL_INT[5:0], and PLL_FRACT[15:0]) will also need to be reprogrammed in accordance with the procedures and tables listed in Section 1.4.9, "Adaptations for Clock-Limited Master Devices" of this data sheet. Once these steps have been successfully executed, an accurate color subcarrier frequency will be produced by the CX25898/9 and colorful PAL, SECAM, or NTSC analog output will be seen.

Occasionally, fine-tuning and hand-adjustment of registers 0xAE (MSC[7:0]) and 0xB0 (MSC[15:8]) are required as a final step to fully dial in and remove errors in the color subcarrier frequency. Consult your local Conexant representative for any required technical assistance.

1.4.8 Autoconfiguration and Interface Bits

The default operation of the encoder is tied into its 48 autoconfiguration modes. Autoconfiguring the device occurs when bits CONFIG[5:3] and CONFIG[2:0] in register 0xB8 are programmed to any state from 000000 to 101111. At the conclusion of this serial write, default values are copied from the CX25898/9's internal ROM into the most important timing registers with indices 0x38 and 0x76 to 0xB4, inclusive. All other registers are not changed at the conclusion of an autoconfiguration mode command.

After an autoconfiguration command, the CX25898/9 device remains in the same interface it was in before the command execution. The lone exception to this is autoconfiguration modes #44 and #31, which switch the encoder into pseudo master interface. Depending on which autoconfiguration mode# was initiated, the
CX25898/9 will expect to receive either a 320x200, 320x240, 640x400, 640x480, 720x400, 720x480, 720x576, 800x600, or 1024x768 active digital input frame and output a NTSC or a PAL composite and/or S-video signal. See Table 39 for a description of CONFIG[5:0] and Appendix B for more detail on each autoconfiguration mode.

Using an autoconfiguration mode is the easiest method for bringing up the most popular desktop, game/Direct X, DOS boot-up screen, and DVD resolutions. This is true regardless of the interface used between the encoder and graphics controller. To turn the direction of the SYNCs around and/or change the interface, simply reprogram the encoder via several serial writes.

The bits that control the interface are SLAVE, EN_BLANKO, EN_DOT, and EN_OUT. Since the abilities of graphics controllers vary greatly, Tables 5 through 11 have been compiled to explain the relationship between the Interface bits and the actual interface itself. Even more permutations of the following interfaces are possible but Tables 5 through 11 capture the six most popular architectures and bit settings.

Table 5. Master Interface without a BLANK* Signal (Input or Output)

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb[1] of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb[2] of Register 0xC4)
MASTER BLANK* is an output from the encoder or BLANK* is NOT included as part of the interface.	0	1	0	1

FOOTNOTE:
(1) MSb = Most Significant Bit
(2) LSb = Least Significant Bit

- The state of the SLAVE bit dictates whether the CX25898/9 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. In other words, SLAVE will determine whether the overall interface is master or pseudo-master. The SLAVE bit allows the graphics controller vendor to switch between master video timing and slave video timing through software.
- EN_BLANKO is high (=1), signifying the CX25898/9's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25898/9 to use its internal counters to determine the active versus the blanking regions.
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25898/9 and also enables HSYNC* and VSYNC* outputs.

Table 6. Master Interface with a BLANK Input to the CX25898/9*

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
MASTER BLANK* SIGNAL transmitted to the encoder and received as an input.	0	0	1	1

- The state of the SLAVE bit dictates whether the CX25898/9 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. In other words, SLAVE will determine whether the overall interface is master or pseudo-master. The SLAVE bit allows the graphics controller vendor to switch between master video timing and slave video timing through software.
- EN_BLANKO is low (= 0), signifying the CX25898/9's BLANK* port is an input.
- EN_DOT = 1 telling the CX25898/9 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and where the blanking region starts (falling edge).
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25898/9 and also enables HSYNC* and VSYNC* outputs.

Table 7. Pseudo-Master Interface without a BLANK Signal (Input or Output) to the CX25898/9 (Default at Power-Up)*

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
PSEUDO MASTER BLANK* is NOT included as part of the interface.	1	1	0	1

- SLAVE bit = 1 so the CX25898/9 is the video timing slave. It expects to receive the syncs from the graphics controller.
- EN_BLANKO is high (=1), signifying the CX25898/9's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25898/9 to use its internal counters to determine the active versus the blanking regions.
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25898/9.
- Interface of CX25898/9 encoder after power-up.

Table 8. Pseudo-Master Interface with a BLANK Input to the CX25898/9*

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
PSEUDO MASTER BLANK* SINGAL transmitted to the CX25898/9 and received as an input.	1	0	1	1

- SLAVE bit = 1 so the CX25898/9 is the video timing slave. It expects to receive the syncs from the graphics controller.
- EN_BLANKO is low (= 0), signifying the CX25898/9's BLANK* port is an input.
- EN_DOT = 1 telling the CX25898/9 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and where the blanking region starts (falling edge).
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25898/9.

Figure 10. Slave Interface without a BLANK* Signal (Input or Output)

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)	EN_XCLK (MSb of Register 0xA0)
SLAVE BLANK* is NOT included as part of the interface.	1	1	0	0	1

- After autoconfiguration mode #28 or #29, the CX25898/9 expects active low VSYNC* and HSYNC* signals from the controller. The format of pixels at the input of the encoder needs to be 24-bit YCrCb multiplexed unless modifications are made to the IN_MODE[3:0] 4-bit sequence.
- In addition to Table 10, another bit must be programmed manually with this interface. The most significant bit of CX25898/9 register 0xA0 must be set. This guarantees that EN_XCLK is high (=1) which will allow the CX25898/9 to accept CLKI as the pixel clock source.
- SLAVE bit = 1 means the CX25898/9 is the video timing slave. It expects to receive the syncs from the graphics controller. Since the encoder is in slave interface, the HSYNC* and VSYNC* outputs will be three-stated, and the encoder will be set up to receive these timing signals from the graphics controller.
- EN_BLANKO is high (=1), signifying the CX25898/9's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0, telling the CX25898/9 to use its internal counters to determine the active versus the blanking regions.
- EN_OUT = 0, ensures the clock output port (CLKO) is three-stated from the encoder.

Figure 11. Slave Interface with a BLANK* Input to the CX25898/9

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)	EN_XCLK (MSb of Register 0xA0)
SLAVE BLANK* SIGNAL transmitted to the CX25898/9 and received as an input.	1	0	1	0	1

- After autoconfiguration mode #28 and #29, the CX25898/9 expects active low VSYNC* and HSYNC* signals from the controller. The format of pixels at the input of the encoder needs to be 24-bit YCrCb multiplexed unless modifications are made to the IN_MODE[3:0] 4-bit sequence.
- In addition to Table 11, another bit must be programmed manually with this interface. The most significant bit of CX25898/9 register 0xA0 must be set. This guarantees that EN_XCLK will be high (=1) which will allow the CX25898/9 to accept CLKI as the pixel clock source.
- SLAVE bit = 1 so the CX25898/9 is the video timing slave. It will expect to receive the syncs from the graphics controller. Since the encoder is in slave interface, the HSYNC* and VSYNC* outputs will be three-stated, and the CX25898/9 will be set up to receive these timing signals from the graphics controller.
- EN_BLANKO is low (= 0), signifying the CX25898/9's BLANK* port is an input.
- EN_DOT = 1, telling the CX25898/9 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and the HACTIVE register to denote where the blanking region starts.
- EN_OUT = 0: This will ensure the clock output port (CLKO) is three-stated from the encoder.

NOTE: Autoconfiguration Mode #28 for NTSC DVD Playback and Mode #29 for PAL DVD Playback place the encoder into slave CCIR601-compliant interface where it expects a BLANK* input and YCrCb digital input format. The EN_XCLK bit = 1 in these modes as well.

1.4.9 Adaptations for Clock-Limited Master Devices

Ideally, the graphics controller or proprietary ASIC, in combination with the CX25898/9, operates in either master or pseudo-master interface. Occasionally, using either of the clock master configurations is not possible because the master device does not have the capabilities of receiving a clock from the encoder, nor can it synchronize the digital data with this clock on its return. If either limitation exists, only slave interface can be used for the system configuration. Often, within the slave interface, the data master can only generate certain discrete clock frequencies. This means the encoder has to make extra accommodations for proper Standard-Definition TV (SDTV) out to be displayed.

Fortunately, the encoder does have the flexibility to adapt to almost any incoming clock frequency in the range from 20 MHz to 80 MHz. All that is required is to follow the procedure in Table 9, which forces the encoder to accept a frequency through CLKI that does not match any CX25898/9 autoconfiguration frequency. Once the CX25898/9's 4-byte wide MSC register is reprogrammed accordingly, the result is the generation of the correct color subcarrier frequency for NTSC or PAL and corresponding proper S-Video or Composite TV output.

Tables 9 and 10 contain the procedures required for the encoder to accept a frequency through CLKI that is not equal but is close to the chosen CX25898/9 autoconfiguration mode clock frequency. Completion of the steps contained in the two tables will modify the MSC register and PLL_INT and PLL_FRACT registers correctly and thus produce an accurate NTSC or PAL analog output.

Table 9. Adjustment to the Encoder's MSC Registers

1. What is input frequency to CX25898/9's CLKI input from data master?
2. Depending on answer to step 1, find an autoconfiguration mode that has a frequency close to the incoming input frequency (within 1 MHz is preferred).
3. Look up the clock frequency for the chosen autoconfiguration mode in Appendix B.
4. Determine the scaling factor 'x' where
5. x = input frequency to CLKI input (usually from data master)/ autoconfiguration mode frequency as specified in Appendix B
6. Determine the autoconfiguration mode's MSC[31:0] value in hex by reading back the CX25898/9's registers; 0xB4(=MSb), 0xB2, 0xB0, 0xAE(=LSb). These register values can also be found by looking them up in Appendix B. The values determined will have to be cascaded together.
7. Convert the MSC[31:0] 4-byte hexadecimal value to decimal.
8. Divide the total found from step 6 by the scaling factor 'x' found from step 4.
9. Convert the answer from step 7 to the hexadecimal format. This value should be comprised of a total of 4 bytes. The most significant byte will likely not change from the previous value in register MSC[31:24]. Other MSC values may not change either but the least significant bytes should have definitely been modified.
10. Program the bytes determined from step 8 into the CX25898/9's MSC[31:0] registers. Write these bytes in order to registers 0xB4 (most significant byte = MSC[31:24]), 0xB2, 0xB0, and 0xAE (least significant byte = MSC[7:0]).

Table 10. Adjustment to the PLL_INT and PLL_FRACT Registers

1. What is input frequency to CX25898/9's CLKI input from data master?
2. Depending on answer to step 1, find an autoconfiguration mode that has a clock frequency close to the incoming CLKI frequency (within 1 MHz is preferred).
3. Look up the desired clock frequency for the chosen autoconfiguration mode in Appendix B.
4. Determine the scaling factor 'x' where:
   x = input frequency to CLKI input (usually from data master) / autoconfiguration mode frequency as specified in Appendix B
5. Determine the PLL_INT value in hex by reading back the CX25898/9's register 0xA0 for that autoconfiguration mode. This register value can also be found by looking it up in Appendix B.
6. Convert the PLL_INT register value to decimal.
7. Multiply the answer found in step 6 by 2^{16} = 65536.
8. Determine the PLL_FRACT value in hex by reading back the CX25898/9's register 0x9E and 0x9C. These two registers cascade to form the PLL_FRACT[15:0] 2-byte value. These register values can also be found by looking them up in Appendix B.
9. Convert the 2-byte PLL_FRACT register value to decimal.
10. From steps 7 and 9, add the PLL_INT and PLL_FRACT decimal values.
11. Multiply the total found from step 10 by the scaling factor 'x' found from step 4.
12. Convert the answer from step 11 to the hexadecimal format. The value should be comprised of a total of three bytes. The most significant byte will likely be the original PLL_INT[7:0] byte from step 2.
13. Program the bytes determined from step 12 into the CX25898/9's PLL_INT[7:0] and PLL_FRACT[15:0] registers. The most significant byte from step 12 is the new PLL_INT value. Write this to register 0xA0. The 2 least significant bytes from step 12 is the new PLL_FRACT value. Write these bytes in order to registers 0x9E and 0x9C respectively.

1.4.10 Input Formats

The device can convert a wide range of input formats to analog standard-definition video TV outputs. The input can be either noninterlaced or interlaced active digital data from a minimum of 320x200 to a maximum of 1024 x 768 pixels per frame for standard TV outputs. Many other nonstandard input formats can be encoded as well. For detailed information on the CCIR601 mode, please refer to the *DVD Movie Playback Architecture and Solutions Application Note*. This application note can be obtained from your local Conexant Systems sales office.

For instructions on how to display nonstandard resolutions on the TV, request the *Supporting TV Out with Non-Standard Graphics Input Resolutions Application Note* from your local Conexant Systems sales office. Your local Conexant FAE can also offer assistance in generation of encoder register sets to support nonstandard resolutions.

1.4.11 Input Pixel Timing

The device can accept the input data in either RGB or YCrCb digital formats. Data can be input either a full pixel at a time clocked in on the rising edge of CLKI only (mode 2x = 1), or in various multiplexed modes, using both edges of CLKI.

In YCrCb format, either 24-bit 4:4:4 data or 16-bit 4:2:2 data can be input. In RGB format, either 15-bit 5:5:5, 16 bit 5:6:5, or 24-bit RGB can be input. In 16-bit 4:2:2 YCrCb input format, multiplexed Y, Cr, and Cb data is input through the PIX[11:4] or PIX[7:0] input pins. The Y data is input on the falling edge of CLKI. The Cr/Cb data is input on the rising edge of CLKI. The Cb/Y/Cr/Y sequence begins at the first active pixel. In 24-bit 4:4:4 YCrCb input format, multiplexed Y, Cr, and Cb data is input through the PIX[23:0] inputs. Both the rising and falling edge of CLKI sample the input data.

In RGB input format, input data is sampled as 12 bits at a time in 24-bit RGB format or 8 bits at a time in 15/16 bit RGB format on both the rising and falling edge of CLKI. Table 2 shows the data pin assignments for all available multiplexed input formats.

In addition, several 24-bit and 16-bit alternate multiplexed data formats exist for maximum flexibility. See Table 2 for these pin-to-bit assignments.

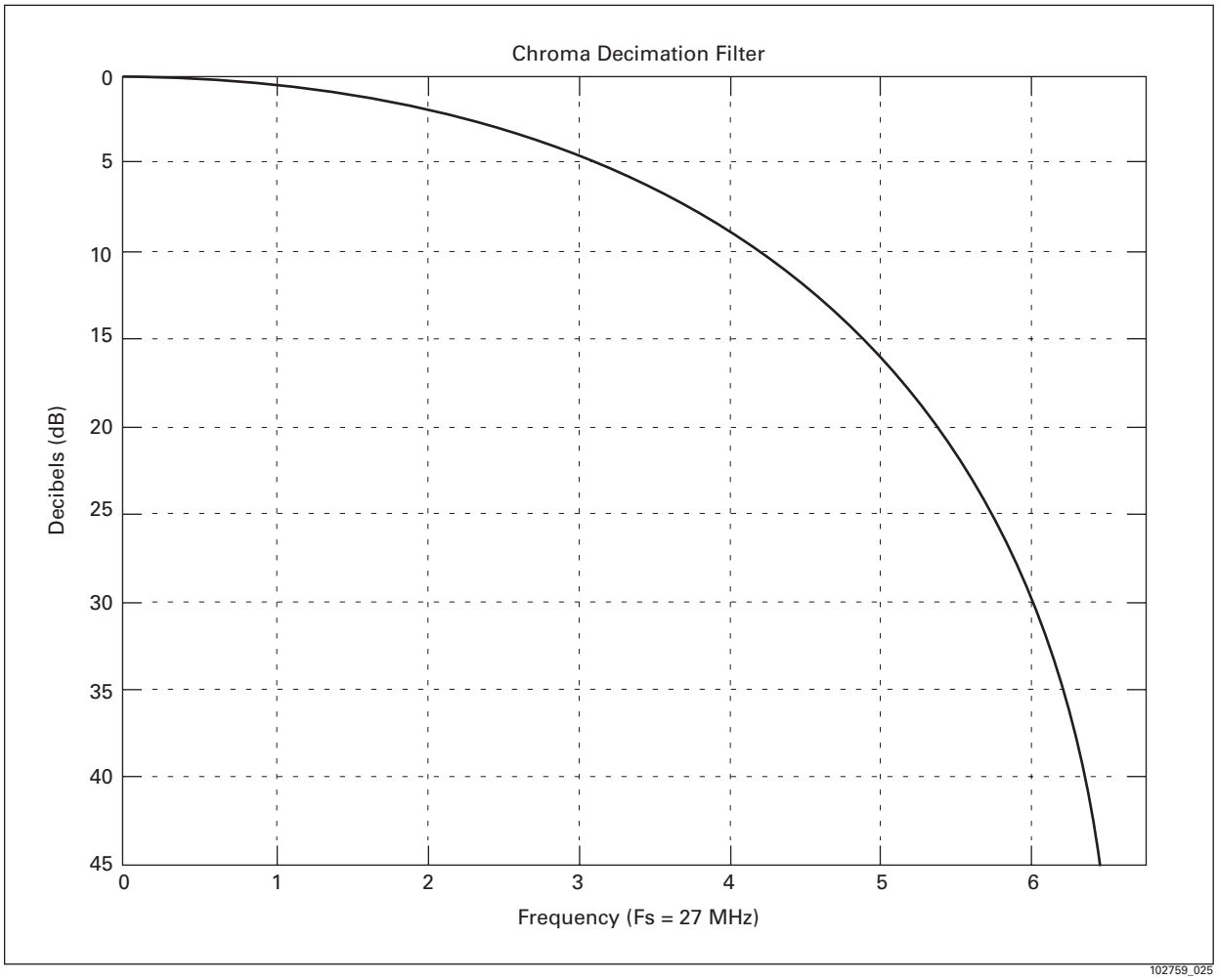
1.4.12 YCrCb Inputs

With the encoder's IN_MODE [3:0] set to YCrCb mode, the encoder must receive digital component YCrCb data as an input. If this occurs, the encoder will convert the YCrCb input to an internal Y/R-Y/B-Y for further processing through the device. Y has a nominal range of 16–235; Cr and Cb have a nominal range of 16–240, with 128 (80 hex) equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

This encoder can also receive either standard YCrCb or HDTV YPrPb digital data for conversion into RGB or YP_RP_B HDTV outputs. It is critical that either pseudo-master or slave interface be used for conversion to HDTV as well.

Figure 12 illustrates the frequency response of the sub-sampling process. If 4:4:4 data is input, it is subsampled to 4:2:2 prior to overscan compensation and flicker filtering.

Figure 12. Decimation Filter Response at Sampling Frequency (Fs) of 27 MHz



The resulting 4:2:2 output must then be converted to YUV values and then scaled for the output range of the DACs. The MY, MCR, and MCB registers must be programmed to perform this conversion. The scaling equations are as follows:

$MY = (int)\ [V100/(219.0 * V_{FS}) * 2^{16} + 0.5]$

$MCR = (int)[(128.0/127.0) * V_{100} * 0.877/(224.0 * V_{FS} * 0.713 * sinx) * 2^{16} + 0.5]$

$MCB = (int)[(128.0/127.0) * V_{100} * 0.493/(224.0 * V_{FS} * 0.564 * sinx) * 2^{16} + 0.5]$

where: V_{100} *= 100% white voltage (0.661 V for NTSC, 0.7 V for PAL/SECAM)*
V_{FS} *= Full scale output voltage (1.28 V)*
F_{sc} = color subcarrier frequency (see Table 54)
F_{CLK} *= Analog pixel rate*
$Sinx = Sin\ (\pi \cdot F_{SC}/F_{CLK})/(\pi \cdot F_{SC}/F_{CLK})$

1.4.13 RGB Inputs

With IN_MODE[3:0] set to a RGB mode, the encoder must receive digital gamma-corrected RGB data as an input. If this occurs, the RGB data will be converted to Y/R-Y/B-Y as follows:

$$Y[9:0] = INT(0.299 * 2^{10} * R[7:0]) + INT(0.587 * 2^{10} * G[7:0]) + INT(0.114 * 2^{10} * B[7:0]) + 2^{7}] * 2^{-8}$$
$$0 \leq Y[9:0] \leq 1023$$

For 15- and 16-bit RGB input formats, individual R, G, and B values are left justified to eight bit numbers.

After the initial conversion, the Y/R-Y/B-Y values are sub-sampled to 4:2:2 data prior to overscan compensation and flicker filtering.

The resulting 4:2:2 output must then be converted to YUV values and then scaled for the output range of the DACs. The MY, MCR, and MCB registers must be programmed to perform this conversion. The scaling equations are:

$$MY = (int)[V_{100}/(255 * V_{FS}) * 2^{16} + 0.5]$$
$$MCR = (int)[(128.0/127.0) * V_{100} * 0.877/(127 * V_{FS} * sinx) * 2^{15} + 0.5]$$
$$MCB = (int)[(128.0/127.0) * V_{100} * 0.493/(127 * V_{FS} * sinx) * 2^{15} + 0.5]$$

where: V_{100} = 100% white voltage (0.661 V for NTSC, 0.7 V for PAL)
V_{FS} = Full scale output voltage (1.28 V)
F_{sc} = color subcarrier frequency (Table 54)
F_{CLK} = analog pixel rate
$Sinx = Sin(\pi F_{SC}/F_{CLK})/(\pi F_{SC}/F_{CLK})$

For SECAM formulas review the SECAM section.

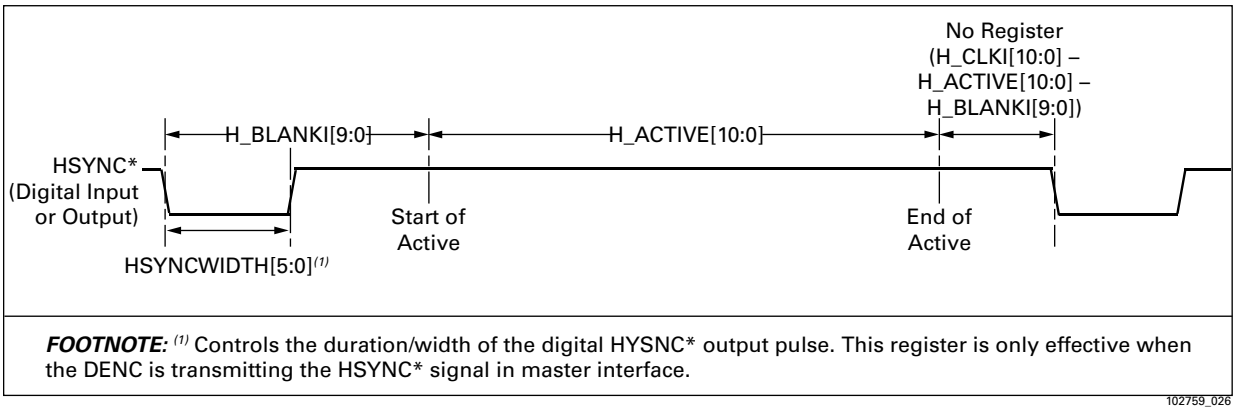
This encoder can also receive RGB digital data for conversion to RGB or YP_RP_B HDTV outputs. It is critical that either pseudo master or slave interface be used for conversion to HDTV as well.

Input Pixel Horizontal Sync

The HSYNC* pin provides line synchronization for the pixel input data. It is an output in master interface and an input in slave and pseudo-master interface. In the master interface, it is a pulse two CLKI cycles (by default) in duration whose leading edge indicates the beginning of a new line of pixel data. The period between two consecutive HSYNC* pulses is H_CLKI CLK cycles. The first active pixel should be presented to the device H_BLANKI minus the internal pipelined clock (5 clock cycles) after the leading edge of HSYNC*. The next H_ACTIVE pixels are accepted as active pixels and used in the construction of the output video. In the slave interface the exact number of clocks per line (H_CLKI) must be provided as calculated for the desired overscan ratio. Only the leading edge of HSYNC* is used, and the low period of the pulse must be at least two CLKI cycles in duration. HSYNC* is clocked into the encoder by the rising edge of CLKI.

The polarity of the HSYNC* signal is changed by the HSYNCI register bit. The default convention is active low. The HSYNCWIDTH register controls the duration/width of the digital HSYNC output pulse when the interface is master. Figure 13 illustrates the relationship between all horizontal timing registers.

Figure 13. Horizontal Timing Register Relationship



FOOTNOTE: *(1)* Controls the duration/width of the digital HYSNC* output pulse. This register is only effective when the DENC is transmitting the HSYNC* signal in master interface.

102759_026

1.4.14 Input Pixel Vertical Sync

The VSYNC* pin provides field synchronization for the pixel input data. It is an output in master interface, and an input in the slave and the pseudo-master interfaces.

For noninterlaced input timing in master interface, VSYNC* is a pulse one horizontal line time in duration whose leading edge indicates the beginning of a frame of input pixel data. The leading edge coincides with the leading edge of HSYNC*. The period between two consecutive pulses is V_LINESI horizontal lines. The first line of active data should be presented to the device V_BLANKI lines after the leading edge of VSYNC*. The next V_ACTIVEI lines are accepted as active lines and used in the construction of the output video.

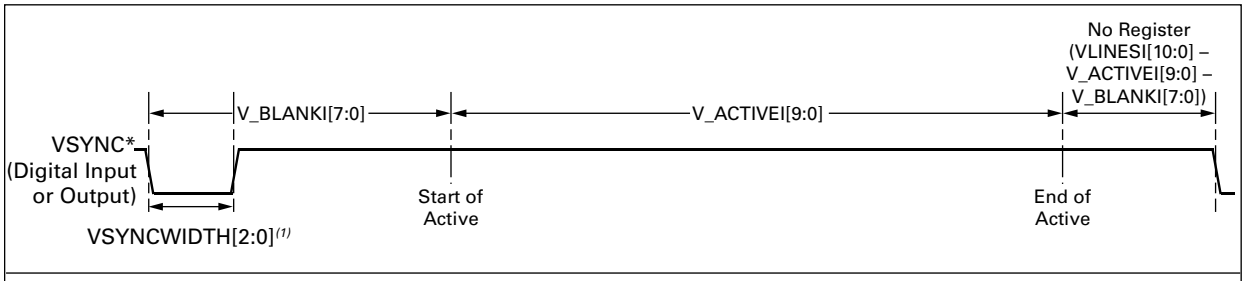
The PC encoder disregards lines after the leading edge of VSYNC* but before VSYNC* + V_BLANKI lines by not encoding them. In slave interface, the period must be exactly the frame rate of the desired video format. Only the leading edge of the VSYNC* is used, and the high and low duration must be at least two CLKI cycles. The beginning of the frame of data is indicated by the next leading edge of HSYNC* coincident with or after the leading edge of VSYNC*.

For interlaced input timing, only the slave interface is supported. The period must be exactly the frame rate of the desired video format. If the leading edge of HSYNC* and VSYNC* are coincident, that indicates the input is in odd field, and the internal line counter is reset to line 1 at the leading edge of VSYNC*. If the leading edges of HSYNC* and VSYNC* are not coincident, and separated by a minimum of two CLKI cycles, this indicates the input is an even field. In this case, the internal line counter is reset to line 2 at the beginning of the next line. Only the leading edge of VSYNC* is used, and the high and low VSYNC* width must be at least two CLKI cycles. VSYNC* is clocked in by the rising edge of CLKI.

The polarity of the VSYNC* input and output can be programmed by the VSYNCI register bit. The default convention is active low. The VSYNCWIDTH register controls the duration/width of the digital VSYNC output pulse when the interface is master. The FLD_MODE bits allow further flexibility in the HSYNC* and VSYNC* timing relationship.

Figure 14 illustrates the relationship between all vertical timing registers.

Figure 14. Vertical Timing Register Relationship



FOOTNOTE: *(1)* Controls the duration/width of the digital VYSNC* output pulse. This register is only effective when the DENC is transmitting the VSYNC* signal in master interface.

102759_027

1.4.15 Input Pixel Blanking

Input pixel blanking can be controlled by either the BLANK* pin or by the internal registers. Blanking can be programmed independently of master or slave interface using the EN_BLANKO register bit. As an output (EN_BLANKO = 1), pixel blanking is generated based on the active area defined by the H_BLANKI, H_ACTIVE, V_BLANKI, and V_ACTIVEI registers. With EN_BLANKO = 1, the BLANK* pin is output in the proper relationship to the syncs to indicate the location of active pixels. As an input (EN_BLANKO = 0), when the BLANK* pin goes high, it indicates the start of active pixels at the pixel input pins. If the blanking area is determined internally, the H_BLANKI and V_BLANKI registers must be programmed properly, as they define the amount of pixels (or lines) that elapse between the leading edge of SYNC and the first active pixel (line). This area is commonly referred to by Graphic Processing Units (GPUs) as the "back porch." There is no register in the DENC that defines the time between the end of active and the leading edge of SYNC ("front porch" area). This parameter is obtained by subtracting H_ACTIVE and H_BLANKI from HCLKI (HTOTAL). The same concept applies vertically. The duration of active data is still determined by the H_ACTIVE register. The BLANK* signal is clocked in by the rising edge of CLKI.

An additional function for the BLANK* pin is used if the EN_DOT register bit is set. If EN_DOT = 1, the BLANK* pin becomes an input whose rising edge defines the data master's character clock boundary. This is used internally by the encoder to keep track of the exact pixel count for controllers that cannot operate at pixel clock rates but instead operate at VGA character clock rates.

The polarity of the BLANK* input/output can be programmed by the BLANKI register bit. The default convention is active low. The BLNK_IGNORE bit only has an effect if the encoder is receiving data in the CCIR656 format.

Table 11 summarizes the direction of the BLANK* signal in each interface. For more information refer to Section 1.4.16.

Table 11. Allowable BLANK* Signal Directions by Interface

Encoder Interface	Allowable Direction of BLANK*
Master	Input or Output
Pseudo-Master	Input
Slave	Input

1.4.16 Overscan Compensation

Overscan compensation is the process by which the encoder converts the digital input lines to the appropriate number of output lines for producing a full-screen image on the television receiver. This conversion is done in accordance with the Vertical Scaling Ratio (VSR). VSR is the ratio of the number of input lines received to number of output lines per field generated by the encoder (i.e., 262.5 lines/field for NTSC and 312.5 lines/field for PAL-BDGHI and SECAM). Using the correct amount of compensation in both the horizontal and vertical dimensions (at least 10 percent) will ensure that the entire digital image normally seen on the PC monitor is satisfactorily mapped to the analog television without any pixels or lines hidden in unviewable or blanked areas.

Increasing the Horizontal Overscan Compensation (HOC) percentage while keeping the Vertical Overscan Compensation (VOC) percentage the same will have several effects on the VGA Encoder. First, the number of output clocks per line (H_CLKO) will increase. Correspondingly, the clock frequencies shared between the data master and the encoder (i.e., CLKO = CLKI) will increase. Therefore, the original number of active pixels will be squeezed into a smaller analog video display region because the frequency at which input data is clocked into the CX25898/9 has increased. Since the CX25898/9 now processes active data at a faster rate than CCIR601-only compatible encoders, the graphics controller will need to transmit more blank pixels per line (i.e., HTOTAL must increase to match CX25898/9's H_CLKI) to make up the difference.

Increasing the (VOC) percentage while keeping the Horizontal Overscan Compensation percentage the same will have several different effects on the VGA Encoder. First, the H_CLKO total will stay the same as will the pixel rate (i.e., CLKI = CLKO). These parameters are dictated by the HOC value only. Second, the number of total vertical input lines (V_LINESI = data master's VTOTAL) will increase, which will increase the internal VSR. The net result is that more active pixels and more active lines will be used to generate each output line. The only way for the graphics controller to transmit these additional input lines with the same clock frequency as before is to decrease the amount of blanked pixels per line.

To support a custom overscan ratio, an entire set of overscan compensation calculations is required. This results in as many as 25 new register values for the VGA Encoder. For overscan selection, contact your Conexant FAE. Each computation is somewhat interdependent on the others but the basic overscan equations are as follows:

(*) VSR = (V_LINESI) / (# of total output lines per field)

and

(**) # Blanked Pixels = {[H_CLKO / VSR] – H_ACTIVE}

For illustrative purposes, the calculations used to generate the 13.785 percent HOC percentage for Autoconfiguration Mode 0–640x480 RGB in, H_CLKO = 1792, NTSC output, are shown below:

From Appendix B:

Number of clocks necessary to latch in the V.S.R. # of input lines for every 1 analog output line = 1792 CLKs [i.e., H_CLKO]

Encoder must ensure input is 2X upsampled.

Therefore:

active CLKs per analog line = 2*(H_ACTIVE)

active CLKs per analog line = 1280 active CLKs per analog line

percent of input used to create active video area = {1280 active CLKs / 1792 total CLKs} = 71.4286 percent

Therefore:

(x) = active region percent of analog output line = 71.4286 percent

(y) = active region percent of typical analog video for NTSC = 52.65556 µs / 63.55556 µs = (y) = 82.4945 percent of line is active

Ratio of [x/y] = {71.4286 percent / 82.4945 percent} = 0.862147

HOC percentage = 1–{Ratio of [x/y]}

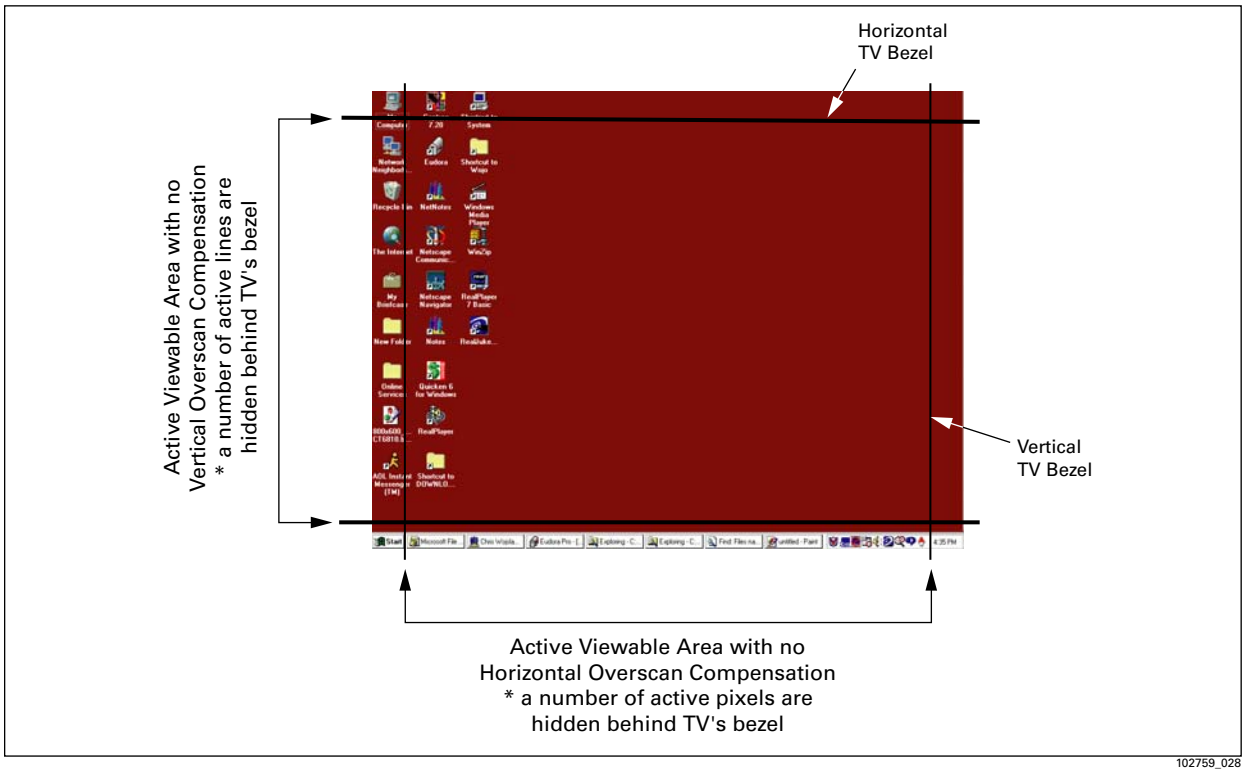
HOC percent = 1–0.862147 = 13.785 percent = HOC percentage for Autoconfiguration Mode 0

As a result, 13.785 percent of the horizontal active region within each line of an NTSC signal will be forcibly blanked by the encoder. For most TVs, this will resize the upsampled digital image properly so all of the pixels fit horizontally within the bezeled area of North American or Japanese TVs. The 13.785 percent overscan percentage is equally distributed on either side of the horizontal active region (i.e., 13.785 percent / 2 = 6.89 percent extra blanking for the beginning and end of the line). The original 640 active pixels (i.e., H_ACTIVE) will then be squeezed into the remaining analog active region with the faster pixel rate.

The explanation of the vertical overscan percentage value is similar. For autoconfiguration mode #0, V_ACTIVEO is 212, which means there are 210 full active lines per field. The first and last lines are filtered lines that assist in smoothing the transitions into and out of the active region to avoid flickering and are not counted. Any NTSC standard calls for 243 active lines per field, so 210/243 = 0.864198 of the vertical active region is used. This calculation yields a vertical overscan compensation percentage of 100–86.4198 = 13.5802 percent.

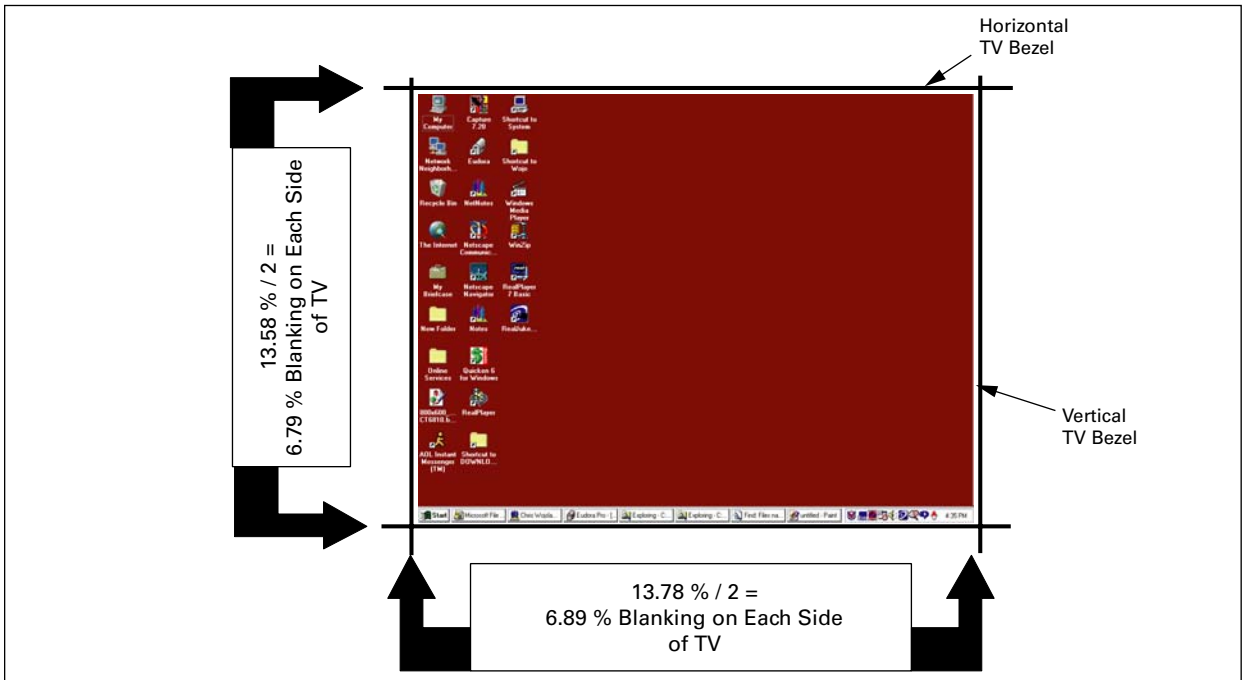
Flicker filtering, vertical overscan compensation, and horizontal overscan compensation are NOT SUPPORTED in any interlaced RGB or YCrCb input format sent to the VGA Encoder. Interlaced input data is commonly used as a DVD output format from a MPEG2 Decoder chip. Because of the data and image content types, flicker filtering and overscan compensation are not necessary in this case. Before and after effects of overscan compensation are illustrated in Figures 15 and 16.

Figure 15. Windows Desktop TV Out Image from Encoder without Overscan Compensation



102759_028

Figure 16. Windows Desktop TV Out Image from CX25898/9 with Overscan Compensation



GENERAL NOTE: Overscan percentages taken from CX25898/9's Autoconfiguration Mode 0.

102759_029

In Figure 16, the VGA Encoder overscan compensated the 640 horizontal active pixels of data to fit within the viewable video region. With 13.78 percent HOC, the active data is contained within a 45.397 μs. portion of time within each active line while the remaining 7.26 μs (52.65556 μs.–45.397 μs.) part of the active region is blanked by the encoder.

The net result of overscan compensation will be an interlaced NTSC, PAL, or SECAM video image that fits within the bezel area of a TV Monitor. Correct choice of the HOC and VOC percentages is important so that no regions of the active input image will be hidden behind the plastic of the TV unit. Various TVs require different HOC and VOC values to fully utilize the entire viewable area of the TV. Varying amounts of blanking would be required depending on the HOC and VOC percentages and active input resolutions.

Ultimately, the blanked regions are dictated by the BLANK* signal itself and/or the internal pixel counter for the CX25898/9. Actual transmission of null or blanked pixels is not necessary since the encoder ignores any data sent to it via the pixel input port within the blanked regions. Only the active pixels need to be sent to the encoder from the controller during the digital active period.

1.4.17 Standard Flicker Filtering

To understand what flicker filtering is, one must understand two of the primary differences between the analog video standards used by TVs and the technology used in today's computer monitors.

First, computer monitors receive their video signal in a more basic, pristine form than TVs do. As discussed earlier, the video signal sent by a computer to its monitor is broken into multiple electrical components (red, green, blue, and sync) while a TV signal has all necessary information combined into a single composite signal or separate Luma and Chroma analog channels (S-Video). In order to process this composite signal, a TV must break it up into its original components, inevitably degrading the picture's brightness, saturation, and hue quality and creating distortions.

A second factor contributing to the decreased quality of images displayed on TV monitors is interlacing, a technique by which a complete TV picture is drawn in two passes from the top to the bottom on the picture tube. In interlacing, the first pass paints all the odd lines, and the second pass paints the even lines. Noticeable flicker occurs when the images in the odd lines are very different from the images in the even lines. As the odd and even lines are alternately displayed, the eye perceives the quick appearing and disappearing of visual information. This results in the irritation called flicker. Flicker is especially noticeable when viewing thin horizontal lines that only take up a single row within the odd or even field. If, for example, the line happens to be on an odd row, it totally disappears every time the even rows are displayed, resulting in that item appearing and disappearing at the field rate on the TV.

Unlike TV monitors, computer monitors paint an entire image in one pass from top to bottom, in a display format called noninterlaced or progressive. Images displayed in a noninterlaced format do not suffer from the same flicker problems.

For improved image quality and reduced flickering, the Conexant PC Encoder contains a 5-tap or 5-line flicker filter for both the Luma (F_SELY[2:0]) channel and Chroma (F_SELC[2:0]) channel. Conexant's standard flicker-filter works by applying a mathematically weighted, user-selected 2, 3, 4, or 5-line averaging algorithm to the incoming pixels of data. This slightly alters the digital information that is processed for eventual conversion to the odd and even lines of a TV picture so that the alternating lines are more similar to each other. This way, when the lines appear and disappear in the interlacing process, the flicker is less noticeable. The more similar the lines are made to appear, the less flicker is visible.

As the flicker artifact is reduced further and further, more and more information is being altered by the encoder and potentially lost from the original picture. Vertical resolution is therefore sacrificed and text clarity suffers, especially for small fonts below 10 points (10/72 of an inch) in size. For this reason, the amount of flicker filtering is programmable and should be controlled by the end user. Finding an optimal standard flicker filter setting for Luma and Chroma is somewhat subjective in nature and ensures that a pleasing image is seen on the television.

Unlike other vendors' encoder products, the CX25898/9 integrates both a standard flicker filter and additional adaptive flicker filter. This implementation allows for the preservation of small font text clarity and other tiny video details lost with only one filtering step. The adaptive feature eliminates more flicker with less loss of resolution because it is able to selectively apply a more aggressive flicker reduction level only to those portions of an image where the effect will be beneficial. Encoders lacking this adaptive filter apply the standard

flicker filtering process to the entire screen. Small text and icons often become unreadable, and thin, horizontal lines often completely disappear. The CX25898/9's adaptive flicker filter prevents this from happening and is described in Section 1.4.18.

As long as progressive RGB or YCrCb data is received in encoder mode, the CX25898/9's flicker filter is effective with any active resolution from 320x200 to a maximum of 1024 x 768. The flicker reduction is present on any interlaced standard-definition video output such as NTSC, PAL, or SECAM. The DIS_FFILT register bit turns off the standard flicker filter. The vertical scaling can be disabled by setting the internal V_SCALE register to 4096 for a noninterlaced input. Finally, the CX25898/9 supports up to 24-bit color processing, meaning that the converted image will feature the same depth of color as the original computer picture.

While the CX25898/9 is generating a VGA style RGB or a YP_RP_B or RGB HDTV set of outputs, the standard flicker filter cannot be utilized. This is the case regardless of the resolution (480p, 720p, 1080i, etc.) received by the Conexant device.

1.4.18 Adaptive Flicker Filter

Adaptive Flicker Filtering is an enhanced feature included with the CX25898/9. It allows the encoder to automatically alter the amount of flicker filtering based on the image being processed. The result is a higher-quality optimized image because a superior balance between vertical resolution and flicker reduction has been achieved. The adaptive flicker filter is enabled via the ADPT_FF bit. There are four possible settings ranging from 2-line (most observable flicker, greatest vertical resolution) to 5-line (minimal observable flicker, moderate vertical resolution). The luminance and chrominance outputs are independent in terms of the level of adaptive flicker filtering. When the adaptive flicker filter is on, the manual flicker filter is off and vice versa.

Vertical filtering in the PC Encoder serves three purposes:

- Vertical polyphase interpolation filtering to upsample the image data vertically. This increases the resolution and accuracy of the subsequent vertical downsampling required to fit the entire image into the visible region of the television.
- Anti-alias filtering to reduce aliasing artifacts when downsampling vertically.
- Flicker filtering to reduce the flicker produced when vertical high-frequency content is displayed on an interlaced device.

The vertical interpolation filtering and vertical anti-alias filtering requirements are driven by the amount of vertical down scaling required, and do not vary substantially with image content. The flicker filtering requirement, however, is dependent upon the image content.

Regions of the image with vertical high-frequency content will flicker in proportion to the amplitude of that high-frequency content. Regions with high-amplitude, vertical- high frequency content require substantial flicker filtering, but regions with low amplitude or no vertical high-frequency content require little or no flicker filtering.

For this reason, the CX25898/9 provides adaptive flicker filtering. It analyzes the image content to detect areas that require strong flicker filtering, and adjusts its vertical filtering to apply stronger flicker filtering to those regions. This analysis and adjustment occurs on a pixel by pixel basis, so each pixel in the output line has the optimal amount of flicker filtering applied to it.

The Adaptive_FF1 and Adaptive_FF2 registers (0x34 and 0x36) configure the adaptive algorithm. The Y_ALTFF[1:0] and C_ALTFF[1:0] fields allow the selection of the alternative (i.e., usually stronger) flicker filter level to combine with the standard flicker filter level selected by fields F_SELY[1:0] and F_SELC[1:0] (register 0xC8). This creates an array of flicker filters for the Y channel and C channel respectively. The actual flicker filter amount applied for a given pixel output depends on the detection and location of any high-amplitude vertical high-frequency content within the input samples that creates that output pixel.

The amplitude of the high-frequency content that triggers an adaptation of the flicker filter can be adjusted via the Y_THRESH[2:0] and C_THRESH[2:0] bit fields. The FFRTN bit offers two ways to combine the standard and alternate flicker filters to generate an array of flicker filters. The YSELECT bit allows the Chroma channel flicker filter to be adapted based on the Chroma channel or the Y (i.e., Luminance) channel content.

NOTE: Neither standard nor adaptive flicker filtering is supported by the CX25898/9 in noninterlaced video output formats (VGA style RGB or YUV, HDTV 480p, 525p, 540p, 625p, or 720p), or interlaced HDTV (1035i or 1080i).

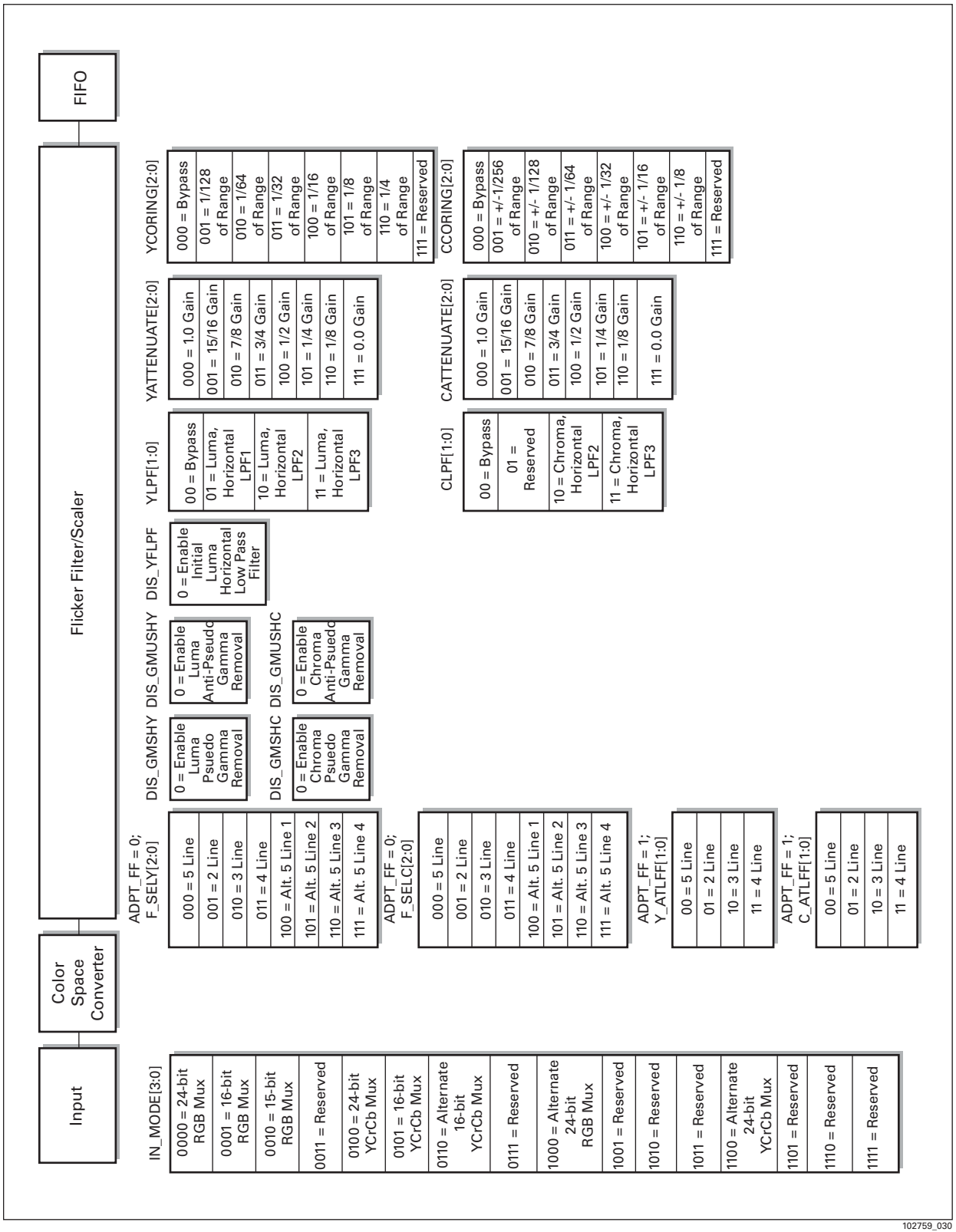
Table 12 summarizes recommended configurations of the adaptive flicker filter for various types of image content and resolutions. Figure 17 illustrates the standard and adaptive flicker filter control registers and their control levels. The internal low-pass filter, brightness, saturation, and coring control levels are also shown.

Table 12. Optimal Adaptive and Standard Flicker Filter Settings for Common PC Applications and Resolutions

	Standard FF settings		CX25898/9 Adaptive FF settings								
Desktop Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**YSELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	3-line	3-line	On	4-line	4-line	000	000	On(2)	On(2)	1	0
640x480 in, PAL-BDGHI out(3)	3-line	3-line	On	4-line	4-line	100	100	On(2)	On(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	010	010	Off(2)	On(2)	1	0
800x600 in, PAL-BDGHI out(3)	4-line	4-line	On	5-line	5-line	010	010	On(2)	On(2)	1	0
1024x768 in, NTSC out(1)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0
1024x768 in, PAL-BDGHI out(3)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0
Web Page Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**Y_SELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	4-line	3-line	On	4-line	4-line	100	100	Off(2)	Off(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	010	010	Off(2)	Off(2	1	0
1024x768 in, NTSC out(1)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0
Word Processing Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**Y_SELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	3-line	3-line	On	4-line	4-line	010	010	Off(2)	On(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	100	100	On(2)	Off(2)	1	0

FOOTNOTE:
(1) NTSC-J, PAL-M, and PAL-60 video outputs should use the NTSC standard and Adaptive FF settings.
(2) On denotes a 1 bit setting. Off denotes a 0 bit setting.
(3) PAL-N, PAL-M, and PAL-60 video outputs should use the PAL-BDGHI standard and Adaptive FF settings.

Figure 17. Flicker Filter and Video Adjustment Control Diagram



1.4.19 VGA Registers Involved in the TV Out Process

Timing constraints for the Conexant encoder are driven by the timing requirements of the analog video output (NTSC, PAL, or SECAM) together with the active resolution and overscan compensation ratio (i.e., amount of blanking in the active region) of the television image. To explain what specific CRTC or VGA registers within the graphics controller need to be involved in displaying a nonstandard or desktop format on both a TV and CRT, one can work backwards from those output signal timing requirements to determine the input timing requirements.

Each output field has a vertical blanking region and an active region. These regions are defined relative to the vertical sync pulse, horizontal sync pulse, given format (i.e., number of lines per field), and a given pixel clock frequency (i.e., number of pixel clocks per line). Within each line of the active region there is a horizontal blanking period (that includes a horizontal sync pulse) and an active period (where the image data is located). Given those parameters, at least six registers within every generic graphics controller need to be changed for display of each active and total resolution.

Table 13 lists the VGA/CRTC registers of the data master involved in the TV out process.

Table 13. VGA/CRTC Registers Involved in TV Out Process

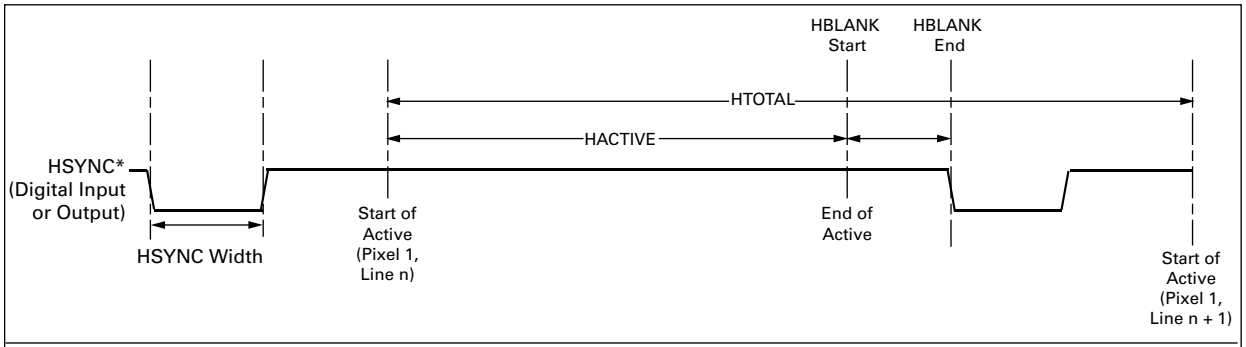
Register Name	Description
Start VBLANK/VSYNC* and End VBLANK/VSYNC*	These VGA registers work in combination with each other to control the scan line at which the vertical blanking period begins and the point at which it ends. This register pair correlates closely to the encoder's V_BLANKI value.
VACTIVE (or Vertical Display End)	Dictates the specific number of active lines for the present digital frame. VACTIVE should equal the encoder's V_ACTIVEI value.
VTOTAL	Specifies the number of scan lines from one VSYNC* active to the next VSYNC* active pulse. The difference between VTOTAL and VACTIVE is the amount of blanked lines. VTOTAL should equal the encoder's V_LINESI value.
Vertical Retrace Start(1) and Vertical Retrace End(1)	Controls the start of the vertical retrace pulse which signals the display to move up to the beginning of the active display. This field contains the value of the vertical scanline counter at the beginning of the first scanline where the vertical retrace signal is asserted. The end of this pulse is controlled by the Vertical Retrace End register. The Vertical Retrace Start register is always greater than HACTIVE and Start VBLANK, but less than Vertical Retrace End. The Vertical Retrace End register is always less than VTOTAL and less than or equal to End VBLANK.
HBLANK/HSYNC* Start and HBLANK/HSYNC* End	This VGA register set works in combination with each other to control the value of the pixel or character clock counter where the HSYNC* signal becomes active and the position at which HSYNC* becomes inactive. This register pair correlates closely to the encoder's H_BLANKI value.
HACTIVE (or Horizontal Display End)	Dictates the specific number of active pixels per line. HACTIVE should equal the encoder's H_ACTIVE value.
HTOTAL	Specifies the number of pixel clocks or character clocks from one HSYNC* active to the next HSYNC* active pulse. In other words, this is the total time required for both the displayed and non displayed portions of a single scan line. The difference between HTOTAL and HACTIVE is the amount of blanked pixels per line. HTOTAL should equal the encoder's H_CLKI value.
Horizontal Retrace Start(1) and Horizontal Retrace End(1)	Specifies the pixel clock at which the GPU begins sending the horizontal synchronization pulse to the display which signals the VGA monitor to retrace back to the left side of the screen. The end of this pulse is controlled by the End Horizontal Retrace register. This pulse may appear anywhere in the scan line, as well as set to a position beyond the Horizontal Total register which effectively disables the horizontal synchronization pulse. The Horizontal Retrace Start register is always greater than HACTIVE and HBLANK Start, but less than Horizontal Retrace End. The Horizontal Retrace End register is always less than HTOTAL and less than or equal to HBLANK End.

FOOTNOTE:

(1) These registers affect timing and the image on a VGA monitor much more so than the timing required by the encoder for TV out. For some GPUs, these registers might not have any effect on the digital timing required for TV out.

Figure 18 illustrates the relationship between all horizontal timing registers in a generic GPU. This timing diagram may not reflect the functionality of all GPUs including those for notebook PCs, set-top boxes, or other types of consumer systems. The designer is strongly urged to consult the data sheet of other vendors' products to confirm their timing relationships and CRTC register functionality.

Figure 18. Horizontal Timing Relationship—Generic GPU

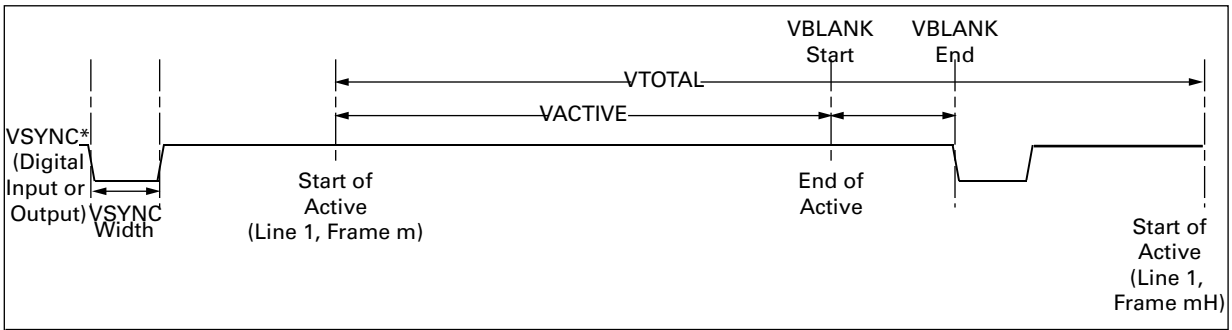


GENERAL NOTE: Figure 18 does not match the horizontal timing register relationship of the CX25898/9 encoder illustrated in Figure 13. There are several subtle differences such as the GPU's first pixel being equivalent to the start of active. Conversely, the encoder's first pixel is always considered to be the beginning of HSYNC*.

102759_031

Figure 19 illustrates the relationship between all vertical timing registers in a generic GPU.

Figure 19. Vertical Timing Relationship—Generic GPU



GENERAL NOTE: Figure 19 does not match the vertical timing register relationship of the CX25898/9 encoder illustrated in Figure 14. There are several subtle differences such as the GPU's first line being equivalent to the start of active. Conversely, the encoder's first line is always considered to be the beginning of VSYNC*.

102759_032

To achieve VGA compatibility, the controller must manipulate some of its own VGA register settings in order to produce a hi-quality dual display on both the computer monitor and TV. It should be noted that the encoder has no way of knowing that a different VGA mode has been selected. As a result, it relies on the serial bus master device to reconfigure it via an autoconfiguration mode or complete register set rewrite to make adjustments in its timing.

When the two devices are programmed correctly, (i.e., matching HTOTAL, VTOTAL, HACTIVE, VACTIVE) regardless of the interface, the required input HSYNC*/VSYNC* to first input active pixel or line spacing matches the output HSYNC*/VSYNC* to first output active pixel or line spacing. When this occurs, the graphics controller always transmits active data at the time the CX25898/9 expects to receive it. Superior TV out quality is achieved only when this type of timing symmetry exists.

1.4.20 Output Modes

The CX25898/9 encoder can generate following types of video outputs: Composite (CVBS), S-Video (separate Luma [Y] and Chroma [C] channels), YUV, Component 480i YC_RC_B, VGA-style RGB, Euro SCART, Component (YP_RP_B) for HDTV, or RGB for HDTV. These outputs are selected by the OUT_MODE[1:0] register bits in combination with the HDTV_EN and EN_SCART bits.

While the encoder is in VGA style RGB, no color space conversion is possible from input to output. Analog RGB is transmitted from a digital RGB input and analog YUV is output from a digital YCrCb input.

When outputting standard-definition RGB, the device outputs VGA/SVGA analog RGB with a bilevel sync. In this mode, the R, G, and B input data is fed to the DACs after the addition of a horizontal sync and, if the SETUP bit is 1, a setup pedestal is added. The output currents are scaled so that the DACs output the proper 1 V full-scale (sync tip to peak white) levels for driving a CRT monitor. The graphics controller must provide all the timing control (including separate HSYNC and VSYNC signals) for the monitor, which results in the encoder operating as a slave in this case. Only the PIX[23:0], BLANK*, HSYNC*, and VSYNC* input pins and the RGB analog output pins are active. The BLANK*, HSYNC*, and VSYNC* pins are automatically enabled as inputs in this mode.

Each of the four video signals generated by the OUT_MODE[1:0] field can be multiplexed to any DAC using the OUT_MUXA[1:0], OUT_MUXB[1:0], OUT_MUXC[1:0], and OUT_MUXD[1:0] register bits. To do this, program the 2-bit value representing the desired type of output into the appropriate OUT_MUXx[1:0] register. As an example, suppose a system requires Composite video (i.e., 00 binary) to be output from DAC_A, chroma (10) on DAC_B, luma (01) on DAC_C, and Composite video (00) on DAC_D. This scheme could be accomplished by programming register 0xCE with 0001 1000 binary or 18 hex.

The LUMADLY[1:0] register bits control the amount of delay for the Y_DLY (11 binary) analog output. The allowable delay ranges from 0 (no delay) to 3 pixel clocks.

All digital-to-analog converters are designed to drive standard video levels into a combined RLOAD of 37.5 Ω (doubly-terminated 75 Ω loads to ground). Unused outputs should be disabled by setting the corresponding DACDISx bit to minimize the supply current or left as a no connect. Disabling unused DAC outputs reduces cross chroma distortion and improves overall picture quality.

1.4.21 Analog Horizontal Sync

The HSYNC_WIDTH[7:0] register determines the duration of the horizontal sync pulse embedded within each standard-definition analog line. The beginning of the horizontal sync pulse corresponds to the reset of the internal horizontal pixel counter. The horizontal line rate is determined by the H_CLKO[11:0] register. The internal horizontal counter is reset to 1 at the beginning of the horizontal sync and counts up to H_CLKO.

The sync rise and fall times are automatically controlled. The sync peak-to-peak amplitude is programmable over a range of values by SYNC_AMP[7:0]. Incrementing the SYNC_AMP by 1 increases the sync amplitude of the analog sync pulse by 30 mV.

1.4.22 Analog Vertical Sync

The analog vertical sync duration is selectable as either 2.5 total lines or 3 total lines by the register bit VSYNC_DUR. If VSYNC_DUR = 1, 3 lines are selected; if VSYNC_DUR = 0, 2.5 lines are selected.

The device automatically blanks the video from the start of the horizontal sync interval through the end of the color burst, as well as the vertical sync to prevent erroneous video timing generation.

1.4.23 Analog Video Blanking

Analog video blanking is controlled by the H_BLANKO, V_BLANKO, and V_ACTIVEO registers. Together they define an active region where pixels are displayed. V_BLANKO defines the number of lines from the leading edge of the analog vertical sync to the first active output line per field. V_ACTIVEO defines the number of active output lines. H_BLANKO defines the number of output pixels from the leading edge of horizontal sync to the first active output pixel. H_ACTIVE defines the number of active output pixels.

The device automatically blanks video from the start of the horizontal sync interval through the end of the burst, as well as the vertical sync interval to prevent erroneous video timing generation.

1.4.24 Video Output Standards Supported

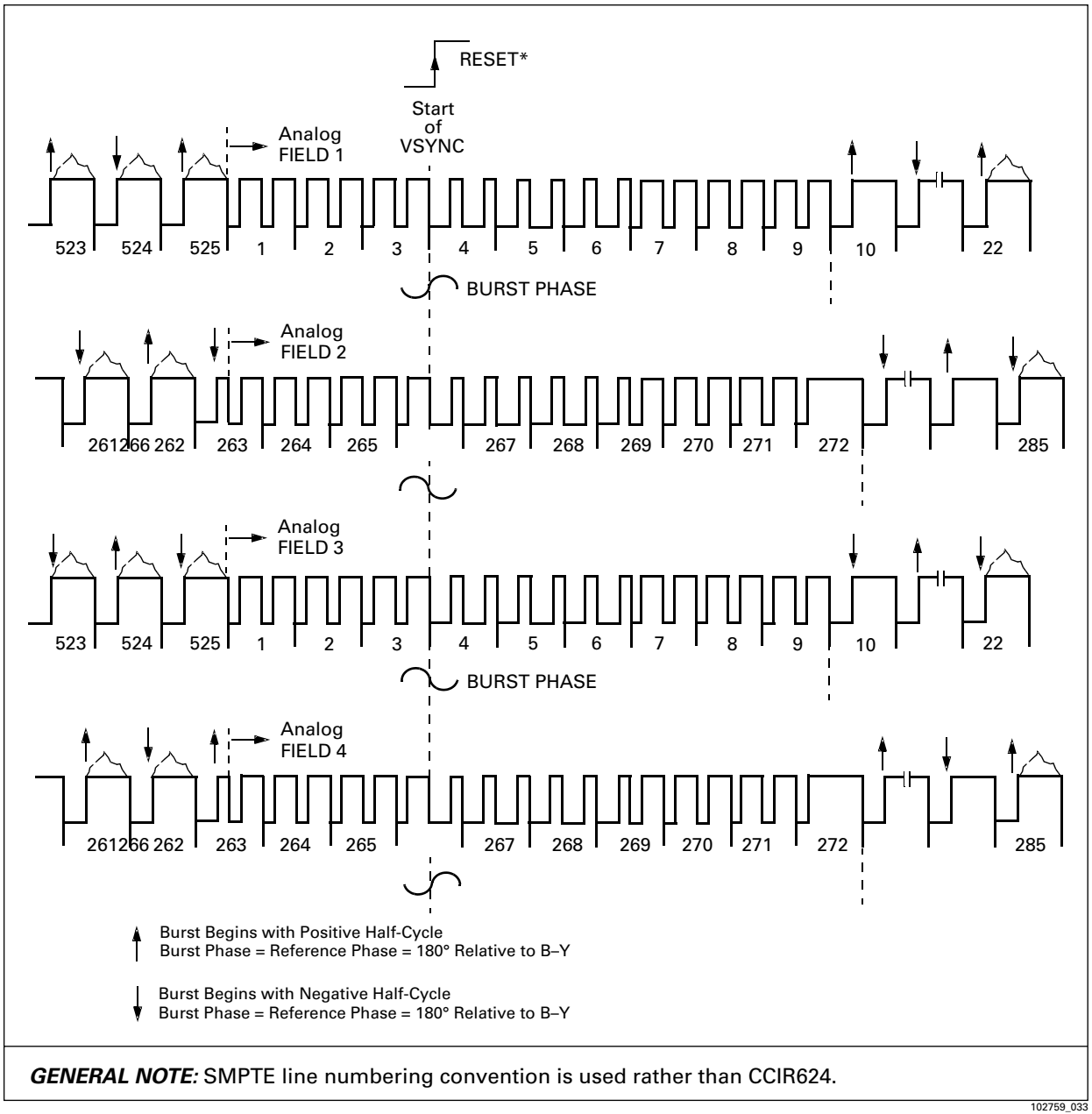
Several bits (625LINE, SETUP, VSYNC_DUR, PAL_MD, FM, DIS_SCRST) and various autoconfiguration modes control the generation of standard-definition video standards. They allow the generation of all the different NTSC, PAL, and SECAM standard-definition video standards. The aforementioned bits control the specific encoding process parameters. It is likely other registers may need to be modified to meet all the video parameters of the particular video standard. The most important bit settings for generation of standard-definition video inputs are shown in Table 20. Other CX25898/9 registers and bits must be reprogrammed to generate different video output.Video timing modes supported by the Conexant encoder are illustrated in Figures 21 through 30. These show typical events that occur for each type of video format.

Figure 20. Important Bit Settings for Generation of Standard-Definition Video Outputs

Video Output Bit	NTSC-M	NTSC-Japan	PAL-BDGHI	PAL-N	PAL-Nc	PAL-M	PAL-60[1]	SECAM-B, G, H[2]	SECAM-D, K, K1[3]	SECAM-L[4]
VSYNC_DUR	1	1	0	1	0	1	1	0	0	0
625LINE	0	0	1	1	1	0	0	1	1	1
SETUP	1	0	0	1	0	1	0	0	0	0
PAL_MD	0	0	1	1	1	1	1	0	0	0
DIS_SCRST	0	0	0	0	0	0	0	1	1	1
FM	0	0	0	0	0	0	0	1	1	1

FOOTNOTE:
(1) PAL-60 used primarily in China.
(2) SECAM-B, G, H used primarily in the Middle East.
(3) SECAM-D, K, K1 used primarily in Russia and Eastern European nations.
(4) SECAM-L used primarily in France.

Figure 21. Interlaced 525-Line (NTSC) Video Timing



GENERAL NOTE: SMPTE line numbering convention is used rather than CCIR624.

102759_033

Figure 22. Interlaced 525-Line (PAL-M) Video Timing

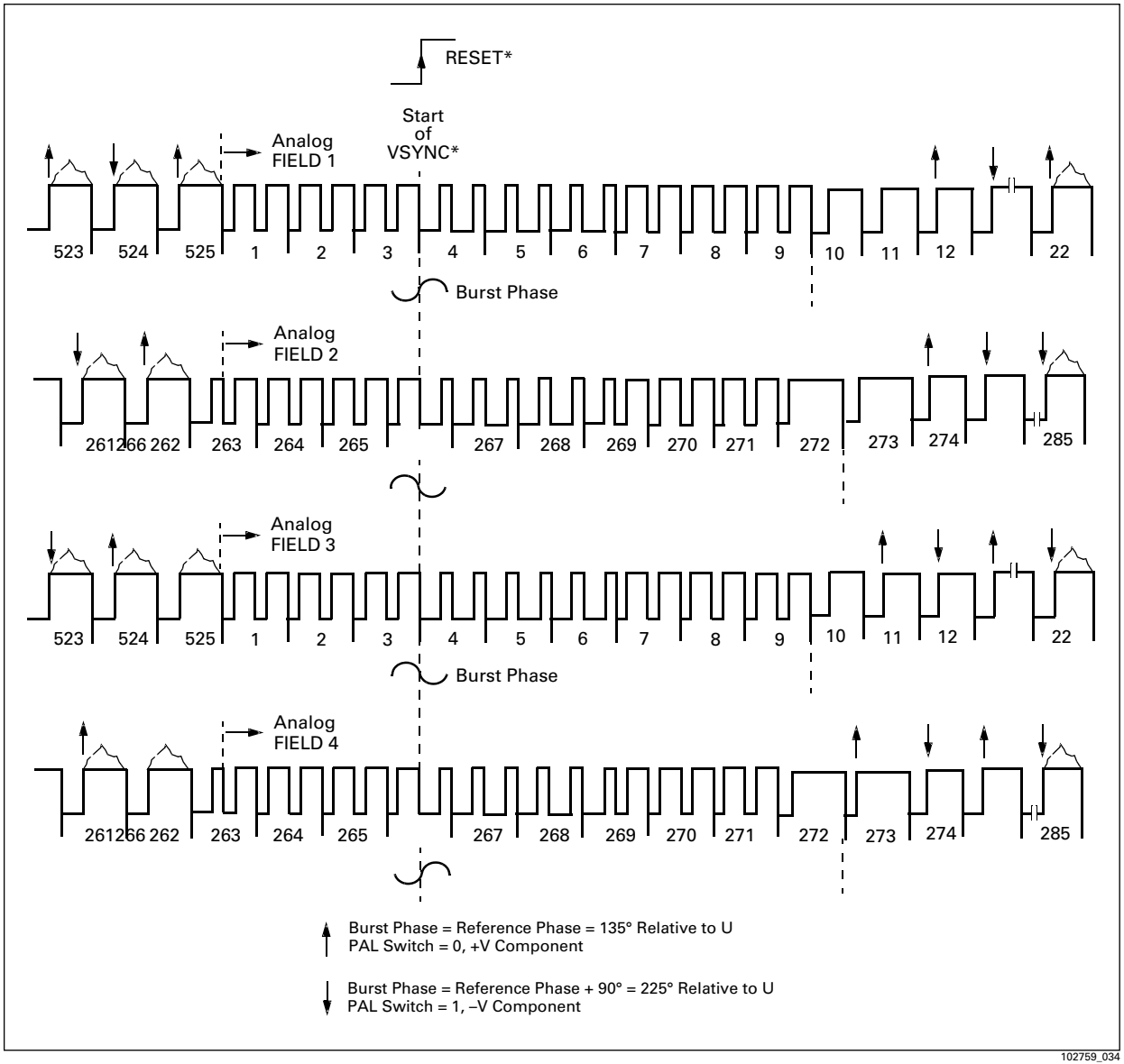


Figure 23. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 1–4)

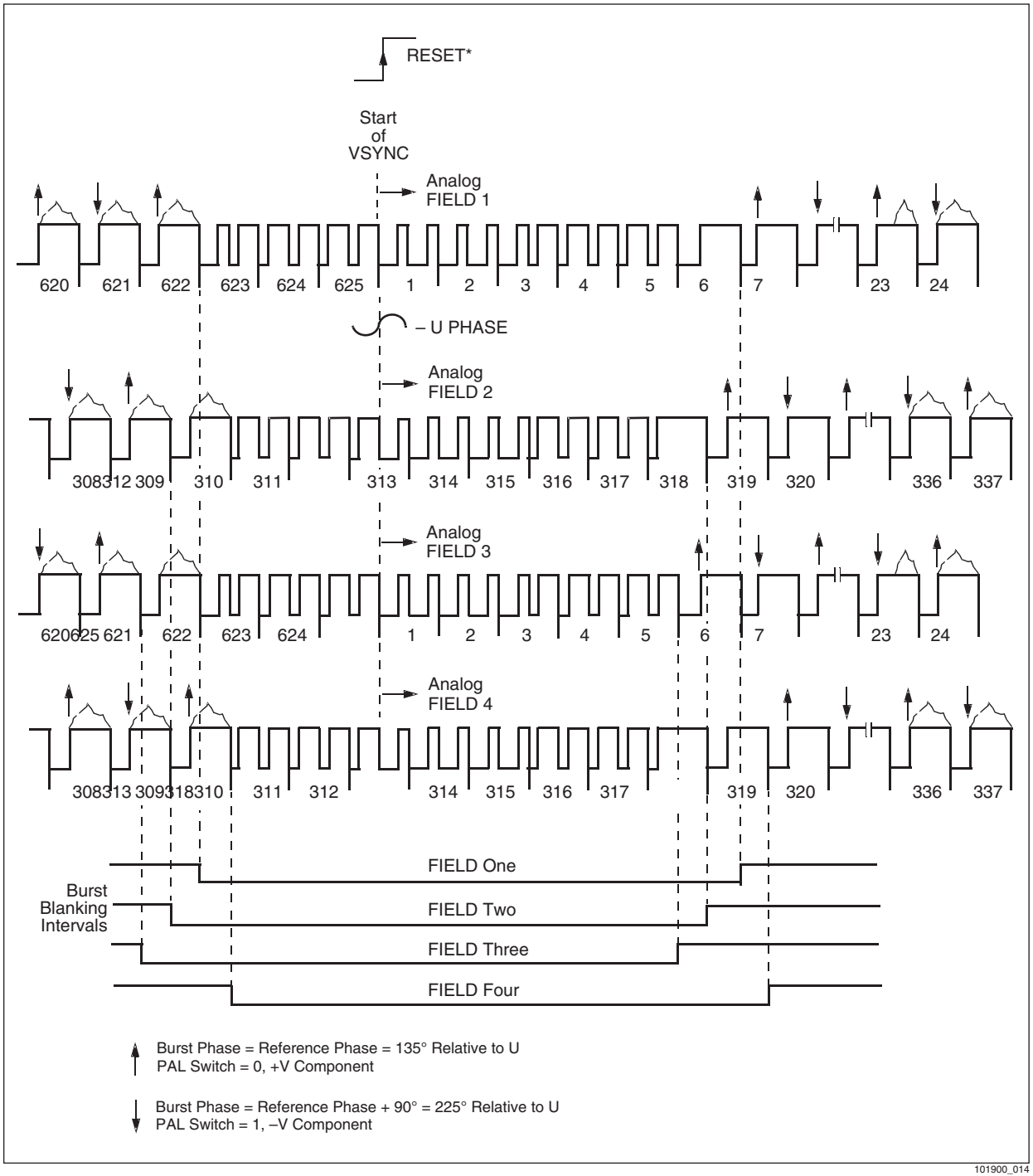


Figure 24. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 5–8)

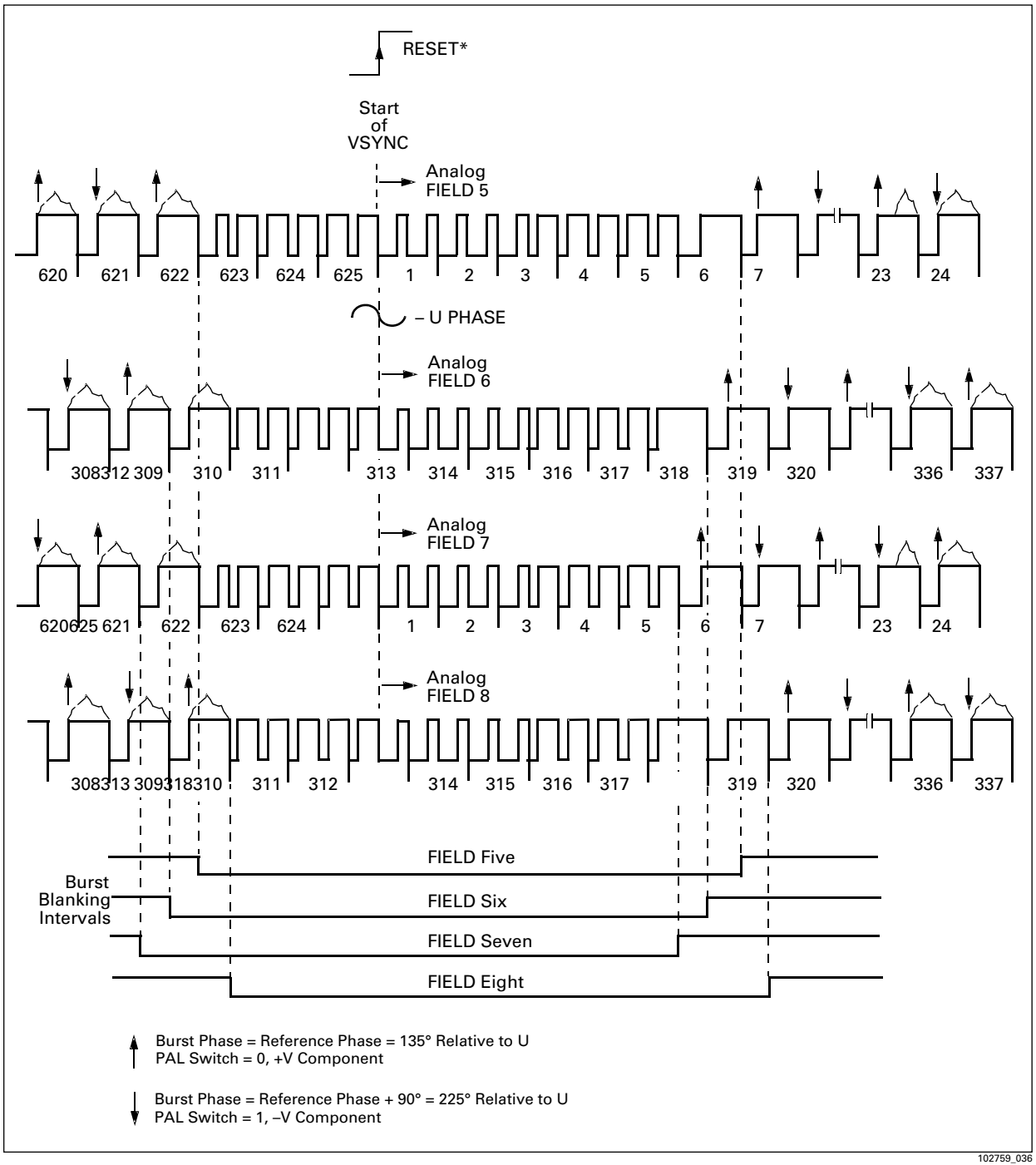


Figure 25. Interlaced 625-Line (PAL-N) Video Timing (Fields 1–4)

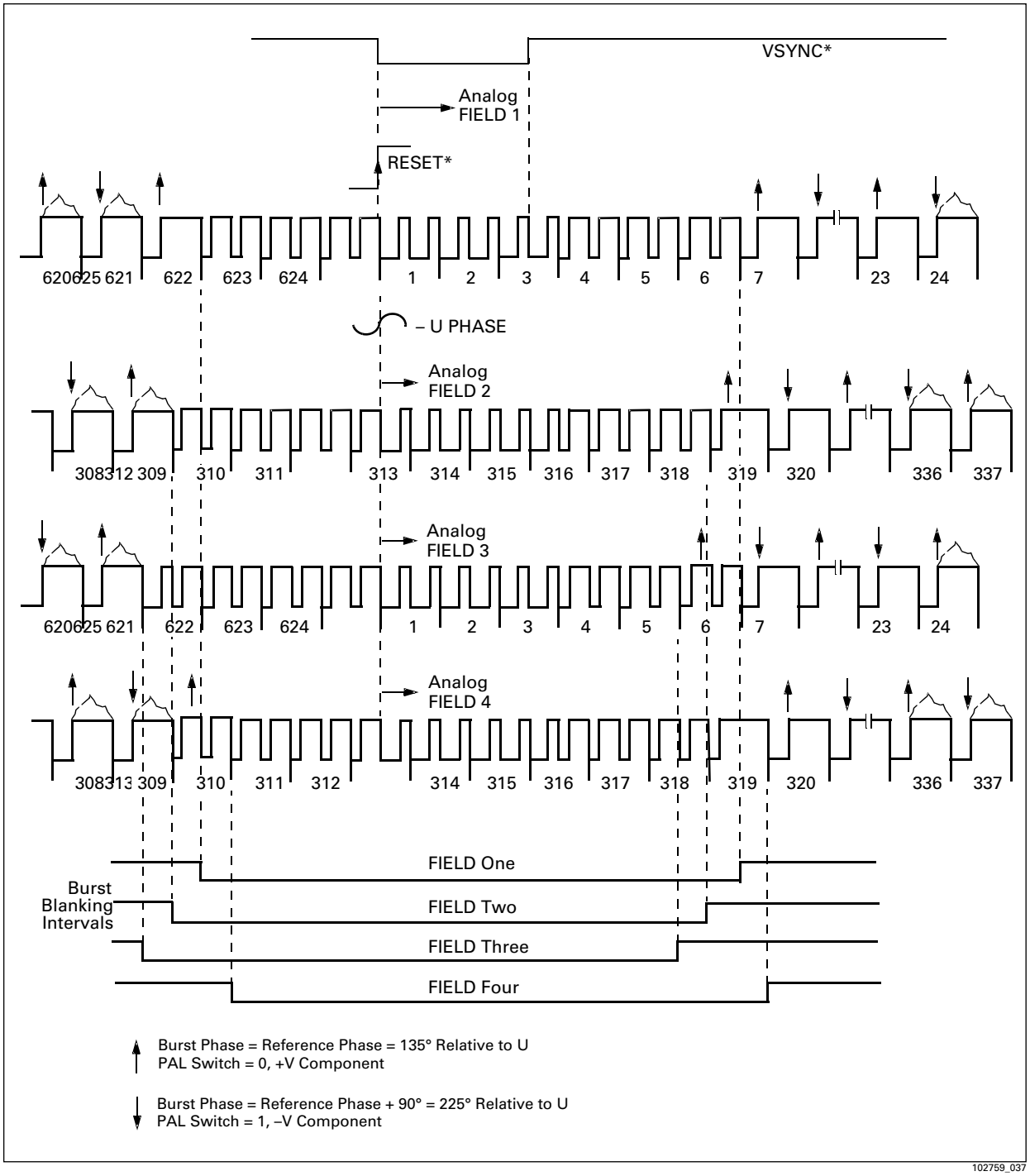


Figure 26. Interlaced 625-Line (PAL-N) Video Timing (Fields 5–8)

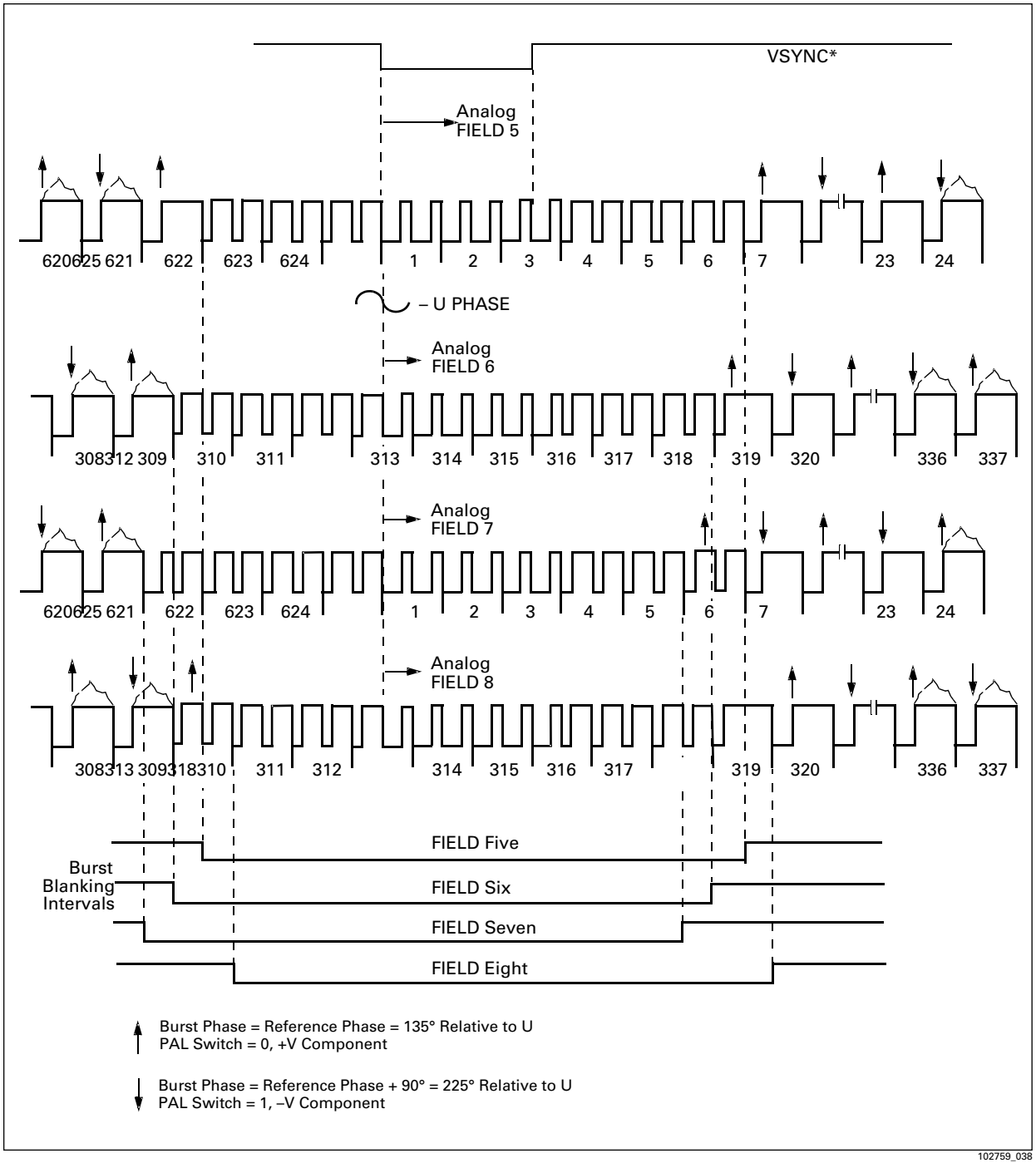


Figure 27. Noninterlaced 262-Line (NTSC) Video Timing

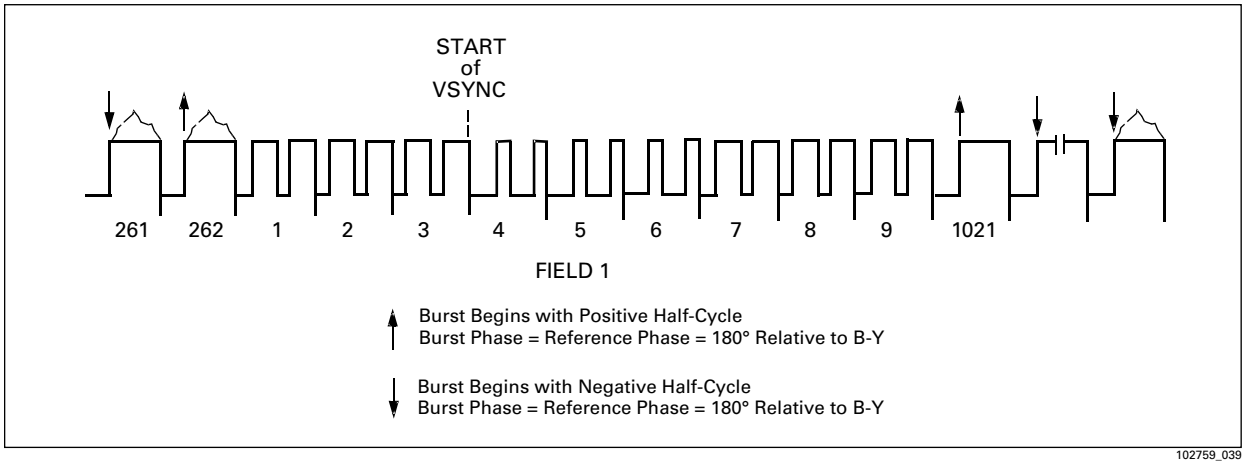


Figure 28. Noninterlaced 262-Line (PAL-M) Video Timing

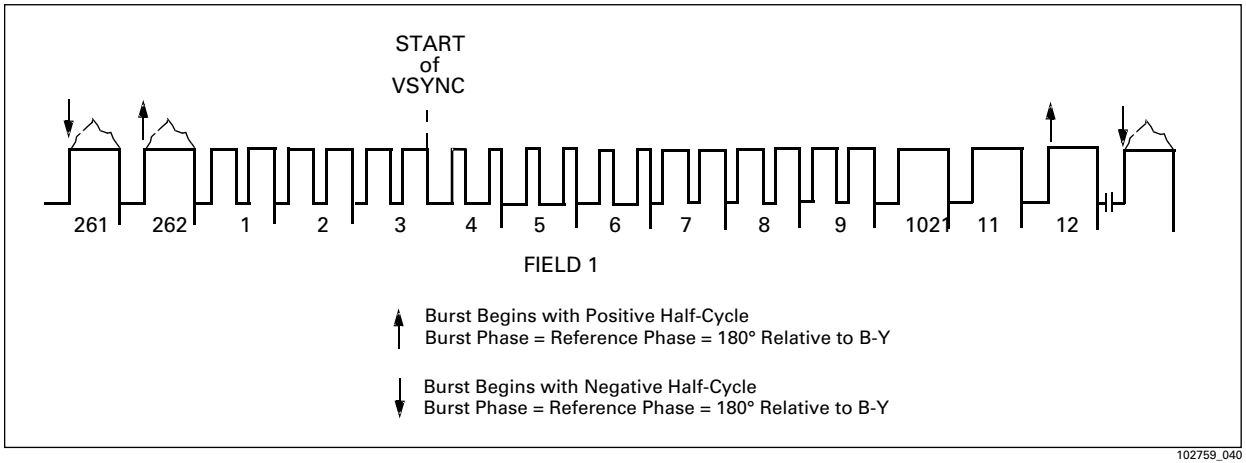


Figure 29. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, Nc) Video Timing

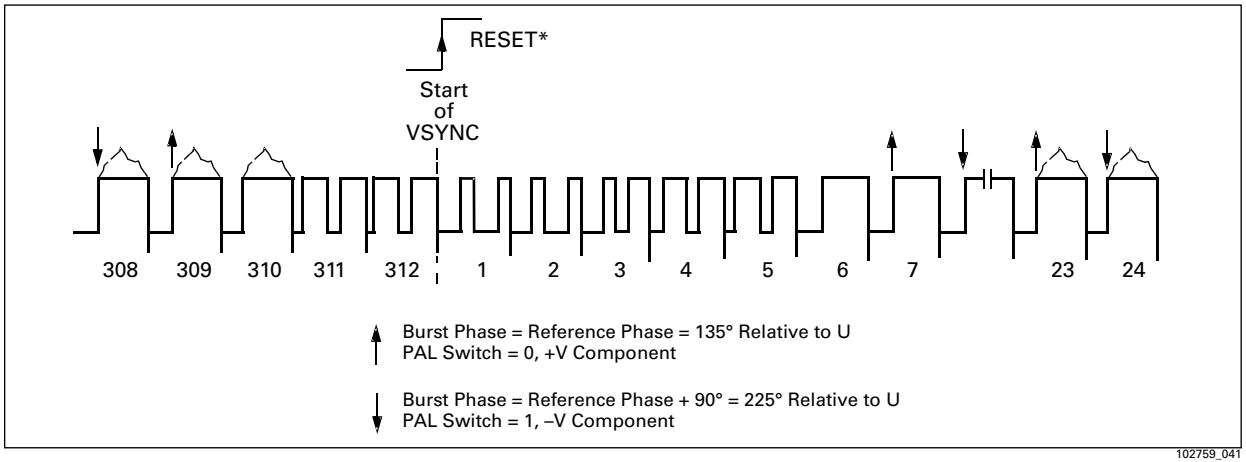
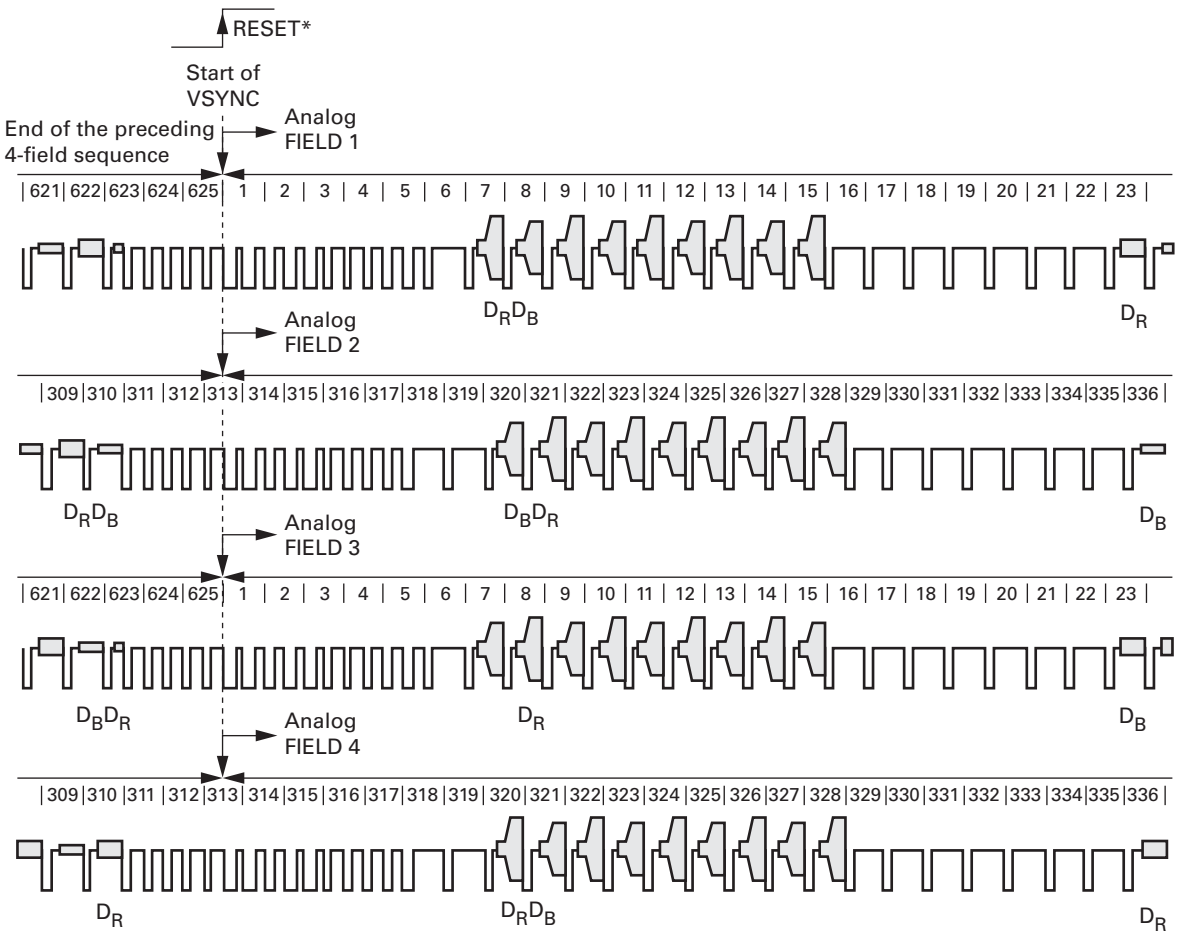


Figure 30. Interlaced 625-Line (SECAM-B, D, G, K, K1, L, M) Video Timing (Fields 1-4)



GENERAL NOTE:

1. D_R and D_B color subcarrier signal sequences over four consecutive fields shown above.
2. D_R color subcarrier frequency is 4.406250 MHz.
3. D_B color subcarrier frequency is 4.250000 MHz.

102759_042

1.4.25 Subcarrier Generation

The device uses a 32-bit-word to synthesize the subcarrier. The value of the subcarrier increment required to generate the desired subcarrier frequency is found with the following equations:

NTSC:

$MSC[31:0] = int ((455/(2 * H\_CLKO)) * 2^{32} + 0.5)$

PAL:

$MSC[31:0] = int (((1135/4+1/625)/H\_CLKO) * 2^{32} + 0.5)$

PAL-M (Brazil):

$MSC\ [31:0] = int ((909/(4 * H\_CLKO)) * 2^{32} + 0.5)$

PAL-Nc (Argentina):

$MSC[31:0] = int (((917/4 + 1/625)/H\_CLKO) * 2^{32} + 0.5)$

SECAM:

$MSC\_DB[31:0] = int (272/(H\_CLKO) * 2^{32} + 0.5)$

$MSC\_DR[31:0]^{(1)} = int (282/(H\_CLKO) * 2^{32} + 0.5)$

where: H_CLKO is the number of output clocks/line (this is register 0x76 and the low nibble of 0x86).

NOTE: When generating SECAM, the MSC register becomes the MSC_DR register.

This allows the generation of any desired color burst subcarrier frequency for any desired standard-definition video standard. The 32-bit subcarrier increment must be loaded by the serial interface before the subcarrier is enabled. The device is reset to disable chroma until the last byte of the 32-bit increment loads, at which time the chroma is enabled, unless the DCHROMA bit is set.

In order to prevent any residual errors from accumulating, the subcarrier DTO (Discrete Time Oscillator) is reset every four fields for NTSC formats and every eight fields for PAL formats. For best quality in SECAM, the DIS_SCRST bit should be set preventing a subcarrier phase reset at the beginning of each color field sequence. Furthermore, the SECAM subcarrier is generated on lines 23-310 and 336-623 automatically unless disabled by the PROG_SC bit.

1.4.26 Subcarrier Phase Reset/Offset

In order to maintain correct SC-H phasing, the subcarrier phase is set to 0 degrees on the leading edge of the analog vertical sync every four (NTSC) or eight (PAL) fields, unless the DIS_SCRST (bit four of register 0xA2) is set to a logical 1. This is true for both interlaced and noninterlaced outputs. The subcarrier phase can be adjusted from the nominal 0 degrees phase by the PHASE_OFF[7:0] register, where each LSb change corresponds to a 360/256 = 1.406 degrees change in the phase.

Setting DIS_SCRST to 1 may be useful in situations where the ratio of CLK/2 to HSYNC* edges in a color frame is noninteger, which could produce a significant phase impulse by resetting to 0.

1.4.27 Burst Generation

The subcarrier burst generation is a function of the video standard (e.g., NTSC, PAL, or SECAM), the subcarrier frequency increment (MSC[31:0]), and the burst horizontal begin and end register settings (HBURST_BEGIN[7:0] and HBURST_END[7:0]). To calculate the value of HBURST_END[7:0] subtract 128 from the desired location in clock cycles. The burst will automatically be blanked during the horizontal sync preventing invalid sync pulses from being generated. Burst blanking is automatically controlled by the selected video format. Burst rise and fall times are automatically generated by the device. The burst amplitude is controllable through the BST_AMP[5:0] field.

1.4.28 Video Amplitude Scaling and SINX/X Compensation

Both the luminance and chrominance video amplitudes can be scaled by the MY, MCR, and MCB registers. This allows various colorimetry standards to be achieved, and can also be used to boost the chroma to compensate for the sin x/x loss of the DACs. Appendix A shows the range of values achievable and values for various video formats.

The DAC output response is a typical sinx/x response. For the composite video output, this results in a slightly lower than desired burst and chroma amplitude value. This is compensated for, to some extent, by choosing an output filter that boosts the frequency response slightly. Another method which can be used effectively, and is used by default in the auto configuration modes, is to boost the burst and chroma gain as programmed by the BST_AMP and MCR/MCB register values by a factor of
(x/sinx). The amount of sinx/x amplitude reduction is calculated by:

$sinx/x = sin(\pi * Fsc/F_{CLK}) / (\pi * Fsc/F_{CLK})$ *[in radians]*

Fsc = desired subcarrier burst frequency

F_{CLK} *= analog pixel rate*

1.4.29 Chrominance Disable

The chrominance subcarrier can be turned off by setting the DCHROMA bit to a logical 1. This disables the subcarrier burst as well, providing luminance-only signals on the CVBS output and a static blank level on the chrominance output.

1.4.30 FIELD Pin Output

Like its predecessors, the Bt868/869 and the CX25870/1/2/3/4/5, this PC encoder includes a FIELD pin output. This signal is output only and is accessed through pin 28. The frequency of the FIELD pin is 30 Hz during an NTSC video output, and 25 Hz throughout a PAL or SECAM video output. The only programming step required to obtain the FIELD output is to serially write the EN_OUT bit to 1.

The purpose of this signal is to provide a digital TTL compatible output which tracks the analog interlaced field presently being transmitted by the CX25898/9 DACs. The peak-to-peak amplitude of this output will be from 0 V to the level present on the VDDO pins. If these pins are tied to 3.3 V, then the FIELD high state is transmitted at a 3.3 V level. If these pins are tied to 1.5 V or lower voltage,

then the FIELD high state is transmitted at a 1.5 V or lower level. The logical 0 level from FIELD will always be GND/VSS regardless of the logical 1 voltage.

The FIELD output transitions after the rising edge of CLKI, two clock cycles following the leading edge of the digital HSYNC* input or output. Figure 31 shows the relationship between the FIELD and Composite (CVBS) outputs and VSYNC* input for NTSC. Figure 32 illustrates this same relationship for PAL.

Figure 31. FIELD Pin Output Timing Diagram: NTSC-M, J, 4.43, PAL-M, 60

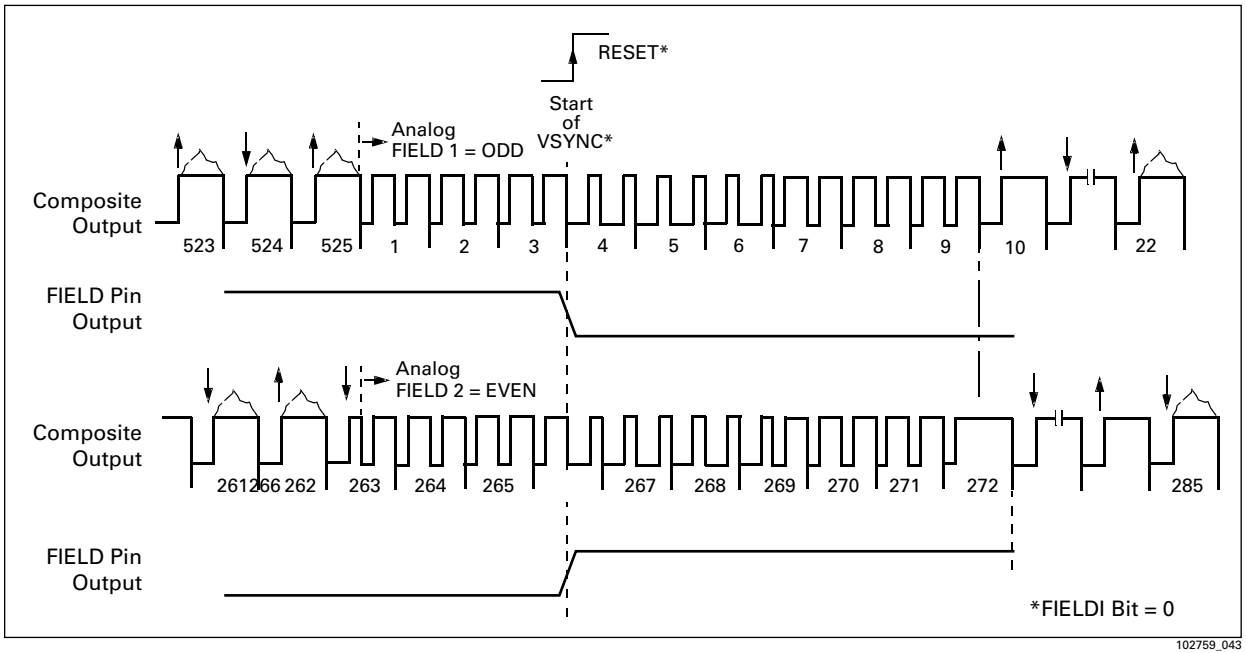
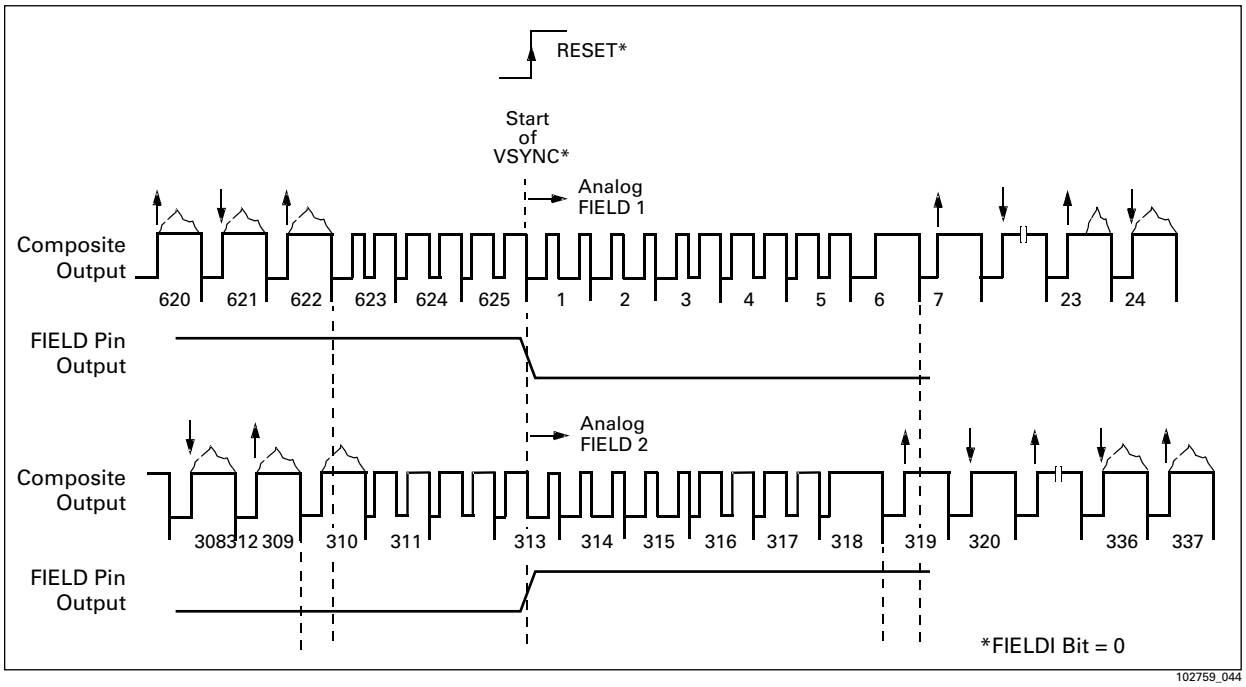


Figure 32. FIELD Pin Output Timing Diagram (PAL-B, D, G, H, I, N, Nc)



By default, the internal FIELDI bit will be 0 which forces the encoder to transmit a logical 1 during transmission of an EVEN field and logical 0 for the period of an ODD field. To change the FIELD polarity, reprogram the FIELDI bit.

If the encoder is the timing master and sends out HSYNC* and VSYNC*, then after a power-on, pin, or timing reset (setting of bit 7, register 0x6C), the encoder and the flicker filter portions of the device start at line 1, pixel 1 of their respective timing generation. For the CX25898/9, this means the ODD field is always the first field conveyed after a power-on reset, pin reset, or timing reset.

When the CX25898/9 receives an interlaced data format, its FIELD pin represents only the output field presently being generated by the on-chip DACs. When the CX25898/9 receives progressive (i.e., noninterlaced) frames which have no field associated with it, the CX25898/9's input timing generator still keeps track of frames received. As a result, after the entire second frame has been received, the input and encoder sections become resynchronized. This resynchronization is done through an internal frame sync signal. This action, in turn, forces the CX25898/9 to the beginning of the odd field and changes the FIELD pin back to its odd state.

If the CX25898/9 is the timing slave (i.e., it accepts HSYNC* and VSYNC*) receives pin reset or timing reset (register 0x6C, bit 7) this causes the input timing generator to send the encoder the aforementioned frame sync. This sets the encoder to the beginning of the odd field, which is conveyed through the FIELD pin. The first digital HSYNC* and VSYNC* combination then corresponds to the encoder's EVEN output field. The second digital HSYNC* and VSYNC* combination will again cause a frame sync and the encoder will start sending the ODD field both from its DACs and FIELD pin. This ODD–EVEN–ODD–EVEN … field sequence continues indefinitely.

1.4.31 Buffered Crystal Clock Output

The buffered crystal clock output (XTAL_BFO) pin provides a buffered output (0 V to the voltage on the VDDO pin peak-peak) of whatever frequency is found between the encoder's XTALIN and XTALOUT pins. This signal can then be used as a much more accurate input clock to the graphics controller because controllers typically utilize clock sources with errors between 75–150 ppm. This implementation ultimately results in better VGA picture quality because the clock driving the data master is within the same tolerance (i.e., 25 ppm) as the TV out encoder. This can also lead to a considerable savings in cost, component count, and PC board space because the crystal attached to the data master has been completely eliminated.

On power-up, the encoder will transmit a 0 to 3.3 V signal (or whatever voltage is received by the VDDO pins) at a frequency equal to the frequency of the crystal found between the XTALIN and XTALOUT ports. The tolerance of the XTAL_BFO signal will match the tolerance found within the encoder's crystal. The CX25898/9 was designed to expect a 13.500 MHz ± 25 ppm crystal. As a result, all the PLL_INT and PLL_FRACT register values found within each CX25898/9 autoconfiguration mode possess this set of default values.

The CX25898/9 also has the flexibility to support an alternate 14.31818 MHz crystal with a tolerance of ± 25 ppm. To switch the encoder to operate with this crystal frequency, install an appropriate crystal and crystal circuit between the XTALIN and XTALOUT ports. After any autoconfiguration mode has been set, the PLL_INT and PLL_FRACT registers must be manually programmed in accordance with the equations in Section 1.4.5.

For CX25898/9 designs, a small (e.g., 33 Ω) series resistor should be added to XTAL_BFO, as close as possible to the signal source device. This reduces overshoot and undershoot on this signal as it changes states. The buffered crystal clock output pin should be floated if not used. Disabling the XTAL_BFO pin is possible through the XTAL_BFO_DIS bit.

1.4.32 Noninterlaced Output

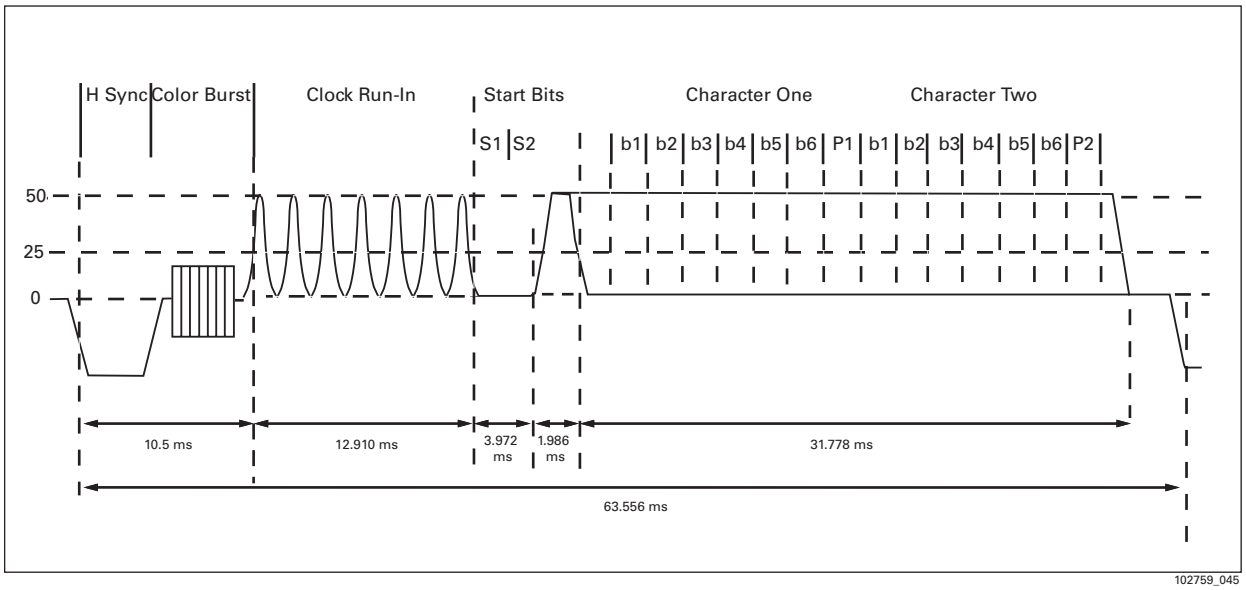
This is a legacy video output mode, continued for backward compatibility to the CX25870/1/2/3/4/5 encoders. It is not recommended for new designs. The CX25898/9 is programmed for noninterlaced video out via the NI_OUT bit, and it is recommended that the DIS_SCRST bit be set to a one. Although only the odd field will be transmitted, the FIELD pin will continue to change state on the leading edge of the analog vertical sync. A 30 Hz offset should be subtracted from the color subcarrier frequency while in NTSC mode so that the color subcarrier phase is inverted from field to field. The transition from interlaced to noninterlaced in master interface occurs during odd fields to prevent synchronization disturbance.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan >2x) may not function properly.

1.4.33 Closed Captioning

The CX25898/9 encodes NTSC/PAL–M Closed Captioning (CC) on scan line 21, and NTSC/PAL–M extended data services on scan line 284, in accordance with the EIA-608B (CEA-608B) standard shown if Figure 33. The bit rate for CC-encoded data is 0.5035 MHz for 525-line video systems. For 625-line systems, this bit rate falls to 0.500 MHz. Four 8-bit registers (CCF1B1, CCF1B2, CCF2B1, and CCF2B2) provide the data while bits ECCF1 and ECCF2 enable display of the data. A logical 0 corresponds to the blanking level of 0 IRE, while a logical 1 corresponds to 50 IRE above the blanking level.

Figure 33. EIA-608B (CEA-608B)-Compliant Line 21 Waveform (NTSC)



NOTE: Figure 33 reprinted courtesy of *EIA/CEA-608B* specification.

Closed captioning for PAL–B, D, G, H, I, N, Nc is similar to that for NTSC. Closed-caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC system, except that encoding is provided on lines 22 and 335, for closed captioning and extended data services, respectively.

The CX25898/9 generates the clock run-in start bits and appropriate timing automatically. The user must control the 2 bytes of data for each field. Each of these 2 bytes is a 7-bit and odd parity ASCII character, which represents text or control characters for positioning or display control. For the purposes of CC or EPS, only the Y signal for S-video or Component YCrCb outputs is used. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47 Section 15.119 (10/91 edition or later) for programming information. The EIA608 standard describes ancillary data applications for Field 2 Line 21 (line 284).

When CCF1B2 is written, CCSTAT_O is set; when CCF2B2 is written, CCSTAT_E is set. After the CC bytes for the odd field are encoded, CCSTAT_O is cleared; after the CC bytes for the even field are encoded, CCSTAT_E is cleared. If the ECCGATE bit is set, no further encoding is performed until the appropriate registers are written again; a null is transmitted on the appropriate CC line in that case. If the ECCGATE bit is not set, the user must rewrite the CC registers prior to reaching the CC line; otherwise the last bytes are re-encoded. The CC data bytes are double-buffered to prevent loss of data during the encoding process.

The equations governing CCR_START and CC_ADD registers are listed below.

CCR_START:

- For NTSC:
  *((H_CLKO*10.003*27) / 1716) + 60*
- For PAL, SECAM:
  *((H_CLKO*10.003*27) / 1728) + 60*

CC_ADD:

- For NTSC:
  $2^{22}/H\_CLKO$
- For PAL, SECAM:
  $(2^{22}*1728) / (1716*H\_CLKO)$

1.4.33.1 Copy Generation Management System-Analog

The Copy Generation/Guard Management System (CGMS) is a copy control system for DVD recorders that either prevents copies or controls the number of copies that can be made. CGMS can be added to either analog (CGMS-A) or digital signals (CGMS-D). DENCs such as CX25898/9 encoders only output analog TV, so, for the purposes of this data sheet, CGMS-A is discussed. CGMS-D protection is not possible with CX25898/9 encoders.

CGMS is a copy control system consisting of two bits in the MPEG-2 compressed video stream that indicate whether copying of the content is permitted or not. For CGMS to work, the bits must be set during the authoring process. Next, the DVD player or other system adds CGMS data to its analog video output stream through the encoder. Lastly, the DVD recorder recognizes and responds correctly to the CGMS bit setting.

When the DENC is generating NTSC, CGMS-A is identical to closed captioning in that it embeds data in the field blanking interval on line 21. Line 20 can also be used for CGMS-A in 525-line analog formats. Whereas closed captioning uses 16 bits or 2 bytes worth of data, CGMS-A uses only 2 bits of this overall sequence. The analog timing provided by the CX25898/9 will match the waveform shown in Figure 33 for both CGMS-A and CC.

Most standards for CGMS-A copy protection are unclear in terms of PAL output, so these standards will be minimally discussed in this section. Refer to Section 1.4.34.1 for this encoder's PAL Wide-Screen Signaling (WSS) capabilities.

In summary, for NTSC, all aspects of CGMS-A can be supported with CX25898/9 encoders, because the timing and waveform for CGMS-A matches that timing and waveform required for support of NTSC closed captioning which also adheres to the EIA-608 standard.

When line 21 is utilized for other purposes, CX25898/9 can place closed-caption content (whose waveform and timing are defined in the EIA/CEA-608-B standard) within one of the following lines in the Vertical Blanking Interval (VBI): line 19, line 20, line 21, or line 22 of 525-line NTSC systems. The CCSEL[3:0] bit field in the CX25898/9 controls which line receives the CC/CGMS-A content. The CC and CGMS-A bits must reside on the same line.

When the DENC is generating HDTV 720p and 1080i Y PR PB outputs, the device transmits a data waveform for HDTV signals compliant with the EIAJ CPR-1204-2, CEA-770.3-C and CEA 805A-TYPEA standards, because, in terms of timing and the analog waveforms, they are identical. The display/pixel clock is 74.25 MHz at VSYNC = 60 Hz for each supported standard. The start symbol and data symbol width are the same and equal to 1.038 µs (for 1080i) and 0.782 µs (for 720p). The start symbol position (from 0H, start of line to bit 0 of the header) is 4.15 µs (for 1080i) and 3.13 µs (for 720p). The number of data bits encoded per symbol is 1 or bilevel. A logical high level is nominally 70 percent of peak white (i.e., 490 mV), and logical low is nominally 0 percent of peak white (0 mV).

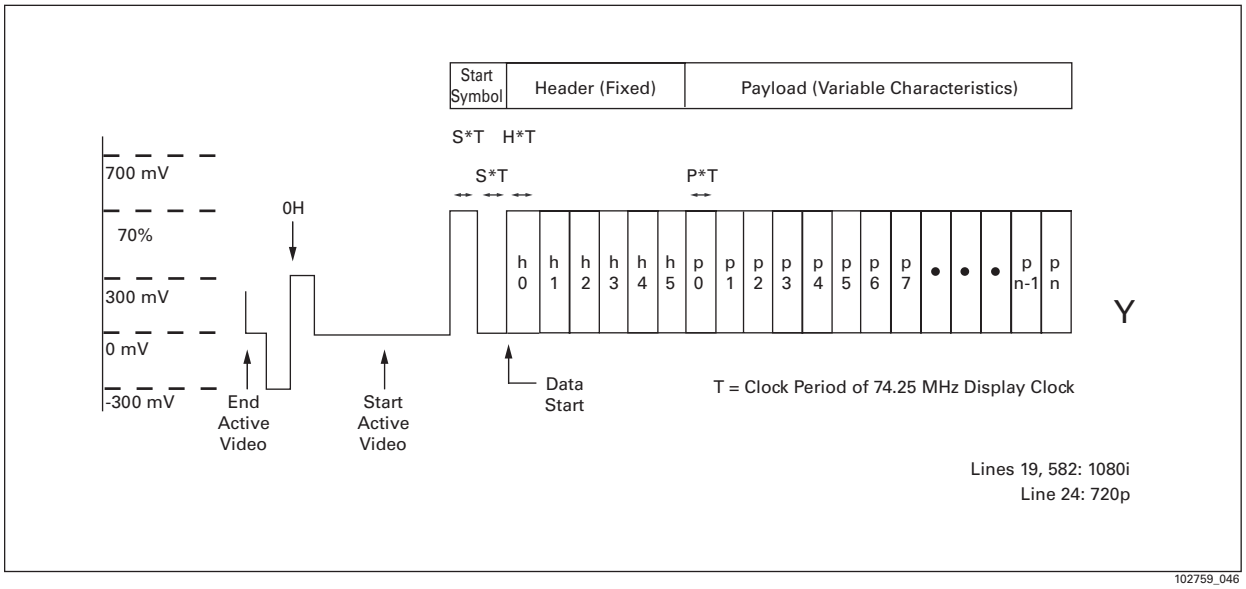
Like SDTV, CGMS-A HDTV 720p and 1080i are just two specific data bits in the larger Type A Packet Payload Data sequence within the vertical blanking interval. The CX25898/9 encoder does not support the CEA 805A-TYPEB standard in 720p and 1080i for a number of reasons:

1. First, and most importantly, the position of Type A packet for 720p format must be in VBI line 24. Position of Type B Packet for 720p format must be in VBI line 23. The position of Type A packet for 1080i format must be in VBI lines 19 and 582. Position of Type B Packet for 1080i format must be in VBI lines 18 and 581. This DENC cannot place CGMS-A and WSS data on alternate lines within the HDTV VBI for 720p or 1080i.
2. Second, the Type B payload data symbol width (i.e., each analog bit interval) is different from the Type A payload data symbol width, along with other timing parameters.
3. Third, Type B Packet payload data is placed in 128 bits (16 bytes) versus only 14 bits for Type A Packet payload data.

In summary, for 720p and 1080i, CX25898/9 supports EIAJ CPR-1204-2, CEA-770.3-C, and CEA 805A-TYPEA standards. Since CGMS-A is a subset of CEA-770.3-C and CEA 805A-TYPEA, then CX25898/9 transmits compliant CGMS-A in accordance with these standards.

The CX25898/9 encodes CGMS-A bits as two bits of the overall data payload in the TYPEA data sequence in accordance with the CEA 805A-TYPEA waveform shown in Figure 34.

Figure 34. CEA 805A-TYPEA-Compliant HDTV 1080i, 720p Waveform



NOTE: Figure 34 reprinted courtesy of *CEA 805A-TYPEA* specification.

For HDTV 480p Y PR PB outputs, the CX25898/9 encoder transmits a data waveform for HDTV signals compliant with the EIAJ CPR-1204-1, CEA-770.1-C, CEA-770.2-C, and CEA 805A-TYPEA standards, because, in terms of timing and the analog waveform, they are identical. The display/pixel clock is 27.000 MHz at VSYNC = 60 Hz for each supported standard. The start symbol and data symbol width are the same and equal to 0.963 µs. The start symbol position (from 0H, start of line to bit 0 of the header) is 5.778 µs. The number of data bits encoded per symbol is 1 or bilevel. A logical high level is nominally 70 percent of peak white (i.e., 490 mV), and logical low is nominally 0 percent of peak white (0 mV).

The CX25898/9 encoder does not support the CEA 805A-TYPEB standard in 480p for the following reasons:

1. First, and most importantly, the position of Type A packet for 480p format must be in VBI line 41. Position of Type B Packet for 480p format must be in VBI line 40. This DENC cannot place CGMS-A and WSS data on alternate lines within the HDTV VBI for 480p.
2. Second, the Type B payload data symbol width (i.e., each analog bit interval) is different from the Type A payload data symbol width, along with other timing parameters.
3. Third, Type B Packet payload data is placed in 128 bits (16 bytes) versus 14 bits for Type A Packet payload data.

The four possible states of the CGMS bits are listed below:

- No more copies (one generation copy has been made).
- No copying is permitted.
- Copying is permitted without restriction.
- One generation of copies may be made.

1.4.34 Wide Screen Signaling—Standard-Definition TV

Ratios of 16:9 and other non-4:3 aspect ratios within SDTV are being adopted in increasing numbers. To assist in the management of this type of program material received by TVs, a WSS set of standards have recently been developed. These documents have allowed broadcasters, consumer equipment makers, and encoder vendors to a display 16:9 and other non-4:3 programs in their correct aspect ratio while simultaneously increasing their control over copyrighted media.

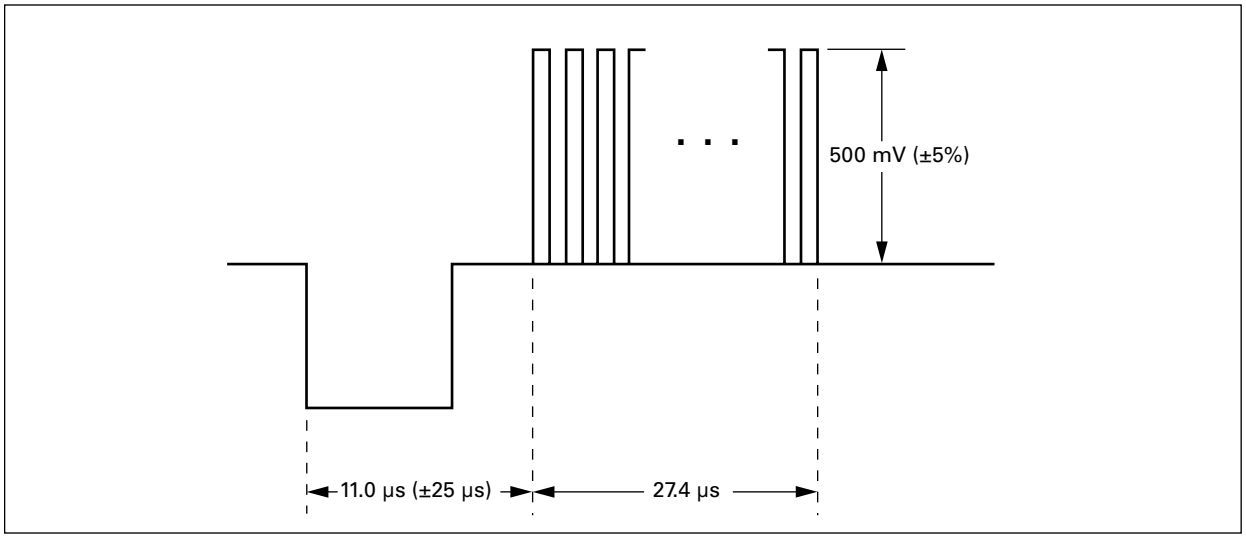
It is the intention of Macrovision to eliminate pirated copies. On the other hand, copyright management, a subset of WSS described in the EN 300 294 specification, is used to control the amount of legal copies allowed. For this type of copyright management to work, the equipment making the copy (e.g., VCR) must recognize and respond to the data being broadcasted. The WSS based encoder within the DVD player or game console transmits the data on the first part of PAL, line 23, and for NTSC, lines 20 and 283.

The CX25898/9 supports the most popular WSS standards for encoding of data into analog PAL or analog NTSC video signals. The PAL encode process for WSS is accomplished by using approximately the first 40 microseconds of Field 1's line 23 as described in the EN 300 249 (version 1.3.2) standard while the copyright management information is transmitted using a portion of these same bits. The 525-line NTSC composite and S-Video outputs comply with the EIAJ CPR-1204, IEC 61880-1 standards. For analog YUV video signals, WSS information will be present only on the Luma (Y) signal. For HDTV 480p Y PR PB outputs, the CX25898/9 encoder adheres to the EIAJ CPR-1204-1, CEA 805A-TYPEA only, CEA 770.1-C, and CEA 770.2-C (2H) standards, respectively. For HDTV 720p/1080i Y PR PB outputs, the CX25898/9 encoder adheres to the EIAJ CPR-1204-2 standard.

1.4.34.1 WSS for PAL-B, D, G, H, I, N, Nc Outputs (CGMS-A PAL)

For 625-line systems such as PAL, the first portion of line 23 is used to transmit the all the WSS information. An illustration of an encoded PAL Composite or Luma video signal from the CX25898/9 that contains WSS data is shown in Figure 35.

Figure 35. Horizontal Timing for PAL Output-Line 23 that Contains WSS Data



The peak-to-peak amplitude of the pulses present on line 23 is 500 mV with a tolerance of 5 percent. The signal's shape will be a sine-squared pulse based waveform. When WSS encoding is turned on, the clock frequency for WSS data encoded onto line 23 by the CX25898/9 is 5 MHz. The data is encoded using a format called biphase L coding. Basically, this means the encoder will output a sequence of three 500 mV. (above blanking level) pulses for a duration of 200 ns $\pm$10 ns each then transmit three elements of the video blank level for a duration of 200 ns $\pm$10 ns each. This 111 000 sequence comprises any single data bit written to the WSSDAT registers. Writing a 0 data bit to WSSDAT would force the CX25898/9 to output the opposite element sequence of 000 111. Consult your particular WSS standard for additional details on the biphase L coding format and the significance of each data bit to a WSS-compliant television.

The WSS sequence for PAL present on line 23 is normally comprised of a run-in code, a start code, and 14 bits of data unique to the broadcast content itself. The run-in code consists of seven hexadecimal elements plus a single bit (1 F 1C 71 C7 Hex) at 5 MHz. The start code consists of exactly six hexadecimal elements (1E 3C 1F Hex) also at 5 MHz. These two initial codes are generated by the CX25898/9 automatically. These codes are detected by enhanced PALplus TVs as a trigger mechanism to change the TV's Aspect Ratio, display enhanced services content, display subtitles, or respond to the reserved bits that get encoded after the initial codes.

The aspect ratio data consists of four data bits (b3 through b0) that specify the aspect ratio that should be used by the television if it has WSS and/or copyright management capability. Data bit b0 is considered the LSb. Descriptions of the four aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with black bars on the left and the right sides.

Option #2—14:9 aspect ratio: This content is best displayed with a 14:9 aspect ratio picture. The 14:9 aspect ratio picture should be centered on the display, with black bars on the left and the right sides.

Option #3—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

Option #4—greater than 16:9 aspect ratio: This content is best displayed with an aspect ratio exceeding 16:9. The >16:9 aspect ratio picture should be displayed as in Option #3 or use the full height of the display by zooming in.

For actual data bit assignments (e.g. b3, b2, b1, b0), and specific usage information (formats, positions, and number of active lines) for the Aspect Ratio, consult the ITU-R BT.1119 standard.

The enhanced services content that follows the Aspect Ratio information consists of a single data bit that turns on either camera mode or film mode. This data bit is denoted as b4.

The next 3 bits are all assigned a value of 0 since they are reserved. This bit field is comprised of b5, b6, and b7.

The subtitles data follows the three consecutive zeros. It consists of three data bits (b8 through b10) that specify whether or not subtitles are present and the position and/or appearance of the subtitles themselves. Data bit b8 is considered the LSb and controls whether or not subtitles exist within Teletext.

NOTE: A separate IC is required for transmission of Teletext-encoded data since the CX25898/9 does not have this capability. The combination DENC + DVI transmitter, CX25890/1/2, has an integrated Teletext encoder.

Bits b9 and b10 work in tandem to dictate the position of subtitles within Teletext. The allowable positions of teletext subtitles are inside the active image, outside the active image, or no open subtitles.

The final three bits are all assigned a value of 0 because they are reserved. This bit field is comprised of b11, b12, and b13.

An oscilloscope photo of an actual 625-line WSS signal from the CX25898/9 is shown in Figure 36. In this photo, the Conexant encoder has already been programmed into autoconfiguration mode #1 for a 640x480 input resolution and PAL-I output with roughly 16.5 percent overscan compensation. The input and output clock frequency of 29.50008 MHz in combination with the WSSINC equation below dictates a final WSSINC value of 2 B6 3D hex. For the WSS data, 4F hex has previously been written to register 0x60, A0 hex to register 0x62, and 00 hex to register 64 hex. This data has been encoded into the WSS PAL Composite signal, shown in Figure 36. Remember, all WSS (and/or copyright management) data registers must be filled with appropriate bit information for that standard. The data bits encoded below have no particular significance and are only meant as an illustration.

The CX25898/9 will not transmit new WSS data within line 23 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has been programmed. This byte of information can be the same value as before, or not, but it must be written to via the serial bus. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded.

Figure 36. WSS PAL Composite Signal

In summary, to enable WSS within line 23 of the PAL Composite signal (or Luma channel within a PAL S-Video output) perform the sequence of serial writes found in Table 14.

Table 14. Switching Conexant Encoder into PAL WSS Output Operation

Step	Procedure
A	Configure the encoder so it generates a standard PAL-B, D, G, H, or -I output with the desired overscan compensation percentage. This can be done through the use of a standard PAL autoconfiguration mode (Appendix B) or a custom register set.
B	Probe or look up the input clock frequency to the encoder. This frequency can be found in Appendix B for all autoconfiguration modes and almost always matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 625-line formats: WSSINC (decimal) = 2^{20} / (200*10^{-9} * F_{CLK})*(1)*
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66.
E	Program the CX25898/9's register 6A through 66 with the hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to 4 hex. The EWSSF2 bit has no effect with WSS or CGMS since Field 2-line 23 may not contain any encoded elements with the PAL output.
G	Write the WSSDAT registers with correct data per the ITU-R BT.1119 and EN 300 294 standards. The encoder generates the PAL WSS run-in and start code automatically but the data is under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal. WSSDAT[1], least significant bit of register 60, contains the data bit b0 as described in the standards, and WSSDAT[14] contains the most significant data bit, b13. Any information written to WSSDAT[20:15], in register 64, will be ignored for PAL WSS.
H	Use an oscilloscope or VM700 from Tektronix to verify WSS data is present on line 23 of Field 1 within the PAL video signal. Use 75 Ω termination.

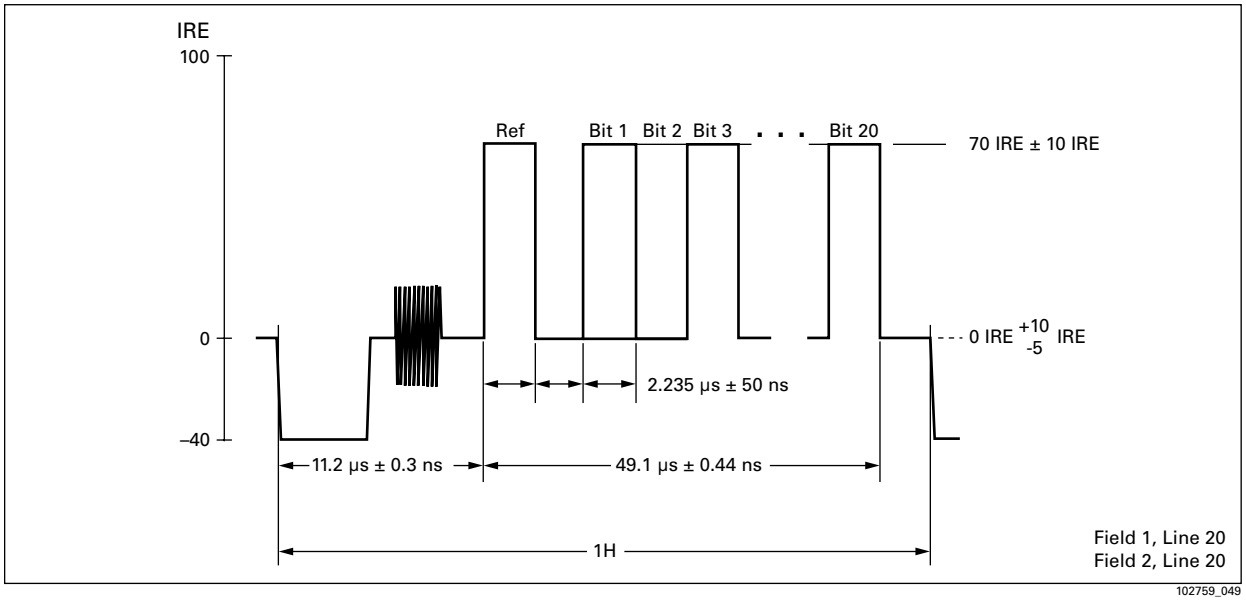
FOOTNOTE:
(1) The F_{CLK} term will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated.

The CX25898/9 is compliant with both major standards governing Wide Screen Signaling within 625-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *ITU-R BT.1119* and *EN 300 294* standards.

1.4.34.2 WSS for NTSC -M, J Outputs

For 525-line systems such as NTSC, lines 20 and 283 are used to transmit the all the WSS information required by the enhanced television receiver. An illustration of a typical NTSC video output Composite or Luma signal containing WSS data from the CX25898/9 is shown in Figure 37.

Figure 37. Typical WSS NTSC Analog Waveform Compatible to EIAJ CPR-1204 and IEC 61880-1



The bit frequency of each WSS bit encoded within line 20 and/or line 283 is the NTSC color subcarrier frequency divided by 8 (i.e., FSC / 8) or about 447.443 kHz. The peak-to-peak amplitude of the waveform present on line 23 is 490 mV with a tolerance of 14 percent. The signal's shape will be a sine-squared, pulse-based waveform. The data format utilized for CPR-1204 based information is standard binary whereby a 1 is denoted by a waveform level of 70 IRE (~490 mV) and a 0 as 0 IRE (video blank level).

The NTSC WSS sequence present on lines 20/283 is comprised of a start code, a data payload, and a Cyclic Redundancy Check (CRC) sequence. The total sequence of 22 bits takes up approximately 49.1 microseconds of line 20 or line 283. Each WSS bit therefore has a period of 2.235 µs ± 50 ns, as shown in Figure 37. The start code consists of 2 consecutive bits—a 1 and then a 0 transmitted in this order. The Conexant video encoder automatically generates the start code. This is a reference signal used as a trigger mechanism by Japanese-enhanced WSS TVs to change features such as the aspect ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25898/9 will not transmit new WSS data within lines 20 or 283 until the final WSSDAT register, address 0x64–WSSDAT[20:13], has be programmed. This byte of information can be the same value as before, or not, but it must be written to via the serial bus. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, without the presence of black bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the NTSC image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the program's 3D information, source information, signal format, category code, control code, character code, or the fact that Word 2 simply contains no additional data. This bit field is comprised of b3, b4, b5, and b6, where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the *EIAJ (Electronic Industries Association of Japan) CPR-1204* standard *(March 1997),* page 3.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the length and time remaining of the broadcast or the 3D signal format or audio and pull-down information or data pertaining to the consumer equipment package ID and code. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the *EIAJ CPR-1204* standard *(March 1997)* pages 4–9.

The final six bits (b20, b19, b18, b17, b16, b15) comprise the error check code called CRC. The CRC used for NTSC WSS EIAJ CPR-1204 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 20/283 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25898/9 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204* standard *(March 1997)* page 10.

In summary, to enable WSS within line 20 or line 283 of the NTSC Composite signal (or Luma channel within a NTSC S-Video output), perform the sequence of serial writes found in Table 15.

Table 15. Serial Writes Required to Switch Conexant Encoder into NTSC WSS Output Operation

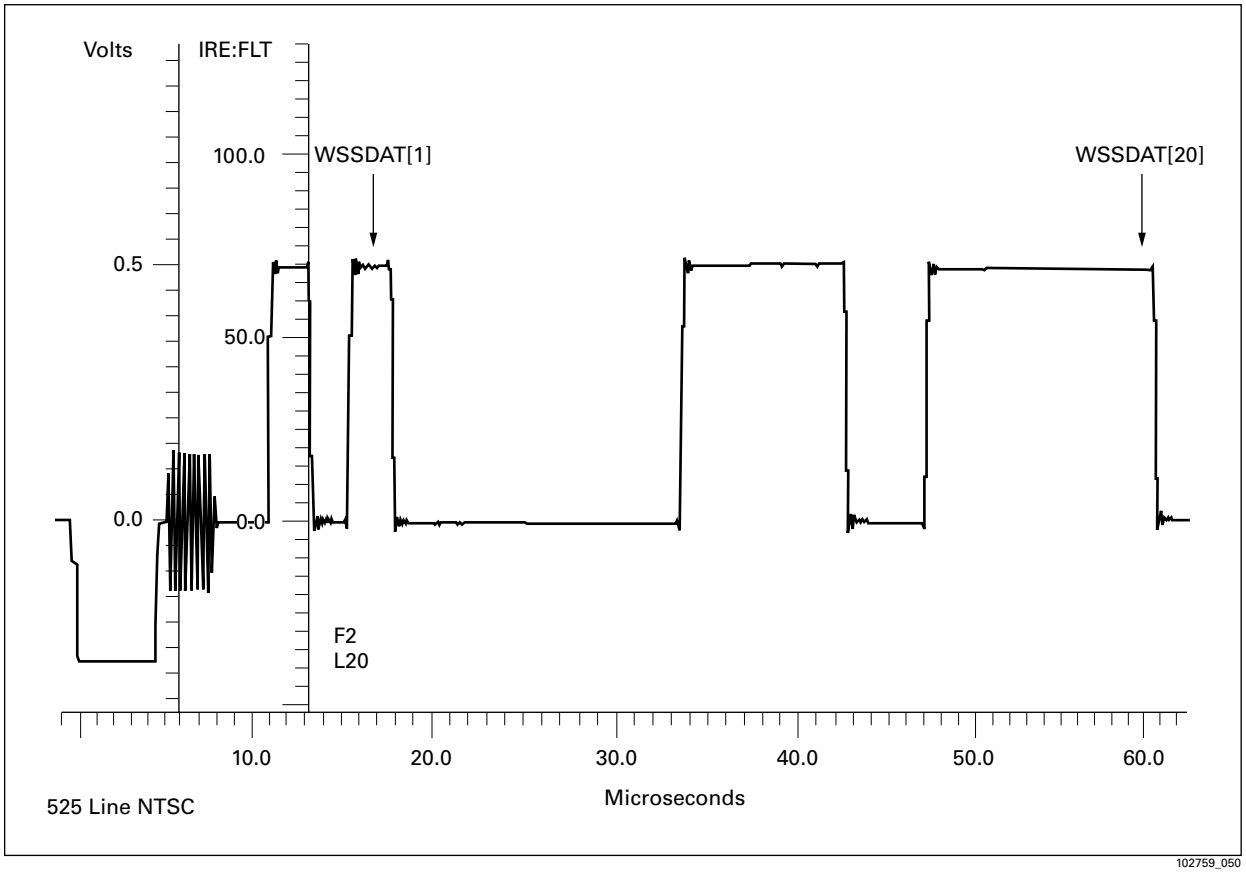
Step	Procedure
A	Configure the encoder so it generates a standard NTSC-M or NTSC-J output with the desired overscan compensation percentage. This can be done through the use of a standard NTSC autoconfiguration mode (Appendix B) or a custom register set.
B	If a NTSC-M (North America, Taiwan) output is desired, leave the SETUP bit set to 1. If a NTSC-J output is desired, reset the SETUP bit to 0.
C	Probe or look up the input clock frequency to the encoder. This frequency can be found in Appendix B for all autoconfiguration modes and almost always matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
D	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 525-line formats: WSSINC (decimal) = 2^{20} / (2.234*10^{-6}* F_{CLK})*(1)*
E	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For autoconfiguration mode #0, with F_{CLK} equal to 28.195793 MHz, WSSINC converts to 0 41 06 hex.
F	Program the CX25898/9's register 6A through 66 with the five hexadecimal nibbles from the previous step.
G	Set the EWSSF2 bit and EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to 0x0C. These bits have the effect of turning on WSS encoding for Field 2 (EWSSF2 bit) and Field 1 (EWSSF1).
H	Write the WSSDAT registers with correct data per the EIAJ CPR 1204 standard. The encoder generates the NTSC WSS start code automatically but the data and CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
I	Use an oscilloscope to verify WSS data is present on line 20 and/or line 283 within the NTSC video signal. Figure 38 shows the CX25898/9 encoder's Field 1, line 20 NTSC output after the encoder was previously programmed into autoconfiguration mode #0 and WSS enabled. The data encoded onto line 20 is FC F0 1 hex. WSSDAT[20:13] (register 0x64) has been written with FC, WSSDAT[12:15] (register 0x62) equals F0, and WSSDAT[20:13] (lowest nibble of register 0x60) has been written with C1. Register 0x60 also turned on WSS on Fields 1 and 2.

FOOTNOTE:

(1) The F_{CLK} term will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated.

An illustration of a WSS NTSC waveform with WSSDAT = FC F0 1 hex from the CX25898/9 is shown in Figure 38.

Figure 38. CX25898/9 WSS NTSC Line 20 Analog Waveform; WSSDAT = FC F0 1 hex



WSSDAT[2:0] = FC F0 1 hex in Figure 38 is just sample data. It has no correlation to the CRC or other required Word 1 and 2 values to actually enable WW/CGMS-A. This data was used to illustrate that WSSDAT[1] is placed at the beginning of line 20, and WSSDAT[20] is placed at the end of line 20.

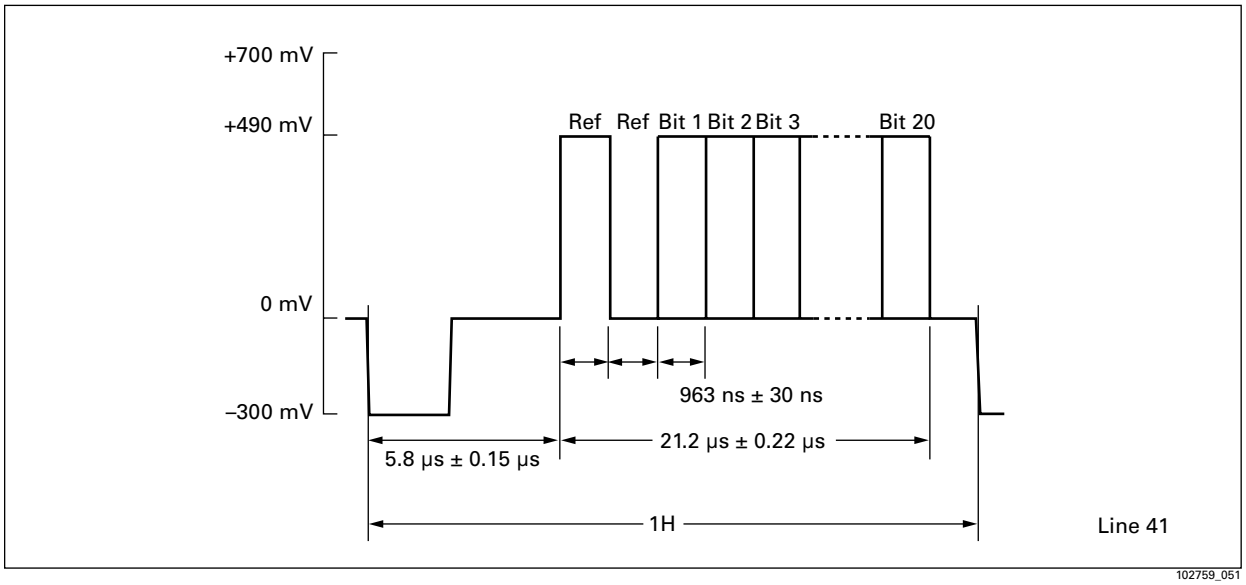
The CX25898/9 is compliant with Japan's *EIAJ CPR 1204* standard and the world IEC 61880-1 standard governing Wide Screen Signaling within 525-line television systems. For exact bit settings, definitions, timing, and other requirements, consult these documents.

1.4.35 Wide Screen Signaling—High-Definition TV

1.4.35.1 WSS for 480p (525p) HDTV Outputs

For HDTV systems that receive the progressive 480p (525p in Japan) resolution, line 41 is used to transmit all the WSS information required by the enhanced television receiver. An illustration of a typical 480p (525p) Luma (Y) video signal containing WSS data from the CX25898/9 is shown in Figure 39.

Figure 39. Typical WSS 480p (525p) Luma Analog Waveform



NOTE: Figure 39 is compatible with EIAJ CPR-1204-1 and CEA 805A_TYPEA.

The bit frequency of each WSS bit encoded within line 41 is the horizontal scanning frequency multiplied by a factor of 33 which equates to 1038.5 kHz. The peak-to-peak amplitude of the waveform present on line 41 is 490mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 41. The data format used for CPR-1204-1 based information is standard binary, whereby a 1 is denoted by a waveform level of 490 mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 480p (525p) HDTV WSS sequence present on line 41 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 21.2 µs of this line. Each WSS bit therefore has a period of 0.963 µs ±30 ns as shown in Figure 39. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX25898/9 video encoder. This is a reference signal used as a trigger mechanism by Japanese-enhanced WSS 480p (525p) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25898/9 will not transmit new WSS data within line 41 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has been programmed. This byte of information can be the same value as the previous WSS data payload, or

not, but it must be written to via the serial bus to trigger a new WSS encode operation. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 480p (525p) image appears without horizontal black stripes (no letterbox), or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the program's 3D information, source information, signal format, category code, control code, character code, or the fact that Word 2 simply contains no additional data. As of the print date of this data sheet, only Word1 values between 0001 and 1010 binary are defined. This bit field is comprised of b3, b4, b5, and b6, where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the *EIAJ (Electronic Industries Association of Japan) CPR-1204-1 standard (March 1998) page 2*.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the *EIAJ CPR-1204 standard (March 1997) pages 4–9* and *EIAJ CPR-1204-1 standard (March 1998) pages 2–4.*

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-1 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 41 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25898/9 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204-1 (March 1997) page 10* and/or CEA 805A_TYPEA (CEA 770-1-C and CEA 770-2 (2H) 480p) standards.

To summarize, to enable WSS within line 41 of the 480p (525p) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 16.

Table 16. Serial Writes Required to Switch Conexant Encoder into HDTV 480p (525p) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 480p (525p) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set.
B	The input clock frequency to the encoder must be 27.00000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 480-line HDTV formats: WSSINC (decimal) = 2^{20} / (963*10^{-9}* F_{CLK})[(1)] = 104856/26.001 = 40328
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 480p HDTV Y PR PB, with F_{CLK} equal to 27.00000 MHz, WSSINC converts to 0 9D 88 hex.
E	Program the CX25898/9's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit (bit 6) and EWSSF2 bit (bit 1) to 1 by programming the upper nibble of register 0x60 to C hex. Setting these bits has the effect of turning on WSS encoding within the 480p (525p) HDTV Y analog output.
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 41 within the HDTV video signal. Some multiformity HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore a single gray line which will be the WSS-encoded data.

FOOTNOTE:

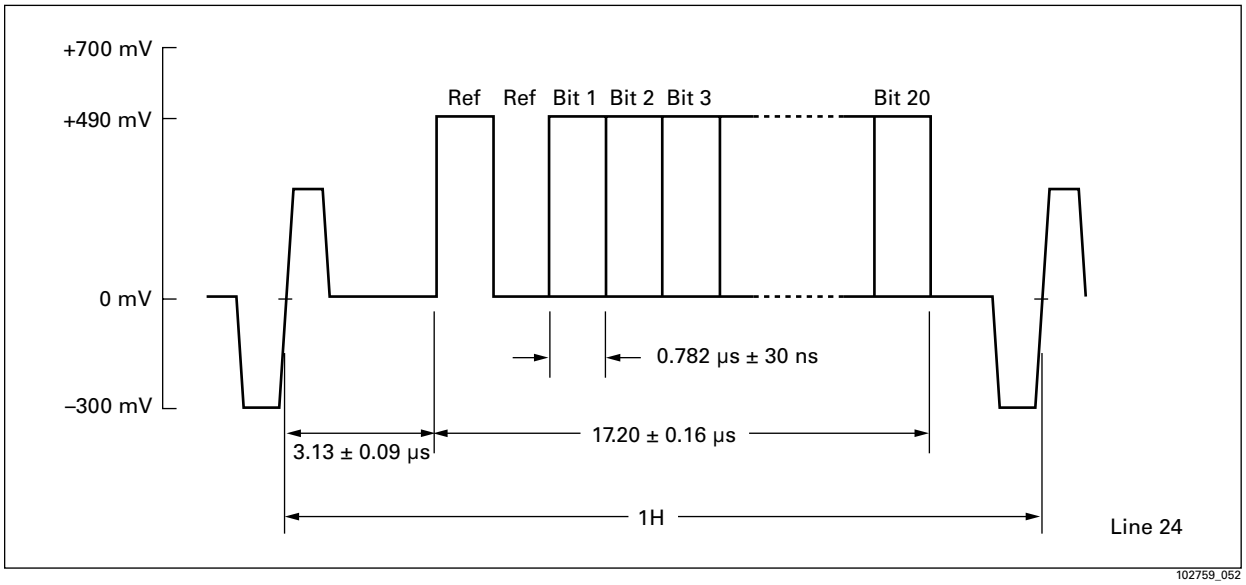
(1) The F_{CLK} term will remain the same for 480p HDTV. However, F_{CLK} will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of HDTV and standard-definition formats.

The CX25898/9 is compliant with Japan's *EIAJ CPR 1204-1 standard* governing Wide Screen Signaling within 525-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-1 standard* itself.

1.4.35.2 WSS for 720p (750p) HDTV Outputs

For HDTV systems that receive the progressive 720p (750p in Japan) resolution, line 19 (per *SMPTE 296M standard*) or line 24 (per Japan's *EIAJ CPR-1204-2*) is used to transmit all the WSS information required by the enhanced television receiver. An illustration of a typical 720p (750p) Luma (Y) video signal containing WSS data from the CX25898/9 is shown in Figure 40.

Figure 40. Typical WSS 720p (750p) Luma Analog Waveform



NOTE: Figure 40 is compatible with EIAJ CPR-1204-2.

The bit frequency of each WSS bit encoded within line 24 is the horizontal scanning frequency multiplied by (1650 / 58) which equates to 1278.8 kHz. The peak-to-peak amplitude of the waveform present on line 24 is 490 mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 24. The data format utilized for CPR-1204-2 based information is standard binary whereby a 1 is denoted by a waveform level of 490 mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 720p (750p) HDTV WSS sequence present on line 24 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 17.2 microseconds of this line. Each WSS bit therefore has a period of 0.782 µs ± 30 ns as shown in Figure 40. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX25898/9 video encoder. This is a reference signal used as a trigger mechanism by Japanese enhanced WSS 720p (750p) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25898/9 will not transmit new WSS data within line 24 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has be programmed. This byte of information can be the same value as the previous WSS data payload, or not, but it must be written to via the serial bus to trigger a new WSS encode

operation. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 720p (750p) image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the time remaining in the program, or the fact that Word 2 simply contains no additional data. Word 1's bit field is comprised of b3, b4, b5, and b6 where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g. b3, b4, b5, b6), consult the EIAJ (Electronic Industries Association of Japan) *CPR-1204-2 standard (January 2000) page 3*.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of al

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-2 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 24 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25898/9 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204 standard (March 1997) page 10*.

To summarize, to enable WSS within line 24 of the 720p (750p) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 17.

Table 17. Serial Writes Required to Switch Conexant Encoder into HDTV 720p (750p) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 720p (750p) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set.
B	The input clock frequency to the encoder must be 74.25000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 720-line HDTV formats: WSSINC (decimal) = 2^{20} / (0.782*10^{-6}* F_{CLK})$^{(1)}$ = 104856/58.0635= 18059
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 720p HDTV Y PR PB, with F_{CLK} equal to 74.25000 MHz, WSSINC converts to 0 46 8B hex.
E	Program the CX25898/9's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit (bit 6) and EWSSF2 bits (bit 1) to 1 by programming the upper nibble of register 0x60 to C hex. Setting these bits has the effect of turning on WSS encoding within the 720p (750p) HDTV Y analog output.
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 24 within the HDTV video signal. Some multi-format HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore a single gray line which will be the WSS encoded data.

FOOTNOTE:

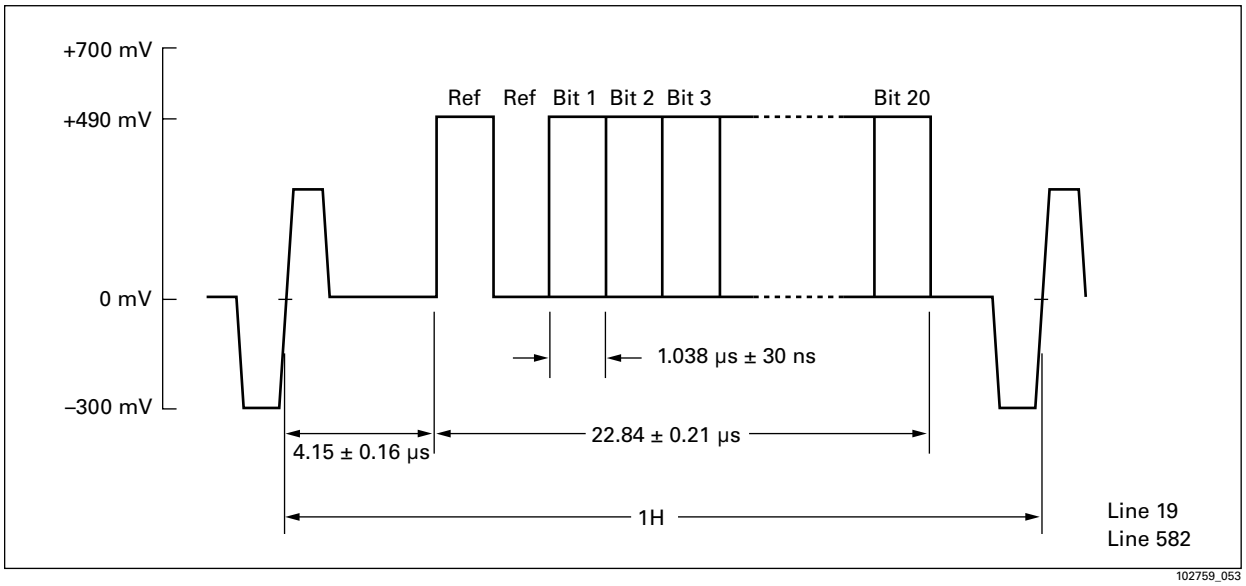
(1) The F_{CLK} term will remain the same for 720p HDTV. However, F_{CLK} will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of other HDTV and standard-definition formats.

The CX25898/9 is compliant with Japan's *EIAJ CPR 1204-2 standard* governing Wide Screen Signaling within 750-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-2 standard* itself.

1.4.35.3 WSS for 1080i (1125i) HDTV Outputs

For HDTV systems that receive the interlaced 1080i (a.k.a. 1125i in Japan) resolution, lines 17 and 579 per the SMPTE 274M standard are used to transmit all the WSS information required by the enhanced television receiver. According to Japan's EIAJ CPR-1204-2 standard, lines 19 and 582 are used to transmit this same WSS information required by the enhanced television receiver. An illustration of a typical 1080i (1125i) Luma (Y) video signal containing WSS data from the CX25898/9 is shown in Figure 41.

Figure 41. Typical WSS 1080i (1125i) Luma Analog Waveform



NOTE: Figure 41 is compatible with EIAJ CPR-1204-2.

The bit frequency of each WSS bit encoded within line 19/582 is the horizontal scanning frequency multiplied by (2200 / 7) which equates to 963 kHz. The peak-to-peak amplitude of the waveform present on line 19/582 is 490 mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 19 or 582 or both. The data format utilized for CPR-1204-2 based information is standard binary whereby a 1 is denoted by a waveform level of 490 mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 1080i (1125i) HDTV WSS sequence present on line 19 or 582 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 22.8 µs of this line. Each WSS bit therefore has a period of 1.038 µs ±30 ns as shown in Figure 41. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX25898/9 video encoder. This is a reference signal used as a trigger mechanism by Japanese enhanced WSS 1080i (1125i) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25898/9 will not transmit new WSS data within line 19/582 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has been programmed. This byte of information can be the same value as the previous WSS data payload, or

not, but it must be written to via the serial bus to trigger a new WSS encode operation. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 1080i (1125i) image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the time remaining in the program, or the fact that Word 2 simply contains no additional data. Word 1's bit field is comprised of b3, b4, b5, and b6 where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the EIAJ (Electronic Industries Association of Japan) CPR-1204-2 standard (January 2000), page 3.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the *EIAJ CPR-1204* standard (March 1997) pages 4–9.

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-2 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 19/582 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25898/9 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204* standard (March 1997) page 10.

To summarize, to enable WSS within line 19 or line 582 of the 1080i (1125i) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 18.

Table 18. Switching Conexant Encoder into HDTV 1080i (1125i) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 1080i (1125i) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set. Make certain that the HSYNCI and VSYNCI bits in register C6 are programmed properly to match the polarity of the incoming HSYNC and VSYNC signals. Failure to do so will prevent 1080i WSS from being enabled.
B	The input clock frequency to the encoder must be 74.25000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 1080-line HDTV formats: WSSINC (decimal) = 2^{20} / (1.038*10^{-6}* F_{CLK})$^{(1)}$ = 104856/77.0715= 13605
D	Once WSSINC has been solved, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 1080i HDTV Y PR PB, with F_{CLK} equal to 74.25000 MHz, WSSINC converts to 0 35 25 hex.
E	Program the CX25898/9's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set both the EWSSF2 bit and EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to C hex. These bits have the effect of turning on WSS encoding for Field 2 (EWSSF2 bit) and Field 1 (EWSSF1).
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 19 and/or line 582 within the HDTV video signal. Some multi-format HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore one or two gray lines which will be the WSS encoded data.

FOOTNOTE:

(1) The F_{CLK} term will remain the same for 1080i HDTV. However, F_{CLK} will change very time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of HDTV and standard-definition formats.

The CX25898/9 is compliant with Japan's *EIAJ CPR 1204-2 standard* governing Wide Screen Signaling within 1125-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-2 standard* itself.

1.4.36 Chrominance and Luminance Processing

The CX25898/9 accepts digital pixels in either a YCrCb or RGB format. After receipt, these pixels are sent through an internal multiplexer and then 2x sampled. Next, the input data is converted to an internal YUV format. After that, the Y and UV components are filtered and finally upsampled to the system clock frequency.

The luminance signal is always low-pass filtered using the upsampling filter response illustrated in Figure 42. Additional peaking or reduction filters can be enabled (see Figures 43, 44, and 45), using the PKFIL_SEL[1:0] register field. The peaking filters are optimized for high bandwidth frequency response, and optimal picture quality.

The default chrominance filter response is illustrated in Figure 46. An alternate wide bandwidth response can be selected using register bit CHROMA_BW, as illustrated in Figure 47.

Figure 42. Digital Luminance Upsampling Filter

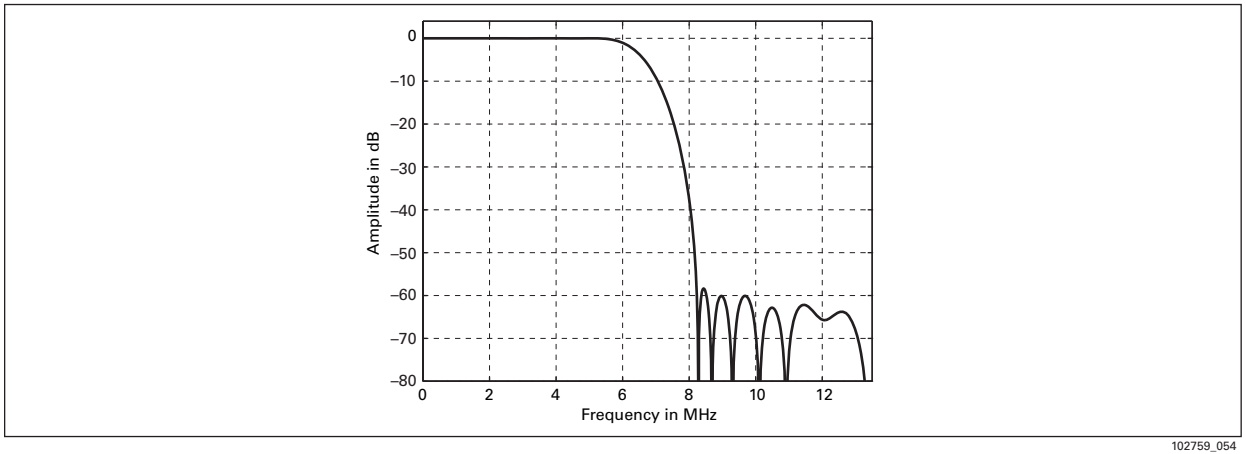


Figure 43. Text Sharpness (Luminance Upsampling) Filter with Peaking Options

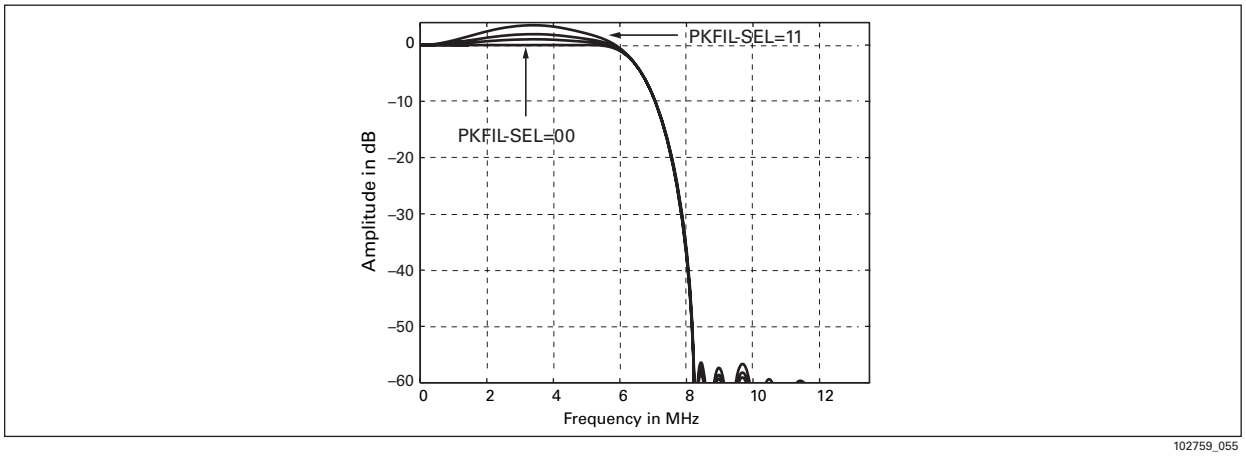


Figure 44. Close-Up of Text Sharpness (Luminance Upsampling) Filter with Peaking and Reduction Options

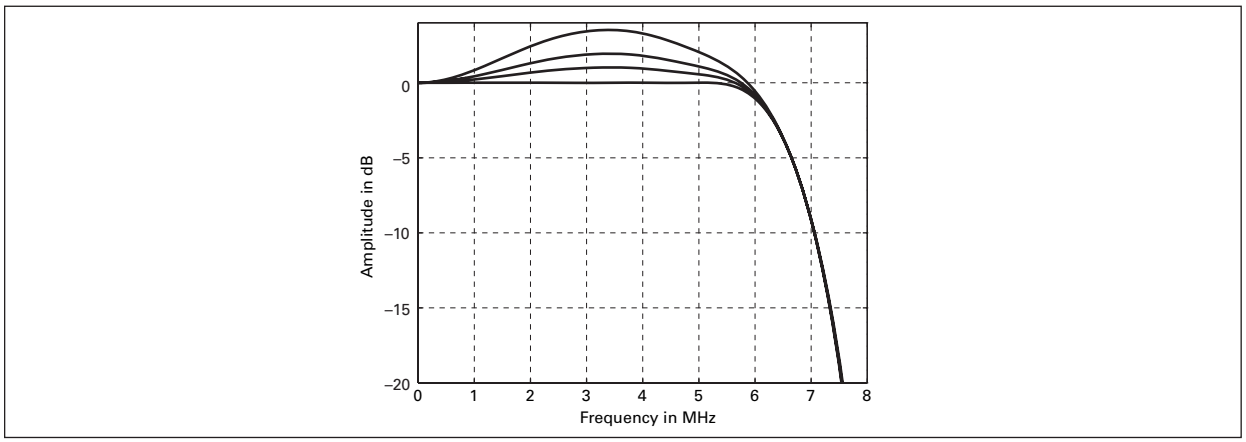


Figure 45. Zoom-In of Text Sharpness (Luminance Peaking) Filter Options

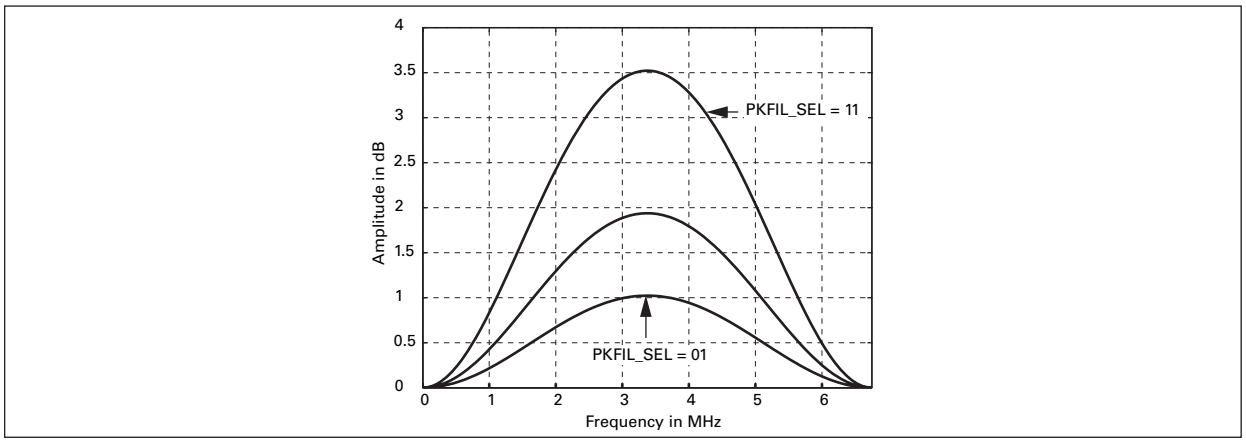


Figure 46. Digital Chrominance Standard Bandwidth Filter (CHROMA_BW = 0—Default)

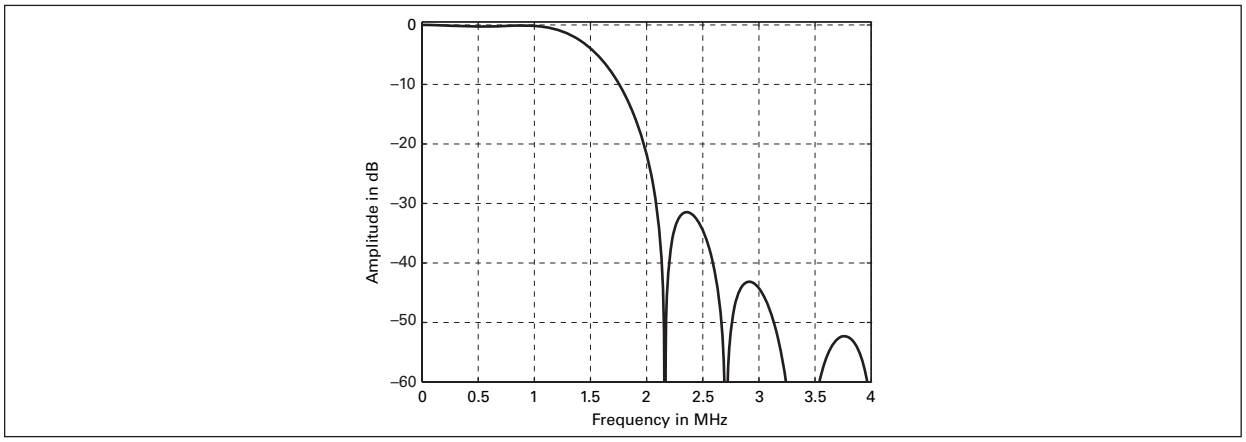
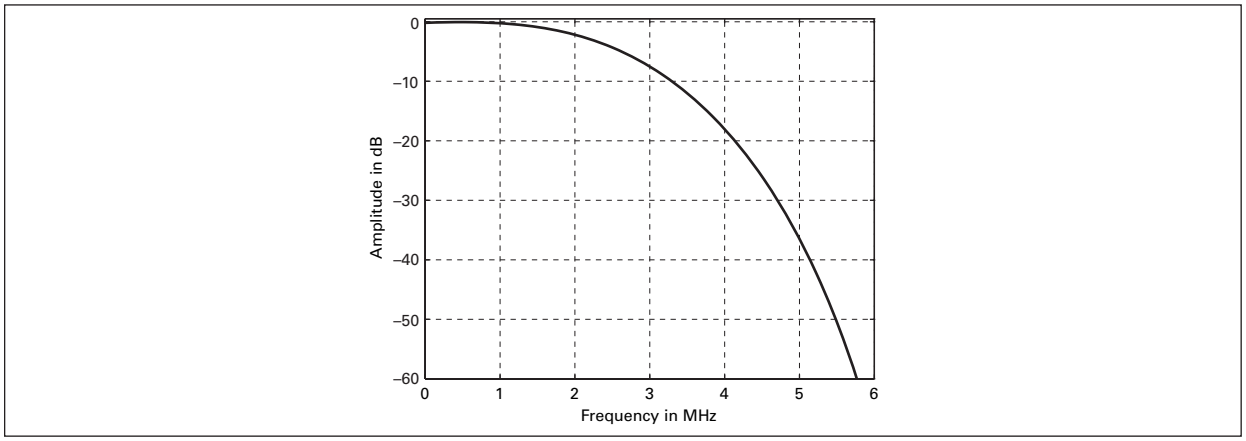


Figure 47. Digital Chrominance Wide Bandwidth Filter (CHROMA_BW = 1)



1.4.37 Color Bar and Blue Field Generation

This encoder has two internal color bar generators. Preflicker HDTV filter color bars are enabled by setting the FFCBAR bit to a logical 1. Postflicker SDTV filter color bars are enabled by setting the ECBAR bit to a logical 1. The SDTV color bars have 100 percent amplitude levels and 75 percent chroma levels.

FFCBAR color bars are optimized for RGB input mode and ECBAR color bars are optimized for YCrCb input mode.

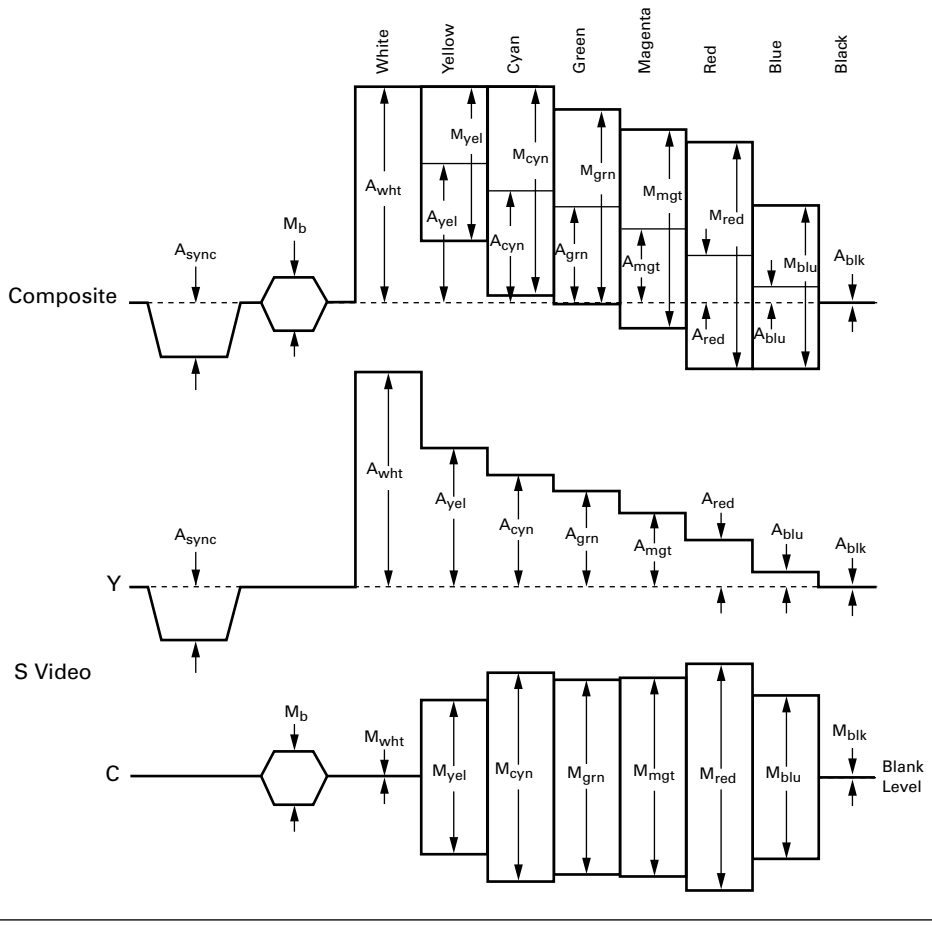
The device uses the H_BLANKO register value to determine the starting point of the color bars, and the H_ACTIVE register value to determine the width. Eight bars are displayed, with the colors and amplitudes being generated internally. The pixel inputs (PIX[23] to PIX[0] are ignored in color bar mode. The CX25898/9 must be programmed with the appropriate MY, MCR, and MCB register values for the desired input format, RGB or YCrCb. This can be done through an autoconfiguration mode.

The CX25898/9 also produces a SDTV blue field by setting register bit BLUEFLD to 1. Pixel inputs are ignored while any of the color generation wave forms are being produced.

While SDTV color bars (ECBAR =1) or blue field are generated, the DENC does not need to receive the HSYNC*, VSYNC*, BLANK*, or CLKI input signals. The only requirement for these patterns is the presence of the main encoder clock found between the XTALIN and XTALOUT ports (master, pseudo-master interface).

Figure 48 and Tables 19 and 20 illustrate the voltage amplitudes for the different color bar outputs from the Conexant encoder.

Figure 48. Composite and S-Video Analog Voltage Levels (SDTV Color Bars)



GENERAL NOTE:
1. Ax is the DC (luminance) amplitude referenced to black, except for A_{blk} and A_{sync}, which are referenced to blank.
2. Mx numbers are the peak-to-peak amplitudes of the subcarrier waveform.

102759_060

Table 19. Composite and Luminance Color Bar Amplitudes

Y and Composite Amplitudes	A_{sync}	A_{wht}	A_{yel}	A_{cyn}	A_{grn}	A_{mgt}	A_{red}	A_{blu}	A_{blk}
NTSC-M (V)	–0.286	0.661	0.441	0.347	0.292	0.203	0.149	0.054	0.0536
NTSC-J (V)	–0.286	0.714	0.477	0.375	0.316	0.220	0.161	0.059	0
PAL-B (V)	–0.300	0.700	0.465	0.368	0.308	0.217	0.157	0.060	0

GENERAL NOTE: A_x is the DC (luminance) amplitude referenced to black, except for A_{blk} and A_{sync}, which are referenced to blank.

Table 20. Composite and Chrominance Color Bar Magnitudes

C and Composite Magnitudes	M_b	M_{wht}	M_{yel}	M_{cyn}	M_{grn}	M_{mgt}	M_{red}	M_{blu}	M_{blk}
NTSC-M (V)	0.286	0	0.444	0.630	0.589	0.589	0.629	0.444	0
NTSC-J (V)	0.286	0	0.480	0.681	0.636	0.636	0.681	0.480	0
PAL-B (V)	0.300	0	0.470	0.663	0.620	0.620	0.664	0.470	0

GENERAL NOTE:
1. M_x numbers are the peak-to-peak amplitudes of the subcarrier waveform.

1.4.38 CCIR656 Mode Operation

Data transmitted from MPEG2 video decoders or various multimedia processors is often done in a format called CCIR656. This format is similar to CCIR601 in many ways but is unique in that the video sync information is embedded as codes in the data stream. As a result, no digital HSYNC or VSYNC signals are required as part of the physical interface between the timing master and slave devices. Applications for CCIR656 typically include consumer appliances such as Video CD players, DVD players, set-top boxes, and MPEG add-in cards where pin counts are limited.

The actual digital CCIR656 input data delivered to the CX25898/9 is interlaced 4:2:2 YCrCb over eight physical lines. In addition, there are two timing reference codes, one at the beginning of each video data block (Start of Active Video, SAV) and one at the end of each video data block (End of Active Video, EAV). These timing reference values consist of a unique 4-word sequence that conveys when the active video starts and ends. The CCIR656 compliant master device embeds both SAV and EAV codes into the stream where appropriate.

While in CCIR656 Mode, the CX25898/9 acts as the timing slave device. An illustration of a correct connection scheme for the slave interface is shown in Figure 49.

All data between the EAV code and SAV code are automatically inserted by the Conexant encoder. An 80 hexadecimal number is inserted for Cb and Cr samples and 10 hexadecimal for Y samples. This blanking data and SAV/EAV codes are the only differences between the CCIR656 mode and CCIR601 mode operation.

NOTE: Both EAV and SAV codes contain a prefix of FF0000 prior to the unique "XY" event code.

Pertinent SAV and EAV codes are contained in Table 21.

Figure 49. CX25898/9 Connection to CCIR656-Compatible Master Device

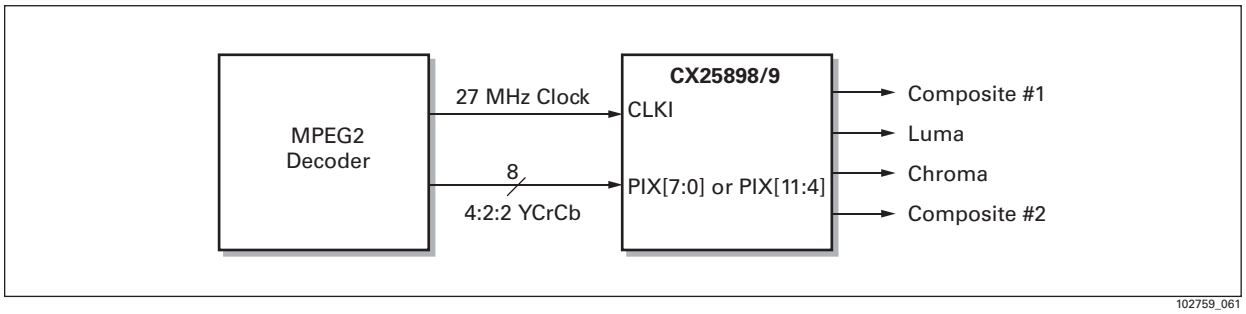


Table 21. CCIR656 "XY" Events

"XY" Event	SAV	EAV
Odd Field Vertical Blanking Lineq	0xAB	0xB6
Odd Field Active Video Line	0x80	0x9D
Even Field Vertical Blanking Line	0xEC	0xF1
Even Field Active Video Line	0xC7	0xDA

While in CCIR656 Mode, the encoder adheres to all input guidelines specified in the ITU-R BT.656-3 standard. This specification was developed for the transmission of color video signals in YCrCb format at a pixel rate of 27.000 MHz without the use of dedicated timing reference signals.

To display a DVD movie on a TV and computer monitor simultaneously, CCIR656 data must be sent from a MPEG2 decoding master device directly to the CX25898/9 encoder. Finally, various software steps are necessary so the encoder is set up to accept the interlaced YCrCb data and video timing reference codes.

The first programming step is to configure the CX25898/9 to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x480 and output a standard NTSC video output. The pertinent set of conditions for this option are:

Type of Digital Video Input:	Interlaced 4:2:2 YCrCb
Active Resolution (HorizontalxVertical):	720 pixels x 480 lines
Overscan Compensation:	None. Horizontal = 0%; Vertical = 0%
Interface:	Pseudo-master or slave
Pixel Rate	27.000 MHz
Type of Analog Video Output:	Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 28 is a perfect fit. As a result, simply use the MPEG2 decoders' serial bus mastering ability to program the CX25898/9s CONFIG[5:3] and CONFIG [2:0] fields with a binary value of 011 100. This translates into writing a hexadecimal number of 0x34 to register 0xB8, since both bits 7 and 3 are reserved, and therefore 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4, including register 0x38. The exact data transferred into these registers is contained in Appendix B.

After completion of the autoconfiguration command, the encoder expects to receive interlaced 4:2:2 YCrCb data from the clock and timing master device at a rate of 27.000 MHz with blanking regions being defined by HSYNC* and VSYNC*. Since these external signals, by definition, do not exist in CCIR656 mode, a second and final programming step is required.

After enabling autoconfiguration mode 28, the programmer must make sure to set the E656 bit to 1. This is bit 6 of register 0xD6 and enables a CCIR656 input to be received via the CX25898/9's PIX[7:0] port or PIX[11:4] port, depending on the state of the IN_MODE[3:0] field. Once this is done, the encoder disregards the synchronization signals.

Only after the completion of these steps will a DVD stream be properly encoded and rendered onto the television by the VGA Encoder.

For CCIR656 Mode operation with a PAL Composite or S-Video output, use Autoconfiguration Mode 29 instead of autoconfiguration mode 28 and program the master device to send a digital frame with an active resolution of 720x576.

1.4.39 CCIR601 Mode Operation for DVD Playback

Data coming from a DVD is often decoded by a MPEG2 decoder or graphics controller into a format called CCIR601. CCIR601 is the more common name for 4:2:2 YCrCb data at a 27 MHz pixel rate, as specified in the ITU-R BT.601 standard. This specification was developed specifically for the digitalization of color video signals.

To play a DVD movie on a television in addition to a CRT monitor, CCIR601 data must be sent from a MPEG2 decoding master device directly to the CX25898/9 encoder. This can be either a dedicated MPEG2 decoder chip or a graphics controller with this functionality. Various software steps are necessary so that the encoder enters slave or master interface and is set up to accept the interlaced YCrCb data or noninterlaced RGB digital format. After all of these steps have been executed properly, a DVD movie stream is properly encoded and rendered onto the television by the VGA encoder.

There are different capabilities among graphics controllers, MPEG2 decoders, and proprietary ASICs that impact the particular DVD implementation. This section seeks to cover the most common hardware/software configurations and the trade-offs associated with each. If the reader has an interface idea about the routing of data from the CCIR601 source to encoder that is not discussed here, please contact your local Conexant Field Applications Engineer for further technical support.

1.4.39.1 CCIR601 Data In/NTSC Out

The first option to playing a DVD movie via the CX25898/9 is to send the digital video CCIR601 data directly to the encoder from the MPEG2 decoder. In this case, the graphics controller does not have any effect on the CCIR601 digital stream arriving at the input of the encoder because it bypassed the data or the data was routed around the controller. In either case, the CX25898/9 must be configured to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x480 and output a standard NTSC video output. The pertinent set of conditions for this option are:

- Type of Digital Video Input: Interlaced 4:2:2 YCrCb
- Active Resolution (HorizontalxVertical): 720 pixels x 480 lines
- Overscan Compensation: None. Horizontal = 0%; Vertical = 0%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.000 MHz
- Type of Analog Video Output: Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 28 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011100. This translates into writing a hexadecimal number of 0x34 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate value for this type of DVD configuration into

its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix B.

After completion of the autoconfiguration command, the encoder expects to receive interlaced CCIR601 data from the clock and timing master device at a rate of 27.000 MHz. If this occurs, approximately 40 clocks later (i.e., pipeline delay through the decoder), the CX25898/9 begins transmitting a NTSC-compatible S-Video or Composite Video signal containing the DVD movie.

1.4.39.2 CCIR601 Data In/PAL Out

The second option is very similar to the first. In this scenario, the interlaced CCIR601 video data is transmitted directly to the encoder from the MPEG2 decoder. However, instead of generating a NTSC signal, the encoder produces a PAL-BDGHI compatible DVD movie output. The active resolution changes as well for this alternative by increasing to 720x576.

To enable DVD playback in this scenario, the CX25898/9 must be configured to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x576 and output a standard PAL video output. The pertinent set of conditions for this option are:

- Type of Digital Video Input: Interlaced, 4:2:2 YCrCb
- Active Resolution (HorizontalxVertical): 720 pixels x 576 lines
- Overscan Compensation: None. Horizontal = 0%; Vertical = 0%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.000 MHz
- Type of Analog Video Output: Standard PAL[PAL-BDGHI]

Given this set of conditions, autoconfiguration mode 29 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011 100. This translates into writing a hexadecimal number of 0x35 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate value for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix B.

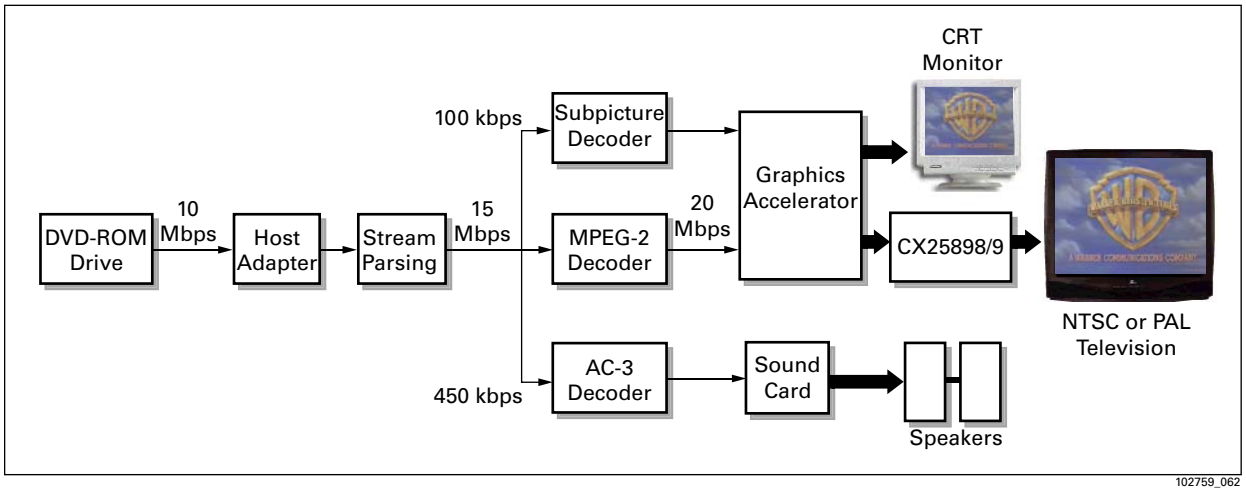
After completion of the autoconfiguration command, the encoder expects to receive interlaced CCIR601 data from the clock and timing master device at a rate of 27.000 MHz. If this occurs, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.4.39.3 VGA-Compatible RGB Data In/NTSC Out

The third option for DVD playback is unlike the previous two methods. In this case, the MPEG2 decoder's 4:2:2 YCrCb interlaced data is sent as an input to the graphics controller. In turn, the controller deinterlaces and color space converts the CCIR601 data into a noninterlaced RGB format. The encoder finally ends up receiving this standard VGA digital data from the graphics controllers digital output port for generation into an analog TV signal.

This design is illustrated in Figure 50.

Figure 50. DVD Playback Utilizing Graphics Controller for Color-Space and Progressive Scan Conversion



To enable DVD playback with this architecture, the graphics controller must be able to de-interlace and color space convert the CCIR601 input data from the MPEG2 decoding source. Furthermore, since the pixel clock frequency is not 27.000 MHz any longer, the graphics controller must have the ability to synchronize the pixel data to the clock rate dictated by the CX25898/9's CLKO signal. Finally, the controller must be able to function as the clocking master and timing slave as described in Section 1.4.7.

The recommended interface for the CX25898/9 for this option is master and the encoder must be programmed to accept noninterlaced RGB data and output a standard NTSC video output. The pertinent factors for the NTSC option are:

- Type of Digital Video Input: Progressive Scan/Noninterlaced; 24-bit RGB per pixel Multiplexed Input Format
- Active Resolution (HorizontalxVertical): 720x480
- Overscan Compensation Ratio: Minimal; Horizontal = 1.24%; Vertical = 1.23%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.6923 MHz
- Type of Analog Video Output: Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 44 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 101100. This translates into writing a hexadecimal number of 0x54 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix B.

After completion of the autoconfiguration command, the encoder enters master interface. In addition, the CX25898/9 will expect to receive digital frames with an active resolution of 720x576 comprised of noninterlaced RGB data at a pixel rate of 27.6875 MHz. If these events occur, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.4.39.4 VGA-Compatible RGB Data In/PAL Out

The CX25898/9 can also be programmed to accept noninterlaced RGB data and output a standard PAL video output with ultra-low overscan compensation. The pertinent factors for this PAL option are:

- Type of Digital Video Input: Progressive Scan/Noninterlaced; 24-bit RGB per pixel Multiplexed Input Format
- Active Resolution (HorizontalxVertical): 720x576
- Overscan Compensation Ratio: Minimal; Horizontal = 0.017%; Vertical = 1.00%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.6875 MHz
- Type of Analog Video Output: Standard PAL [PAL-B, D, G, H, I]

Given this set of conditions, autoconfiguration mode 31 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011100. This translates into writing a hexadecimal number of 0x37 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers in contained in Appendix B.

After completion of the autoconfiguration command, the encoder enters master interface. In addition, the CX25898/9 will expect to receive digital frames with an active resolution of 720x576 comprised of noninterlaced RGB data at a pixel rate of 27.6875 MHz. If these events occur, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.4.40 SECAM Output

Unlike the Bt868/869, the CX25898/9 now includes an encoder block for conversion of digital video data into a SECAM Composite (CVBS) and/or a SECAM S-Video signal.

Like other standard-definition video outputs, any active resolution from 320x200 to 1024x768 can be supported with the SECAM encoder block. The circuit accepts RGB or YCrCb data in a variety of multiplexed input formats, reformats the digital data, and finally routes the stream through the four on-chip Digital-to-Analog Converters (DACs). The encoder supports all variations of the SECAM analog video standard including those commonly used in France (SECAM-L), Eastern Europe/Russia (D, K, K1), and Greece/Middle East (B, G, H).

The SECAM specific processing is achieved in this block by pre-emphasizing the color difference signals. Once data is received, it is converted to an internal YUV format. Next, the Y component is filtered and then upsampled to the system clock frequency while the UV components are used to frequency modulate the two subcarrier frequencies appropriately.

For information on the luminance signal, peaking and reduction filters, and default chrominance filter, see Section 1.4.36.

The color subcarrier frequencies, 4.25000 MHz for Db and 4.40625 MHz for Dr, are controlled by a number of registers, chiefly MSC_DB[31:0] for Db and MSC[31:0] for Dr. Figure 51 illustrates the SECAM pre-emphasis filter response at higher (>3 MHz) frequencies within the standard-definition television passband. The figure illustrates the SECAM-specific, pre-emphasis filter response for the modulated chrominance signal.

Table 22 lists three complete register sets for the most common desktop input resolutions with the SECAM output. This output adheres to the SECAM target video parameters included in Table 53. Correct timing occurs only if the Conexant encoder is programmed correctly with the register values listed in Table 22, the master device provides the RGB data at the listed clock frequency (CLKI and CLKO), and the interface bits are modified to match the desired connection type.

Figure 51. SECAM High Frequency Pre-emphasis Filter

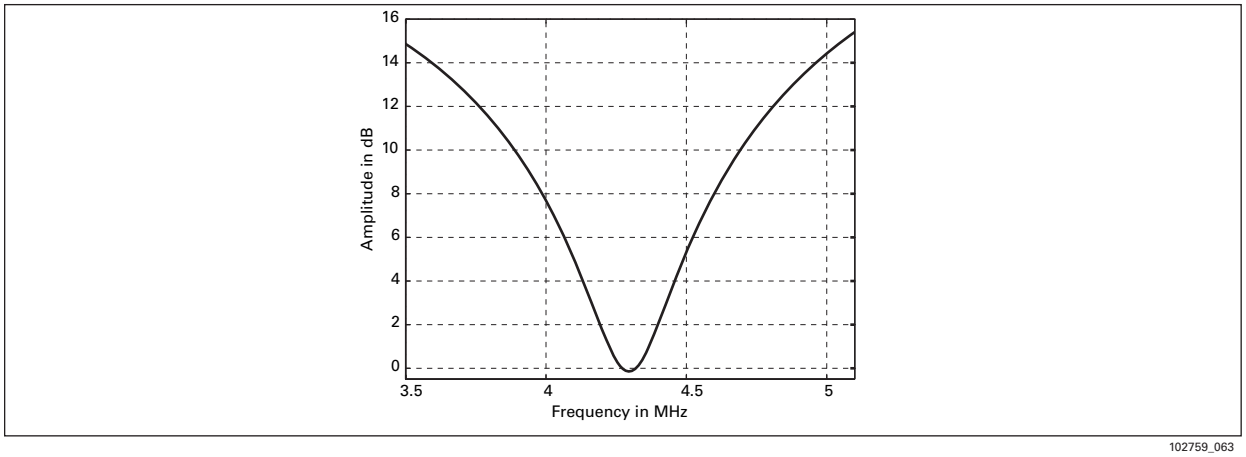


Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(1 of 5)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	**800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%**	**1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%**
CLKI and CLKO Frequency	29.500007 MHz	36.000000 MHz	67.687489 MHz
State of PLL_32CLK bit	0	0	1
Internal Pixel Clock Frequency	29.500007 MHz	36.000000 MHz	45.124993 MHz
Register Address	**CX25898/9 Register Values**	**CX25898/9 Register Values**	**CX25898/9 Register Values**
0x00	00	00	00
0x02	00	00	00
0x04	00	00	00
0x06	00	00	00
0x2E	00	00	00
0x30	00	00	00
0x32	00	00	00
0x34	00	00	00
0x36	00	00	00
0x38	00	00	20
0x3A	00	00	00
0x3C	80	80	80
0x3E	80	80	80
0x40	80	80	80
0x42*(1)*	8B	8E	9B
0x44*(1)*	A0	E3	5D
0x46*(1)*	E1	38	1C
0x48*(1)*	24	1E	18
0x4A*(1)*	28	3A	5F
0x4C*(1)*	3B	77	C4

Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(2 of 5)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
0x4E[1]	25	1C	13
0x50[1]	28	3A	5F
0x52[1]	3B	77	C4
0x54[1]	25	1C	13
Register Address	**CX25898/9 Register Values**	**CX25898/9 Register Values**	**CX25898/9 Register Values**
0x56[1]	AC	18	7A
0x58[1]	20	27	31
0x5A	00	00	00
0x5C	00	00	00
0x5E	00	00	00
0x60	00	00	00
0x62	00	00	00
0x64	00	00	00
0x66	3C	E3	D9
0x68	00	00	00
0x6A	00	00	00
0x6C[2]	46	46	46
0x6E	00	00	00
0x70	0F	0F	0F
0x72	00	00	00
0x74	01	01	01
0x76	60	00	48
0x78	80	20	00
0x7A	8A	AA	D4
0x7C	A6	CA	FC

Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(3 of 5)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
0x7E	68	9A	E2
0x80	C1	0D	79
0x82	2E	29	28
0x84	F2	FC	FE
0x86	27	39	4B
0x88	00	00	00
0x8A	B0	C0	91
0x8C	0A	8C	5E
0x8E	0B	03	0D
Register Address	**CX25898/9 Register Values**	**CX25898/9 Register Values**	**CX25898/9 Register Values**
0x90	71	EE	B6
0x92	5A	5F	76
0x94	E0	58	00
0x96	06	0A	3F
0x98	00	66	A4
0x9A	50	96	A0
0x9C	72	0	55
0x9E	1C	0	15
0xA0	0D	10	1E
0xA2	8C	8C	24
0xA4	F0	F0	F0
0xA6	58	57	56
0xA8(1)	76	5F	4B
0xAA(1)	4D	3E	31
0xAC	8C	8C	8C

Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(4 of 5)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
0xAE[1]	EA	55	76
0xB0[1]	BE	55	4A
0xB2[1]	3C	55	FF
0xB4[1]	26	1F	18
0xB6	00	0	0
0xB8	01	3	33
0xBA	00	0	0
0xBC	00	0	0
0xBE	00	0	0
0xC0	00	0	0
0xC2	00	0	0
0xC4[3]	01	1	1
0xC6[4]	03	3	3
Register Address	**CX25898/9 Register Values**	**CX25898/9 Register Values**	**CX25898/9 Register Values**
0xC8	1B	1B	1B
0xCA	C0	C0	C0
0xCC	C0	C0	C0
0xCE[5]	24	24	24
0xD0	00	0	0
0xD2	00	0	0

Table 22. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(5 of 5)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
0xD4	00	0	0
0xD6	00	0	0
0xD8	40	40	40

FOOTNOTE:
(1) This is a SECAM specific register.
(2) Register 0x6C contains the TIMING_RESET bit. Set this bit as your last programming step and the CX25898/9 will clear it automatically later.
(3) Register 0xC4 contains the EN_OUT bit. Adjust according to your design's interface as necessary.
(4) Register 0xC6 contains the EN_BLANKO, EN_DOT, and IN_MODE[2:0] bits. Adjust according to your design's interface as necessary.
(5) Register 0xCE contains the OUT_MUXD[1:0], OUTMUXC[1:0], OUTMUXB[1:0], and OUTMUXA[1:0] bit fields for output routing. Adjust according to your design's interface as necessary.

The procedure required to obtain a SECAM output with an overscan compensation percentage that differs from those solutions in Table 22 is fairly simple. First, configure the encoder so it generates a standard PAL-B, D, G, H, I output with the desired overscan compensation percentage. This can be done through the use of a PAL-B, D, G, H, I autoconfiguration mode, a hand-generated, or a predefined register set. Second, perform a full register read-back from the CX25898/9. Carefully note the value for register 0xA2. Third, program the bits found in Table 23 to their new state within the CX25898/9.

Table 23. Vital SECAM Bit Settings–Register 0xA2

Bit Name	Location	State for PAL-BDGHI	State for SECAM
FM	Bit 7 of register 0xA2	0	1
PAL_MD	Bit 5 of register 0xA2	1	0
VSYNC_DUR	Bit 3 of register 0xA2	0	0

Finally, calculate the values, found in Table 24, for the MSC_DB[31:0], MCR[7:0], MCB[7:0], FILFSCONV[5:0], FIL4286INCR[7:0], and MSC[31:0] registers for the particular SECAM overscan solution. To accomplish this task, read back both values that comprise the HCLKO[11:0] register, convert it to decimal (base 10), and use it in the equations below. After solving each SECAM register equation, perform a conversion back to a hexadecimal number and program the appropriate registers with their new SECAM specific values. Refer to Table 24.

The equations for generation of a SECAM output based on a RGB input only are:

- MSC_DB[31:0] = int ((272 / H_CLKO[11:0]) * 2^{32} + 0.5)
- DR_LIMITP[10:0] = ((4.756 MHz/ Internal Pixel Clock Frequency)*2^13)
- DR_LIMITN[10:0] = ((3.9 MHz/ Internal Pixel Clock Frequency)*2^13)
- DB_LIMITP[10:0] = ((4.756 MHz/ Internal Pixel Clock Frequency)*2^13)

- DB_LIMITN[10:0] = ((3.9 MHz/ Internal Pixel Clock Frequency)*2^13)
  - If PLL_CLK32 is 0, then Internal Pixel Clock Frequency = CLKI = CLKO.
  - If PLL_CLK32 is 1(for some overscan ratios in 800x600 and all 1024x768 resolutions), then Internal Pixel Clock Frequency = (2/3) * CLKI
- FIL4286INCR[7:0]: Six equations required to find hex value
  - SCINCR_OFF = int(8192 * 4.286 * 1728 / (27 * H_CLKO[11:0]) + 0.5)
  - SCINCR_OFFh = dec2hex(SCINCR_OFF)
  - SCINCR_OFFb = hex2bin(SCINCR_OFFh)
  - SCINCR_INTb = SCINCR_OFFb and (bitwise AND operator) with 111111111(binary)
  - SCINCR_INTnot = NOT[SCINCR_INTb]
  - FIL4286INCR[7:0] = [BIN2DEC{SCINCR_INTnot}]/2
- FILFSCONV[5:0] = int((27 * H_CLKO[11:0] * 1.087) / 1728 + 0.5)

For RGB input only:

- MCR[7:0] = int ((920.26) / (288036.0 * H_CLKO[11:0] * SINX) * 2^{26} + 0.5)

where SINX = [sin (2π * Fsc / CLKI)] / (2π * Fsc / CLKI)

- MCB[7:0] = int ((598.15) / (288036.0 * H_CLKO[11:0] * SINX) * 2^{26} + 0.5)

where SINX = [sin (2π * Fsc / CLKI)] / (2π * Fsc / CLKI)

- MSC[31:0] = int ((282 / H_CLKO[11:0]) * 2^{32} + 0.5)
- MY = same as PAL, no change required for SECAM

For YCrCb input only:

- MCR[7:0] =
  int (1.902/(224*0.713)*(0.28/F_{CLK})/(84*SINX)*2^{27}+0.5)
- MCB[7:0] =
  int (1.505/(224*0.564)*(0.28/F_{CLK})/(84*SINX)*2^{27}+0.5)
- MY = same as PAL, no change required for SECAM

Table 24. SECAM Specific Registers within the Conexant VGA Encoder

Register Address	Description	Value for PAL-BDGHI	Value for SECAM
0x42	MSC_DB[7:0]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x44	MSC_DB[15:8]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x46	MSC_DB[23:16]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x48	MSC_DB[31:24]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x4A	DR_LIMITP[7:0]	Not Used for PAL-BDGHI	Use DR_LIMITP[10:0] equation
0x4C	DR_LIMITN[7:0]	Not Used for PAL-BDGHI	Use DR_LIMITN[10:0] equation
0x4E	DR_LIMITN[10:8] and DR_LIMITP[10:8]	Not Used for PAL-BDGHI	Use DR_LIMITN[10:0] equation Use DR_LIMITP[10:0] equation
0x50	DB_LIMITP[7:0]	Not Used for PAL-BDGHI	Use DB_LIMITP[10:0] equation
0x52	DB_LIMITN[7:0]	Not Used for PAL-BDGHI	Use DB_LIMITN[10:0] equation
0x54	DB_LIMITN[10:8] and DB_LIMITP[10:8]	Not Used for PAL-BDGHI	Use DB_LIMITN[10:0] equation Use DB_LIMITP[10:0] equation
0x56	FIL4286INCR[7:0]	Not Used for PAL-BDGHI	Use FIL4286INCR[7:0] equation
0x58	Bits 5–0 are FILFSCONV[5:0]	Not Used for PAL-BDGHI	Use FILFSCONV[5:0] equation
0xA8	MCR[7:0]	Overscan Ratio Dependent	Use MCR[7:0] equation
0xAA	MCB[7:0]	Overscan Ratio Dependent	Use MCB[7:0] equation
0xAE	MSC[7:0]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB0	MSC[15:8]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB2	MSC[23:16]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB4	MSC[31:24]	Overscan Ratio Dependent	Use MSC[31:0] equation

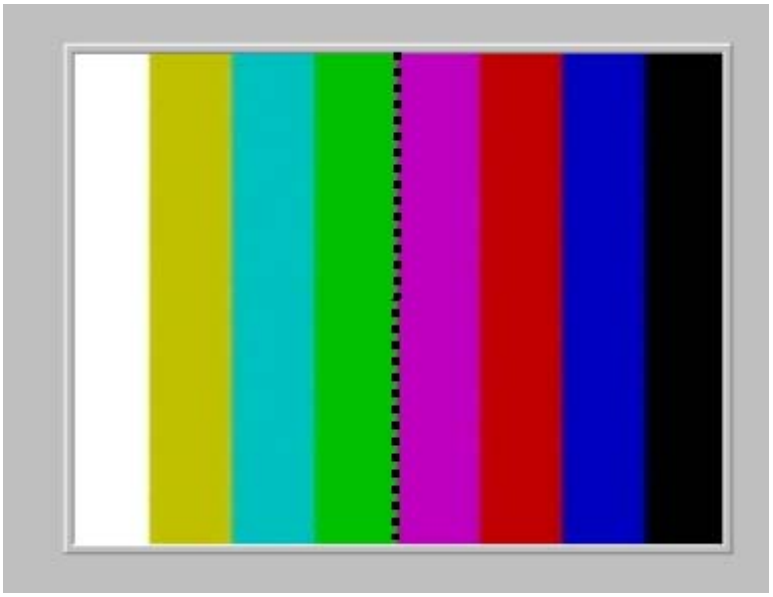
1.4.41 Elimination of Dot Crawl in Composite NTSC Output

One of the possible types of analog video outputs the CX25898/9 can generate is composite (abbreviated CVBS) video. With this sort of output, all video data is carried in a single signal that combines chrominance (hue and saturation) and luminance (brightness) information. Generally, this signal is transferred between video devices using a single interconnect cable with an RCA connector on both ends.

Composite video differs versus S-Video, which separates the color and brightness information into two separate signals. S-Video (also known as Y/C-Video) transfers chrominance (color portion of video signal denoted C) and luminance (brightness portion of the video signal denoted Y) information separately resulting in a higher picture quality than Composite video. Since Composite video joins the chrominance and luminance signals together into one unified signal, the two components must be divided out from each other at the television by a comb filter or other method. This process naturally results in some distortion and picture degradation and exhibits the worst image quality as compared to other forms of video connection.

One of the most common distortion artifacts seen with Composite video is an annoyance called dot crawl. Another name for this is vertical zipper. Due to the nature of the color subcarrier-switching pattern found in NTSC, dot crawl only occurs when the CX25898/9 is generating NTSC-M or NTSC-J Composite and not PAL, SECAM, or any other analog interlaced video standard. Because it is somewhat content dependent, dot crawl is sometimes difficult to see. This artifact is most noticeable when the video image contains a sharp color separation in adjacent vertical lines or pixels. For instance, in standard 75-percent or 100-percent color bars, there is a region of that test image from left to the right where the green bar ends and the magenta bar begins. This is shown in Figure 52 along with an example of the dot crawl artifact.

Figure 52. NTSC Composite Output: Standard 75 Percent Color Bars With Dot Crawl Artifact



Green-to-magenta is a difficult region to encode because these colors have almost completely opposite hues (green's chrominance phase is 240°, whereas magenta's is 61°). Hence, when the drastic phase shift transition occurs, a line of continuously moving dots rolling vertically through the transition region can be

seen. There are a number of circuit-based fixes that can be implemented to marginally improve this artifact, such as improving the chrominance/luminance filtering in the TV and refining the low-pass filters used for each of the CX25898/9's analog signal output lines.

Ultimately though, the best solution for minimizing dot crawl is to create a checkbox on the TV out page, and embed the source code for the Frozen Dots' algorithm behind it that allows the end-user the ability to turn NTSC Composite dot crawl on or off. Sample source code for freezing and eliminating the dot crawl is listed in Table 25.

Table 25. Source Code for Elimination of Dot Crawl in NTSC Composite Video *(1 of 3)*

```
//   Assumptions:
//
//        - We only freeze dots when using NTSC CVBS out
//        - TTO and ATO are same for 525-line and 625-line modes
//        - NTSC is always 525-line
//        - 2^32 == 0x100000000 hex
//        - 2^31 ==  0x80000000 hex
//        - TTO - 'Total Time per Output Line' = 63.55556E-6 (.00006355556 sec.) for
       NTSC
//        - ATO - 'Active Time per Output Line' = 52.65556E-6 (.00005265556 sec.) for
       NTSC
//        - HOC = Horiz. Overscan Compensation = 13.79 / 100 (.1378530858) (or some
       other input)
//                     2^32 x (1 - HOC) x ATO x (455 + 1/525)
//              MSC = ----- + .5
//                                (4 x H_ACTIVE x TTO)


//    Determining the MSC expression:
//
// DWORD  dwMSC = (348948560744.3 / H_ACTIVE) + .5;
//             = ( ( pow(2,32) * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 4 * H_ACTIVE
       * TTO ) ) + 0.5;
//                reduce
//             = ( ( pow(2,31) * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 2 * H_ACTIVE
       * TTO ) ) + 0.5;
//                re-express equation
//            = ( ( 0x80000000 * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 2 * H_ACTIVE
       * TTO ) ) + 0.5;
//                substitute
//              = ( ( 0x80000000 * ( 1 - HOC ) * .00005265556 * ( 455.0 + 1/525 ) ) /
       ( H_ACTIVE * .00012711112 ) ) + 0.5;
```

***Table 25. Source Code for Elimination of Dot Crawl in NTSC Composite Video** (2 of 3)*

```
//   Assumptions:
//                reduce
//             = ( ( 0x80000000 * ( 1 - HOC ) * .00005265556 * 455.001919 ) / (
      H_ACTIVE * .00012711112 ) ) + 0.5;
//                substitute
//            = ( ( 0x80000000 * ( 1 - .1378530858 ) * .00005265556 * 455.001919 ) /
      ( H_ACTIVE * .00012711112 ) ) + 0.5;
//                reduce
//             = ( ( 2147483648 * .8621469142 * .00005265556 * 455.001919 ) / (
      H_ACTIVE * .00012711112 ) ) + 0.5;
//                reduce
//             = ( 44357657.97721 / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//                lose the rounding-up
//             = 44357657.97721 / ( H_ACTIVE * .00012711112 );
//                reduce
//             = 348967564578.2 / H_ACTIVE;
//                lose the insignificant decimal point.
//                the only problem is that the number on top is greater than 32 bits.
//              so, we either have to use large integers, floats, or expand/simplify
//                the expression.
//             = 348967564578 / H_ACTIVE;
//                expand
//             = ( 348967564578 / 128 ) / ( H_ACTIVE / 128 );
//                reduce and re-express.  we're done.
//             = 0xA2802CEA / ( H_ACTIVE / 128 );
//                or, reduce and re-express with a GCD of 640 and 800.
//                expand
//             = ( 348967564578 / 160 ) / ( H_ACTIVE / 160 );
//                reduce and re-express.  we're done.
//             = 0x820023EE / ( H_ACTIVE / 160 );

//   Frozen dots only works with NTSC Composite
if( bNTSC )
{
     //   To get frozen dots, calculate MSC with increment.
DWORD       dwMSC = 0x820023EE / ( H_ACTIVE / 160 );
regAE.ucMSC = dwMSC & 0x000000FF;
```

Table 25. Source Code for Elimination of Dot Crawl in NTSC Composite Video *(3 of 3)*

```
//   Assumptions:
regB0.ucMSC = ( dwMSC & 0x0000FF00) >> 8;
regB2.ucMSC = (dwMSC & 0x00FF0000) >> 16;
regB4.ucMSC = (dwMSC & 0xFF000000) >> 24;
}
```

GENERAL NOTE:

1. Frozen Dots only functions with an NTSC Composite video output and either a 640X480 or 800X600 digital input coming from the graphics controller. Modifications required to above source code to enable frozen dots with a 1024x768 active digital input coming from the graphics controller.
2. For optimal visual quality of the NTSC CVBS image, Frozen Dots should be disabled during multimedia applications such as playing a game or watching a DVD Movie. Frozen Dots should be enabled during nonmultimedia applications such as e-mailing, word processing, presentations, and other scenarios where menus and small graphics will be frequently displayed.
3. H_ACTIVE is the number of digital pixels per horizontal input line. Make sure a case statement or some other line of code is included for turning on this feature when the user's desired video output is NTSC (NTSC-M video standard is used in USA, NTSC-J in Japan, most of Southeast Asia, etc.) and turning the feature off when the user's desired video output is PAL (different variations used in Western and Central Europe, South America, etc.).
4. The only marked improvement between this set of equations and the set that was embedded in older versions of Cockpit is that Conexant was able to further solve for the MSC[31:0] value, successfully deriving an equation which will stay within 32 bits. It works fine for 640x480, and 800x600 because 160 divides both 640 and 800 evenly.

Manual adjustment of register 0xB6 = PHASE_OFF in the CX25898/9 and/or manual adjustment of register 0xAE = MSC[7:0] can also have the same type of special effects as the algorithm in Table 25. By increasing or decreasing these values slowly, the subcarrier phase and subcarrier increment will change, and with certain register combinations, the crawling dots will appear at certain points to stand still.

1.4.42 Macrovision Copy Protection

The CX25899 device supports Version 7.1.L1 of the Macrovision specification for copy protection for all NTSC, PAL, and SECAM video outputs. The CX25898 does not support the Macrovision feature.

NOTE: The CX25899 will power-up with Macrovision copy protection enabled as required by Macrovision Version 7.1.L1.

The CX25899 device also provides Macrovision 525p (480p) copy protection for progressive scan outputs. Another term for this technology is the DVD 1.03 Macrovision copy protection scheme. This type of HDTV copy protection turns on automatically after a power-on reset and after the CX25899 begins transmitting 480p YP_RP_B. The designer only needs to program HDTV copy protection specific registers if Macrovision was off previously.

For detailed instructions and lists of default register values for the CX25898 obtain a Macrovision license and then ask for the *Macrovision Process Supplement Application Note* from your local Conexant salesperson or field application engineer.

1.4.43 HDTV Output Mode

The CX25898/9 includes an HDTV Output Mode that generates the analog RGB or analog YP_BP_R component video outputs necessary for driving a Japan D-type or generic HD input port. To drive the Japan D connector with required 0 V, 2.2 V, and 5 V signal lines to express the type of format and whether the timing is progressive or interlaced requires the integration of an external device such as a PLD.

While generating HDTV outputs, the device accepts RGB, YCrCb, or YPrPb digital data in a 480p, 720p, or 1080i ATSC resolution.

In addition, the 576p (625p) resolution defined in the ITU-R BT.1358 standard and the 1035i resolution defined in the ITU-R BT.709-4 standard are supported. Finally, many custom HD resolutions such as 540p, used by RCA set-top boxes, are acceptable as well.

After a pipeline delay, it outputs either analog RGB or analog YP_BP_R signals and automatically inserts trilevel synchronization pulses (when necessary) and vertical synchronizing broad pulses.

1.4.44 SCART Output

In this mode of operation, the CX25898/9 can be used successfully to provide one full Red/Green/Blue/CSYNC (or optionally, a 2-signal Luminance and Chrominance) SCART/Peritel output to drive SCART-compatible televisions or VCRs. Many PAL/European TVs being manufactured now have SCART compatible sockets, that allows the television and the set top box, graphics card, or game console driving it to work in RGB color instead of the standard composite. The picture quality for full SCART is significantly better due to the individual RGB Composite signals being sent directly to the TV color guns. This is opposed to the TV having to modulate and decode the RGB signals from another color format. This ultimately yields a crisper picture.

On power-up, the CX25898/9 will output NTSC standard-definition television outputs. To switch the device into SCART Output Mode with three sync-less Red/Green/Blue (RGB) analog outputs and a single Composite Video output from pin #59, program the encoder into a satisfactory PAL output mode and then perform the serial writes listed in Table 26.

Table 26. Serial Writes Required to Switch CX25898/9 into SCART Output Operation

Bit Name	Location	Value	Comment
EN_SCART	Bit 3—Register 0x6C	1	Enables SCART Output mode. DACs will transmit Video[0-3] as SCART compatible RGB/CVBS outputs. By default, in SCART Output mode, the encoder will transmit: DACA = Video[0] = Red DACB = Video[1] = Green DACC = Video[2] = Blue DACD = Video[3] = Composite Video signal
OUT_MUXD[1:0] OUT_MUXC[1:0] OUT_MUXB[1:0] OUT_MUXA[1:0]	Bits 7:0—Register CE	E4	By configuring the DAC routing register, the encoder will now transmit: DACA = Video[0] = 00 = Red DACB = Video[1] = 01 = Green DACC = Video[2] = 10 = Blue DACD = Video[3] = 11 = Composite Video signal
OUT_MODE[1:0]	Bits 3:2—Register D6	11	Forces encoder to generate SCART (R/G/B/CVBS) output mode.

NOTE: No change to the incoming or outgoing HSYNC* and VSYNC* signal frequencies are necessary for SCART generation. The sync rates should continue to match those found with PAL-BDGHI transmission.

While the CX25898/9 is in SCART output mode, the composite sync output (Video[3]) contains a standard bilevel analog sync along with all other components that comprise a standard PAL-BDGHI video signal. The sync pulse has an amplitude of 0 mV to 300 mV peak-to-peak and a duration of 4.70 µs by default. The amplitude can only be adjusted through the use of external passives, but its width can be adjusted through serial writing of the CX25898/9 HSYNC_WIDTH register.

The CX25898/9's PAL Composite Signal should be used by the subsystem to provide the positive-going Video output/sync output expected by SCART-

compliant display devices. In other words, the Composite Sync output should be fed into the Video Input (Contact #20-CEI IEC 933-1) on the SCART connector. SCART_CSYNC will possess the same bandwidth and time delays as the CX25898/9 RGB primary color signals.

The RGB primary color signals generated in SCART mode will not contain any embedded syncs. For each output, the difference between the peak value (pure white) and blanking level is 0.7 V (± 3 dB). Therefore, the blanking level will reside at GND (0 mV) and the maximum level is 700 mV for RGB. The HSYNC* and VSYNC* digital inputs received by the CX25898/9 continue to act as a trigger to start a new line and new frame respectively as is the case with Composite and SVHS outputs. The RGB signals are blanked in accordance with the values contained in the H_BLANKO and V_BLANKO registers, with H_CLKO and H_ACTIVE playing a lesser role.

The primary color signals expect a 75 Ω load from the display device. Correct RGB amplitudes are generated when the CX25898/9's SCART outputs each see an equivalent impedance of 37.5 Ω between the source and destination.

By default, the RGB positive-going signals are transmitted from the CX25898/9 in the manner shown in Table 27.

Table 27. Default SCART Outgoing Signal Assignments

Pin # on CX25898/9	SCART Output
72 = DACA	Video[0] = Red Primary Color
73 = DACB	Video[1] = Green Primary Color
74 = DACC	Video[2] = Blue Primary Color
75 = DACD	Video[3] = Composite Video Signal
GENERAL NOTE: 1. Video[0–3] can be routed out of any of the 4 on-chip DACs by adjusting the appropriate OUT_MUXA/B/C/D[1:0] bits.	

Other major characteristics of the CX25898/9 SCART Output Mode are:

- DAC detection possible in this mode for R, G, and B outputs.
- Acceptable digital RGB inputs include 24/16/or 15 bits per pixel multiplexed, noninterlaced RGB.
- Acceptable digital YCrCb inputs include 24/16 bits per pixel multiplexed, noninterlaced YCrCb.
- CX25898/9 can operate in master, pseudo-master, or slave interface.
- Pixel sampling rate in this mode is determined based on the incoming and outgoing clock frequencies (CLKI and CLKO).
- DAC resolution for all DACs = 10-bits.
- Compliance with the European EN50-049 SCART connector standard. Blue should be received as Pin #7, Green as Pin #11, Red as Pin #15, and CVBS Out from the CX25898/9 as Composite Out at Pin #19 (Display Side of Connector).
- Compliance with the CEI IEC Publication 933-1 standard. Blue should be received as Pin #7, Green as Pin #11, Red as Pin #15, and CVBS Out from the CX25898/9 as Composite Out at Pin #19 (Display Side of Connector).

The CX25898/9 is compliant with the major standards and technical reports governing the SCART interface. Table 28 summarizes the pins to be used for transmission of SCART RGB/CVBS video with this Conexant device.

Table 28. CX25898/9 SCART Outputs for Different SCART Standards

RGB Standard	Red	Green	Blue	Composite/Blanking
European EN50-049 SCART(1) connector	Pin 15	Pin 11	Pin 7	Pin 19 —Composite Sync Out (To Display)
CEI IEC 933-1: (1) BBC SCART Arrangement #1	Pin 15	Pin 11	Pin 7	Pin 19—Composite Sync Out (To Display)
Y- C Standard	**Chroma**	**x**	**Luma**	**x**
Luminance - Chrominance(2) SCART: BBC SCART Arrangement #2	Pin 15	—	Pin 20	—

FOOTNOTE:

(1) Red/Green/Blue signals levels are from 0 V + 0.7 V peak-to-peak with 75 Ω load impedance.

(2) The Luminance-Chrominance Outputs for SCART are equivalent to PAL-BDGHI S-Video. Therefore, OUTMODE[1:0] should be programmed to 00, the EN_SCART bit should be reset to 0, and the OUTMUXA/B/C[1:0] bits adjusted according to which DACs must transmit Luminance(Video[1]) and Chrominance(Video[2]).

A specialized cable and connector are required to connect the CX25898/9's RGB/CSYNC or Y/C outputs to the TV's SCART input. This cable can be procured from various European electronic stores and comes in at least two different arrangements. Consult the CEI IEC 933-1 specification (*Audio, Video, and Audiovisual systems-Interconnections and Matching Values*) for a precise illustration of their 21-contact SCART connector, video signal peak-peak values, and cordset types.

The most common types of SCART connectors are the so-called Type I and Type II variety. Figures 53 and 54 illustrate the recommended Type I and Type II SCART connector pinout arrangements.

Figure 53. CX25898/9 Driving a Type I SCART Connector (EN 50-049 and IEC 933-1 Compliant)

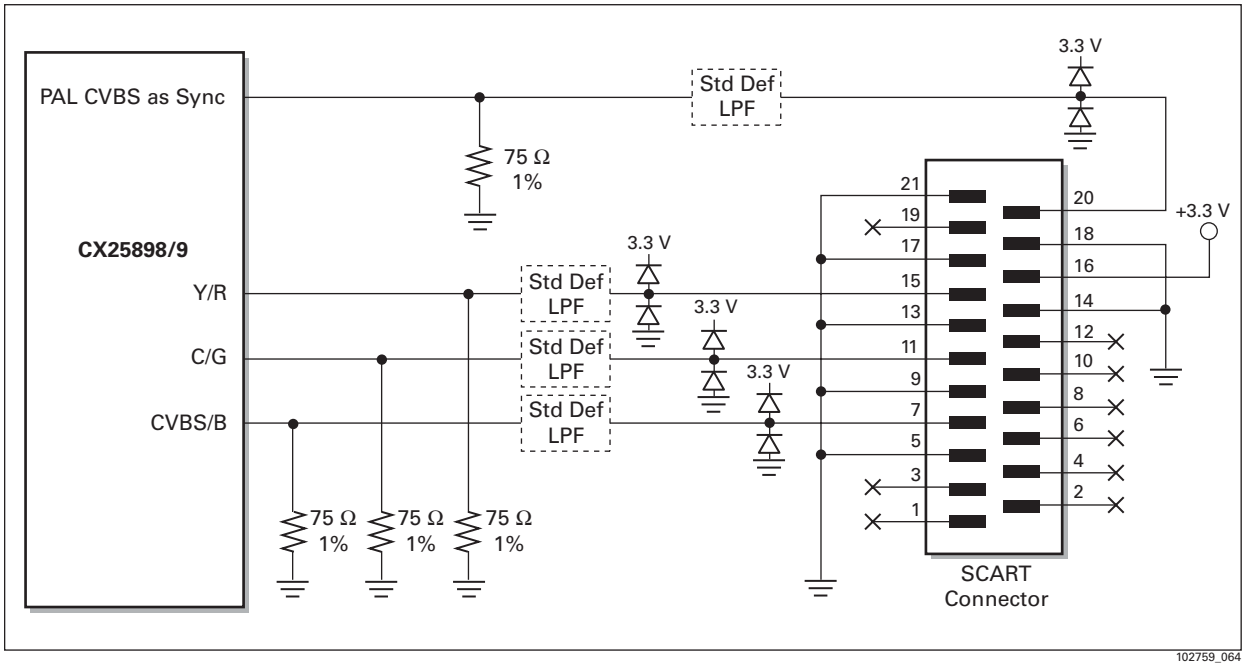
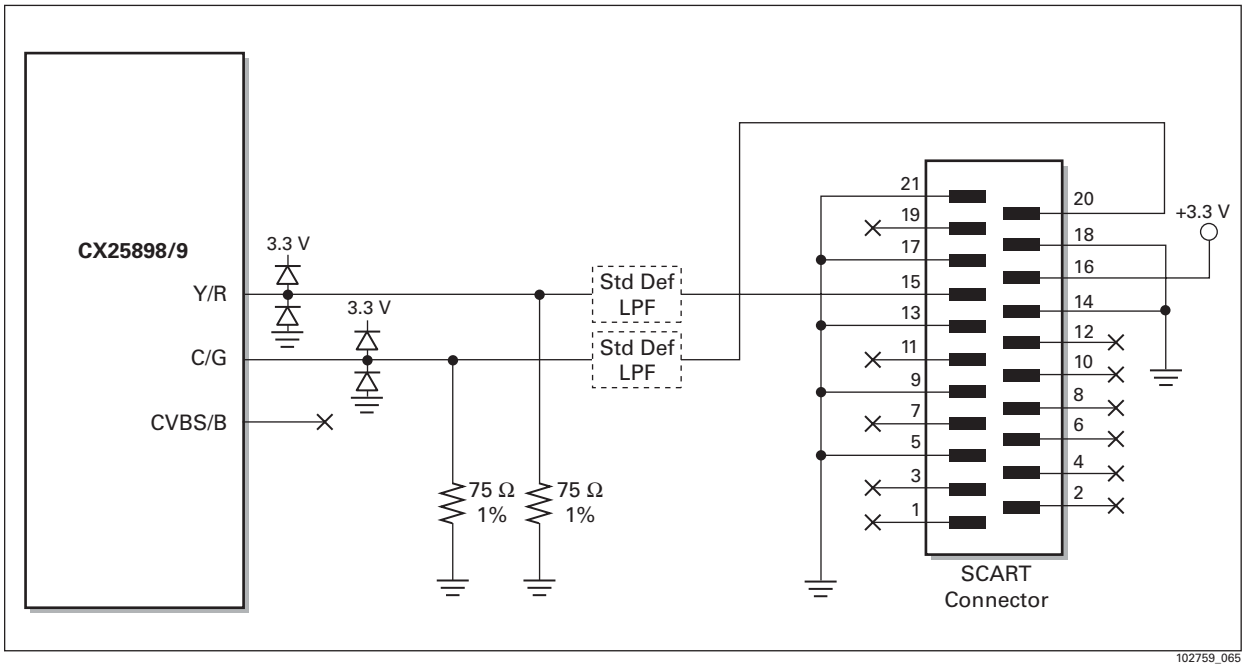


Figure 54. CX25898/9 Driving a Type II SCART Connector (Y/C and BBC SCART Compliant)



Conexant recommends that any designer utilizing the CX25898/9 with either type of SCART output utilize the same DAC low-pass filters used for standard-definition TV outputs.

1.4.45 Y CR CB 480i (YUV) Standard-Definition Component Video Outputs

In this mode of operation, the CX25898/9 provides a set of Component Video Y, CB (B–Y), CR (R–Y) outputs based on a 480 line interlaced RGB or YCrCb digital input format. Some DVD players, such as those made by Toshiba and Panasonic, call the Component Video Output format by their branded name, ColorStream. Others refer to the two EIA standards governing this video format–EIA-770.1 and EIA-770.2-A, and state this video type as Interlaced Component Video, 480i Component Video, or Component YUV. Regardless of the different names, the video format remains the same. For instructions on how to configure the CX25898/9, to generate progressive 480p Component Video (or Color Stream Pro), refer to the HDTV sections. The CX25898/9 and CX25870/1/2/3/4/5 are the only encoders that can supply HDTV outputs.

The designer can enable ColorStream by using three of the CX25898/9's DACs to generate two color difference signals (P_R and P_B sometimes referred to as C_R and C_B) and a single luminance signal (Y). These three channels allow the video generating device to bypass the TV's internal Y/C separator and color decoder circuits. The analog information therefore gets routed directly into the TV's matrix decoder. By sending the pure component video signal directly to a Component Video or ColorStream input-equipped television or video projector, the input signal forgoes the extra processing that normally would degrade the analog image.

The advantage of this type of video is increased image quality combined with more lifelike colors and crisper detail. Because the video information is transferred over three separate connecting cables instead of two (for S-Video) or one (for Coaxial or RCA/Composite), 480i Component Video yields the best standard-definition TV quality available. However, because we are still dealing with standard 480 line interlaced resolutions, this format remains inferior to High-Definition TV.

Output devices that require generation of this format include, but are not limited to, Digital TV set top boxes, Satellite DBS Receiver Decoders, and DVD players. Input media capable of decoding ColorStream include television receivers and/or professional monitors.

While in the Component Video mode, all 10 bits of the CX25898/9's D/A converters are available for encoding. This results in a D/A conversion more accurate than conventional 8-or 9-bit based MHz systems. The end result is a more artifact-free and clear image.

Some major characteristics governing the interlaced standard-definition television analog component video interface are as follows:

Pixels per Active Line	Active Lines per Frame	Frame Rate (Hz)	Output Scanning Format	Total Samples per Line	Total Lines per Frame
720	480	30 / 1.001	Interlaced	858	525

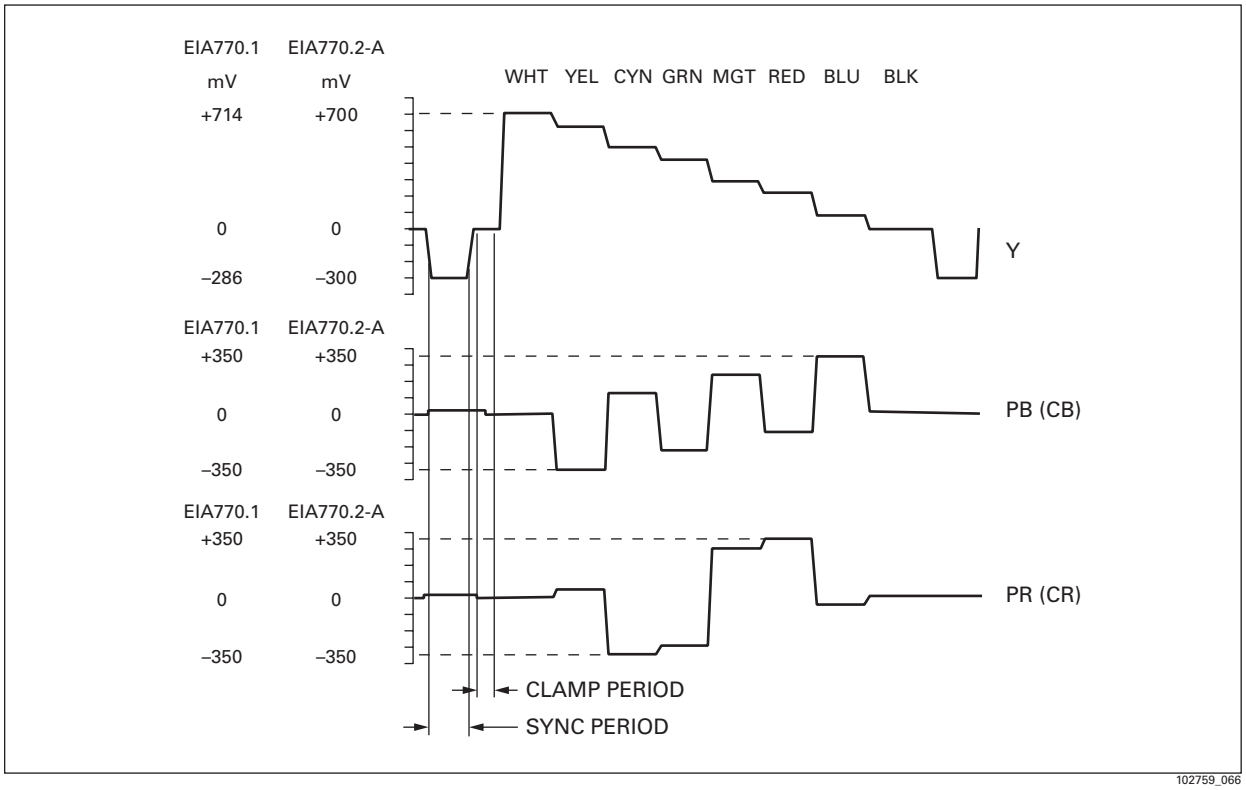
- The digital input stream can be received in a progressive (i.e., noninterlaced) format or interlaced format. Interlaced data must be transmitted as ODD–EVEN–ODD … fields. The fields carry every other scan line in succession with succeeding fields carrying the lines not scanned by the previous field.
- Each field will be divided into an active picture area and a VBI. Similarly, each line will be divided into an active pixel area and a horizontal blanking interval.
- The 480i video output will be capable of either a 4:3 or 16:9 aspect ratio through embedding of Wide Screen Signaling (WSS) bits into the appropriate lines in the VBI. Review the WSS and CGMS sections for more details.

If configured properly, the CX25898/9's EIA 770.2-A compliant Component Video luminance signal has a peak amplitude of 700 mV from the blanking level, with zero setup. A negative-going bilevel sync pulse of 300 mV, conforming to the timing requirements in Figure 55, is added to the Luma signal as the only timing reference for the complete Y P_R P_B (YC_RC_B) set of signals.

Neither P_R (C_R) nor P_B (C_B) will contain an embedded sync pulse. Both will have a maximum peak amplitude of ±350 mV. The DC level of P_R and P_B during the horizontal line shown in Figure 55 will be at reference black with a voltage of 0 V. It will be generated in conformance with the EIA 770.2-A and EIA770.1 standards. The only differences between these standards are the presence of the 7.5 IRE setup pedestal and slightly different luminance levels. Check Tables 29 and 30 for complete programming instructions for either standard.

The three component video signals Y, P_B (C_B), and P_R (C_R)will be coincident with respect to each other within ± 5.0 ns. Any filtering that introduces group delay exceeding 5.0 ns should be discarded and redesigned.

Figure 55. Y P_R P_B Component Video Signals using 100/0/100/0 Color Bars as the Digital Input Signal (Courtesy– EIA-770.2-A standard, page 8 and EIA-770.1 standard)



To switch the device into 480i Component Video Output Mode with bilevel syncs embedded into each of the three Y P_R P_B analog outputs, first, program up the CX25898/9 into a fully functional NTSC over-scan solution where Composite and/or S-Video is being generated out of at least three of the encoder's outputs. Next, change the registers listed in Table 29 to the indicated values.

Table 29. Common Registers Required to Switch CX25898/9 into EIA-770.2-A- or EIA-770.1-Compliant Component Video Outputs

Register/Bit Name	Location	Value	Comment
MCOMPY[7:0]	Bits 7:0—Register 3C	80 (hex)	Gain multiplication factor for Y analog output.
MCOMPU[7:0]	Bits 7:0—Register 3E	90 (hex)	Gain multiplication factor for P_B (C_B) analog output.
MCOMPV[7:0]	Bits 7:0—Register 40	66 (hex)	Gain multiplication factor for P_R (C_R) analog output.
SETUP	Bit 1—Register A2	1 (binary)	Required for EIA770.1 compliance. Enables 7.5 IRE pedestal normally present within NTSC-M active video lines.
OUT_MODE[1:0]	Bits 3:2—Register D6	10 (binary)	Enables Component Video output mode. CX25898/9 DACs will transmit Video[0-3] as EIA-770.2-A or 770.1 compliant Y PR (C_R), PB (C_B), and Y_DELAY outputs
OUT_MUXA[1:0] OUT_MUXB[1:0] OUT_MUXC[1:0] OUT_MUXD[1:0]	Bits 1:0—Register CE Bits 3:2—Register CE Bits 5:4—Register CE Bits 7:6—Register CE	00 (binary) 01 (binary) 10 (binary) 11 (binary)	By default, in Component Video output mode, the CX25898/9 will transmit: DACA = Video[0] = PR (C_R) = V DACB = Video[1] = Y DACC = Video[2] = PB (C_B)= U DACD = Video[3] = Y_DELAY (not used with this type of output)

For EIA-770.1 compliant Component Video out, no other programming steps are required for the CX25898/9 beyond Table 29.

For the more common EIA-770.2-A compliant Component Video out, a few additional programming steps are required. These are listed in Table 30.

Table 30. Unique Registers Required to Switch CX25898/9 into EIA-770.2-A- Compliant Component Video Outputs

Register/Bit Name	Location	Value	Comment
SETUP	Bit 1—Register A2	0 (binary)	Required for EIA770.2-A compliance. Removes 7.5 IRE pedestal normally present within NTSC-M active video lines.
SYNC_AMP[7:0]	Bits 7:0—Register A4	F0 (hex)	Multiplication factor for adjusting the analog sync amplitude tip to –300 mV for EIA-770.2-A.
MY[7:0]	Bits 7:0—Register AC	85 (hex)	Additional gain multiplication factor for Y EIA-770.2-A analog output. This register needs to be increased by 6 percent of its nominal value. For a NTSC output based on a RGB digital input, this register would be increased 6 percent to 8C (hex) from a nominal value of 85 (hex).

The analog Y, PB (C_B), and PR (C_R)- Video[0-3] outputs can be routed out of any of the four on-chip DACs by adjusting the appropriate OUT_MUXA/B/C/D[1:0] bits. All of the OUT_MUX bits are contained in register 0xCE.

Because the CX25898/9 device has four DACs and only three are needed for Component Video, the designer can choose to use the fourth output, usually

from DACD, for any purpose deemed necessary. This output can be configured to either the Y P_R (C_R), P_B (C_B), or Y_DELAY output via OUT_MUXD. If the output is not going to be used whatsoever, Conexant recommends DAC_D be disabled by setting DACDISD (bit 3, Register BA). This saves on power dissipation.

The Component Video output signals expect a 75 Ω load to ground from the display medium. Correct Y, P_R, P_B amplitudes will be generated only when each CX25898/9 output sees an equivalent impedance of 37.5 Ω between the source and destination.

The CX25898/9 is compliant with the major standards and technical reports governing the Standard-Definition TV Analog Component Video interface. The name of these standards are as follows:

- EIA 770.2-A–Standard-Definition TV Analog Component Video Interface
- EIA 770.1–Standard-Definition TV Analog Component Video Interface
- ANSI/SMPTE Standard 170M (1994) (M/NTSC) for Television–Composite Analog Video Signal–NTSC for Studio Applications

To obtain any of these specifications, visit Global Engineering Documents at:

http://global.ihs.com/

Conexant recommends that any designer utilizing the CX25898/9 with a Component Video output utilize the same DAC low-pass filters used for standard-definition TV outputs.

1.4.46 VGA(RGB)—DAC Output Operation

In this mode of operation, the CX25898/9 acts as a general-purpose triple high-speed D/A converter used to drive video receivers, such as PC monitors. The encoder accomplishes this by bypassing most of the encoder blocks utilized for television outputs, such as the Flicker Filter and FIFO and instead routing the RGB or YCrCb digital data straight through to the on-chip 10-bit DACs. Once the data arrives at the DACs, it is quickly converted to a set of 700 mV peak-to-peak analog outputs, streamed through the respective DAC_X output pins, and routed within the rest of the graphics system according to the PCB layout.

Optimal performance is achieved when the CX25898/9's current controlled DACs are terminated into appropriate resistive loads to produce voltage outputs. The chip's DAC outputs are specifically designed to produce video output levels with a total peak-peak active-region amplitude of 700 mV when directly connected to a single-ended, doubly terminated (Req = 37.5 Ω) load. With the recommended loading of two 75 Ω ± 1 percent resistors (one each for the transmitting and receiving side), the full-scale video amplitude is from 286 mV (blanking) to 986 mV (maximum luminance) and synchronization pulses from 0 mV (negative sync tip) to 286 mV (blanking) respectively. The analog synchronization pulse is generated by the CX25898/9 every time it receives a falling edge on either the HSYNC* or the VSYNC* input by default. These sync pulses can be disabled for the RGB outputs by performing the serial writes listed in Table 31.

On power-up, the CX25898/9 will output NTSC standard-definition television outputs. To switch the device into VGA-DAC Output Mode with bilevel syncs embedded on every Red/Green/Blue (RGB) analog output, perform the serial writes listed in Table 32 only.

Table 31. Serial Writes Required to Remove Bilevel Syncs from all VGA/DAC Outputs

Bit Name	Location	Value	Comment
RGB2PRPB	Bit 6—Register 0x2E	0	Default state. No need to reprogram.
BPB_SYNC_DIS	Bit 3—Register 0x2E	1	Disables sync on Blue output
GY_SYNC_DIS	Bit 4—Register 0x2E	1	Disables sync on Green output
RPR_SYNC_DIS	Bit 5—Register 0x2E	1	Disables sync on Red output
GENERAL NOTE: 1. When all bits in Tables 31 and 46 are programmed correctly, the active video level range will be from +286 mV to +986 mV.			

Table 32. Serial Writes Required to Switch CX25898/9 into VGA/DAC Output Operation

Bit Name	Location	Value	Comment
SLAVE	Bit 5—Register 0xBA	1	Ensures CX25898/9 in slave or pseudo-master interface

Table 32. Serial Writes Required to Switch CX25898/9 into VGA/DAC Output Operation

Bit Name	Location	Value	Comment
EN_XCLK	Bit 7—Register 0xA0	1	CLKI used as pixel clock source.
SETUP	Bit 1—Register 0xA2	0	Setup off. The +56 mV pedestal setup is disabled for active video lines.
OUT_MODE[1:0]	Bits 3:2—Register D6	11	Video[0-3] = 11 = VGA Output Mode: DAC_A = Video[0] = Red DAC_B = Video[1] = Green DAC_C = Video[2] = Blue
DAC_DISD	Bit 3—Register 0xBA	1	Disables DACD output. Current is set to 0 mA. Output voltage goes to 0 V.

Of course, the master device's timing signals (HSYNC*, VSYNC*, CLKI) and the digital data sent to the CX25898/9 must also be adjusted to ensure the proper operation of this mode.

Some applications, such as VESA compliant PC Monitors, dictate that the embedded bilevel syncs be completely absent from the RGB analog outputs. Fortunately, the CX25898/9 can provide VESA's syncless outputs as long as the additional set of bits found in Table 31 are programmed as shown in this table. Complete all serial writes listed in Tables 31 and 32.

The outputs generated from the serial writes listed in Table 31 and Table 32 will not contain any embedded syncs, nor will they contain the positive DC offset voltage present with the CX25898/9 in VGA out mode. Therefore, the blanking level will reside at 0 mV, and the maximum luminance level is 700 mV for the three different outputs. The HSYNC* and VSYNC* digital inputs received by the CX25898/9 will continue to cause blanking, but this is irrelevant since the data itself is blanked at these times.

The VESA Video Signal Standard specification requires that the DAC analog output stay between 0.0 Vdc and 0.700 Vdc +.07 V (or –.03 V) with no excursions at all times. Clearly, the blank and maximum luminance levels for the CX25898/9 are in compliance with this specification.

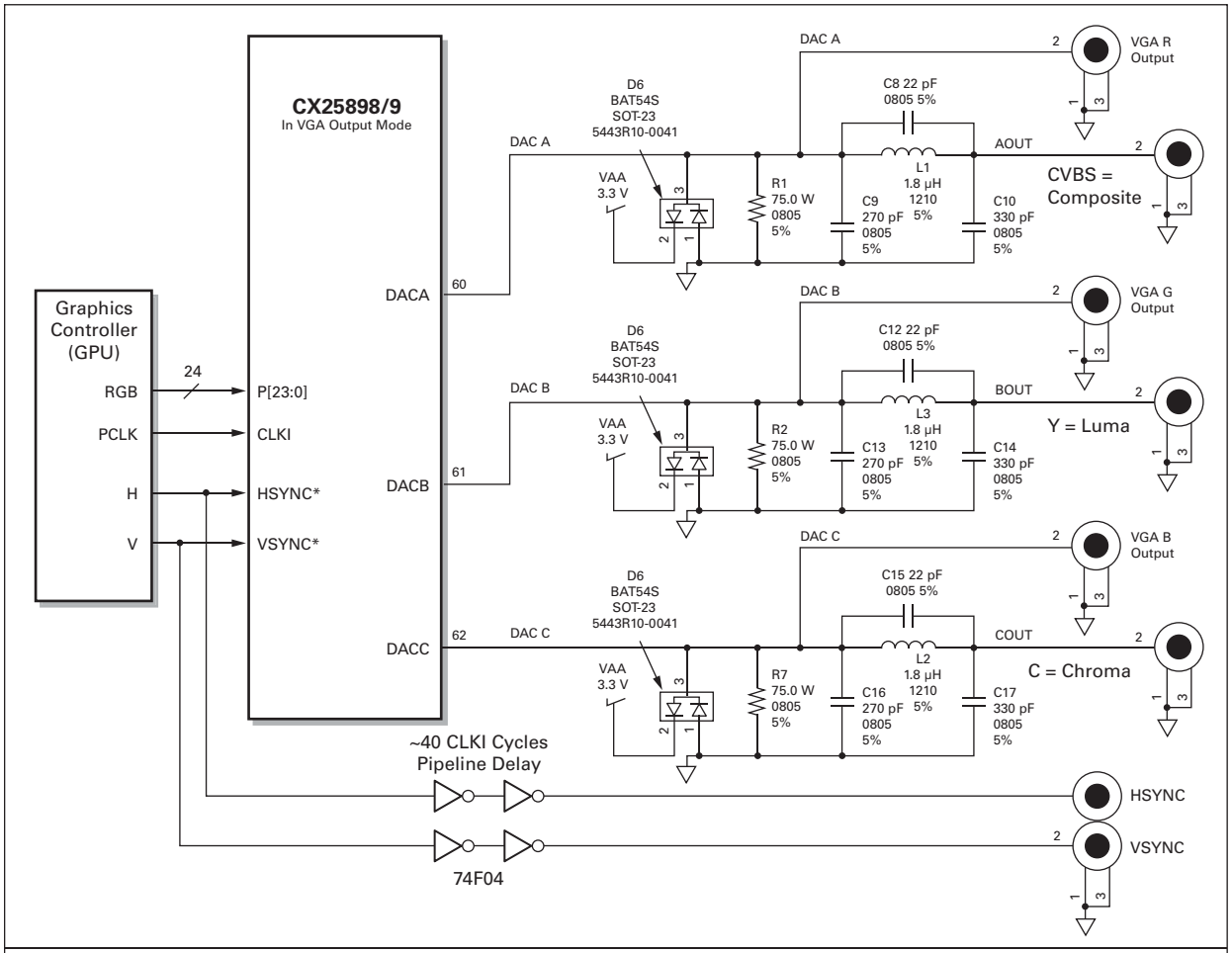
Other major characteristics of the CX25898/9 VGA—DAC Output Mode are:

- Maximum active input resolution = 1024 x 768 or any other active resolution that ensures less than an 80 MHz pixel clock rate
- Acceptable digital RGB inputs include 24/16/ or 15 bits per pixel multiplexed RGB
- Acceptable digital YCrCb inputs include 24/16 bits per pixel multiplexed YCrCb
- CX25898/9 can only be a slave to the data master in this type of operation
- Sampling rate in this mode is determined based on the incoming clock frequency (CLKI)
- DAC resolution for all DACs = 10-bits

Conexant recommends that any designer utilizing the CX25898/9 in this mode circumvent the three capacitors and one inductor found in the DAC low-pass filters used for standard-definition TV outputs. Figure 56 illustrates one method of bypassing the capacitors and inductor. Note that an additional RCA (or other type) of connector is recommended in this case for the Red. Green, and Blue VGA Outputs.

Finally, since the encoder cannot transmit analog HSYNC and VSYNC signals directly to the VGA monitor, digital sync signals must be taken from the GPU, buffered (e.g., with a pair of 74F04 inverters) and level-shifted. An additional delay of approximately 40 input pixel clocks must also be imparted on both HSYNC and VSYNC as well to compensate for the pipeline delay of R/G/B through the encoder. Figure 56 shows this concept. In VGA modes where embedded syncs in the R/G/B outputs are used, the buffers are not necessary.

Figure 56. Filterless DAC Outputs for VGA (RGB) DAC Output with Sync Buffers



GENERAL NOTE:

1. Make sure to have only one of the paired outputs plugged in simultaneously.
2. The VGA R/G/B HSYNC*/VSYNC* outputs can drive either a standard DB15 female connector or 5 separate male BNC connectors.
3. The 74F04 buffers help isolate any noise generated from the monitor, including reflections from coupling.

102759_067

1.4.47 TV DAC Detection Procedures

This encoder can determine whether or not the DAC output is connected to a monitor by verifying that the output is doubly-terminated in VGA, NTSC/PAL/SECAM, SCART, Component Video (YCRCB), or HDTV out modes. The MONSTATx bit for the corresponding DAC is set to 1 if both of the following conditions occur: the device senses a double-terminated load and the CHECK_STAT register bit is set. While CHECK_STAT is set, the output is forced to 2/3 of VREF when terminated and 4/3 of VREF if unterminated. The MONSTATx bit reflects the condition when the DAC output is less than or equal to VREF. The CHECK_STAT bit is automatically cleared after ten clock cycles.

The status of each of the three CX25898/9's DACs can be checked at any time using two different methods. The first method is called Standard serial read-back. To perform a check of each MONSTATx bit and in turn, gather correct information about the connection status of each D-A converter, and follow the Standard DAC detection algorithm procedure in Table 33.

Table 33. Standard DAC Detection Algorithm for the CX25898/9

1. Set the SRESET bit of the 0xBA register to 1. This usually means register 0xBA will need to be written with 80 hex (for master interface) or A0hex for (for pseudo-master or slave interface). This will force the encoder into its default configuration mode 640x480 RGB in NTSC out video off.
2. Set both the EN_REG_RD and EACTIVE bits to 1. This usually means register 0x6C will need to be written with 44 hex (for all video output modes except SCART). The state of the EACTIVE bit will not impact DAC detection results.
3. Set the CHECK_STAT bit of register 0xBA to 1. This usually means register 0xBA will need to be written with 40 hex (for CX25898/9 in master interface) or 60 hex (for pseudo-master or slave interface).
4. Read register 0x06, which contains the MONSTAT_A, MONSTAT_B, MONSTAT_C, and MONSTAT_D bits in the upper nibble. Bit 7 (MSb) of register 0x06 contains the monitor detection status for DAC_A (MONSTAT_A) while bit 4 contains the monitor detection status for SCART_CSYNC (MONSTAT_D).
5. Check to see if any of the MONSTAT_x bits are 1. If any true result is obtained, at least one television has been detected and therefore connected to the CX25898/9.
6. If all MONSTAT_x bits are 0, repeat step 4 and step 5 again. Read register 0x06 and check the MONSTAT_x bits again. After the 64th iteration, if none of the MONSTAT_x bits are 1, a TV is not connected. Algorithm ends with a null result.

NOTE: If the SRESET, EN_REG_RD, and EACTIVE bits were set previously prior to the start of this TV detection algorithm, there is no need to set these again. Bypass steps 1 and 2, and begin the routine at step 3.

NOTE: Monitor status detection cannot be performed on a disabled DAC (DACOFF = 1 or DACDISx = 1)

Sample C code for the Standard TV Detection Algorithm is listed below for assistance. Sixteen different permutations of the upper nibble of register 0x06 are possible. Each of these results signifies different MONSTAT_x and therefore DAC connection schemes.

```
BOOLEAN IsTvConnected()
{
Register* reg;

reg = OurTvEncoder->GetRegister(0xba);
reg->Write(0x80); // SRESET is set to one

reg = OurTvEncoder->GetRegister(0x6c);
reg->Write(0x44); // EN_REG_RD = 1 and EACTIVE = 1

BYTE val;
reg = OurTvEncoder->GetRegister(0xba);
val = reg->Read();
val |= 0x40; // CHECK_STAT is set to one

BYTE status;
BYTE count = 64;  // if TV connected to any DAC, loop usually
requires no more than 25 iterations
// before returning TRUE
reg = OurTvEncoder->GetRegister(0x06);
do {
status = reg->Read();
} while( ((status & 0xF0) == 0) && (--count > 0) );

if( count > 0 )
return TRUE; // tv is connected

return FALSE; // tv is not connected
}
```

NOTE: DAC detection can be performed while the DENC generates SDTV or HDTV outputs.

The second method that can be used to readback from the encoder is called the ***Legacy*** method. This is because the procedure that follows was the only manner in which Conexant's first generation encoder (i.e., Bt868/869) could be read from. For compatibility purposes, this method was carried forward and exists in this third- generation encoder.

The Legacy procedure to follow for serial read-back and TV detection purposes is shown in Table 34. The ESTATUS[1:0] Read-Back Bit Map for the Legacy Algorithm is provided in Table 35.

Table 34. Legacy DAC Detection Algorithm

1. Write 01 to the ESTATUS[1:0]{bits D7=msb and D6 of register 0xC4}bit field. This sets up the encoder to read the MONSTAT data and check if the DACs have a TV connected.
2. Wait 2 ms to allow the analog nodes to reach their operating point.
3. Write the CHECK_STAT register bit to a one (bit D6 of register BA). This will latch the MONSTAT data internally and then clear itself.
4. Read the MONSTAT data by issuing 0x89 or 0x8B for the CX25898/9's device address. This ensures the least significant bit of the device write portion of the transaction is 1, which indicates to the encoder that it must send a byte of data on the next serial transaction. Do not write a subaddress to the encoder (this is not necessary since the first generation encoder only had one read register) and then read the next byte after the ACK. The 8-bit read in Step 1 contains either the CX25898/9's ID&VERSION (if ESTATUS was written to 00) or the CX25898/9's Monitor Detection for DACs C, B, and A + Closed Caption Status info and the FIELD # (if ESTATUS = 01). If ESTATUS was written to 10 in Step 1, the read byte will contain the PLL_LOCK, FIFO status bits, PAL bit, and BUSY bit.
5. If ESTATUS = 01, the serial master should receive one byte of information telling it the following information in this order:
6. Monitor Connection Status for DACA output (MONSTAT_A = most significant bit).
7. Monitor Connection Status for DACB output (MONSTAT_B).
8. Monitor Connection Status for DACC output (MONSTAT_C).
9. CCSTAT_E, CCSTAT_O.
10. FIELD2, FIELD1, FIELD0 (least significant bit). The FIELD[2:0] bits indicate the field number that was last encoded. 000 indicates the 1st field.
11. The serial master must issue a STOP condition to finish the Read transaction. An ACK is not necessary before closing the transaction because the CX25898/9 just ignores the ACK anyway. In reality, the CX25898/9 does not really care about ending a transaction properly as long as a proper START condition is used to start the next transaction. In the read mode when the CX25898/9 is driving the SDA port, ending the transaction cannot take place until the encoder releases control of the SID line. This happens during the transition from when the last bit of the register is output to the receiving of the ACK.
12. The graphics controller, acting as the serial master, should clear the CHECK_STAT register bit back to 0 (bit D6 of register BA) by writing zero to the CHECK_STAT register bit (bit D6 of register BA) to display standard video again from the CX25898/9 VGA encoder.

Table 35. ESTATUS[1:0] Read-Back Bit Map for Legacy Algorithm

ESTATUS [1:0]	7	6	5	4	3	2	1	0
00	ID[2:0]			VERSION[4:0]				
01	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_O	FIELD[2:0]		
10	Reserved	SECAM	PLL_RESET_OUT	PLL_LOCK	FIFO_OVER	FIFO_UNDER	PAL	RESERVED

GENERAL NOTE:
1. Descriptions of these bits are found in Table 39.

To reiterate, a START condition needs to be issued by the serial master to start the next transaction. In the read mode, when the CX25898/9 is driving the SID port, an end to the transaction cannot take place until the encoder releases control of the SID line. This event happens during the transition from when the last bit of the register is output to the receiving of the ACK.

1.4.48 Sleep/Power Management

There are a number of sleep/power down options for the CX25898/9. These options can be grouped into three different categories. The first category pertains to power management during normal operation.

- DIS_PLL bit:
  In nonsleep mode, when an external clock is being used, and the PLL is not needed, this bit will disable the PLL function.
- XTL_BFO_DIS bit:
  This disables the crystal buffer when it is not needed.
- DIS_CLKO bit:
  This will disable the CLKO output pin when not needed, i.e., an external clock is used in slave interface or to reduce sleep current.
- DACDISx/DACOFF bits:
  Each individual DAC can be powered down by setting its corresponding DACDISx bit. This is useful only if some of the DACs are not being utilized by the graphics system. The entire analog subsection of the device can be powered-down with the DACOFF bit, allowing digital operations to continue while reducing the power in the analog circuitry. This will achieve a significant reduction in power while maintaining all digital functionality.

The second category pertains to software enabled sleep operation.

- SLEEP_EN bit:
  Shuts down all internal clocks except the serial port interface clock. Disables all digital I/O pins except these: SLEEP, ALTADDR, CLKO, XTAL_IN, and XTAL_OUT. Disables the PLL. Turns off all DACs and VREF; the SLEEP and RESET* pins are never disabled.
- PLL_KEEP_ALIVE bit:
  When the PLL is used to provide a system clock, this bit keeps it functioning if the rest of the chip is slept through either the sleep pin or sleep bit. This bit has no affect if DIS_PLL is set.

The third category relates to the pin driven sleep operation.

- SLEEP pin:
  In addition to what the SLEEP_EN bit does, the sleep pin shuts down the serial port interface, shuts down the crystal, and disables the ALTADDR pin. If the SLEEP pin = 1, the only way the encoder can return to normal operation is by resetting the SLEEP pin in 0. The encoder will return to normal operation by performing a power-on reset. This means the encoder will enter autoconfiguration mode 0 and expect a 640x480 RGB input, pseudo-master interface, and provide an NTSC output.

To achieve additional power savings, all the power management options available in normal operation are also available in software or pin driven sleep operation.

For the lowest possible power consumption, set the XTAL_BFO_DIS and DIS_CLKO bits in order, then pull the SLEEP (pin 35) high.

2 Internal Registers

2.1 Register Map Overview

A complete register bit map is provided in Table 36. All registers are read/write unless denoted otherwise. The changes between CX25898/9 and CX25874/5 are shaded.

Table 36. Register Bit Map for CX25898/9 *(1 of 3)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
00[1]	ID[7:4]				VERSION[3:0]			
02[1]	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_0	FIELD_CNT[2:0]		
04[1]	Reserved	SECAM	PLL_RESET_ OUT	PLL_LOCK	FIFO_OVER	FIFO_UNDER	PAL	Reserved
06[1]	MONSTAT_A	MONSTAT_B	MONSTAT_C	MONSTAT_D	FIELD_CNT[3:0]			
24	Reserved	EN-VGEN_ADJ	EN_VSYNC_GEN	HD_50HZ_EN	Reserved	Reserved	Reserved	PIX_REVERSE
26	YC2YP	GPO[5]	GPO[4]	GPO[3]	GPO_OE	GPO[2]	GPO[1]	GPO[0]
2E	HDTV_EN	RGB2YPRPB	RPR_SYNC_ DIS	GY_SYNC_DIS	BPB_SYNC_ DIS	HD_SYNC_ EDGE	RASTER_SEL[1:0]	
30	SLEEP_EN	Reserved	XTL_BFO_ DIS	PLL_KEEP_ ALIVE	Reserved	DIS_PLL	DIS_CLKO	Reserved
32	AUTO_CHK	Reserved	Reserved	Reserved	IN_MODE[3]	DATDLY_RE	OFFSET_ RGB	CSC_SEL
34	ADPT_FF	Reserved	Reserved	C_ALTFF[1:0]		Reserved	Y_ALTFF[1:0]	
36	FFRTN	YSELECT	C_THRESH[2:0]			Y_THRESH[2:0]		
38[3]	Reserved	PIX_DOUBLE	PLL_32CLK	DIV2	HBURST_ END[8]	HBURST_ BEGINS[8]	V_LINESI [10]	H_BLANKI [9]
3A	RAND_EN	Reserved	Reserved	Reserved	HALF_CLKO	Reserved	PLL_INPUT	DIV2_ LATCH
3C	MCOMPY[7:0]							
3E	MCOMPYU[7:0]							
40	MCOMPV[7:0]							
42	MSC_DB[7:0]							
44	MSC_DB[15:8]							
46	MSC_DB[23:16]							
48	MSC_DB[31:24]							
4A	DR_LIMITP[7:0]							
4C	DR_LIMITN[7:0]							
4E	Reserved	Reserved	DR_LIMITN[10:8]			DR_LIMITP[10:8]		

Table 36. Register Bit Map for CX25898/9 *(2 of 3)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
50	DB_LIMITP[7:0]							
52	DB_LIMITN[7:0]							
54	Reserved	Reserved	DB_LIMITN[10:8]			DB_LIMITP[10:8]		
56	FIL4286INCR[7:0]							
58	Reserved	Reserved	FILFSCONV[5:0]					
5A	Y_OFF[7:0]							
5C	HUE_ADJ[7:0]							
5E	XDSSEL[3:0]				CCSEL[3:0]			
60	EWSSF2	EWSSF1	Reserved	Reserved	WSDAT[4:1]			
62	WSDAT[12:5]							
64	WSDAT[20:13]							
66	WSSINC[7:0]							
68	WSSINC[15:8]							
6A	Reserved	Reserved	Reserved	Reserved	WSSINC[19:16]			
6C	TIMING_ RST	EN_REG_RD	FFCBAR	BLNK_IGNORE	EN_SCART	EACTIVE	FLD_MODE[1:0]	
6E	HSYNOFFSET[7:0]							
70	HSYNOFFSET[9:8]		HSYNWIDTH[5:0]					
72	VSYNCOFFSET[7:0]							
74	DATDLY	DATSWP	Reserved			VSYNWIDTH[2:0]		
76[3]	H_CLKO[7:0]							
78[3]	H_ACTIVE[7:0]							
7A[3]	HSYNC_WIDTH[7:0]							
7C[3]	HBURST_BEGIN[7:0]							
7E[3]	HBURST_END[7:0]							
80[3]	H_BLANKO[7:0]							
82[3]	V_BLANKO[7:0]							
84[3]	V_ACTIVEO[7:0]							
86[3]	V_ACTIVEO[8]	H_ACTIVE[10:8]			H_CLKO[11:8]			
88[3]	H_FRACT[7:0]							
8A[3]	H_CLKI[7:0]							
8C[3]	H_BLANKI[7:0]							
8E[3]	Reserved	Reserved	Reserved	VBLANKDLY	H_BLANKI[8]	H_CLKI[10:8]		
90[3]	V_LINESI[7:0]							
92[3]	V_BLANKI[7:0]							
94[3]	V_ACTIVEI[7:0]							
96[3]	CLPF[1:0]		YLPG[1:0]		V_ACTIVEI[9:8]		V_LINESI[9:8]	
98[3]	V_SCALE[7:0]							

Table 36. Register Bit Map for CX25898/9 *(3 of 3)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
9A[3]	H_BLANKO[9:8]		V_SCALE[13:8]					
9C[3]	PLL_FRACT[7:0]							
9E[3]	PLL_FRACT[15:8]							
A0[3]	EN_XCLK	BY_PLL	PLL_INT[5:0]					
A2[3]	FM	ECLIP	PAL_MD	DIS_SCRST	VSYNC_DUR	625LINE	SETUP	NI_OUT
A4[3]	SYNC_AMP[7:0]							
A6[3]	BST_AMP[7:0]							
A8[3]	MCR[7:0]							
AA[3]	MCB[7:0]							
AC[3]	MY[7:0]							
AE[3]	MSC[7:0]							
B0[3]	MSC[15:8]							
B2[3]	MSC[23:16]							
B4[3]	MSC[31:24]							
B6	PHASE_OFF[7:0]							
B8[4]	Reserved	CONFIG[5:3]			Reserved	CONFIG[2:0]		
BA	SRESET	CHECK_STAT	SLAVE	DACOFF	DACDISD	DACDISC	DACDISB	DACDISA
BC	CCF2B1[7:0]							
BE	CCF2B2[7:0]							
C0	CCF1B1[7:0]							
C2	CCF1B2[7:0]							
C4	ESTATUS[1:0]		ECCF2(EXDS)	ECCF1(ECC)	ECCGATE	ECBAR	DCHROMA	EN_OUT
C6	EN_BLANKO	EN_DOT	FIELDI	VSYNCI	HSYNCI	IN_MODE[2:0]		
C8	DIS_YLPF	DIS_FFILT	F_SELC[2:0]			F_SELY[2:0]		
CA	DIS_GMUSHY	DIS_GMSHY	YCORING[2:0]			YATTENUATE[2:0]		
CC	DIS_GMUSHC	DIS_GMSHC	CCORING[2:0]			CATTENUATE[2:0]		
CE	OUT_MUXD[1:0]		OUT_MUXC[1:0]		OUT_MUXB[1:0]		OUT_MUXA[1:0]	
D0	CCR_START[7:0]							
D2	CC_ADD[7:0]							
D4	MODE2X	DIV2[2]	Reserved	CCR_START[8]	CC_ADD[11:8]			
D6	CCR_ START[9]	E656	BLANKI	EBLUE	OUT_MODE[1:0]		LUMADLY[1:0]	
D8	CHROMA_ BW	BY_YCCR	PKFIL_SEL[1:0]		FIELD_ID	CVBSD_INV	SC_ PATTERN	PROG_SC

FOOTNOTE:

(1) This register is read-only.

(2) These bits are repeated in other registers. The value of these bits will always match those with the same name. Any redundancy of bits have been done for backwards register compatibility.

(3) This register is reprogrammed by the autoconfiguration process.

(4) *When sequentially writing a new register set to the CX25898/9, make sure to skip register 0xB8.* This is the autoconfiguration register and writing to it will overwrite registers 0x76 through 0xB4 and 0x38 with autoconfiguration values.

2.2 Reading Registers

Following a start condition, writing 0x89 and then the desired subaddress initiates the read-back sequence when the ALTADDR pin is low. The next eight bits of information, returned by the CX25898/9, can be read from the SID pin, most significant bit first. Alternative address 0x8B initiates readback access when the ALTADDR pin is high. Registers 0x00 through 0x06 are read only. All other registers can be read from or written to.

The ID[3:0] bits of register 0x00 indicate the part type. The lower four bits (VERSION[3:0]) indicate the version number of that particular encoder.

For software detection of a connected TV monitor on each DAC output, the MONSTAT_x bits (found in both the 0x06 register and 0x02 register for legacy purposes) should be read accordingly after writing to CHECK_STAT. For a description of this process follow the guidelines and algorithm contained in the TV DAC Detection Procedures section.

To check the status of the monitor connections at the DAC output automatically once per frame during the vertical blanking interval, set the AUTO_CHK bit.

Use the following pseudocode sample to properly read registers within the CX25898/9.

First, there are some basic action assignments:

S_ACK	The slave device generates the acknowledge (i.e., the CX25898/9
M_ACK	The serial master generates the acknowledge.
NACK	No acknowledge is generated by either device.
START	Serial start condition; falling edge of SID occurs when SIC is high.
STOP	Serial stop condition; rising edge of SID occurs when SIC is high.
D_ADDR	The device address is 88 hex with ALTADDR = 0, 8A when it is a 1.

- Next, load 46 hex into register 6C. This will write the EN_REG_RD bit to 1. This enables the serial master to readback all encoder registers.
- Perform the following transaction with the serial master:
- START/D_ADDR/S_ACK/6C/S_ACK/46/S_ACK/STOP
- Next, use the serial master to write the register address from which read-back will occur:
  - START/D_ADDR/S_ACK/<read_address>/S_ACK/STOP
- Finally, read the data starting at the read_address previously issued:
- START/D_ADDR+1/S_ACK/<readdata(0)>/M_ACK/<readdata(1)>/M_ACK/ <readdata(2)>/M_ACK/.../.../<readdata(n-1)>/M_ACK/<readdata(n)>/ NACK/ STOP

where:

readdata(0) is the data from CX25898/9 register <read_address>

readdata(1) is the data from CX25898/9 register <read_address>+1

readdata(2) is the data from CX25898/9 register <read_address>+2

As long as the CX25898/9 detects an acknowledge from the serial master (M_ACK) after providing the read data, it will expect the read transaction to continue.

When no acknowledge is received, the encoder will end the read operation. Using this approach, consecutive register reads can be provided with less software overhead.

As long as the CX25898/9 detects an acknowledge from the serial master (M_ACK) after providing the read data, it will expect the read transaction to continue.

When no acknowledge is received, the encoder will end the read operation. Using this approach, consecutive register reads can be provided with less software overhead.

To read just one register location, every programming step remains the same up to the point where the read data transaction occurs.

In this case, the master should simply substitute a STOP in place of the M_ACK. The final step of the transaction will therefore be:

- START/D_ADDR + 1/S_ACK/<readdata>/NACK/STOP

Table 37 contains the bit map for all of the encoder's read-only registers. Table 38 contains the data details. As mentioned previously, to enable full register readback, the EN_REG_RD bit must be set to 1.

Table 37. Bit Map for Read-Only Registers

Register Address	7	6	5	4	3	2	1	0
00	ID[7:4]				VERSION[3:0]			
02	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_0	FIELD_CNT[2:0]		
04	Reserved	SECAM	PLL_RESET_OUT	PLL_LOCK	FIFO_OVER	FIFO_UNDER	PAL	Reserved
06	MONSTAT_A	MONSTAT_B	MONSTAT_C	MONSTAT_D	FIELD_CNT[3:0]			

Table 38. Data Details for All Read-Only Registers

Bit Names	Data Definition
ID[7:4]	Indicates the part number of the Conexant VGA Encoder. The following ID[3:0] is returned.When the Conexant VGA Encoder present is: 0000Bt868 (Buteo, 1st generation encoder, no Macrovision) 0010Bt869 (Buteo, 1st generation encoder, with Macrovision) 0100CX25870 (Accipiter, 2ndgeneration encoder, no Macrovision) 0110CX25871 (Accipiter, 2nd generation encoder, with Macrovision) 1000CX25872 (Aquila Lite, 3rd generation encoder, no Macrovision) 1010CX25873 (Aquila Lite, 3rd generation encoder, with Macrovision) 1100CX25874 (Aquila, 3rd generation encoder, no Macrovision) 1110CX25875 (Aquila, 3rd generation encoder, with Macrovision) 0101 CX25898 0111CX25899
VERSION[3:0]	Version number: Revision B Revision C Revision D
MONSTAT_A	Monitor connection status for DACA output, 1 denotes monitor connected to DACA.
MONSTAT_B	Monitor connection status for DACB output, 1 denotes monitor connected to DACB.
MONSTAT_C	Monitor connection status for DACC output, 1 denotes monitor connected to DACC.
MONSTAT_D	Monitor connection status for DACD output, 1 denotes monitor connected to DACD.
CCSTAT_E	High if closed-caption data has been written for the even field; it is low immediately after the clock run-in on the extended service line for the even field.
CCSTAT_O	High if closed-caption data has been written for the odd field; it is low immediately after the clock run-in on the closed caption line for the odd field.
FIELD_CNT[3:0]	Field number, where 0000 indicates the first field, 1111 indicates the 15th field. An extra bit was added to accommodate the SECAM standard.
SECAM	Indicates status of SECAM mode. If the encoder is outputting SECAM, this bit will be set to 1.
PLL_RESET_OUT	PLL reset state.
PLL_LOCK	High when PLL is locked. Will be low if PLL loses lock.
FIFO_OVER	Set to one if FIFO overflows. Reset on read.
FIFO_UNDER	Set to one if FIFO underflows. Reset on read.
PAL	Indicates status of PAL mode. If the encoder is outputting PAL or SECAM, this bit will be set to 1. If the encoder is transmitting NTSC, this bit is set to 0.

2.3 Writing Registers

Following a start condition, writing 0x88 as the device ID initiates write access to the CX25898/9 registers when the ALTADDR pin is low. Alternative device ID 0x8A initiates write access when the ALTADDR pin is high. If the data is written sequentially in subaddress order, only the first subaddress needs to be written; the internal address counter will automatically *increment by two* after each write to the next register.

When writing an entirely new, complete register set to the CX25898/9, make sure to skip register 0xB8. This is the autoconfiguration register, and writing any value to it after having loaded values into other registers will replace desired data with unwanted data in register 38 and register indices 0x76–0xB4.

For read/write register programming details, see Table 39. The table is sorted in alphabetical order by bit/register name.

Table 39. Programming Details for All Read/Write Registers *(1 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
625LINE	Bit 2–A2	0 = 525-line format (NTSC-M, NTSC-J, PAL-M), PAL-60, 480p HDTV 1 = 625-line format (PAL-BDGHI, PAL-N, PAL-Nc, SECAM, 625p HDTV
ADPT_FF	Bit 7–34	0 = Disable adaptive flicker filter. (DEFAULT) 1 = Enable adaptive flicker filter.
AUTO_CHK	Bit 7–32	It is recommended that this bit only be used while generating NTSC/PAL/SECAM outputs. 0 = Normal operation. (DEFAULT) 1 = The status of the monitor connections will be automatically checked once per frame during the VBI. This bit should not be set for HDTV output modes.
BLANKI	Bit 5–D6	0 = Active low BLANK* pin. (DEFAULT) 1 = Active high BLANK* pin.
BLNK_IGNORE	Bit 4–6C	0 = Use BLANK* pin to indicate the active pixel region in CCIR 656 mode. (DEFAULT) 1 = Use registers H_BLANKI and V_BLANKI to determine the active pixel region in CCIR 656 mode.
BLUEFLD	Bit 4–D6	0 = Normal operation. (DEFAULT) 1 = Generate standard-definition blue field. The encoder does not require any digital input signals (CLKI, PIX[23]-PIX[7], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
BPB_SYNC_DIS	Bit 3–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Blue/P_B output or bilevel sync on VGA Blue output. (DEFAULT) 1 = Disables trilevel sync on HDTV Blue/P_B output or bilevel sync on VGA Blue output. This bit will have to be set manually for EIA-770.3 compliance.
BST_AMP[7:0]	Bits [7:0]–A6	Color burst amplitude factor. Each bit adjustment represents 1.25 mV of burst amplitude. This register has no effect on the SECAM DR and DB color burst amplitudes.

***Table 39. Programming Details for All Read/Write Registers** (2 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
BY_PLL	Bit 6–A0	0 = Use on chip PLL (DEFAULT) 1 = Bypass PLL (encoder clock is crystal frequency).
BY_YCCR	Bit 6–D8	0 = Luma cross color reduction filter on. 1 = Bypass luma cross color reduction filter. Optimal standard-definition quality most often realized with this setting. (DEFAULT)
C_ALTFF[1:0]	Bits [4:3]–34	Chroma alternate flicker filter selection. This bit will only have an effect when ADPT_FF is set. C_ALTFF should always be programmed to a value greater than or equal to F_SELC. 00 = 5 line (DEFAULT) 01 = 2 line 10 = 3 line 11 = 4 line
C_THRESH[2:0]	Bits [5:3]–36	Controls the sensitivity or limit of turning on the alternate flicker filter for chroma in adaptive mode. (DEFAULT = 000)
CATTENUATE[2:0]	Bits [2:0]–CC	Chroma Attenuation. Used for saturation control. 000 = 1.0 gain No Attenuation (DEFAULT) 001 = 15/16 gain 010 = 7/8 gain 011 = 3/4 gain 100 = 1/2 gain 101 = 1/4 gain 110 = 1/8 gain 111 = 0 gain (Force Chroma to 0)
CC_ADD[11:0]	Bits [3:0]–D4 and Bits [7:0]–D2	Closed-captioning DTO increment.
CCF1B1[7:0]	Bits [7:0]–C0	This is the first byte of closed-caption information for the odd field, line 21 for NTSC or line 22 for PAL. Data is encoded LSb first.
CCF1B2[7:0]	Bits [7:0]–C2	This is the second byte of closed-caption information for the odd field, line 21 for NTSC or line 22 for PAL. Data is encoded LSb first.
CCF2B1[7:0]	Bits [7:0]–BC	This is the first byte of closed-caption information for the even field, line 284 for NTSC or line 335 for PAL. Data is encoded LSb first.
CCF2B2[7:0]	Bits [7:0]–BE	This is the second byte of closed-caption information for the even field, line 284 for NTSC or line 335 for PAL. Data is encoded LSb first.

***Table 39. Programming Details for All Read/Write Registers** (3 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
CCORING[2:0]	Bits [5:3]–CC	Chroma Coring. Values below the CCORING[2:0] limit are automatically clamped to a saturation value of 0. 000 = Bypass (DEFAULT) 001 = 1/128 of range (± 1/256 of range) 010 = 1/64 of range (± 1/128 of range) 011 = 1/32 of range (± 1/64 of range) 100 = 1/16 of range (± 1/32 of range) 101 = 1/8 of range (± 1/16 of range) 110 = 1/4 of range (± 1/8 of range) 111 = Reserved
CCR_START[9] CCR_START[8] CCR_START[7:0]	Bit 7 of D6, Bit 4 of D4, and Bits [7:0] of D0	Closed-captioning clock run-in start in clock cycles from leading edge of HSYNC*. Refer to the closed-captioning (CC) section for more details.
CCSEL[3:0]	Bits [3:0]–5E	Line position of Closed Captioning (CC) Content. Controls which line Closed Captioning (CC) data is encoded. Each line enable is independent. 0001 = Closed Captioning (CC) on line 19 (525-line) and line 21 (625-line) 0010 = Closed Captioning (CC) on line 20 (525-line) and line 22 (625-line) 0100 = Closed Captioning (CC) on line 21 (525-line) and line 23 (625-line) (DEFAULT) 1000 = Closed Captioning (CC) on line 22 (525-line) and line 24 (625-line)
CHECK_STAT	Bit 6–BA	Writing a 1 to this bit checks the status of the monitor connections at the DAC output. This is also automatically performed on any reset condition, including a software reset. This bit is self-clearing.
CHROMA_BW	Bit 7–D8	0 = Normal digital chroma bandwidth. See the figure entitled Digital Chrominance Standard Bandwidth Filter (DEFAULT). 1 = Wide digital chroma bandwidth. See the figure entitled Digital Chrominance Wide Bandwith Filter.
CLPF[1:0]	Bits [7:6]–96	Chroma Post-Flicker Filter/Scaler Horizontal Low-Pass Filter: 00 = Bypass (DEFAULT) 01 = Reserved 10 = Chroma Horizontal LPF2 setting 11 = Chroma Horizontal LPF3 setting

Table 39. Programming Details for All Read/Write Registers *(4 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
CONFIG[5:0]	Bits [6:4] and Bits [2:0]–B8	The combination of CONFIG[5:3] and CONFIG[2:0] determines the autoconfiguration mode entered by the CX25898/9 immediately after register 0xB8 is written.

CONFIG [5:0]	Input Format	Active Resolution	Output	Output Ratio	Mode
000000	= RGB	640x480	NTSC	Overscan = Lower	Mode 0
000001	= RGB	640x480	PAL-BDGHI	Overscan = Standard	Mode 1
000010	= RGB	800x600	NTSC	Overscan = Alternate	Mode 2
000011	= RGB	800x600	PAL-BDGHI	Overscan = Lower	Mode 3
000100	= YCrCb	640x480	NTSC	Overscan = Lower	Mode 4
000101	= YCrCb	640x480	PAL-BDGHI	Overscan = Standard	Mode 5
000110	= YCrCb	800x600	NTSC	Overscan = Alternate	Mode 6
000111	= YCrCb	800x600	PAL-BDGHI	Overscan = Lower	Mode 7
001000	= RGB	640x400	NTSC	Overscan = Standard	Mode 8
001001	= RGB	640x400	PAL-BDGHI	Overscan = Standard	Mode 9
001010	= RGB	1024x768	NTSC	Overscan = Standard	Mode 10
001011	= RGB	1024x768	PAL-BDGHI	Overscan = Standard	Mode 11
001100	= RGB	320x240	NTSC	Pix Double Set = Standard	Mode 12
001101	= RGB	320x240	PAL-BDGHI	Pix Double Set = Standard	Mode 13
001110	= YCrCb	1024x768	NTSC	Overscan = Higher	Mode 14
001111	= YCrCb	1024x768	PAL-BDGHI	Overscan = Higher	Mode 15
010000	= RGB	640X480	NTSC	Overscan = Standard	Mode 16
010001	= RGB	640x480	PAL-BDGHI	Overscan = Lower	Mode 17
010010	= RGB	800x600	NTSC	Overscan = Lower	Mode 18
010011	= RGB	800x600	PAL-BDGHI	Overscan = Standard	Mode 19
010100	= RGB	640X480	PAL-60 (China)	Overscan = Lower	Mode 20
010101	= YCrCb	640x480	PAL-BDGHI	Overscan = Lower	Mode 21
010110	= YCrCb	800x600	NTSC	Overscan = Lower	Mode 22
010111	= YCrCb	800x600	PAL-BDGHI	Overscan = Standard	Mode 23
011000	= RGB	720x400	NTSC	9-dot font for DOS Overscan =Standard	Mode 24
011001	= RGB	720x400	PAL-BDGHI	9-dot font for DOS Overscan =Standard	Mode 25

***Table 39. Programming Details for All Read/Write Registers** (5 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
CONFIG[5:0] (cont'd)	Bits [6:4] and Bits [2:0]–B8	The combination of CONFIG[5:3] and CONFIG[2:0] determines the autoconfiguration mode entered by the CX25898/9 immediately after register 0xB8 is written.

CONFIG [5:0]	Input Format	Active Resolution	Output	Output Ratio	Mode
011101	= YCrCb	720x576	PAL-BDGHI	Interlaced Input, Slave Interface Overscan = 0% DIV2 set. EN_XCLK set. CCIR601 timing.	Mode 29
011110	= YCrCb	1024x768	NTSC	Overscan = Lower	Mode 30
011111	= RGB	720x576	PAL-BDGHI	Overscan = ~ 0% Noninterlaced Input for DVD	Mode 31
100000	= RGB	640x480	NTSC	Overscan = Higher	Mode 32
100001	= RGB	640x480	PAL-BDGHI	Overscan = Higher	Mode 33
100010	= RGB	800x600	NTSC	Overscan = Higher	Mode 34
100011	= RGB	800x600	PAL-BDGHI	Overscan = Higher	Mode 35
100100	= YCrCb	640x480	NTSC	Overscan = Higher	Mode 36
100101	= YCrCb	640x480	PAL-BDGHI	Overscan = Higher	Mode 37
100110	= YCrCb	800x600	NTSC	Overscan = Higher	Mode 38
100111	= YCrCb	800x600	PAL-BDGHI	Overscan = Higher	Mode 39
101000	= RGB	800x600	NTSC	Overscan = Standard	Mode 40
101001	= RGB	320x200	PAL-BDGHI	Pix Double Set Overscan = Standard	Mode 41
101010	= RGB	1024x768	NTSC	Overscan = Higher	Mode 42
101011	= RGB	1024x768	PAL-BDGHI	Overscan = Higher	Mode 43
101100	= RGB	720x480	NTSC	Noninterlaced Input for DVD Overscan = ~ 0%	Mode 44
101101	= RGB	320x200	NTSC	Pix Double Set Overscan = Standard	Mode 45

CSC_SEL	Bit 0–32	0 = Standard color space conversion for RGB to Y (R-Y) (B-Y) based on Y =0 .299R +0 .587G +0 .114 B (DEFAULT) 1 = HDTV color space conversion for RGB to Y (R-Y) (B-Y) based on Y = 0.2126R + 0.7152G + 0.0722B
CVBSD_INV	Bit 2–D8	0 = Normal operation. (DEFAULT) 1 = Invert CVBS_DLY output.
DACDISA	Bit 0–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACA output. Current is set to 0 mA; output will go to 0 V.

***Table 39. Programming Details for All Read/Write Registers** (6 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
DACDISB	Bit 1–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACB output. Current is set to 0 mA; output will go to 0 V.
DACDISC	Bit 2–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACC output. Current is set to 0 mA; output will go to 0 V.
DACDISD	Bit 3–BA	0 = Normal Operation. (DEFAULT) 1 = Disables DACD output. Current is set to 0 mA; output will go to 0 V.
DACOFF	Bit 4–BA	0 = Normal operation. (DEFAULT) 1 = Disables DAC output current and internal voltage reference for all DACs. This will limit power consumption to just the internal digital circuitry. DACs cannot be detected while DACs are off.
DATDLY	Bit 7–74	0 = No delay in falling edge pixel data. (DEFAULT) 1 = Delays the falling edge pixel data by 1 full clock period. This bit is used to correct a multiplexed input data sequence that delivers a pixel on a falling edge and the following rising edge (rather than a rising edge and the following falling edge, as expected).
DATDLY_RE	Bit 2–32	0 = No delay in rising edge pixel data. (DEFAULT) 1 = Delays the rising edge pixel data by 1 full clock period. This bit is used together with DATSWP to correct a multiplexed input data sequence that delivers a pixel on a falling edge and the following rising edge with the falling edge and rising edge data swapped.
DATSWP	Bit 6–74	0 = VGA Encoder expects an order of rising edge data/falling edge data coming from the graphics controller (DEFAULT). 1 = Swaps the falling edge pixel data with the rising edge pixel data at the input of the pixel port.
DB_LIMITN[10:8] DB_LIMITN[7:0]	Bits [5:3]–54 and Bits [7:0]–52	Lower bound limit for DB frequency deviation in SECAM. Review SECAM Output Section.
DB_LIMITP[10:8] DB_LIMITP[7:0]	Bits [2:0]–54 and Bits [7:0]–50	Upper bound limit for DB frequency deviation in SECAM. Review SECAM Output Section.
DCHROMA	Bit 1–C4	0 = Normal operation. (DEFAULT) 1 = Disable the chrominance portion of video output. Composite and S-Video outputs appear as gray scale.
DIS_CLKO	Bit 1–30	0 = Enable CLKO output. (DEFAULT) 1 = Three-state CLKO output. This will disable the CLKO output when not needed, i.e., an external clock is used (Slave Interface). Disabling CLKO is also effective in reducing the current draw in SLEEP mode.
DIS_FFILT	Bit 6–C8	0 = Enables Standard Flicker Filter. (DEFAULT) 1 = Disables Standard Flicker Filter.

Table 39. Programming Details for All Read/Write Registers *(7 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
DIS_GMSHC	Bit 6–CC	0 = Enables Chroma Pseudo Gamma Removal. (DEFAULT) 1 = Disables Chroma Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMSHY	Bit 6–CA	0 = Enables Luma Pseudo Gamma Removal. (DEFAULT) 1 = Disables Luma Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMUSHC	Bit 7–CC	0 = Enables Chroma Anti-Pseudo Gamma Removal. (DEFAULT) 1 = Disables Chroma Anti-Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMUSHY	Bit 7–CA	0 = Enables Luma Anti-Pseudo Gamma Removal. (DEFAULT) 1 = Disables Luma Anti-Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_PLL	Bit 2–30	0 = PLL enable. (DEFAULT) 1 = PLL disable. In nonsleep mode, if an external clock is being used and the PLL is not needed, this bit will disable the PLL function. Some of the special modes are not available when the PLL is disabled.
DIS_SCRST	Bit 4–A2	0 = Normal operation. The subcarrier phase is reset to 0 at the beginning of each color field sequence. (DEFAULT) 1 = Disables subcarrier reset event at beginning of field sequence.
DIS_YLPF	Bit 7–C8	0 = Enable Luma Initial Horizontal Low-Pass filter. (DEFAULT) 1 = Disable Luma Initial Horizontal Low-Pass filter.
DIV2	Bit 6–D4 and Bit 4–38	0 = Normal operation. (DEFAULT) 1 = Divides input pixel rate by two (for any interlaced timing input). Useful for DVD playback resolutions. The DIV2 bit in register D4 was kept for Bt868/869 and CX25870/1/2/3/4/5 compatibility purposes. The DIV2 bit in register 38 is autoconfigurable. These bit values always mirror each other. Changing the state of one DIV2 register field automatically updates the other DIV2 register field.
DIV2_LATCH	Bit 0–3A	This bit only has an effect when DIV2 = 1. 0 = Data is clocked at rising edge of CLKI. (DEFAULT) 1 = Data is clocked at rising and falling edges of CLKI.
DR_LIMITN[10:8] DR_LIMITN[7:0]	Bits [5:3]–4E and Bits [7:0]–4C	Lower bound limit for DR frequency deviation in SECAM. Review SECAM Output Section.
DR_LIMITP[10:8] DR_LIMITP[7:0]	Bits [2:0]–4E and Bits [7:0]–4A	Upper bound limit for DR frequency deviation in SECAM. Review SECAM Output Section.
E656	Bit 6–D6	0 = Input pixel format defined by IN_MODE[3:0] register. (DEFAULT) 1 = CCIR 656 input on PIX[7:0] port, or PIX[11:4] port.

Table 39. Programming Details for All Read/Write Registers *(8 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
EACTIVE	Bit 2–6C	0 = Black burst. (DEFAULT) 1 = Enable normal video.
ECBAR	Bit 2–C4	0 = Normal operation. (DEFAULT) 1 = Enable standard-definition color bars. The encoder does not require any digital input signals (CLKI, PIX[23]–PIX[0], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
ECCF1(ECC)	Bit 4–C4	0 = Disables closed-caption encoding on field 1. (DEFAULT) 1 = Enables closed-caption encoding on field 1.
ECCF2(EXDS)	Bit 5–C4	0 = Disables closed-caption encoding on field 2. (DEFAULT) 1 = Enables closed-caption encoding on field 2.
ECCGATE	Bit 3–C4	0 = Normal closed-caption encoding. (DEFAULT) 1 = Enables closed-caption encoding constraints. After encoding, future encoding is disabled until a complete pair of new data bytes is received. This prevents encoding of redundant or incomplete data.
ECLIP	Bit 6–A2	0 = Normal operation. (DEFAULT) 1 = Enable clipping; DAC values less than 31 hex are made 31 by the encoder.
EN_BLANKO	Bit 7–C6	Interface bit: Works in conjunction with EN_DOT, EN_OUT, and SLAVE. Controls direction of BLANK* signal. 0 = Enables BLANK* as an input. 1 = Enables BLANK* pin as an output, or no BLANK* signal is utilized in the system interface. (DEFAULT)
EN_DOT	Bit 6–C6	Interface bit: Works in conjunction with EN_BLANKO, EN_OUT, and SLAVE. Controls blanking method. 0 = Encoder uses its internal counters to determine the active-versus-blanked regions of input data. (DEFAULT) 1 = Encoder uses the BLANK* signal being received to determine where active video starts (rising edge by default) and where blanking region starts (falling edge by default).
EN_OUT	Bit 0–C4	Interface bit: Works in conjunction with EN_BLANKO, EN_DOT, and SLAVE. Turns timing outputs on or off. 0 = Three-state (CLKO, HSYNC*, VSYNC*, BLANK* and FIELD) timing outputs. 1 = Allows CLKO and other outputs to be enabled, depending upon EN_BLANKO register bit and the SLAVE bit. (DEFAULT)
EN_REG_RD	Bit 6–6C	0 = Use ESTATUS[1:0] register to select readback status registers. Enable Bt869-like Legacy read-back method. (DEFAULT) 1 = Enable Standard serial register readback of all registers.

Table 39. Programming Details for All Read/Write Registers *(9 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
EN_SCART	Bit 3–6C	Enables SCART video output for Europe. OUT_MODE[1:0] field must be set to 11 (VGA Mode) and HDTV_EN bit must be set to 0. 0 = Enables VGA mode. DACs will output analog RGB with standard bilevel (-40 IRE) analog syncs (DEFAULT). 1 = Enables SCART output mode. DAC will transmit SCART compatible RGB outputs and a composite video output, which includes an analog sync.
EN_VGEN_ADJ	Bit 6–24	Enable alternate VSYNC timing when EN_VSYNC_GEN is set. 0 = Use default settings as give in SMPTE274 spec. Note: the HD_50HZ_EN bit will change these values appropriately. 1 = Use the VLINESI register for the number of vertical lines and use the HCLKO for the number of horizontal pixels to place the 2nd field VSYNC.
EN_VSYNC_GEN	Bit 5–24	Enable VSYNC generation for proper 1080i timing. 0 = generate 2nd field VSYNC based on incoming VSYNC. Assume 2nd field VSYNC comes at the midline point. 1= Generate 2nd field VSYNC internally at midline point. When EN_VSYNC_GEN is set, the timing generator can generate the VSYNC at a default point that depends on HD_50HZ_EN, or the customer can override this default by setting the EN_VGEN_ADJ bit.
EN_XCLK	Bit 7–A0	0 = Encoder generates pixel clock based on its mode settings and transmits this frequency via the CLKO pin for master and pseudo-master interfaces. (DEFAULT) 1 = Use CLKI pin as pixel clock source. This bit must be set for slave interface.
ESTATUS[1:0]	Bits [7:6]–C4	Bt868/869 Legacy serial readback status bit selection. Used in conjunction with EN_REG_RD, CHECK_STAT, AUTO_CHK, and MONSTAT_x bits. Review the table entitled ESTATUS Readback Bit Map.
EWSSF1	Bit 6–60	0 = Disable field 1 WSS data. (DEFAULT) 1 = Enable field 1 WSS data.
EWSSF2	Bit 7–60	0 = Disable field 2 WSS data. (DEFAULT) 1 = Enable field 2 WSS data (only applicable to 525 line standard-definition and 1080i high-definition outputs only).
F_SELC[2:0]	Bits [5:3]–C8	Chroma Standard Flicker Filter: 000 = 5-Line (DEFAULT): most aggressive setting 001 = 2-Line: least aggressive setting 010 = 3-Line 011 = 4-Line 100 = Alternate 5-Line 101 = Alternate 5-Line 110 = Alternate 5-Line 111 = Alternate 5-Line

***Table 39. Programming Details for All Read/Write Registers** (10 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
F_SELY[2:0]	Bits [2:0]–C8	Luma Standard Flicker Filter: 000 = 5-Line (DEFAULT): most aggressive setting 001 = 2-Line: least aggressive setting 010 = 3-Line 011 = 4-Line 100 = Alternate 5-Line 101 = Alternate 5-Line 110 = Alternate 5-Line 111 = Alternate 5-Line
FFCBAR	Bit 5–6C	0 = Normal operation. (DEFAULT) 1 = Enable high-definition or standard-definition flicker filtered color bars. The encoder does not require any digital input signals (CLKI, PIX[23]–PIX[7], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
FFRTN	Bit 7–36	Alternate flicker filter detect and select. This bit is effective only when ADPT_FF = 1. 0 = Once the adaptive algorithm selects the alternate filter, use that filter's coefficients for the rest of the samples for that line. For example, the sequence could be STD/STD/ALT/ALT/ALT; (DEFAULT) 1 = Once the adaptive algorithm selects the alternate filter, use the filter's coefficients for that sample only. For example, the sequence with FFRTN=1 could be STD/STD/ALT/STD/STD.
FIELD_ID	Bit 3–D8	0 = Suppress the SECAM field synchronization signal. (DEFAULT) 1 = Enable the SECAM field synchronization signal (bottle-neck pulses).
FIELDI	Bit 5–C6	0 = Logical 0 from the FIELD pin indicates an even field is being output. (DEFAULT) 1 = Logical 1 from the FIELD pin indicates an odd field is being output.
FILFSCONV[5:0]	Bits [5:0]–58	Adjust SECAM high-frequency pre-emphasis filter according to the clock frequency. Review the SECAM Output section for the correct equations.
FIL4286INCR[7:0]	Bits [7:0]–56	Adds a phase offset to the UV digital components. Review the SECAM Output section for the correct equations.
FLD_MODE[1:0]	Bits [1:0]–6C	CX25898/9 uses this bit to interpret HSYNC* and VSYNC* edges and field detection in slave mode. 00 = A leading edge of VSYNC* that occurs within ±1/4 of HCLKI from the leading edge of HSYNC* indicates the beginning of odd field. A leading edge of VSYNC* that occurs within ±1/4 of HCLKI from the center of the line indicates the beginning of even field. 01 = A leading edge of VSYNC* occurs during HSYNC* active indicates the beginning of odd field. A leading edge of VSYNC* occurs during HSYNC* inactive indicates the beginning of even field. 10 = A leading edge of VSYNC* coincides with the leading edge of HSYNC* indicates the beginning of odd field. A leading edge of VSYNC* does not coincide with the leading edge of HSYNC* indicated the beginning of even field. (DEFAULT) 11 = Reserved.

***Table 39. Programming Details for All Read/Write Registers** (11 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
FM	Bit 7–A2	This bit must be enabled for a valid SECAM video output. 0 = QAM color encoding (NTSC/PAL). (DEFAULT) 1 = FM color encoding (SECAM).
GY_SYNC_DIS	Bit 4–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Green/Y output or bilevel sync on VGA G output. (DEFAULT) 1 = Disables trilevel sync on HDTV Green/Y output or bilevel sync on VGA G output.
GPO-0E	Bit 3:26	General purpose output. High impedance output.
H_ACTIVE[10:8] H_ACTIVE[7:0]	Bits [6:4]–86 and Bits [7:0]–78	Number of active input and output pixels.
H_BLANKI[9] H_BLANKI[8] H_BLANKI[7:0]	Bit 0–38, Bit 3–8E, and Bits [7:0]–8C	Number of CLKI clock cycles between the digital HSYNC* leading edge and first active pixel.
H_BLANKO[9:8] H_BLANKO[7:0]	Bits [7:6]–9A and Bits [7:0]–80	Number of CLKO clock cycles between leading edge of analog horizontal sync and active video.
H_CLKI[10:8] H_CLKI[7:0]	Bits [2:0]–8E and Bits [7:0]–8A	Number of CLKI clock cycles between consecutive leading edges of the digital HSYNC* signal.
H_CLKO[11:8] H_CLKO[7:0]	Bits [3:0]–86 and Bits [7:0]–76	Number of CLKO clock cycles per analog line.
H_FRACT[7:0]	Bits [7:0]–88	Fractional number of input clocks per line. No effect if 00.
HALF_CLKO	Bit 3–3A	0 = Normal operation. (DEFAULT) 1 = CLKO (clock output) frequency divided by 2 while being transmitted.
HBURST_BEGIN[8] HBURST_BEGIN [7:0]	Bit 2–38 and Bits [7:0]–7C	This register contains the number of CLKO clock cycles between the analog horizontal sync falling edge and the 50% point of the first colorburst cycle.
HBURST_END[8] HBURST_END[7:0]	Bit 3–38 and Bits [7:0]–7E	This register contains the number of CLKO clock cycles minus 128 between the analog horizontal sync falling edge and the 50% point of the last colorburst cycle. Make sure to subtract 128 CLKO clock cycles from the calculated 50% point of the last colorburst cycle value and load into this register.
HD_50HZ_EN	Bit 4–24	Enable 50 Hz mode for 1080i.
HD_SYNC_EDGE	Bit 2–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1 and RASTER_SEL is nonzero. 0 = Trilevel sync edges transition time is equal to 4 input clocks. (DEFAULT) 1 = Trilevel sync edges transition time is equal to 2 input clocks.

***Table 39. Programming Details for All Read/Write Registers** (12 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
HDTV_EN	Bit 7–2E	Enable HDTV output mode, OUT_MODE[1:0] register bits must be set to 11 (VGA mode) and EN_SCART must = 0. 0 = Enables VGA mode. DACs will output analog RGB with standard bilevel (-40 IRE) analog syncs. 1 = Enables HDTV output mode. DACs will output HDTV compatible RGB or component video (Y/ P_R/ P_B) outputs. Trilevel syncs and vertical synchronizing/broad pulses will be inserted automatically if RASTER_SEL[1:0] = nonzero. The EN_SCART bit must be 0 for HDTV Output Mode to be functional.
HSYNC_WIDTH [7:0]	Bits [7:0]–7A	Analog horizontal sync width in number of CLKO clock cycles.
HSYNCI	Bit 3–C6	0 = Configures the encoder to send/receive an active low HSYNC* digital signal (DEFAULT) 1 = Configures the encoder to send/receive an active high HSYNC* digital signal.
HSYNOFFSET[9:8] HSYNOFFSET[7:0]	Bits [7:6]–70 and Bits [7:0]–6E	A 2s-complement number. The values range from –512 pixels to +511 pixels. This register manipulates the falling edge position of the digital HSYNC* output from the CX25898/9. The default value is 0 and denotes the standard position of the HSYNC* leading edge. This register is only effective in master interface. (DEFAULT = 0x00)
HSYNWIDTH[5:0]	Bits [5:0]–70	Controls the duration/width of the digital HSYNC output pulse. Value will be hexadecimal and its units are in terms of pixels. A value of 0 is a disallowed condition. The acceptable range is 0x02 pixels to 0x3F pixels (=63 decimal). The default value is 0x02. Never set to 0. This register is only effective in master interface. (DEFAULT = 0x02)
HUE_ADJ[7:0]	Bits [7:0]–5C	This register controls the color hue. It does this by adjusting the color subcarrier phase during the video active region. Increasing this value by 1 unit has the effect of increasing the phase by (360/256) = 1.406 degrees. (DEFAULT = 0x00)

***Table 39. Programming Details for All Read/Write Registers** (13 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
IN_MODE[3] and IN_MODE[2:0]	Bit 3–32 and Bits [2:0]–C6	This bit is used in conjunction with IN_MODE[2:0] to configure the encoder to receive a desired input pixel format. Format of input pixels when IN_MODE[3] = 0 (MSb of this 4-bit sequence): 0000 = 24-bit RGB multiplexed 0001 = 16-bit RGB multiplexed 0010 = 15-bit RGB multiplexed 0011 = 24-bit RGB nonmultiplexed 0100 = 24-bit YCrCb multiplexed 0101 = 16-bit YCrCb multiplexed 0110 = Alternate 16-bit YCrCb multiplexed 0111 = 24-bit YCrCb nonmultiplexed Format of input pixels when IN_MODE[3] = 1(MSb of this 4-bit sequence): 1000 = Alternate 24-bit RGB multiplexed 1001 = Reserved 1010 = 16-bit RGB nonmultiplexed 1011 = Alternate 24-bit RGB nonmultiplexed 1100 = Alternate 24-bit YCrCb multiplexed 1101 = Reserved 1110 = Alternate 16-bit YCrCb nonmultiplexed 1111 = Alternate 24-bit YCrCb nonmultiplexed
LUMADLY[1:0]	Bits [1:0]–D6	Used to program the luminance delay in pixels for the CVBS_DLY and Y_DLY output modes. This binary number provides for a delay of up to three pixels in time. 00 = No delay (DEFAULT) 01 = 1 pixel 10 = 2 pixels 11 = 3 pixels
MCB[7:0]	Bits [7:0]–AA	Multiplication factor for Cb (or B-Y) component prior to subcarrier modulation.
MCOMPU[7:0]	Bits [7:0]–3E	Multiplication factor for component video U output. Value 0x80 (DEFAULT) represents 1.0 scale factor.
MCOMPV[7:0]	Bits [7:0]–40	Multiplication factor for component video V output. Value 0x80 (DEFAULT) represents 1.0 scale factor.
MCOMPY[7:0]	Bits [7:0]–3C	Multiplication factor for component video Y output. Value 0x80 (DEFAULT) represents 1.0. scale factor.
MCR[7:0]	Bits [7:0]–A8	Multiplication factor for Cr (or R-Y) component prior to subcarrier modulation.
MODE2X	Bit 7–D4	0 = Normal operation (DEFAULT). 1 = Divides selected input clock by two (allows for single edge rather than double-edge clock input for pixel latching) for noninterlaced type of data and timing inputs.
MSC[31:0]	Bits [7:0]–B4, B2, B0, AE	Subcarrier increment.

***Table 39. Programming Details for All Read/Write Registers** (14 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
MSC_DB[31:0]	Bits [7:0]–48,–46, –44, –42	Subcarrier increment for Db component of SECAM. MSC_DB = int ((272/H_CLKO) * 2^{32} + 0.5)
MY[7:0]	Bits [7:0]–AC	Multiplication factor for Luma component. Controls adjustment of contrast.
NI_OUT	Bit 0–A2	0 = Interlaced analog video output. (DEFAULT) 1 = Noninterlaced analog video output. Odd (first) field is always transmitted.
OFFSET_RGB	Bit 1–32	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Standard RGB digital input. Range is 0 – 255 decimal. (DEFAULT) 1 = HDTV OFFSET RGB digital input. Range is 16 – 235 decimal.
OUT_MODE[1:0]	Bits [3:2]–D6	00 = Video[0] = Composite (CVBS), Video[1] = Luminance (Y), Video[2] = Chrominance (C), Video[3] = Luma_Delay (Y_DLY). Routing of Video [0] – [3] from DACs controlled with OUT_MUXx bit fields. (DEFAULT) 01 = Video[0–3] is CVBS_DLY/ Y/ C/ Y_DLY. Rarely used. 10 = Video[0–3] is V/ Y/ U/ CVBS. Consult the YCRCB 480i (YUV) Standard-Definition Component Video Outputs section for more programming detail. 11 = Video[0–3] is VGA (RGB/x), SCART (R/G/B/Composite), or HDTV output mode. Consult the SCART Output, VGA (RGB)-DAC Output, and HDTV Appendix E sections for more programming detail.
OUT_MUXA[1:0]	Bits [1:0]–CE	00 = Output Video[0] on DACA (DEFAULT = Composite [CVBS]) 01 = Output Video[1] on DACA 10 = Output Video[2] on DACA 11 = Output Video[3] on DACA
OUT_MUXB[1:0]	Bits [3:2]–CE	00 = Output Video[0] on DACB 01 = Output Video[1] on DACB (DEFAULT = Luminance (Y) 10 = Output Video[2] on DACB 11 = Output Video[3] on DACB
OUT_MUXC[1:0]	Bits [5:4]–CE	00 = Output Video[0] on DACC 01 = Output Video[1] on DACC 10 = Output Video[2] on DACC (DEFAULT = Chrominance) 11 = Output Video[3] on DACC
OUT_MUXD[1:0]	Bits [7:6]–CE	00 = Output Video[0] on DACD 01 = Output Video[1] on DACD 10 = Output Video[2] on DACD 11 = Output Video[3] on DACD (DEFAULT = Luma Delay [Y_DLY])
PAL_MD	Bit 5–A2	Video output switch bit after power-up. 0 = Disable phase alternation (NTSC and SECAM). (DEFAULT) 1 = Enable phase alternation (PAL).
PHASE_OFF[7:0]	Bits [7:0]–B6	Subcarrier phase offset. SCH Phase increased by 1.406 degrees per bit increment. This register is 2s complement in nature (DEFAULT = 00).

***Table 39. Programming Details for All Read/Write Registers** (15 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
PIX_DOUBLE	Bit 6–38	Low resolution pixel doubling bit. 0 = Encoder accepts each pixel input individually and processes it. (DEFAULT) 1 = Encoder replicates/copies each input pixel received. This bit is automatically set for autoconfiguration modes #12, #13, #41, and #45.
PIX_REVERSE	Bit 0–24	Reverse input pins in a bit-wide fashion. Functionally, it is as if the pinout of the PIX bus were flipped as follows. Note that this does not affect the location of test pin functionality. Current Pin → Re-mapped Function PIX[23] → PIX[0] PIX[22] → PIX[1] PIX[21] → PIX2] . → . . → . . → . PIX[1] → PIX[22]
PKFIL_SEL[1:0]	Bits [5:4]–D8	Text sharpening filter. Also referred to as the luma peaking filter selection. 00 = Bypass (DEFAULT) 01 = Filter 1 (1 dB gain) 10 = Filter 2 (2 dB gain) 11 = Filter 3 (3.5 dB gain)
PLL_32CLK	Bit 5–38	Use this bit primarily to support the 1024 x 768 resolution and additional 800 x 600 overscan options. For more details, review the 3:2 Clocking Mode section. 0 = Use PLL 3x pixel clock output. (DEFAULT) 1 = Use PLL generated 2x pixel clock to run the encoder and output timing section. Use PLL generated 3x pixel clock to run the flicker filter. The 3x pixel clock will be output from the CLKO pin during either state of this bit.
PLL_FRACT[15:0]	Bits [7:0]–9E, –9C	Fractional portion of PLL multiplier.
PLL_INPUT	Bit 1–3A	0 = PLL uses the crystal or oscillator between XTALIN and XTALOUT pins to generate the CLKO programmed frequency. (DEFAULT) 1 = PLL uses {CLKI / 2} as the reference for the PLL.
PLL_INT[5:0]	Bits [5:0]–A0	Integer portion of PLL multiplier.

***Table 39. Programming Details for All Read/Write Registers** (16 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
PLL_KEEP_ALIVE	Bit 4–30	0 = Normal operation. (DEFAULT) 1 = Keeps PLL enabled during the sleep mode. This bit is overwritten by DIS_PLL. If the PLL is used to provide a system clock, this bit keeps it functioning if the rest of the chip is slept through either the sleep pin or sleep bit. This bit has no affect if DIS_PLL is set.
PROG_SC	Bit 0–D8	SECAM subcarrier control bit. PROG_SC only has an effect when FM bit is set. 0 = SECAM subcarrier is generated on lines 23–310 and 336–623. (DEFAULT) 1 = SECAM subcarrier is generated on the active lines defined by V_BLANKO[7:0] and V_ACTIVEO[8:0].
RAND_EN	Bit 7–3A	0 = Disable DAC randomizer (DEFAULT) 1 = Enable DAC randomizer to change linearity and yield potentially better TV out quality
RASTER_SEL[1:0]	Bits [1:0]–2E	This bit is only effective when HDTV_EN = 1, and OUT_MODE[1:0] = 11 00 = Device does not generate trilevel sync automatically in HDTV output mode. Trilevel sync periods dictated by active HSYNC* input signal (as HIGHSYNC) and active VSYNC* input signal (as LOWSYNC). This selection must be used to support the 625p (576p) format. (DEFAULT) 01 = Trilevel sync, broad pulse, and timing generation for 480p format. 10 = Trilevel sync, broad pulse, and timing generation for 720p format. 11 = Trilevel sync, broad pulse, and timing generation for 1080i format.
REGFSCONV[5:0]	Bits [5:0]–58	Works in conjunction with FIL_4286INCR[7:0] to set gain on UV digital component. Review the SECAM output section for the correct equations.
Reserved	Various	Reserved for future software compatibility; set to 0 for normal operation.
RGB2YPRPB	Bit 6–2E	HDTV output switching bit. This bit is only effective when HDTV_EN = 1, OUT_MODE[1:0] = 11, RASTER_SEL[1:0] = nonzero, and IN_MODE[3:0] = a RGB input format. 0 = Digital RGB Input to HDTV RGB output. (DEFAULT) 1 = Digital RGB Input to HDTV YP_RP_B output.
RPR_SYNC_DIS	Bit 5–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Red/P_R output or bilevel sync on VGA R output. (DEFAULT) 1 = Disables trilevel sync on HDTV Red/P_R output or bilevel sync on VGA R output. This bit will have to be set manually for EIA-770.3 compliance.
SC_PATTERN	Bit 1–D8	SECAM phase sequence. SC_PATTERN only has an effect when FM bit is set. 0 = 0° 0° 180° 0° 0° 180° SECAM subcarrier phase sequence. (DEFAULT) 1 = 0° 0° 0° 180° 180° 180° SECAM subcarrier phase sequence.

Table 39. Programming Details for All Read/Write Registers *(17 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
SETUP	Bit 1–A2	0 = Setup off. The 7.5 IRE pedestal setup is disabled for active video lines (NTSC-J, PAL-B, PAL-D, PAL-G, PAL-H, PAL-I, PAL-Nc, and SECAM). 1 = Setup on. The 7.5 IRE pedestal setup is enabled for active video lines (NTSC-M, PAL-M, and PAL-N). (DEFAULT)
SLAVE	Bit 5–BA	Interface bit: Works in conjunction with EN_BLANKO, EN_DOT, and EN_OUT bits. Controls whether the interface will be timing Master or timing Slave. 0 = Configures encoder as the timing master. HSYNC* and VSYNC* will be transmitted as outputs when this bit or a combination of this bit and SLAVE pin is 0. 1 = Configures encoder as the timing slave (pseudo-master or slave interface). HSYNC* and VSYNC* will be received as inputs when this bit is 1. (DEFAULT)
SLEEP_EN	Bit 7–30	0 = Normal operation. (DEFAULT) 1 = Enables sleep state. Shuts down all internal clocks except the serial port interface clock. Disables all digital I/O pins except: SLEEP, ALTADDR, CLKI, CLKO, and XTALOUT. Disables the PLL. Turns off all DACs and VREF. SLEEP and RESET* pins are never disabled.
SRESET	Bit 7–BA	0 = Normal Operation. (DEFAULT) 1 = Setting this bit performs a software reset. All registers are reset to their default state, which is 640x480 in, NTSC out, autoconfiguration mode #0. This bit is automatically cleared.
SYNC_AMP[7:0]	Bits [7:0]–A4	Multiplication factor for controlling the analog sync amplitude. SYNC_AMP + 1 LSb (least significant bit) = +1.25 mV increase in the analog sync amplitude.
TIMING_RST	Bit 7–6C	0 = Normal Operation. (DEFAULT) 1 = Enable timing reset. Resets timing and pixel counters to 1 This bit is automatically cleared. The designer should wait a minimum of 1 ms, after the last register write before enabling TIMING_RST.
V_ACTIVEI[9:8] V_ACTIVEI[7:0]	Bits [3:2]–96 and Bits [7:0]–94	Number of active input lines.
V_ACTIVEO[8] V_ACTIVEO[7:0]	Bit 7–86 and Bits [7:0]–84	Number of active output lines/field.
V_BLANKI[7:0]	Bits [7:0]–92	Number of input lines between VSYNC* leading edge and first active line.
V_BLANKO[7:0]	Bits [7:0]–82	Line number of first active output line (number of blank lines + 1).
V_LINESI[10] V_LINESI[9:8] V_LINESI[7:0]	Bit 1–38, Bits [1:0]–96, Bits [7:0]–90	Number of vertical input lines. This register value must match the graphic controller's VTOTAL register for a new overscan ratio.
V_SCALE[13:8] V_SCALE[7:0]	Bits [5:0]–9A and Bits [7:0]–98	Vertical scaling coefficient. VSR = V_ACTIVEI / (ALO * [1 – VOC]) V_SCALE[13:0] = (int) ((VSR – 1) * 2^{12})

***Table 39. Programming Details for All Read/Write Registers** (18 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
VBLANKDLY	Bit 4–8E	0 = Normal operation. (DEFAULT) 1 = The effective vertical blanking value in the second field is V_BLANKI+1. Commonly used in CCIR601 input. No effect if 0.
VSYNC_DUR	Bit 3–A2	0 = Generates 2.5-line VSYNC analog output (found in equalization and serration pulse region). Common for most PAL and SECAM formats. 1 = Generates 3 line VSYNC analog output (found in equalization and serration pulse region). Common for all NTSC, PAL-N, PAL-M, and PAL-60 formats. (DEFAULT)
VSYNCI	Bit 4–C6	0 = CX25898/9 transmits or receives active digital low VSYNC*. (DEFAULT) 1 = CX25898/9 transmits or receives active digital high VSYNC*.
VSYNWIDTH[2:0]	Bits [2:0]–74	Controls the width of the VSYNC* output pulse. Denotes the number of lines the VSYNC* digital signal remains low on field transitions. Value will be hexadecimal and its units are in terms of lines. A value of 0 is a disallowed condition. The acceptable range is 1 line to (2^3 –1) lines. The default value is 1. Never set to 0. This register is only effective in master interface.
WSSDAT[20:1]	Bits [7:0]–64, –62, and Bits [3:0]–60	Wide screen signaling (WSS) data bits. Review WSS section for more details.
WSSINC[19:0]	Bits [3:0]–6A and Bits [7:0]–68,–66	WSS DTO increment bits. Review WSS section for more details.
XDSSEL[3:0]	Bits [7:4]–5E	Line position of Extended Data Services (XDS) Content. Controls which line contains Extended Data Services data. Each line enable is independent of the other. 0001 = Extended Data Services on line 282 (525-line) and line 333 (625-line). 0010 = Extended Data Services on line 283 (525-line) and line 334 (625-line). 0100 = Extended Data Services on line 284 (525-line) and line 335 (625-line). (DEFAULT) 1000 = Extended Data Services on line 285 (525-line) and line 336 (625-line).
XTL_BFO_DIS	Bit 5–30	On power-up, a 50% duty cycle buffered output will be transmitted at the frequency found between the XTALIN and XTALOUT ports from the XTAL_BFO pin #3. 0 = Enable buffer crystal clock output. [DEFAULT] 1 = Disable buffer crystal clock output.
Reserved	Bit 6–30	
Y_ALTFF[1:0]	Bits [1:0]–34	Luma alternate flicker filter selection. This bit will only have an effect when ADPT_FF is set. Y_ALTFF should always be programmed to a value greater than or equal to F_SELY. 00 = 5 line (DEFAULT) 01 = 2 line 10 = 3 line 11 = 4 line

***Table 39. Programming Details for All Read/Write Registers** (19 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
Y_OFF[7:0]	Bits [7:0]–5A	Brightness control. This is the luminance level offset. Expressed as a 2s complement number. (DEFAULT = 0x00) The luminance level offset is referenced from black, and can be adjusted from -22.31 IRE (below black) to +22.14 IRE (above black). Active video will be added to the offset level. Y_OFF is a 2s complement number, such that 0x00 = 0 IRE offset 0x7 is +22.14 IRE offset and 0x8 is –22.31 IRE offset. 1 lsb = 1.25 mV or 175 IRE of adjustment.
Y_THRESH[2:0]	Bits [2:0]–36	Controls the sensitivity or limit of turning on the alternate flicker filter for luma in adaptive flicker filter mode. (DEFAULT = 000)
YATTENUATE[2:0]	Bits [2:0]–CA	Works in conjunction with register MY for contrast control. This bit field adjusts Luma Attenuation in discrete steps. 000 = 1.0 gain (no attenuation) (DEFAULT) 001 = 15/16 gain 010 = 7/8 gain 011 = 3/4 gain 100 = 1/2 gain 101 = 1/4 gain 110 = 1/8 gain 111 = 0 gain (Force Luma to 0)
YC2YP	Bits 7–26	0 = Normal operation (DEFAULT) 1 = Converts YCrCb digital color space to YPrPb color space. This bit should only be set when outputting HDTV analog YP_RP_B based on a YCrCb input format.
YCORING[2:0]	Bits [5:3]–CA	Luma Coring. These bits control the black level coring limit. Values below the YCORING[2:0] limits that follow are automatically clamped to pure black by the encoder. 000 = Bypass (DEFAULT) 001 = 1/128 of range 010 = 1/64 of range 011 = 1/32 of range 100 = 1/16 of range 101 = 1/8 of range 110 = 1/4 of range 111 = Reserved

Table 39. Programming Details for All Read/Write Registers *(20 of 20)*

Bit/Register Names	Bit Location	Bit/Register Definition
YLPF[1:0]	Bits [5:4]–96	Luma Post-Flicker Filter/Scaler Horizontal Low-Pass Filter: 00 = Bypass (DEFAULT) 01 = Luma Horizontal LPF1 setting 10 = Luma Horizontal LPF2 setting 11 = Luma Horizontal LPF3 setting
YSELECT	Bit 6–36	This bit will only have an effect when ADPT_FF is set. 0 = Use the C_THRESH value to determine the threshold for turning on the alternate flicker filter setting for chrominance. (DEFAULT) 1 = Use the Y_THRESH value to determine the threshold for turning on the alternate flicker filter setting for chrominance. Both chroma and luma digital data is automatically processed with their alternate flicker filter settings when the Y_THRESH limit is exceeded.

3 Parametric Information

3.1 DC Electrical Parameters

DC electrical parameters are defined in Tables 40 through 42.

Table 40. DC Recommended Operating Condition

Parameter	Symbol	Min	Typical	Max[2]	Units
Power Supply	VAA_BG, VAA_DAC, VAA_OSC,	3.15	3.30	3.45	V
VDD Core Supply	VDD	1.24	1.2	1.36	V
Serial Input Supply	VDD_SIO	3.15	3.30	3.45	V
Low-Voltage Supply (for interface to 2.5 V master)[1]	VDDO	2.38	2.5	2.63	V
Low-Voltage Supply (for interface to 1.8 V master)[1]	VDDO	1.71	1.80	1.89	V
Low-Voltage Supply (for interface to 1.5 V master)[1]	VDDO	1.425	1.50	1.575	V
Low-Voltage Supply (for interface to 1.3 V master)[1]	VDDO	1.235	1.30	1.365	V
Low-Voltage Supply (for interface to 1.1 V master)[1]	VDDO	1.045	1.10	1.155	V
Voltage Supply (for interface to 3.3 V master)	VDDO	3.15	3.30	3.45	V
Ambient Operating Temperature	T_A	0	—	70	°C
Total DAC Terminated Load	R_{TERM}	37.1	37.5	37.9	Ω
Nominal RSET (series resistor FSADJUST pin to GND)	R_{SET}	398	402	406	Ω

FOOTNOTE:

(1) Any low-voltage interface from 1.1 V to 3.3 V can be accommodated by supplying the VDDO pins with the corresponding lower voltage supply ± 5%.

(2) Stresses above those listed in this column can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 41. DC Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max[2]	Units
Voltage on Any Signal Pin [1]	—	GND – 0.5		VDDO + 0.5[3]	V
Analog Output Short Circuit Duration to Any Power Supply or Common Ground	I_{SC}	—	—	Unlimited	Sec
Storage Temperature	T_S	–65	—	+150	°C
Junction Temperature	T_J	—	—	+125	°C
Peak Reflow Temperature	T_{VSOL}	—	—	260	°C
Thermal Resistance of Package	θ_{JA}	—	33	240	°C/W

FOOTNOTE:

(1) This device employs high-impedance CMOS circuitry on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.

(2) Stresses above those listed in this column can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

(3) VDDx refers to VAA_DAC, VDDO, VDD_SIO, VAA_OSC, VDD, VAA_BG.

Table 42. DC Characteristics for CX25898/9

Parameter	Symbol	Min	Typical	Max	Units
Video D/A Converter Resolution	—	10	10	10	Bits
Output Current-DAC Code 1023 (Iout full scale)	—	—	34.13	—	mA
Output Voltage-DAC Code 1023	—	—	1.28	—	V
Video Level Error (nominal resistors)	—	—	—	5	%
Output Capacitance (of DAC output)	—	—	22	—	pF
Input High Voltage @ 3.3 V (normal operation)	VIH	2.4	—	VDDO + 0.5	V
Input High Voltage @ 2.5 V (low-voltage pins)	VIH	1.75	—	VDDO + 0.5	V
Input High Voltage @ 1.5 V (low-voltage pins only)	VIH	1.05	—	VDDO + 0.5	V
Input High Voltage @ 1.1 V (low-voltage pins only)	VIH	0.77	—	VDDO + 0.5	V
Input Low Voltage @ 3.3 V (normal operation)	VIL	GND – 0.5	—	0.8	V
Input Low Voltage @ 2.5 V (low-voltage pins only)	VIL	GND – 0.5	—	0.6	V
Input Low Voltage @ 1.5 V (low-voltage pins only)	VIL	GND – 0.5	—	0.45	V
Input Low Voltage @ 1.1 V (low-voltage pins only)	VIL	GND – 0.5	—	0.33	V
Input High Current (Vin = 2.4 V)	IIH	—	—	1	µA
Input Low Current (Vin = 0.4 V)	IIL	—	—	–1	µA
Input Capacitance (f =1 MHz, Vin = 2.4 V)	CIN	—	7	—	pF
Input High Voltage (SIC, SID)	VIH	0.7 * VDD	—	VDD_SIO + 0.5	V
Input Low Voltage (SIC, SID)	VIL	GND – 0.5	—	0.3 * VDD_SIO	V
Output High Voltage @ 3.3 V (IOH = –400 µA)	VOH	2.4	—	VDDO	V
Output Low Voltage 3.3 V (IOL = 3.2 mA)	VOL	GND	—	0.4	V
Output High Voltage @ 1.1 V (IOH = –400 µA)	VOH	VDDO – 0.2	—	VDDO	V
Input Low Voltage @ 1.1 V (IOL = 3.2 mA)	VOL	GND	—	GND + 0.2	V
Three-State Current	IOZ	—	—	50	µA
Output Capacitance	CDOUT	—	10	—	pF

GENERAL NOTE:

1. The above parameters are guaranteed over the full temperature range (0 °C to 70 °C), temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 3.3 V.

3.2 AC Electrical Parameters

AC electrical parameters are defined in Table 43.

The AC characteristics for the CX25898/9 were derived under the following normal test conditions. DAC output load ≤ 75 pF. HSYNC*, VSYNC*, BLANK*, and FIELD output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 3.3 V.

Table 43. AC Characteristics for CX25898/9 *(1 of 4)*

Parameter			Symbol	Min	Typical	Max	Units
	EIA/TIA 250C Ref	CCIR 567					
Hue Accuracy	—	—	—	—	–0.8	—	deg p-p
Chroma Amplitude Accuracy	—	—	—	—	–0.6	—	% p-p
Chroma AM Noise (all fields)	1 MHz Red Field	—	—	—	–60.08	—	dB rms
Chroma PM Noise (all fields)	1 MHz Red Field	—	—	—	–57.63	—	dB rms
Differential Gain	6.2.2.1	C3.4.1.3	—	—	0.45	—	% p-p
Differential Phase	6.2.2.2	C3.4.1.4	—	—	0.72	—	deg p-p
RMS SNR (unweighted 100 IRE Y ramp tilt correct)	6.3.1	—	—	—	–68.87	—	dB rms
Peak Periodic SNR @ 3.58 MHz	6.3.2	—	—	—	–94.4	—	dB p-p
100 IRE Multiburst	6.1.1	—	—	—	100	—	IRE
Multiburst @ 0.50 MHz	—	—	—	—	0	—	dB
Multiburst @ 1.0 MHz	—	—	—	—	–0.03	—	dB
Multiburst @ 2.0 MHz	—	—	—	—	–0.13	—	dB
Multiburst @ 3.0 MHz	—	—	—	—	-0.26	—	dB
Multiburst @ 4.0 MHz	—	—	—	—	–0.4	—	dB
Multiburst @ 5.75 MHz	—	—	—	—	–1.51	—	dB
Chroma/Luma Gain Ineq	6.1.2.2	C3.5.3.1	—	—	96.93	—	%
Chroma/Luma Delay Ineq	6.1.2	C3.5.3.2	—	—	–1.83	—	ns
Short Time Distortion 100 IRE/ PIXEL (rising edge)	6.1.6	—	—	—	0.5	—	%

Table 43. AC Characteristics for CX25898/9 *(2 of 4)*

Parameter			Symbol	Min	Typical	Max	Units
Short Time Distortion 100 IRE/ PIXEL (falling edge)	6.1.6	—	—	—	0.5	—	%
Luminance Nonlinearity	6.2.1	—	—	—	1.26	—	% p-p
Chroma/Luma Intermod	6.2.3	—	—	—	–0.01	—	%
Chroma Nonlinear Gain	6.2.4.1	—	—	—	–2.64	—	%
Chroma Nonlinear Phase	6.2.4.2		—	—	–0.09	—	deg
	EIA/TIA 250C Ref	CCIR 567					
PSRR (Power Supply Ripple Rejection Ratio) of DAC output (full scale)	—	—	—	—	30	—	dB
Pixel/Control Setup Time	—	—	1	3	—	—	ns
Pixel/Control Hold Time	—	—	2	0	—	—	ns
Control Output Delay Time	—	—	3	—	—	12.5	ns
Control Output Hold Time	—	—	4	—	—	—	ns
CLKI/O Frequency (standard mode)	—	—	—	—	—	—	MHz
CLKI/O Pulse Width Low Duty Cycle	—	—	—	40	50	60	%
CLKI/O Pulse Width High Duty Cycle	—	—	—	40	50	60	%
CLKO to CLKI Delay	—	—	7	—	—	0.8	CLKO cycles

Table 43. AC Characteristics for CX25898/9 *(3 of 4)*

Parameter	Symbol	Min	Typical	Max	Units
HDTV Output Timing Characteristics: 1080i (Figure 66)					
Low-Sync Width	a	—	576	—	ns
Start of Line to End of Active Video	b	—	28.4	—	µs
High Sync Width	χ	—	608	—	ns
Rising Edge of Sync to Start of Broad Pulse	δ	—	1.78		µs
Start of Line to Start of Active Video	ε	—	2.66	—	µs
Sync Rise Time	ϕ	—	40	—	µs
Total Line Time	—	—	29.68	—	µs
Active Line Time	—	—	25.7	—	µs
HDTV Output Timing Characteristics: 720p (see Figure 66)					
Low-Sync Width	a	—	576	—	µs
Start of Line to End of Active Video	b	—	28.4	—	µs
High Sync Width	c	—	608	—	µs
Rising Edge of Sync to Start of Broad Pulse	d	—	1.78	—	µs
Start of Line to Start of Active Video	e	—	—	—	µs
Sync Rise Time	—	—	—	—	ns
Total Line Time	—	—	29.68	—	µs
Active Line Time	—	—	25.7	—	µs
HDTV Output Timing Characteristics: 576p (625p) (see Figure 67)					
Pulse Width Between Consecutive Equalization-type Pulses	a	—	29.68	—	µs
Total Line Time	b	—	32	—	µs
Analog Sync Width	c	—	2.336	—	µs
Active Line Time	d	—	26.64	—	µs
Sync Fall Time	α	—	100	—	ns
Start of Line to End of Active Video	β	—	31.917	—	µs
Start of Line to Start of Active Video	χ	—	5.25	—	µs
End of Active Video to Next Sync/start of Next Line	δ	—	0.75	—	µs

Table 43. AC Characteristics for CX25898/9 *(4 of 4)*

Parameter	Symbol	Min	Typical	Max	Units
Bilevel Serration-type Pulse Period During VBI	W	—	5H	—	—
Bilevel Vertical Synchronizing Pulse Period During VBI	X	—	5H	—	—
Bilevel Serration-type Pulse Period During VBI Following Equalization-Type Pulses	Y	—	39H	—	—
Total VBI Time	Z	—	1.56	—	ms
HDTV Output Timing Characteristics: 480p (see Figures 68 and 69)					
Pulse Width Between Consecutive Equalization-Type Pulses	a	—	29.6	—	µs
Total Line Time	b	—	31.8	—	µs
Analog Sync Width	c	—	2.346	—	µs
Active Line Time	d	—	26.48	—	µs
Sync Fall Time	α	—	72	—	ns
Start of Line to End of Active Video	β	—	31.2	—	µs
Start of Line to Start of Active Video	χ	—	4.68	—	µs
End of Active Video to Next Sync/start of Next Line	δ	—	0.6	—	µs
Bilevel Serration-type Pulse Period During VBI	W	—	6H	—	—
Bilevel Equalization-Type Pulse Period During VBI	X	—	6H	—	—
Bilevel Serration-type Pulse Period During VBI Following Equalization-Type Pulses	Y	—	30H	—	—
Total VBI Time	Z	—	1.336	—	ms

3.3 Power Consumption Results

Table 44 contains the power consumption numbers of the CX25898/9 under different operating conditions.

Table 44. CX25898/9 Operating Current, Operating Voltage, and Power-Related Results under Different Testing Conditions

Normal Operation = DACA, DACB, DACC, DACD ON)	Tot al Power (W) @3.3 V
640x480 NTSC (mode0)	0.5932
HDTV (720p/1080i)	0.6304

GENERAL NOTE:
1. Results obtained in this table tied all analog supply pins of CX25898/9 to 3.3 V.
2. Results obtained in this table tied all digital supply pins of CX25898/9 to 3.3 V.
3. CX25898/9 used 3.3 V peak-to-peak I/O levels to obtain these results.
4. CX25898/9 core voltage was 1.26 V.

3.4 Timing Diagrams

Figures 57 through 68 provide timing details and diagrams for important CX25898/9 digital input/output signals and analog video outputs.

Figure 57. Timing Details for All Interfaces

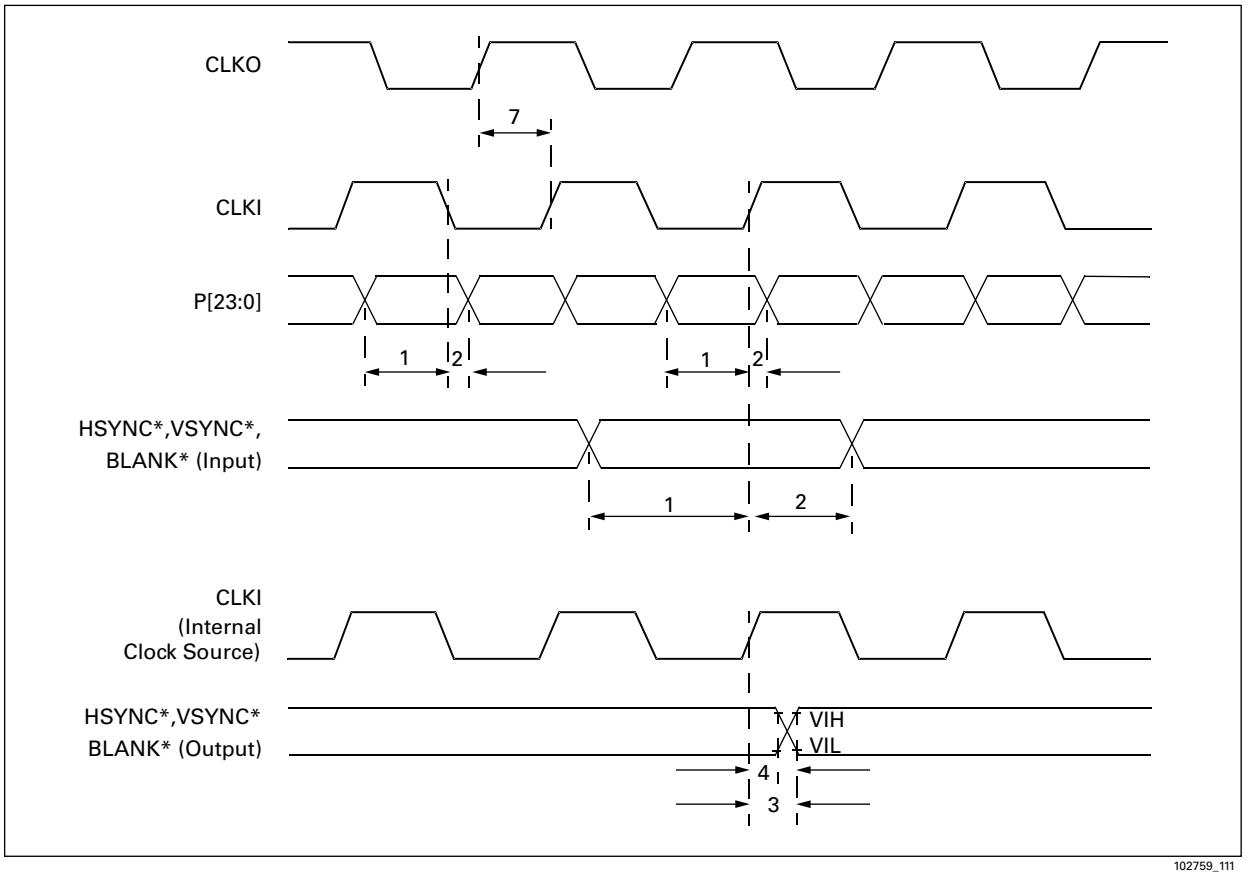


Figure 58. Master Interface Timing Relationship/Noninterlaced RGB/YCrCb Input

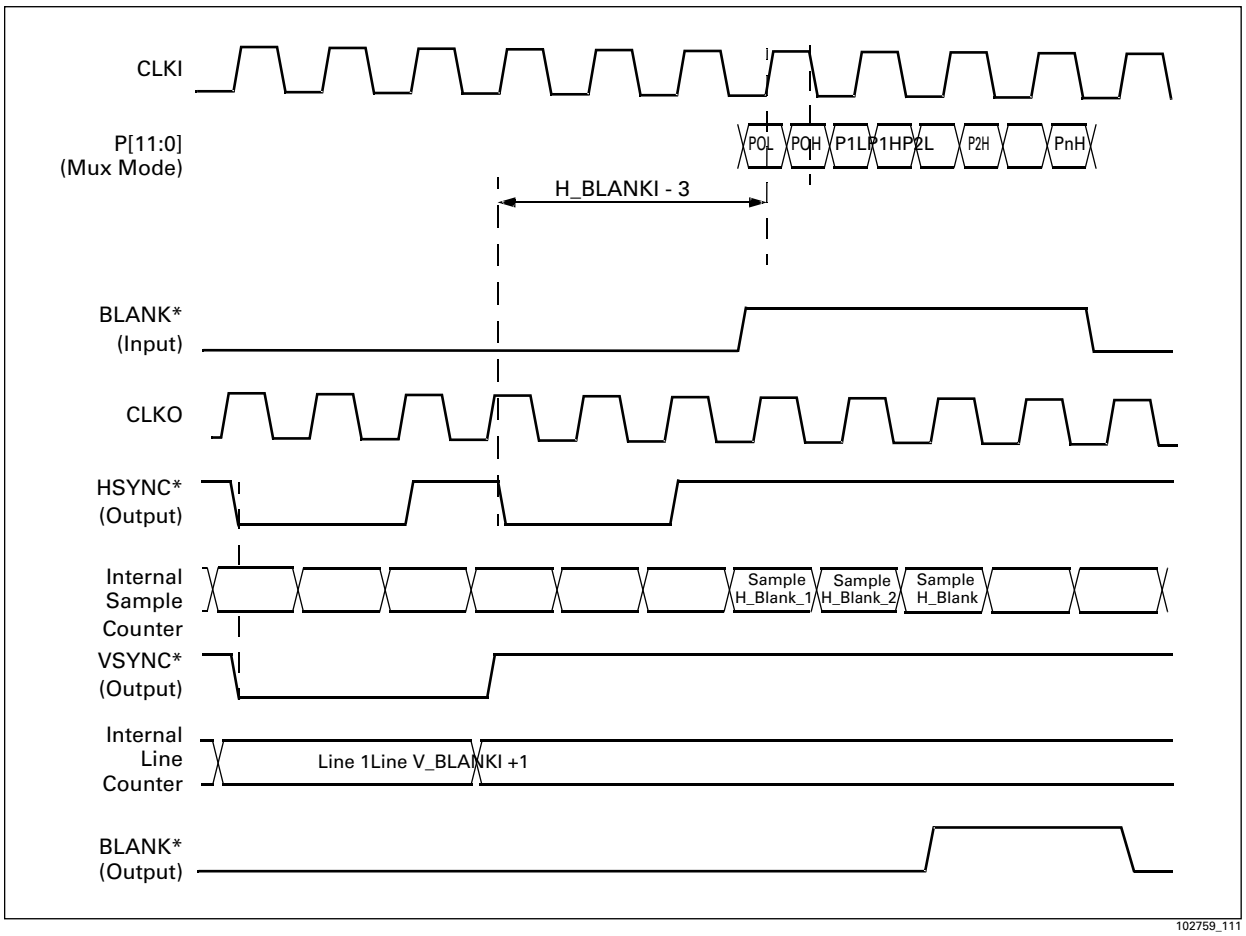
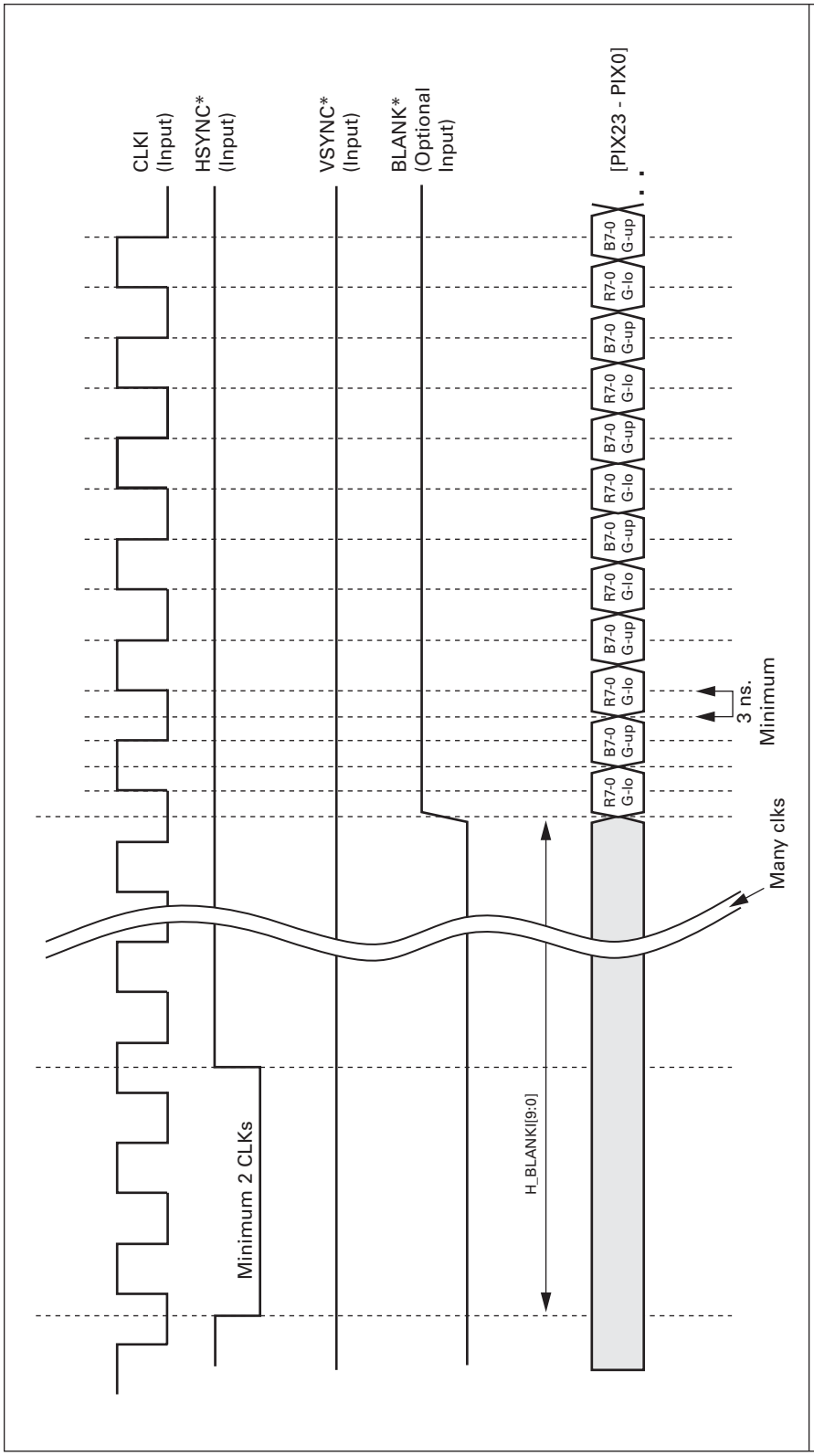


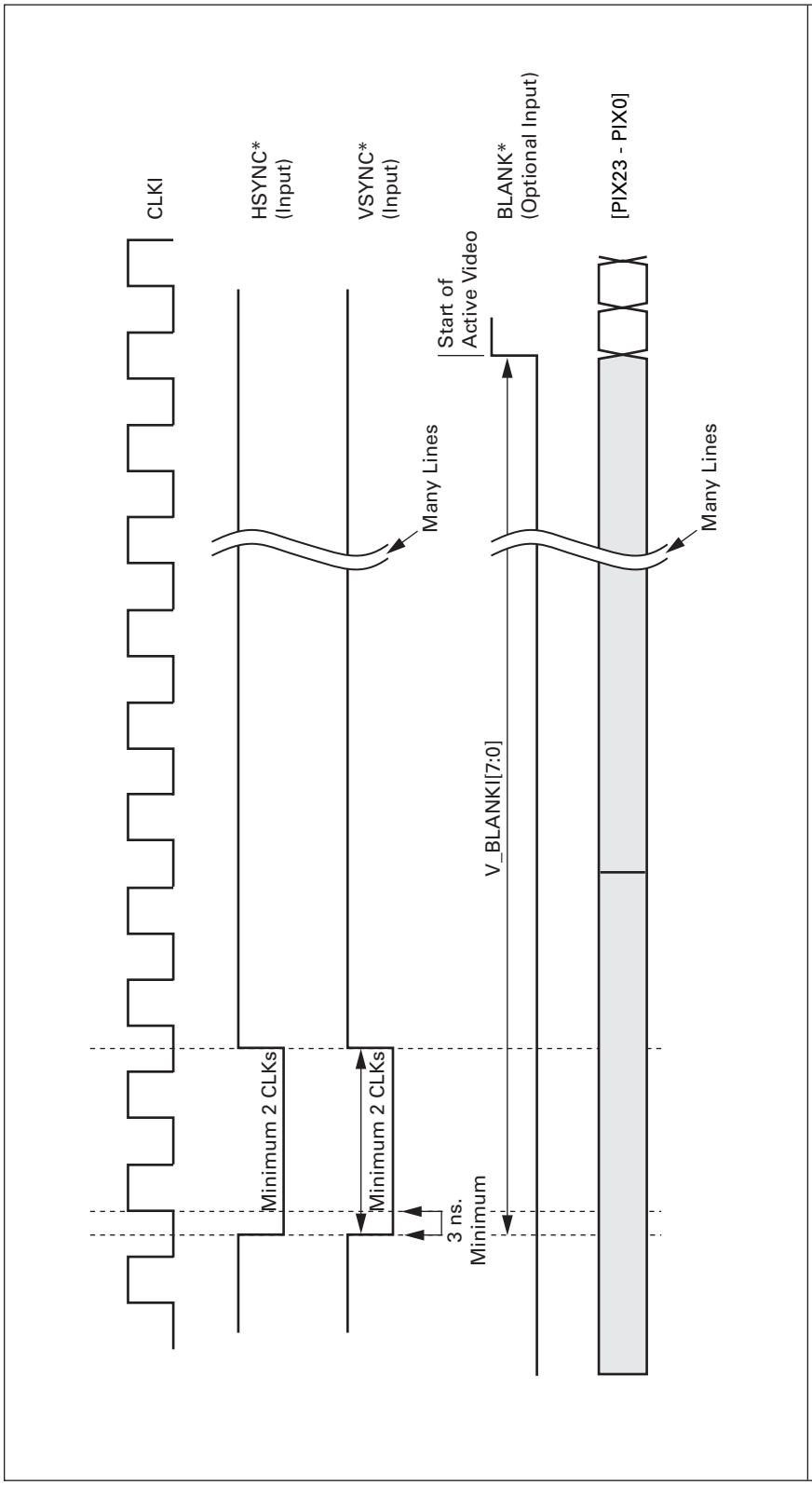
Figure 59. Pseudo-Master Interface Timing Relationship—Active Line/Noninterlaced RGB Input



GENERAL NOTE:

1. The leading edge pixel data (R pixel + G4, G3, G2, and G0 in the 24-bit RGB multiplexed case) and trailing edge pixel data (B pixel + G7, G6, G5, and G1) is clocked in on the rising and falling edge of CLKI, respectively.
2. The CX25898/9's HSYNCI and VSYNCI bits (register 0x06) must be set to 0 (=DEFAULT) in these timing diagrams. This configures the CX25898/9 to check for active low signals on the HSYNC* and VSYNC* pins from the graphics controller.
3. The {R[7:0], G4, G3, G2, and G0} - {B[7:0], G7, G6, G5, and G1} sequence begins with rising edge of BLANK* or the H_BLANKI[9:0] pixel count.
4. The clock frequency (i.e., CLKI) transmitted by the graphics controller must not deviate 25 PPM from the CLKO frequency sent by the CX25898/9. The CX25898/9 is the timing slave device to the Graphics Controller in pseudo-master interface.
5. 24-bit RGB multiplexed input format is illustrated in this diagram. It is assumed CX25898/9's IN_MODE[3:0] bits = 0000.

Figure 60. Pseudo-Master Timing Relationship Blank Line/Noninterlaced RGB/YCrCb Input



GENERAL NOTE:

1. For noninterlaced data transmission, to start each frame, the leading edge of HSYNC* and the leading edge of VSYNC* must be coincident (within 1 CLKI clock cycle). The location of these signals' respective trailing edges is not important relative to each other.
2. The duration of the HSYNC* pulse MUST be at least 2 complete CLKI cycles. The duration of the VSYNC* pulse MUST be a minimum of 2 CLKI cycles as well. It is acceptable for the HSYNC* to remain low for longer than 2 CLKI cycles but the signal's rising edge must be received by the CX25898/9 at least 1 pixel before the next HSYNC* falling edge which denotes the start of the next line. Likewise, VSYNC* can stay low for much longer than 2 CLKI cycles but the signal's rising edge must be received by the CX874/875 at least 1 complete line before the next VSYNC* falling edge which denotes the start of the next frame.
3. If a BLANK* signal is not used as part of the physical interface to a graphics controller, then the CX25898/9's H_BLANK[9:0] and V_BLANKI[7:0] registers must be programmed with values equivalent to the correct amount of horizontal pixel blanking and vertical line blanking from the master.

Figure 61. Slave Interface Timing Relationship/Noninterlaced RGB/YCrCb Input

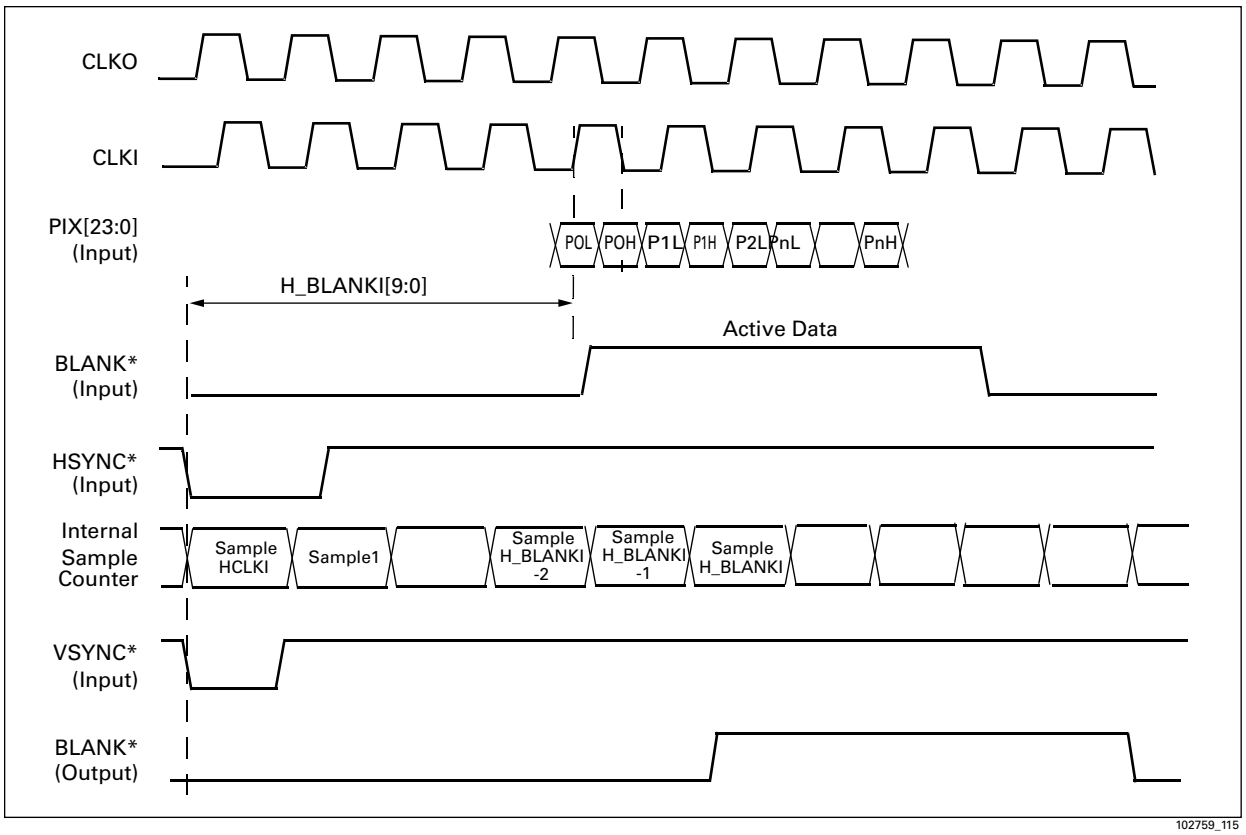
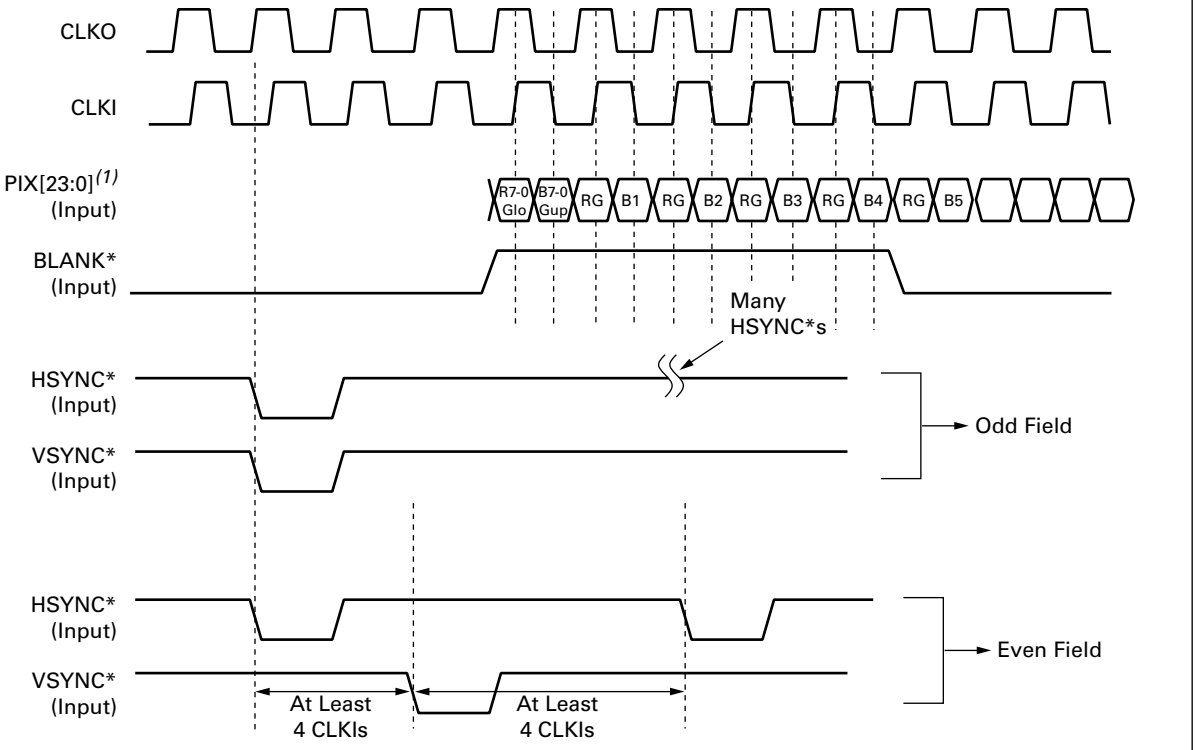


Figure 62. Slave Interface Timing Relationship/Interlaced Multiplexed RGB Input (FLD_MODE = 10—Default)



GENERAL NOTE:

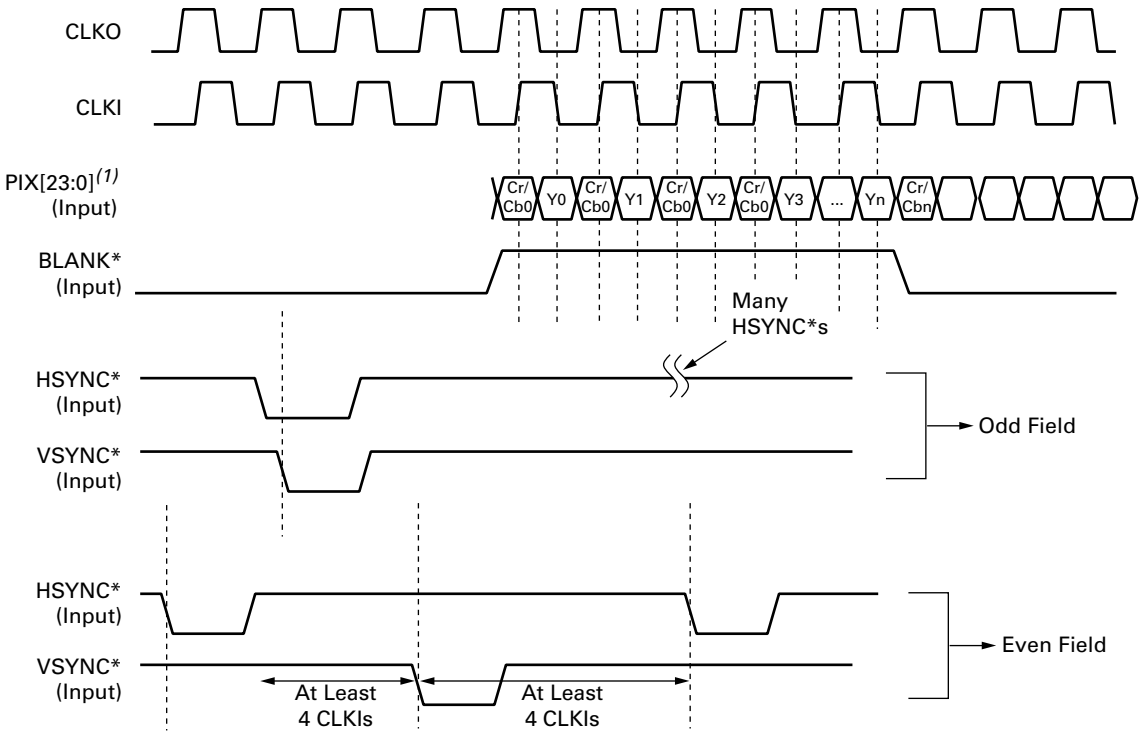
1. The CX25898/9's DIV2 bit must be set.
2. FLD_MODE[1:0] is defined in Table 41.

FOOTNOTE:

(1) IN_MODE[3:0] = 0000, shown in the figure. IN_MODE[3:0] = 0010, 0001, and 1000, adheres to the same timing, but pixel data will be latched differently.

102759_116

Figure 63. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 01)



GENERAL NOTE:

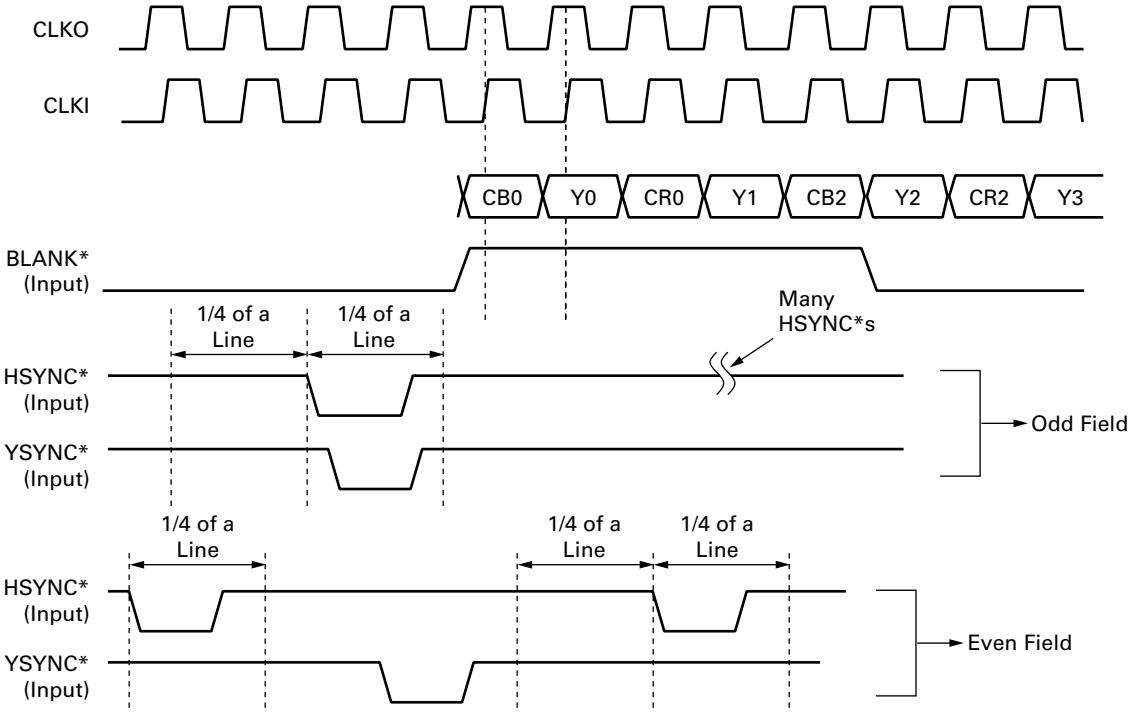
1. The CX25898/9's DIV2 bit must be set.
2. FLD_MODE[1:0] defined in Table 41.

FOOTNOTE:

(1) IN_MODE[3:0] = 0101 and IN_MODE[3:0] = 0110, shown in the figure. IN_MODE[3:0] = 1100 and 0100, adheres to the same timing, but pixel data will be latched differently.

102759_117

Figure 64. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 00)



GENERAL NOTE:

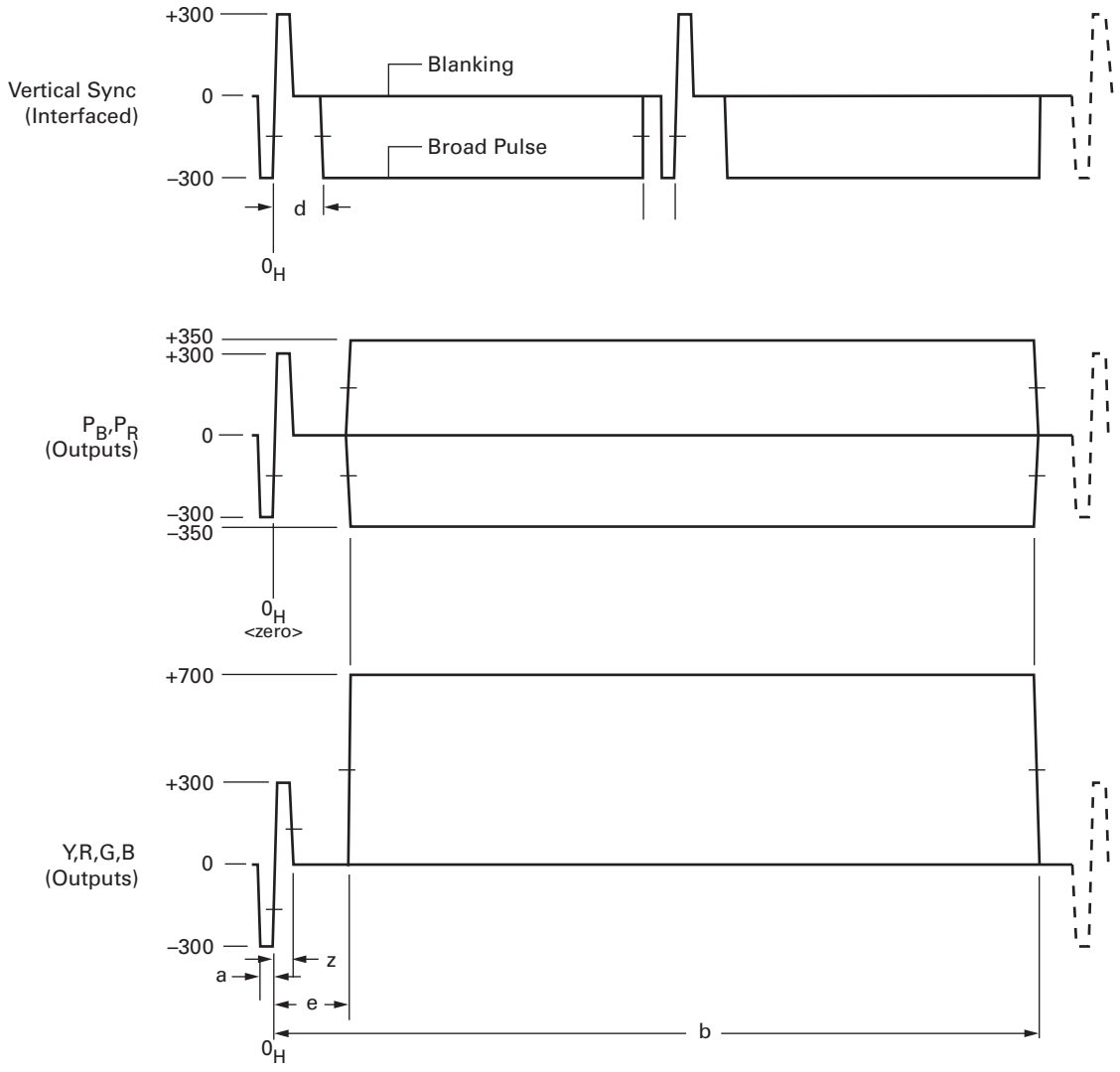
1. The CX25898/9's DIV2 bit must be set.
2. FLD_MODE[1:0] defined in Table 41.

FOOTNOTE:

(1) IN_MODE[3:0] = 0101 and IN_MODE[3:0] = 0110, shown in the figure. IN_MODE[3:0] = 1100 and 0100 adheres to the same timing, but pixel data will be latched differently.

102759_118

Figure 65. HDTV Output Horizontal Timing Details: 1080i

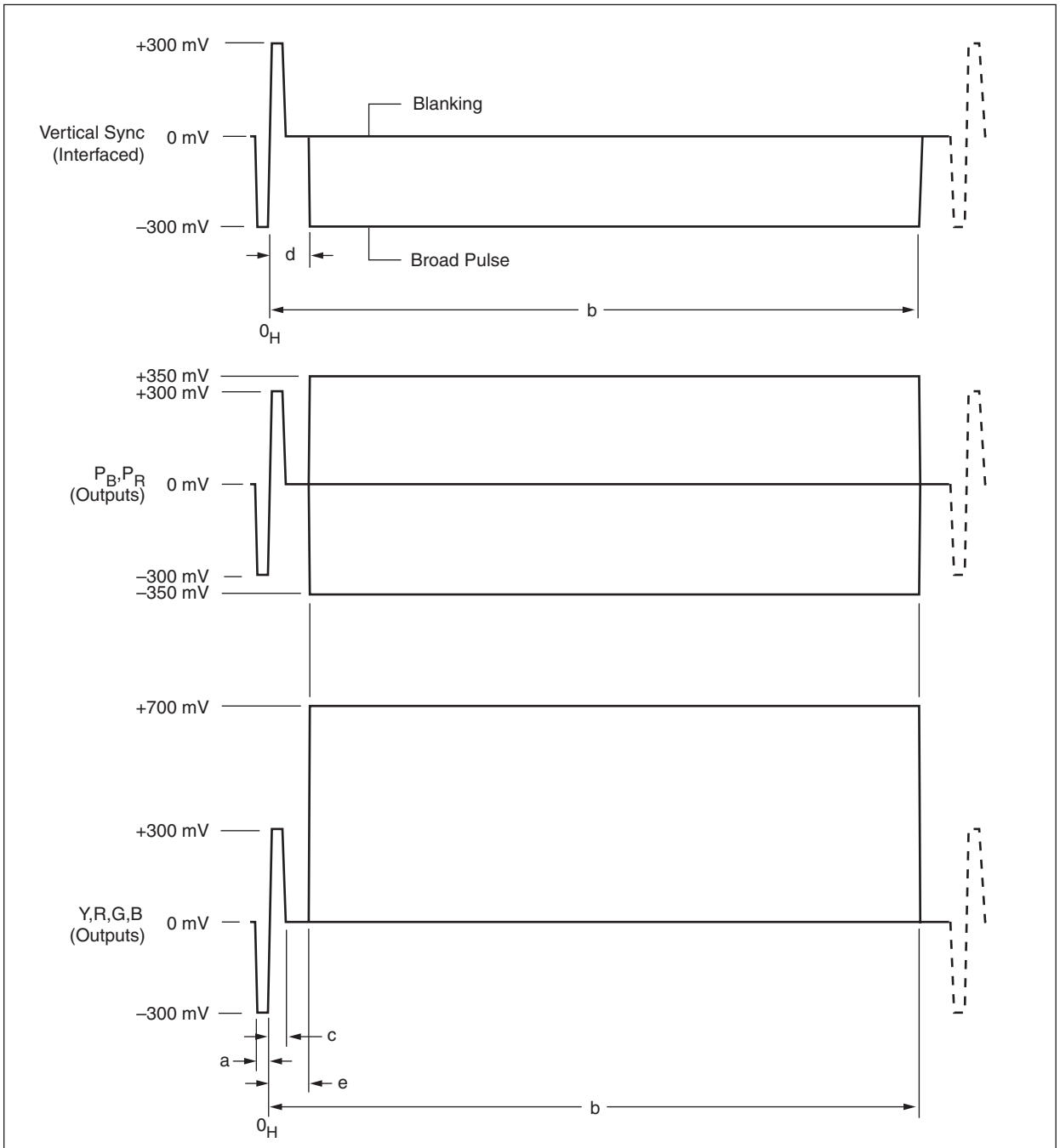


GENERAL NOTE:

1. Values for a, b, c, d, e, and s are given in Table 50.
2. Sync rise time (s) is not shown here.
3. Amplitudes are expressed in mV.

102759_119

Figure 66. HDTV Output Horizontal Timing Details: 720p

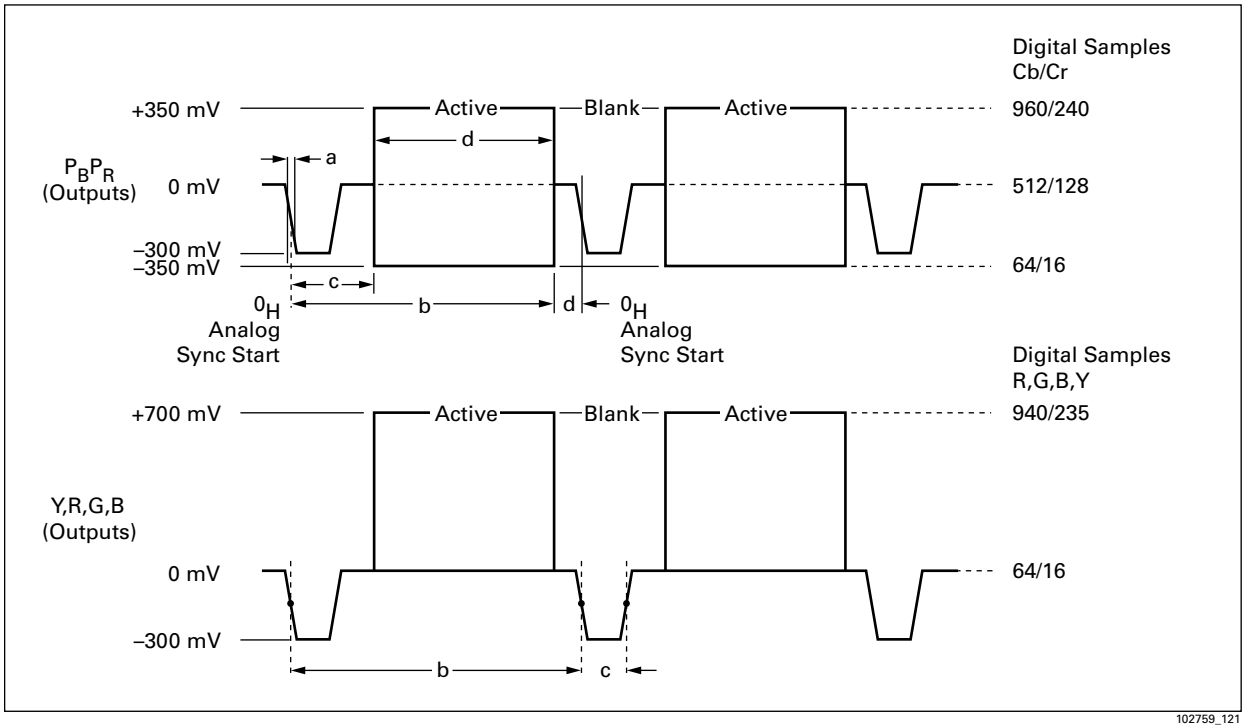


GENERAL NOTE:

1. Values for a, b, c, d, and e are given in Table 50.
2. Sync rise time is not shown here.
3. Amplitudes are expressed in mV.

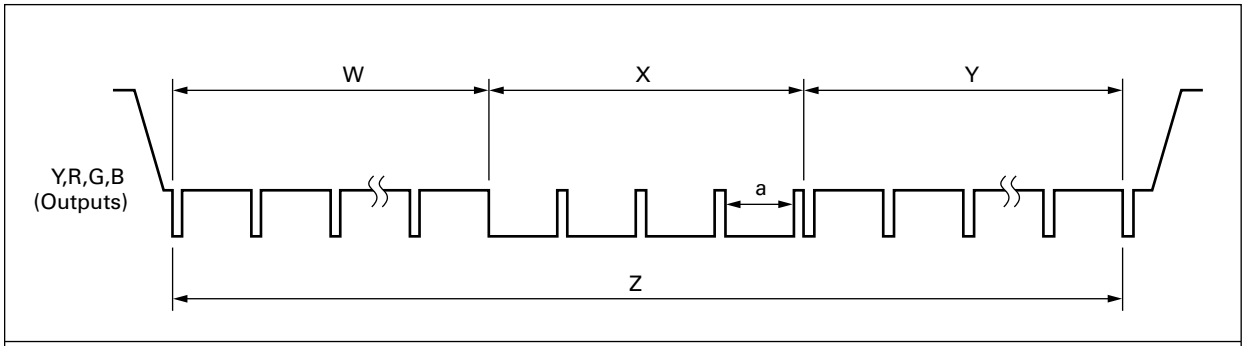
102759_120

Figure 67. HDTV Output Horizontal Timing Details: 480p



102759_121

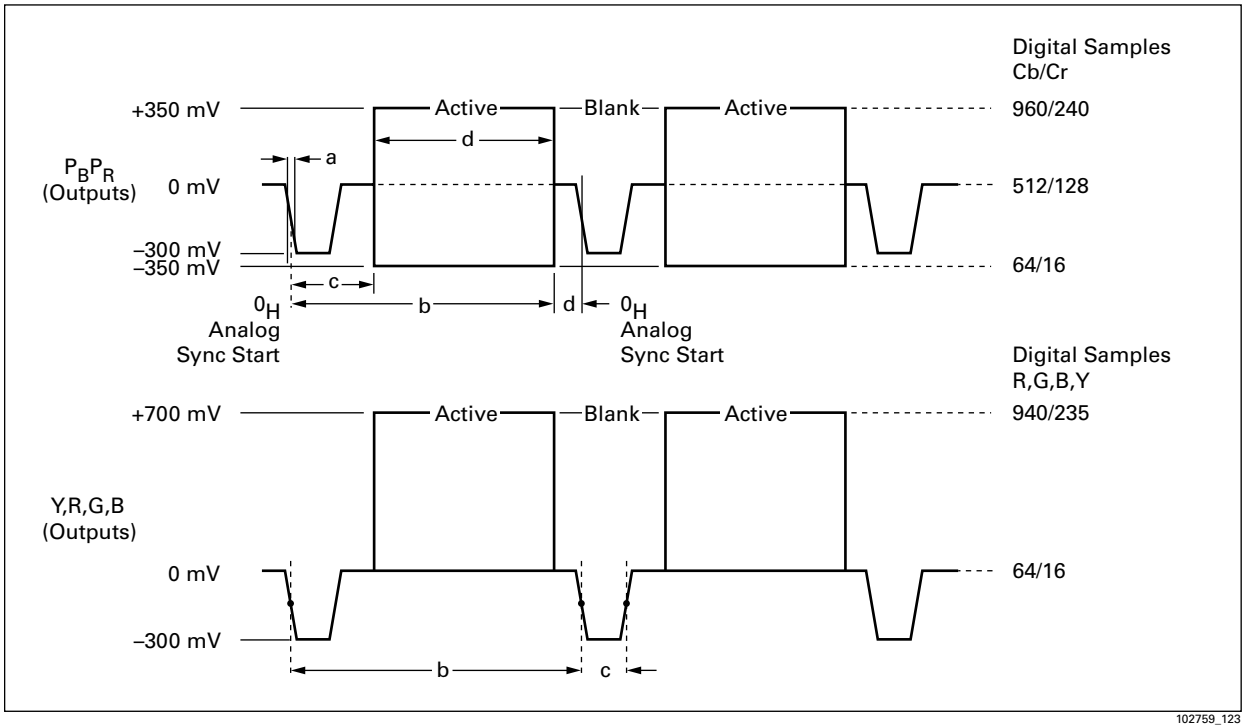
Figure 68. HDTV Output Vertical Timing Details: 480p



GENERAL NOTE: Values for α, β, χ, δ, α, β, χ, δ, W, X, Y, and Z are given in Table 50.

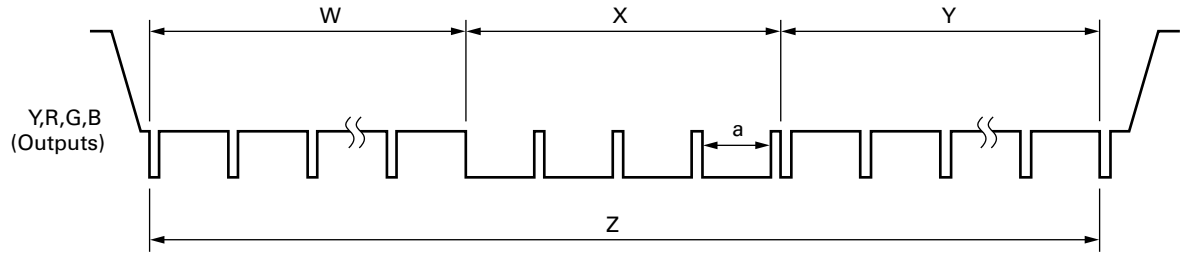
102759_122

Figure 69. HDTV Output Horizontal Timing Details: 576p (625p)



102759_123

Figure 70. HDTV Output Vertical Timing Details: (576p (625p)



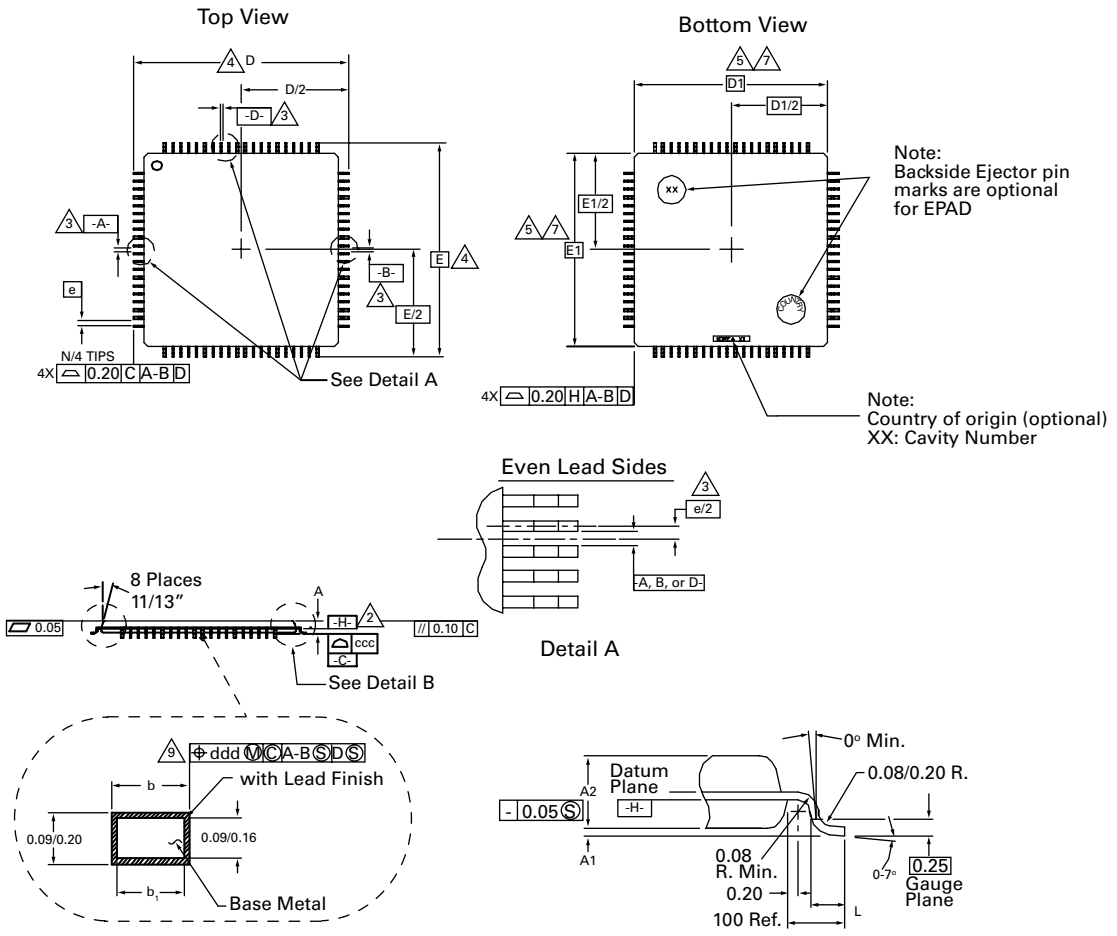
GENERAL NOTE: Values for a, b, c, d, α, β, χ, δ, W, X, Y, and Z are given in Table 48.

102750_124

3.5 Mechanical Specifications

Figure 71 shows the 80-pin TQFP for CX25898/9.

Figure 71. 80-Pin TQFP Package Diagram



Notes:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. N is the total number of terminals.
7. These dimensions to be determined at datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimensions b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material conditions. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 registration MS-026, variation add.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.

Symbol	JEDEC Variation All Dimensions in Millimeters			
	Add			Note
	Minimum	Nominal	Maximum	
A			1.20	
A_1	0.05		0.15	13
A_2	0.95	1.00	1.05	
D_1		14.00 BSC.		4
D		12.00 BSC.		7, 8
E		14.00 BSC.		4
E_1		12.00 BSC.		7, 8
L	0.45	0.60	0.75	
N		80		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b_1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

102778_125

A

Approved Crystal Vendors Appendix

Conexant conducted a series of internal tests and used the results to generate this list of approved crystal vendors for the CX25898/9. Manufacturers not appearing in this list may be acceptable, but verification testing on the target PCB with samples is recommended prior to production.

Standard Crystal (El Monte, CA)

Phone Number: (626) 443-2121

FAX Number: (626) 443-9049

E-mail:stdxtl@pacbell.net

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:AAL13M500000GXE20A

Half Height/50 ppm:AAK13M500000GXE20A

Full Height/25 ppm:Did Not Qualify

MMD Components (Irvine, CA)

Phone Number: (949) 753-5888

FAX Number: (949) 753-5889

E-mail:info@mmdcomp.com

Internet:www.mmdcomp.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50ppm Total Tolerance:A20BA1-13.500 MHz

Half Height/50 ppm:B20BA1-13.500 MHz

Full Height/25 ppm:MMC-135-13.500 MHz (not tested)

Half Height/25 ppm:MMC-136-13.500 MHz (not tested)

General Electronics Devices (San Marcos, CA)

Phone Number: (760) 591-4170

FAX Number: (760) 591-4164

E-mail:gedlm@4dcomm.com

Internet:www.gedlm.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:PKHC49-13.500-.020-.005

Half Height/50 ppm:PKHC49/-13.500-.020-.005

Full Height/25 ppm:PKHC49/-13.500-.020-.0025-15R

Half Height/25 ppm:PKHC49/-13.500-.020-.0025

Fox Electronics (Fort Myers, FL)

Phone Number: (941) 693-0099

FAX Number: (941) 693-1554

E-mail:sales@foxonline.com

Internet:www.foxonline.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:HC49U-13.500 /50/0/70/20 pF

Half Height/50 ppm:HC49S-13.500/50/0/70/20 pF

Full Height/25 ppm:HC49U-13.500 /25/0/70/20 pF

Half Height/25 ppm:HC49S-13.500 /25/0/70/20 pF (not tested)

Bomar Crystal Co. (Middlesex, NJ)

Phone Number: (732) 356-7787

FAX Number: (732) 356-7362

E-mail:sales@bomarcrystal.com

Internet:www.bomarcrystal.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:BRC1C14F-13.50000 or

BC1DDA120-13.50000

Half Height/50 ppm:ACR-49S012025-13.50000 or

BC14DDA120-13.50000

Full Height/25 ppm:BRCIH14F-13.50000 or

BC1AAA120-13.50000

Half Height/25 ppm:BC14AAA120-13.50000 (not tested)

ILSI America (Reno, NV)

Phone Number: (775) 851-8880x103 / (888)355-4574

FAX Number: (775) 851-8882

E-mail:e-mail@ilsiamerica.com

Internet:www.ilsiamerica.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:HC49U-25/25-13.500-20

Half Height/50 ppm:HC49US-FB1F20-13.500

Full Height/25 ppm:Did Not Qualify

Cardinal Components (Wayne, NJ)

Phone Number: (973) 785-1333

FAX Number: (973) 785-0053

E-mail:cardinal@cardinalxtal.com

Internet:www.cardinalxtal.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:C49-A4BRC7-50-13.5D20

Half Height/50 ppm:CLP-A4BRC7-70-13.5D20

Full Height/25 ppm:C49-A4B6C4-25-13.5D20

Half Height/25 ppm:CLP-A4B6C4-25-13.5D20

Raltron Electronics Corp. (Miami, FL)

Phone Number: (305) 593-6033

FAX Number: (305) 594-3973

E-mail:Sales@raltron.com

Internet:www.raltron.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:A-13.500-20-RS1

Half Height/50 ppm:AS-13.500-20-RS1

Full Height/25 ppm:A-13.500-20-RS1

Half Height/25ppm:AS-13.500-20-SMD-NV

Valpey-Fisher (Hopkinton, MA)

Phone Number: (508) 435-6831

FAX Number: (508) 435-5289

Internet:www.valpeyfisher.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:M490013.500020RSVM

Half Height/50 ppm:M49K013.50002099VM

Full Height/25 ppm:M490013.50002099VM

Corning Frequency Control (Mount Holly Springs, PA)

Phone Number: (717) 486-3411

FAX Number: (717) 486-5920

E-mail:sales@ofc.come

Internet:www.corningfrequency.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:TQ RSD 13.5FH50

Half Height/50 ppm:TQ RSD 13.5LP50

Full Height/25 ppm:TQ RSD 13.5FH25

Half Height/25 ppm:TQ RSD 13.5LP25 (not tested)

B

Autoconfiguration Mode Register Values and Details Appendix

This encoder contains 48 autoconfiguration modes. Tables 45 through 53 contain all register values that change when the autoconfiguration register 0xB8 is written. These tables also contain pertinent video parameters for each mode.

Table 45. CX25898/9 Register Values for Autoconfiguration Modes 0–4 *(1 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
Autoconfig Register (index 0xB8) Hexadecimal Value	00	01	02	03	04
Purpose of mode	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	640x480	640x480	800x600	800x600	640x480
Overscan Ratio	Lower	Standard	Alternate	Lower	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.79	16.56	21.62	14.53	13.79
Vertical Overscan Ratio/ Percentage (VOC)	13.58	16.67	11.52	13.19	13.58
Overscan Percentages Delta (HOC - VOC)	0.21	–0.11	10.10	1.34	0.21
H_CLKI = HTOTAL	784	944	880	960	784
VLINES_I = VTOTAL	600	625	735	750	600
H_BLANKI = Horizontal Blanking Region	126	266	66	140	126
V_BLANKI = Vertical Blanking Region	75	90	86	95	75
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	28195793	29500008	38769241	36000000	28195793
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character

Table 45. CX25898/9 Register Values for Autoconfiguration Modes 0–4 *(2 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	00	00
0x76	00	60	A0	00	00
0x78	80	80	20	20	80
0x7A	84	8A	B6	AA	84
0x7C	96	A6	CE	CA	96
0x7E	60	68	B4	9A	60
0x80	7D	C1	55	0D	7D
0x82	22	2E	20	29	22
0x84	D4	F2	D8	FC	D4
0x86	27	27	39	39	27
0x88	00	00	00	00	00
0x8A	10	B0	70	C0	10
0x8C	7E	0A	42	8C	7E
0x8E	03	0B	03	03	03
0x90	58	71	DF	EE	58
0x92	4B	5A	56	5F	4B
0x94	E0	E0	58	58	E0
0x96	36	36	3A	3A	36
0x98	92	00	CD	66	92
0x9A	54	50	9C	96	54
0x9C	0E	72	14	00	0E
0x9E	88	1C	3B	00	88
0xA0	0C	0D	11	10	0C
0xA2	0A	24	0A	24	0A
0xA4	E5	F0	E5	F0	E5
0xA6	76	58	74	57	76

Table 45. CX25898/9 Register Values for Autoconfiguration Modes 0–4 *(3 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0xA8	79	81	77	80	C0
0xAA	44	49	43	48	89
0xAC	85	8C	85	8C	9A
0xAE	00	0C	BA	18	00
0xB0	00	8C	E8	28	00
0xB2	80	79	A2	87	80
0xB4	20	26	17	1F	20

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 46. CX25898/9 Register Values for Autoconfiguration Modes 5–10 *(1 of 3)*

Autoconfiguration Mode #	5	6	7	8	9	10
Autoconfig Register (index 0xB8) Hexadecimal Value	05	06	07	10	11	12
Purpose of Mode	Desktop	Desktop	Desktop	Boot-Up Screen	Boot-Up Screen	Desktop
Type of Digital Input	YCrCb	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	640x480	800x600	800x600	640x400	640x400	1024x768
Overscan Ratio	Standard	Alternate	Lower	Standard	Standard	Standard
Horizontal Overscan Ratio/ Percentage (HOC)	16.56	21.62	14.53	17.47	15.12	15.11
Vertical Overscan Ratio/ Percentage (VOC)	16.67	11.52	13.19	17.70	13.19	14.81
Overscan Percentages Delta (HOC - VOC)	–0.11	10.10	1.34	–0.23	1.93	0.30
H_CLKI = HTOTAL	944	880	960	936	1160	1176
VLINES_I = VTOTAL	625	735	750	525	500	975
H_BLANKI = Horizontal Blanking Region	266	66	140	259	363	133
V_BLANKI = Vertical Blanking Region	90	86	95	76	64	130
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	29500008	38769241	36000000	29454552	28999992	68727276
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	00	00	20
0x76	60	A0	00	50	40	60
0x78	80	20	20	80	80	00
0x7A	8A	B6	AA	8A	88	D8
0x7C	A6	CE	CA	9C	A2	F2
0x7E	68	B4	9A	6A	64	EE

Table 46. CX25898/9 Register Values for Autoconfiguration Modes 5–10 *(2 of 3)*

Autoconfiguration Mode #	5	6	7	8	9	10
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0x80	C1	55	0D	A9	AF	71
0x82	2E	20	29	27	29	24
0x84	F2	D8	FC	CA	FC	D0
0x86	27	39	39	27	27	4B
0x88	00	00	00	00	00	00
0x8A	B0	70	C0	A8	88	98
0x8C	0A	42	8C	03	6B	85
0x8E	0B	03	03	0B	0C	04
0x90	71	DF	EE	0D	F4	CF
0x92	5A	56	5F	4C	40	82
0x94	E0	58	58	90	90	00
0x96	36	3A	3A	36	35	3F
0x98	00	CD	66	00	9A	6E
0x9A	50	9C	96	50	49	AB
0x9C	72	14	00	46	8E	A3
0x9E	1C	3B	00	17	E3	8B
0xA0	0D	11	10	0D	0C	1E
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	58	74	57	75	58	74
0xA8	CE	BE	CB	79	82	77
0xAA	92	87	90	44	49	43
0xAC	A4	9A	A4	85	8C	85
0xAE	0C	BA	18	C7	E9	00

Table 46. CX25898/9 Register Values for Autoconfiguration Modes 5–10 *(3 of 3)*

Autoconfiguration Mode #	5	6	7	8	9	10
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0xB0	8C	E8	28	71	5D	00
0xB2	79	A2	87	1C	23	00
0xB4	26	17	1F	1F	27	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 47. CX25898/9 Register Values for Autoconfiguration Modes 11–15 *(1 of 3)*

Autoconfiguration Mode #	11	12	13	14	15
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
Autoconfig Register (index 0xB8) Hexadecimal Value	13	14	15	16	17
Purpose of Mode	Desktop	Game	Game	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	YCrCb	YCrCb
Active Resolution	1024x768	320x240, Pix_Double Set	320x240, Pix_Double Set	1024x768	1024x768
Overscan Ratio	Standard	Standard	Standard	Higher	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	13.44	13.79	15.84	15.11	13.44
Vertical Overscan Ratio/ Percentage (VOC)	14.24	13.58	19.79	14.81	14.24
Overscan Percentages Delta (HOC - VOC)	–0.80	0.21	–3.95	0.30	–0.80
H_CLKI = HTOTAL	1400	1568	1800	1176	1400
VLINES_I = VTOTAL	975	300	325	975	975
H_BLANKI = Horizontal Blanking Region	329	349	385	133	329
V_BLANKI = Vertical Blanking Region	131	37	50	130	131
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI
Frequency of CLK (Hz)	68249989	28195793	2950000	68727276	68249989
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	40	40	20	20
0x76	60	00	50	60	60
0x78	00	80	80	00	00
0x7A	D6	84	8A	D8	D6
0x7C	FE	96	A4	F2	FE
0x7E	E6	60	66	EE	E6

Table 47. CX25898/9 Register Values for Autoconfiguration Modes 11–15 *(2 of 3)*

Autoconfiguration Mode #	11	12	13	14	15
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x80	87	7D	B7	71	87
0x82	2B	22	32	24	2B
0x84	F8	D5	EA	D0	F8
0x86	4B	27	27	4B	4B
0x88	00	00	00	00	00
0x8A	78	20	08	98	78
0x8C	49	5D	81	85	49
0x8E	0D	1E	1F	04	0D
0x90	CF	2C	45	CF	CF
0x92	83	25	32	82	83
0x94	00	F0	F0	00	00
0x96	3F	31	31	3F	3F
0x98	EC	49	A4	6E	EC
0x9A	A1	42	40	AB	A1
0x9C	55	0E	00	A3	55
0x9E	55	88	00	8B	55
0xA0	1E	0C	0D	1E	1E
0xA2	24	0A	24	0A	24
0xA4	F0	E5	F0	E5	F0
0xA6	56	76	58	74	56
0xA8	7F	79	81	BD	C9
0xAA	47	44	49	87	8F
0xAC	8C	85	8C	9A	A4
0xAE	57	00	32	00	57

Table 47. CX25898/9 Register Values for Autoconfiguration Modes 11–15 *(3 of 3)*

Autoconfiguration Mode #	11	12	13	14	15
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0xB0	F8	00	BB	00	F8
0xB2	F1	80	CD	00	F1
0xB4	18	20	26	14	18

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 48. CX25898/9 Register Values for Autoconfiguration Modes 16–21 *(1 of 3)*

Autoconfiguration Mode #	16	17	18	19	20	21
Autoconfig Register (index 0xB8) Hexadecimal Value	20	21	22	23	24	25
Purpose of Mode	Desktop	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	640x480	640x480	800x600	800x600	640x480	640x480
Overscan Ratio	Standard	Lower	Lower	Standard	Lower	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	16.76	13.63	13.78	16.42	13.78	13.63
Vertical Overscan Ratio/ Percentage (VOC)	14.81	13.19	13.58	15.97	13.58	13.19
Overscan Percentages Delta (HOC - VOC)	1.95	0.44	0.21	0.45	0.20	0.44
H_CLKI = HTOTAL	800	950	1176	950	784	950
VLINES_I = VTOTAL	609	600	750	775	600	600
H_BLANKI = Horizontal Blanking Region	140	271	329	131	126	271
V_BLANKI = Vertical Blanking Region	81	76	94	109	75	76
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	PAL-60	PAL-BDGHI
Frequency of CLK (Hz)	29202793	28500011	52867138	36812508	28195793	28500011
Type of Clock	Pixel Only	Pixel Only	Pixel or Character	Pixel Only	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	20	00	00	00
0x76	40	20	C0	34	00	20
0x78	80	80	20	20	80	80
0x7A	8A	86	A6	AE	84	86
0x7C	9A	A0	BA	CE	9E	A0
0x7E	68	60	98	A0	5E	60
0x80	A1	9D	D9	2B	7D	9D

Table 48. CX25898/9 Register Values for Autoconfiguration Modes 16–21 *(2 of 3)*

Autoconfiguration Mode #	16	17	18	19	20	21
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0x82	24	29	22	2D	22	29
0x84	D1	FC	D4	F4	D4	FC
0x86	27	27	38	39	27	27
0x88	00	00	00	00	00	00
0x8A	20	B6	98	B6	10	B6
0x8C	8C	0F	49	83	7E	0F
0x8E	03	0B	0C	03	03	0B
0x90	61	58	EE	07	58	58
0x92	51	4C	5E	6D	4B	4C
0x94	E0	E0	58	58	E0	E0
0x96	06	36	3A	3B	06	36
0x98	1F	B8	B7	AE	92	B8
0x9A	55	4E	5D	97	54	4E
0x9C	A1	AB	1B	72	0E	AB
0x9E	FA	AA	7F	5C	88	AA
0xA0	0C	0C	17	10	0C	0C
0xA2	0A	24	0A	24	20	24
0xA4	E5	F0	E5	F0	F0	F0
0xA6	75	58	74	57	58	58
0xA8	79	82	78	80	82	CE
0xAA	44	49	43	48	49	93
0xAC	85	8C	85	8C	8C	A4
0xAE	7C	2C	00	01	7C	2C

Table 48. CX25898/9 Register Values for Autoconfiguration Modes 16–21 *(3 of 3)*

Autoconfiguration Mode #	16	17	18	19	20	21
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0xB0	1A	25	00	04	23	25
0xB2	61	D3	00	D5	41	D3
0xB4	1F	27	1A	1E	28	27

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 49. CX25898/9 Register Values for Autoconfiguration Modes 22–26 *(1 of 3)*

Autoconfiguration Mode #	22	23	24	25	26
Autoconfig Register (index 0xB8) Hexadecimal Value	26	27	30	31	32
Purpose of Mode	Desktop	Desktop	Boot-Up Screen	Boot-Up Screen	Desktop
Type of Digital Input	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	800x600	800x600	720x400	720x400	1024x768
Overscan Ratio	Lower	Standard	Standard	Standard	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.79	16.42	17.47	15.12	11.97
Vertical Overscan Ratio/ Percentage (VOC)	13.58	15.97	17.70	13.19	11.93
Overscan Percentages Delta (HOC - VOC)	0.21	0.45	–0.23	1.93	0.04
H_CLKI = HTOTAL	1176	950	1053	1305	1170
VLINES_I = VTOTAL	750	775	525	500	945
H_BLANKI = Horizontal Blanking Region	329	131	291	411	127
V_BLANKI = Vertical Blanking Region	94	109	76	64	115
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	52867138	36812508	33136345	32625000	66272724
Type of Clock	Pixel or Character	Pixel Only	Pixel or 9-Character only	Pixel or 9-Character only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	00	00	00	20
0x76	C0	34	3A	28	F8
0x78	20	20	D0	D0	00
0x7A	A6	AE	9C	9A	D0
0x7C	BA	CE	B0	B6	EA
0x7E	98	A0	88	80	E0
0x80	D9	2B	DD	E3	37

Table 49. CX25898/9 Register Values for Autoconfiguration Modes 22–26 *(2 of 3)*

Autoconfiguration Mode #	22	23	24	25	26
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x82	22	2D	27	29	21
0x84	D4	F4	CA	FC	D7
0x86	38	39	28	28	4A
0x88	00	00	00	00	00
0x8A	98	B6	1D	19	92
0x8C	49	83	23	9B	7F
0x8E	0C	03	0C	0D	04
0x90	EE	07	0D	F4	B1
0x92	5E	6D	4C	40	73
0x94	58	58	90	90	00
0x96	3A	3B	36	35	3F
0x98	B7	AE	00	9A	9A
0x9A	5D	97	50	49	A9
0x9C	1B	72	2E	00	5D
0x9E	7F	5C	BA	80	74
0xA0	17	10	0E	0E	1D
0xA2	0A	24	0A	24	0A
0xA4	E5	F0	E5	F0	E5
0xA6	74	57	75	57	74
0xA8	BF	CB	78	80	77
0xAA	88	90	43	48	43
0xAC	9A	A4	85	8C	85
0xAE	00	01	95	97	2F

Table 49. CX25898/9 Register Values for Autoconfiguration Modes 22–26 *(3 of 3)*

Autoconfiguration Mode #	22	23	24	25	26
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0xB0	00	04	81	1A	A1
0xB2	00	D5	A7	CA	BD
0xB4	1A	1E	1B	22	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 50. CX25898/9 Register Values for Autoconfiguration Modes 27–30 *(1 of 3)*

Autoconfiguration Mode #	**27**	**28[5]**	**29[5]**	**30**
Autoconfig Register (index 0xB8) Hexadecimal Value	33	34	35	36
Purpose of Mode	Desktop	DVD/CCIR601 Input, Slave Interface EN_XCLK bit = 1	DVD/CCIR601 Input, Slave Interface EN_XCLK bit = 1	Desktop
Type of Digital Input	RGB	YCrCb	YCrCb	YCrCb
Active Resolution	800 x 600	720x480	720x576	1024x768
Overscan Ratio	Lower	None (DVD Playback)	None (DVD Playback)	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.78	0.00	0.00	11.97
Vertical Overscan Ratio/ Percentage (VOC)	13.58	0.00	0.00	11.93
Overscan Percentages Delta (HOC - VOC)	0.20	0.00	0.00	0.04
H_CLKI = HTOTAL	1176	858	864	1170
VLINES_I = VTOTAL	750	262	312	945
H_BLANKI = Horizontal Blanking Region	329	10	10	127
V_BLANKI = Vertical Blanking Region	94	19	22	115
Type of Video Output	PAL-60	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	35244758	27000000	27000000	66272724
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	10	10	20
0x76	C0	B4	C0	F8
0x78	20	D0	D0	00
0x7A	A6	7E	7E	D0
0x7C	C6	90	98	EA
0x7E	94	58	54	E0
0x80	D9	03	15	37

Table 50. CX25898/9 Register Values for Autoconfiguration Modes 27–30 *(2 of 3)*

Autoconfiguration Mode #	27	28[5]	29[5]	30
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x82	22	14	17	21
0x84	D4	F0	20	D7
0x86	38	26	A6	4A
0x88	00	15	FA	00
0x8A	98	5A	60	92
0x8C	49	0A	0A	7F
0x8E	0C	13	13	04
0x90	EE	06	38	B1
0x92	5E	13	16	73
0x94	58	F0	20	00
0x96	0A	31	35	3F
0x98	B7	00	00	9A
0x9A	5D	40	40	A9
0x9C	1B	00	00	5D
0x9E	7F	00	00	74
0xA0	17	8C	8C	1D
0xA2	20	0A	24	0A
0xA4	F0	E5	F0	E5
0xA6	57	76	59	74
0xA8	80	C1	CF	BD
0xAA	48	89	93	87
0xAC	8C	9A	A4	9A
0xAE	63	1F	CB	2F

Table 50. CX25898/9 Register Values for Autoconfiguration Modes 27–30 *(3 of 3)*

Autoconfiguration Mode #	27	28[5]	29[5]	30
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0xB0	1C	7C	8A	A1
0xB2	34	F0	09	BD
0xB4	20	21	2A	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 51. CX25898/9 Register Values for Autoconfiguration Modes 31–36 *(1 of 3)*

Autoconfiguration Mode #	31	32	33	34	35	36
Autoconfig Register (index 0xB8) Hexadecimal Value	37	40	41	42	43	44
Purpose of Mode	DVD/ noninterlaced input	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	720 x 576	640x480	640x480	800x600	800x600	640x480
Overscan Ratio	Very Low (DVD Playback)	Higher	Higher	Higher	Higher	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	–0.01	18.34	20.27	19.26	19.03	18.34
Vertical Overscan Ratio/ Percentage (VOC)	0.00	19.34	19.79	19.34	18.40	19.34
Overscan Percentages Delta (HOC - VOC)	–0.01	–1.00	0.48	–0.08	0.63	–1.00
H_CLKI = HTOTAL	886	770	950	1170	950	770
VLINES_I = VTOTAL	625	645	650	805	800	645
H_BLANKI = Horizontal Blanking Region	145	113	271	323	131	113
V_BLANKI = Vertical Blanking Region	42	100	104	125	122	100
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	27687503	29769241	30875015	56454552	37999992	29769241
Type of Clock	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	20	00	00
0x76	EC	64	B8	58	80	64
0x78	D0	80	80	20	20	80
0x7A	82	8C	92	B0	B2	8C
0x7C	9C	9E	AC	C8	D4	9E

Table 51. CX25898/9 Register Values for Autoconfiguration Modes 31–36 *(2 of 3)*

Autoconfiguration Mode #	31	32	33	34	35	36
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0x7E	5A	6E	72	AC	AA	6E
0x80	2F	B5	F3	2D	57	B5
0x82	16	2A	33	2A	31	2A
0x84	22	C5	E9	C5	EC	C5
0x86	A6	27	27	39	39	27
0x88	00	00	00	00	00	00
0x8A	76	02	B6	92	B6	02
0x8C	91	71	0F	43	83	71
0x8E	03	03	0B	0C	03	03
0x90	71	85	8A	25	20	85
0x92	2A	64	68	7D	7A	64
0x94	40	E0	E0	58	58	E0
0x96	0A	36	36	3B	3B	36
0x98	00	50	48	11	F6	50
0x9A	50	57	51	A1	98	57
0x9C	39	14	E4	46	8E	14
0x9E	4E	3B	B8	17	E3	3B
0xA0	0C	0D	0D	19	10	0D
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	59	75	58	74	57	75
0xA8	82	79	81	77	7F	C0
0xAA	49	44	48	43	48	89
0xAC	8C	85	8C	85	8C	9A
0xAE	57	F2	3D	21	E1	F2

Table 51. CX25898/9 Register Values for Autoconfiguration Modes 31–36 *(3 of 3)*

Autoconfiguration Mode #	31	32	33	34	35	36
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0xB0	53	40	E7	0B	5B	40
0xB2	FE	C8	C2	59	DE	C8
0xB4	28	1E	24	18	1D	1E

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 52. CX25898/9 Register Values for Autoconfiguration Modes 37–42 *(1 of 3)*

Autoconfiguration Mode #	37	38	39	40	41	42
Autoconfig Register (index 0xB8) Hexadecimal Value	45	46	47	50	51	52
Purpose of Mode	Desktop	Desktop	Desktop	Desktop	Game	Desktop
Type of Digital Input	YCrCb	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	640x480	800x600	800x600	800x600	320x200, Pix_Double Set	1024x768
Overscan Ratio	Higher	Higher	Higher	Standard	Standard	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	20.27	19.26	19.03	15.59	21.86	18.04
Vertical Overscan Ratio/ Percentage (VOC)	19.79	19.34	18.40	15.64	30.90	18.11
Overscan Percentages Delta (HOC - VOC)	0.48	–0.08	0.63	–0.05	–9.04	–0.07
H_CLKI = HTOTAL	950	1170	950	1170	2000	1170
VLINES_I = VTOTAL	650	805	800	770	315	1015
H_BLANKI = Horizontal Blanking Region	271	323	131	323	453	127
V_BLANKI = Vertical Blanking Region	104	125	122	105	65	150
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	30875015	56454552	37999992	54000000	31500000	71181793
Type of Clock	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel or Character	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	20	00	20	40	20
0x76	B8	58	80	F0	E0	C8
0x78	80	20	20	20	80	00
0x7A	92	B0	B2	AA	94	E0
0x7C	AC	C8	D4	BE	B0	FC
0x7E	72	AC	AA	9E	78	FA

Table 52. CX25898/9 Register Values for Autoconfiguration Modes 37–42 *(2 of 3)*

Autoconfiguration Mode #	37	38	39	40	41	42
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0x80	F3	2D	57	F3	09	AB
0x82	33	2A	31	25	42	28
0x84	E9	C5	EC	CE	CA	C8
0x86	27	39	39	38	27	4B
0x88	00	00	00	00	00	00
0x8A	B6	92	B6	92	D0	92
0x8C	0F	43	83	43	C5	7F
0x8E	0B	0C	03	0C	1F	04
0x90	8A	25	20	02	3B	F7
0x92	68	7D	7A	69	41	96
0x94	E0	58	58	58	C8	00
0x96	36	3B	3B	3B	31	3F
0x98	48	11	F6	EF	21	DE
0x9A	51	A1	98	5E	80	AD
0x9C	E4	46	8E	00	00	E8
0x9E	B8	17	E3	00	00	A2
0xA0	0D	19	10	18	0E	1F
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	58	74	57	74	58	74
0xA8	CD	BE	CB	78	81	77
0xAA	92	87	90	43	48	43
0xAC	A4	9A	A4	85	8C	85
0xAE	3D	21	E1	17	D3	C2

Table 52. CX25898/9 Register Values for Autoconfiguration Modes 37–42 *(3 of 3)*

Autoconfiguration Mode #	37	38	39	40	41	42
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Address**
0xB0	E7	0B	5B	5D	2D	72
0xB2	C2	59	DE	74	08	4F
0xB4	24	18	1D	19	24	13

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table 53. CX25898/9 Register Values for Autoconfiguration Modes 43–47 *(1 of 3)*

Autoconfiguration Mode #	43	44[1]	45	46	47
Autoconfig Register (index 0xB8) Hexadecimal Value	53	54	55	56	57
Purpose of Mode	Desktop	DVD/ noninterlaced input	Game	Desktop for Brazil	Desktop for Argentina
Type of Digital Input	RGB	RGB	RGB	RGB	RGB
Active Resolution	1024x768	720x480	320x200, Pixel_Double Set	640x480	640x480
Overscan Ratio	Higher	Very Low (DVD Playback)	Standard	Standard	Standard
Horizontal Overscan Ratio/ Percentage (HOC)	16.20	1.24	20.20	13.79	16.56
Vertical Overscan Ratio/ Percentage (VOC)	16.67	1.23	21.40	13.58	16.67
Overscan Percentages Delta (HOC - VOC)	–0.47	0.01	–1.20	0.21	–0.11
H_CLKI = HTOTAL	1410	880	1848	784	944
VLINES_I = VTOTAL	1000	525	275	600	625
H_BLANKI = Horizontal Blanking Region	337	140	429	126	266
V_BLANKI = Vertical Blanking Region	147	36	43	75	90
Type of Video Output	PAL-BDGHI	NTSC	NTSC	PAL-M (Brazil)	PAL-Nc (Argentina)
Frequency of CLK (Hz)	70499989	27692310	30461552	28195793	29500008
Type of Clock	Pixel Only	Pixel or Character	Pixel or Character	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	24	00	40	00	00
0x76	C0	E0	90	00	60
0x78	00	D0	80	80	80
0x7A	DC	82	90	84	8A
0x7C	08	92	A2	A4	A6

Table 53. CX25898/9 Register Values for Autoconfiguration Modes 43–47 *(2 of 3)*

Autoconfiguration Mode #	43	44[1]	45	46	47
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x7E	F0	5C	72	6A	70
0x80	BF	1B	CD	7D	C1
0x82	2F	13	2B	22	2E
0x84	F1	F2	C2	D4	F2
0x86	4B	26	27	27	27
0x88	00	00	00	00	00
0x8A	82	70	38	10	B0
0x8C	51	8C	AD	7E	0A
0x8E	0D	03	1F	03	0B
0x90	E8	0D	13	58	71
0x92	93	24	2B	4B	5A
0x94	00	E0	C8	E0	E0
0x96	3F	36	31	36	36
0x98	33	00	C3	92	00
0x9A	A3	50	40	54	50
0x9C	55	C5	D9	0E	72
0x9E	55	4E	89	88	1C
0xA0	1F	0C	0D	0C	0D
0xA2	24	0A	0A	2A	24
0xA4	F0	E5	E5	F0	F0
0xA6	56	76	75	57	57
0xA8	7E	79	78	80	80
0xAA	47	44	44	48	48
0xAC	8C	85	85	8C	8C
0xAE	9B	D1	33	6E	1E

Table 53. CX25898/9 Register Values for Autoconfiguration Modes 43–47 *(3 of 3)*

Autoconfiguration Mode #	43	44[1]	45	46	47
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0xB0	29	45	28	DB	C0
0xB2	26	17	15	76	15
0xB4	18	21	1E	20	1F

GENERAL NOTE:

1. RGB digital input denotes that the CX25898/9 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25898/9's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25898/9 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25898/9's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25898/9 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25898/9 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.
7.
8. Mode 44 would ideally have 858 clocks per line. However, since 858 is not a multiple of 8, then 880 clocks per line was utilized instead.

www.conexant.com
General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters – Newport Beach
4000 MacArthur Blvd.
Newport Beach, CA 92660