CX25874/5
Digital Encoder with Standard-Definition TV and High-Definition TV Video Output

Data Sheet

101900B
August 2004

CONEXANT®

Ordering Information

Model Number	Package	Operating Temperature
CX25874	64-pin TQFP	0 °C – 70 °C
CX25875[(1)(2)(3)]	64-pin TQFP	0 °C – 70 °C

Note(s):
1. Macrovision 7.1.L1 Standard-Definition Television (SDTV) compliant (customer must possess Macrovision license (“) to purchase CX25875).
2. Macrovision 525p (480p) High-Definition Television (HDTV) progressive scan output compliant.
3. Customer must possess Macrovision license to purchase CX25875.

Revision History

Revision	Level	Date	Description
A		August 15, 2002	Initial release
B		August 26, 2004	Second release

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CX25874/5

Digital Encoder with SDTV and HDTV Video Output

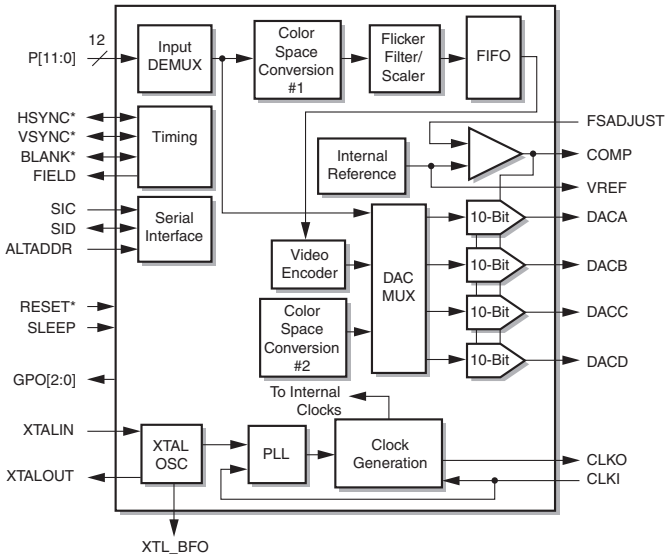
Conexant's CX25874/5 Digital Encoder (DENC) is specifically designed to meet TV out system requirements for the next-generation desktop PCs, notebook PCs, game consoles, progressive DVD players, and set-top boxes. With software-forward compatibility to the CX25870/871, manufacturers can quickly bring to market new solutions that require adaptive flicker filtering, ATSC HDTV outputs, and active resolutions from 320 x 200 (minimum) to 1024 x 768 (maximum).

Adaptive flicker filtering is a Conexant technology in which the encoder looks at the characteristics of the video content on a pixel-by-pixel basis and automatically determines the optimal amount of flicker filtering required. If an end-user wants to work on a spreadsheet while watching a DVD movie in a window, both the text-intensive application requiring a lot of flicker filtering, and the DVD movie requiring very little flicker filtering can look their best.

The CX25874/5 also provides a three-signal analog RGB or YP_RP_B HDTV output. While in HDTV output mode, the CX25874/5 will automatically insert horizontal trilevel synchronization pulses and vertical synchronization broad pulses. The CX25874/5 is compliant with the EIA770-3 and SMPTE 274M/293M/296M standards and supports all major ATSC HDTV resolutions including 480p, 625p (576p), 720p, and 1080i.

All worldwide standard-definition composite outputs are supported, including NTSC-M (N. America, Taiwan), NTSC-J (Japan), NTSC 4.43, PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay), PAL-Nc (Argentina), PAL-60 (China) and SECAM (France, elsewhere). For enhanced TV viewing, S-video (SVHS) can be transmitted as well. The CX25874 and CX25875 are functionally identical, except the CX25875 can output standard-definition video with Macrovision® Level 7.1.L1 copy protection capability, and HDTV with Macrovision 525p (480p) copy protection for progressive scan outputs.

Functional Block Diagram



Distinguishing Features

- 4 high-performance, 10-bit DACs
- HDTV output mode (patents pending)
  - Compliant with EIA770-3 and SMPTE274M (1080i), SMPTE296M (720p), ITU-R.BT1358 (625p and 525p) and ITU-R.BT.709-4 (1035i and CIF 30/ PsF and 60/ I) standards
  - Automatic trilevel sync and broad pulse generation
  - Direct YP_RP_B or RGB HDTV outputs from progressive RGB graphics video in 1080i, 720p, 480p ATSC and ITU-R.BT.1358 625p and 525p resolutions
  - Direct YP_RP_B HDTV outputs from YCrCb or YPrPb graphics video in 1080i, 720p, 480p ATSC and ITU-R.BT.1358 625p and 525p resolutions
  - Support for Japan D1 (525i), D2 (D1+525p), D3 (D2+750p), D4 (D3+1125i) HDTV formats
- Software and register forward-compatible with the Bt868/869, CX25870/871, and CX25872/873
- Worldwide standard-definition TV support: NTSC-M, J, 4.43, PAL-B, D, G, H, I, M, N, Nc, 60, and SECAM
  - NTSC-M, -J, -4.43 SDTV outputs conform to SMPTE 170M standard
  - PAL-B, -D, G, H, I, M, N, Nc, 60 conform to ITU-R.BT.470 standard
- Adaptive flicker filtering for enhanced image quality (patents pending), and peaking filters for text sharpness
- Programmable overscan compensation from 0% to 25%
- Programmable power management
- Wide-Screen Signaling (WSS) and CGMS support for variable clock rates
  - Adheres to EIAJ CPR-1204 and 1204-1, 1204-2, and EN300 294 standards
- 3.3 V operation with scalable low-voltage graphics controller interface and serial bus from 3.3 V to 1.1 V
- Colorstream™ (EIA 770.2) and Super Colorstream™ component video outputs
- Component YC_RC_B analog outputs
- Luma and chroma comb filtering
- SCART RGB or Y/C output for Europe
  - 4th DAC is NTSC/PAL composite
  - EN50-049 and IEC 933-1 compliant

(Continued on next page)

Distinguishing Features (continued)

- S-Video output (simultaneous with composite or 2nd S-Video NTSC, PAL or SECAM)
- Accepts many different input data formats:
  - 15/16/24-bit RGB multiplexed
  - 16-bit 4:2:2 and 24-bit 4:4:4 YCrCb multiplexed
  - Flexible pixel ordering with various alternate formats
- 48 autoconfiguration modes
- CCIR601/ITU-R BT.601 (i.e., 720 x 480i for 525/60 video systems and 720 x 576i for 625/50 video systems) and CCIR656/ ITU-R.BT.601 syncless compatible input modes
- Closed captioning encoding (NTSC/PAL)
- Three general-purpose output ports (GPO[0]–GPO[2])
- VGA RGB or YUV outputs
- Pin compatible with the CX25872/873
- Macrovision 7.1.L1 and 525p (480p) DVD 1.03 Macrovision copy protection (CX25875 only)
- 64-pin TQFP package

Contents

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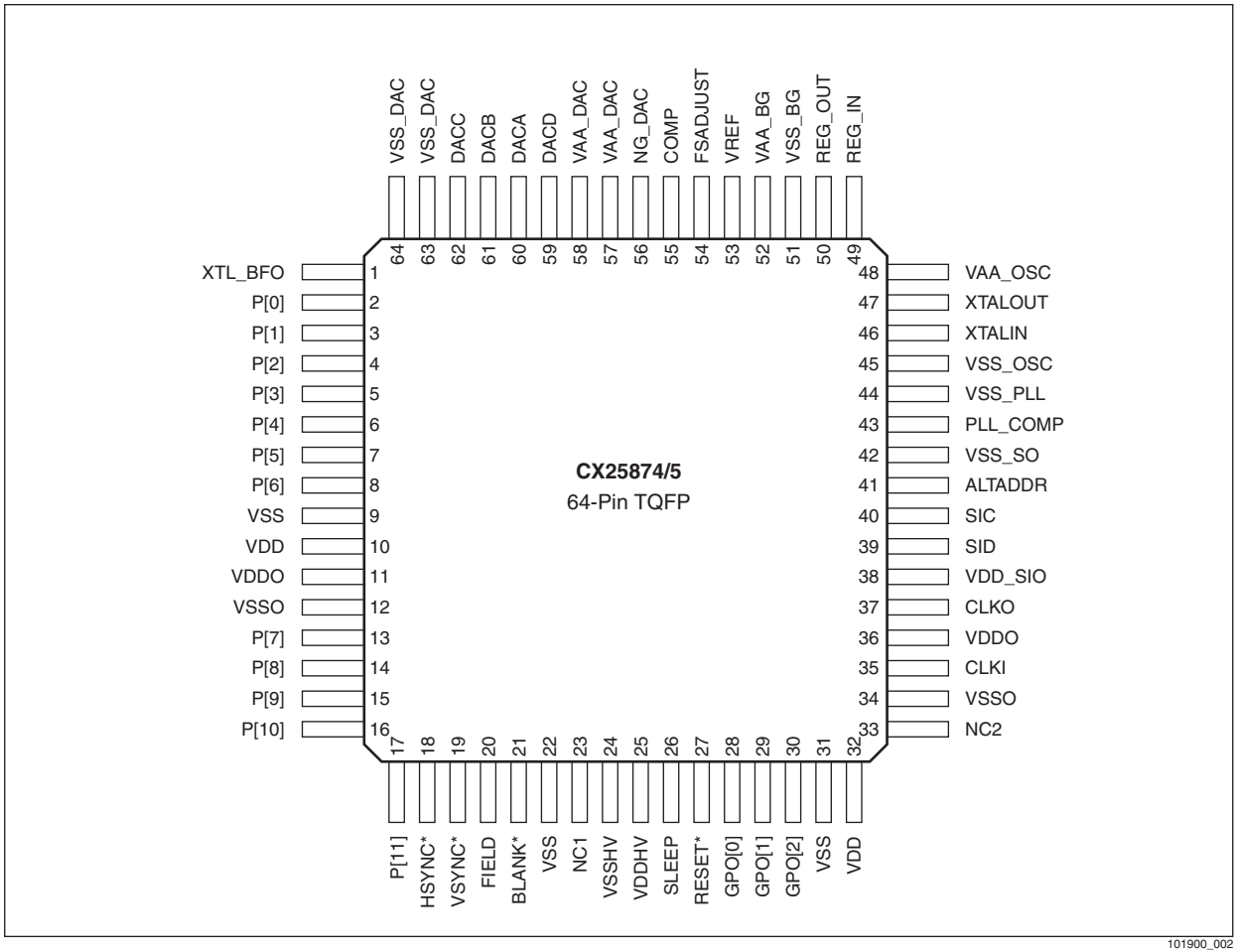
Tables

1 Functional Description

1.1 Pin Descriptions

The pinout diagram for CX25874/5 is illustrated in Figure 1-1. Pin names, Input/Output (I/O) assignments, numbers, and descriptions are listed in Tables 1-1 and 1-2.

Figure 1-1. Pinout Diagram for CX25874/5



The CX25874/5 is not pin-to-pin compatible with the Bt868/869 or CX25870/871. It is pin-to-pin compatible with the CX25872/873 with the exception of pins 28, 29, 30, and 59, which have additional functionality. The CX25874 and CX25875 are pin-to-pin compatible with each other.

Table 1-1. Pin Assignments and Descriptions *(1 of 4)*

Pin Name	I/O	Pin #	Description
XTL_BFO	O	1	Buffered crystal clock output. On power-up, the encoder will transmit a 0 to 3.3 V (or lower) signal at a frequency equal to the frequency of the crystal found between the XTALIN/XTALOUT ports. The XTL_BFO output is at a rate of 13.500 MHz, when used. If unused, XTL_BFO should be left as a no connect.
P[0:6]	I	2–8	Pixel inputs. See Table 1-2 for data and pin assignments for each multiplexed format. The input data is sampled on both the rising and falling edge of CLKI for multiplexed modes. A higher bit index corresponds to a greater bit significance. Note: All unused pixel input pins should be grounded.
VSS	—	9, 22, 31	Digital ground for core logic. All NG and VSS pins must be connected together on the same PCB plane to prevent latchup.
VDD	—	10, 32	Digital power for core logic. All VDD pins must be connected together on the same PCB plane to prevent latchup.
VDDO	—	11, 36	Digital input and output supply pins. These pins should be tied to the I/O power supply.
VSSO	—	12, 34	Digital input and output ground pins. These pins should be tied to ground. All analog and digital ground pins must be connected together on the same PCB plane to prevent latchup. Note: All unused pixel input pins hold be grounded.
P[7:11]	I	13–17	Pixel inputs. See Table 1-2 for data and pin assignments. The input data is sampled on both the rising and falling edge of CLK for multiplexed modes. A higher bit index corresponds to a greater bit significance. P[11] is the most significant pixel input. Note: All unused pixel input pins should be grounded.
HSYNC*	I/O	18	Horizontal sync input/output (TTL compatible). As an output (timing master operation), HSYNC* is output following the rising edge of CLKO. As an input (timing slave operation), HSYNC* is clocked on the rising edge of CLKI. The polarity of the HSYNC* signal can be adjusted with the HSYNCI bit.
VSYNC*	I/O	19	Vertical sync input/output (TTL compatible). As an output (timing master operation), VSYNC* is output following the rising edge of CLKO. As an input (timing slave operation), VSYNC* is clocked on the rising edge of CLKI. The polarity of the VSYNC* signal can be adjusted with the VSYNCI bit.
FIELD	O	20	Field control output (TTL compatible). FIELD transitions after the rising edge of CLK, two clock cycles following falling HSYNC*. It is a logical 0 during odd fields and is a logical 1 during even fields. If unused, FIELD should be left as a no connect. The polarity of the FIELD signal can be adjusted with the FIELDI bit.
BLANK*	I/O	21	Digital composite blanking control (TTL compatible) pin. This can be generated by the encoder or supplied from the graphics controller. If internal blanking is used, this pin can be used to indicate the control character clock edge. If unused, BLANK* should be tied high through a 10 kΩ pullup resistor.
NC	—	23, 33	No connect pins.
VDDHV	—	25	Digital high-voltage supply for internal pads. All VAA pins and VDD HV must be connected together on the same PCB plane to prevent latchup.
SLEEP	I	26	Power-down control input (TTL compatible). A logical 1 configures the device for power-down mode. A logical 0 configures the device for normal operation.

Table 1-1. Pin Assignments and Descriptions *(2 of 4)*

Pin Name	I/O	Pin #	Description
RESET*	I	27	Reset control input (TTL compatible). A logical 0 applied for a minimum of 20 CLKI clock cycles (or 1 μs) resets and disables video timing (horizontal, vertical, subcarrier counters) to the start of VSYNC of the first field. The serial interface registers are also reset to their default values. The hardware RESET* pulse must match the digital I/O voltage levels. The GPU (or Data Master device) must issue at least one transition (more preferred) from a 0 to a 1 on CLKI after power-up and before or during the application of the hardware RESET* pulse. Failure to do so will prevent several encoder clocking modes (most notably PLL32CLK) from working properly. To reiterate, CLKI cannot be left in steady state condition from power-up until after the rising edge of the hardware RESET* pulse. Toggling must occur, and the frequency received at CLKI prior to the end of RESET* must be less than 80 MHz.
GPO[0]	O	28	General-purpose output pin #0. User can select high or low output level through the GPO[0] bit. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins. If unused, tie this pin to GND through a 47 kΩ resistor in series. Inclusion of this resistor allows for a direct replacement of this encoder with the CX25872/873 without altering the layout.
GPO[1]	O	29	General-purpose output pin #1. User can select high or low output level through the GPO[1] bit. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins. If unused, tie this pin to GND through a 47 kΩ resistor in series. Inclusion of this resistor allows for a direct replacement of this encoder with the CX25872/873 without altering the layout.
GPO[2]	O	30	General-purpose output pin #2. User can select high or low output level through the GPO[2] bit. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins. If unused, tie this pin to GND through a 47 kΩ resistor in series. Inclusion of this resistor allows for a direct replacement of this encoder with the CX25872/873 without altering the layout.
VSSO	—	34	Digital output ground pin. Digital ground for syncs and timing pins. All analog and digital ground pins must be connected together on same PCB plane to prevent latchup.
CLKI	I	35	Pixel clock input (TTL compatible). This may be used as either the encoder's main clock (slave interface) or, more commonly, a delayed version of the CLKO signal (same frequency) synchronized with the pixel data input. The GPU (or Data Master device) must issue at least one transition (more preferred) from a 0 to a 1 on CLKI after power-up and before or during the application of the Hardware RESET* pulse. Failure to do so will prevent several encoder clocking modes from working properly. To reiterate, CLKI cannot be left in steady state condition from power-up until after the rising edge of the hardware RESET* pulse. Toggling must occur, and the frequency received at CLKI prior to the end of RESET* must be less than 80 MHz.
CLKO	O	37	Pixel clock output (TTL compatible). In master or pseudo-master interface, this signal is used by the encoder to tell the master the frequency at which data should be transferred. This pin is three-stated if the CLKI pin provides the encoder clock. Voltage level will always be 0 V for low and 1.1 V to 3.3 V for high, depending on power supply driving VDDO pins.

Table 1-1. Pin Assignments and Descriptions *(3 of 4)*

Pin Name	I/O	Pin #	Description
VDD_SIO	—	38	Serial interface supply pin. This pin should be tied 1.1 V to 3.3 V, depending on desired serial interface voltage.
SID	I/O	39	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this pin coupled with the SIC pin. Maximum serial transfer rate is 400 kHz. Minimum serial transfer rate is 100 kHz. The high voltage level to/from the SID pin must match the voltage level of pin 38 = VDD_SIO.
SIC	I	40	Serial interface clock input (TTL compatible). Data is latched into the device via this pin coupled with the SID pin. Maximum serial transfer rate is 400 kHz. Minimum serial transfer rate is 100 kHz. The high voltage level to the SIC pin must match the voltage level of pin 38 = VDD_SIO.
ALTADDR	I	41	Alternate slave address input (TTL compatible). A logical 0 configures the device to respond to a serial write address of 0x88. A logical 1 configures the device to respond to a serial write address of 0x8A. In addition, serial reads to address 0x89 (ALTADDR = 0) or 0x8B (ALTADDR = 1) are possible with this pin.
VSS_SO	—	42	Serial interface ground pin. Digital ground for syncs and timing pins. All analog and digital ground pins must be connected together on same PCB plane to prevent latchup.
PLL_COMP (or VDD_PLL)	—	43	PLL compensation pin. A 1.0 μF ceramic capacitor must be used to decouple this pin to GND. This pin also provides compensation for stable operation of the internal PLL regulator.
VSS_PLL	—	44	PLL ground pin. This pin should be tied to the ground plane.
VSS_OSC	—	45	Crystal oscillator ground pin. All analog and digital ground pins must be connected together on the same PCB plane to prevent latchup.
XTALIN	I	46	A 13.5000 MHz crystal should be connected between these pins. The pixel clock output (CLKO) is derived from these pins in conjunction with an internal PLL. XTALIN can be driven from an external clock oscillator as a CMOS input pin. Internally, this is a CMOS inverter tying XTALOUT to XTALIN. If a single-ended oscillator is utilized, this must drive XTALIN and the biasing circuit illustrated in Figure 1-3 must be integrated for XTALOUT.
XTALOUT	O	47	
VAA_OSC	—	48	Crystal oscillator supply pin. This pin should be tied to the VAA power supply.
REG_IN (or VDD1)	—	49	Pass transistor emitter voltage. Tie this pin to emitter of 2N3904 (or similar) NPN transistor, as shown in Figures 3-5 and 3-6.
REG_OUT	—	50	Pass transistor base voltage. Tie this pin to base of 2N3904 (or similar) NPN transistor, as shown in Figures 3-5 and 3-6.
VSS_BG	—	51	Video DAC bandgap ground. All analog and digital ground pins must be connected together on the same PCB plane to prevent latchup.
VAA_BG	—	52	Video DAC bandgap power. All VAA pins and VDD HV must be connected together on the same PCB plane to prevent latchup.
VREF	O	53	Voltage reference pin. A 0.1 μF ceramic capacitor must be used to decouple this pin to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FSADJUST	I	54	Full-scale adjust control pin. A resistor (RSET) with a value of 402 Ω (±1%) connected between this pin and GND controls the full-scale output current on the analog outputs.

Table 1-1. Pin Assignments and Descriptions *(4 of 4)*

Pin Name	I/O	Pin #	Description
COMP	O	55	Compensation pin. A 0.1 μF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to a minimum.
NG_DAC	—	56	Analog circuit GND. All analog and digital ground pins must be connected together on the same PCB plane to prevent latchup.
VAA_DAC	—	57, 58	DAC Analog power. All VAA pins and VDD HV must be connected together on the same PCB plane to prevent latchup.
DACD	O	59	DACD Analog output. A 75 Ω termination resistor, 1% tolerance, with short traces should be attached between this pin and ground for optimal performance. If unused, leave this pin as a no connect.
DACA	O	60	DACA Analog output. A 75 Ω termination resistor, 1% tolerance, with short traces should be attached between this pin and ground for optimal performance. If unused, leave this pin as a no connect.
DACB	O	61	DACB Analog output. A 75 Ω termination resistor, 1% tolerance, with short traces should be attached between this pin and ground for optimal performance. If unused, leave this pin as a no connect.
DACC	O	62	DACC Analog output. A 75 Ω termination resistor, 1% tolerance, with short traces should be attached between this pin and ground for optimal performance. If unused, leave this pin as a no connect.
VSS_DAC	—	63, 64	Common DAC Analog ground pins. All AGND and VSS pins must be connected together on the same PCB plane to prevent latchup.

Table 1-2. Data and Pin Assignments for Multiplexed Input Formats

Rising Edge of CLKI[1]							
IN_MODE[3:0]	**0000**	**0010/0001**	**0101**	**0100**	**1000**	**0110**	**1100**
Pin	**24-Bit RGB Mode**	**15/16-Bit RGB Mode[2]**	**16-Bit YCrCb Mode**	**24-Bit YCrCb Mode**	**Alternate 24-Bit RGB Mode**	**Alternate 16-Bit YCrCb Mode**	**Alternate 24-Bit YCrCb Mode**
P[11]	G4	G2	Cr/Cb7	Cr7	G3	—	Y3
P[10]	G3	G1	Cr/Cb6	Cr6	G2	—	Y2
P[9]	G2	G0	Cr/Cb5	Cr5	G1	—	Y1
P[8]	B7	B4	Cr/Cb4	Cr4	G0	—	Y0
P[7]	B6	B3	Cr/Cb3	Cr3	B7	Cr/Cb7	Cb7
P[6]	B5	B2	Cr/Cb2	Cr2	B6	Cr/Cb6	Cb6
P[5]	B4	B1	Cr/Cb1	Cr1	B5	Cr/Cb5	Cb5
P[4]	B3	B0	Cr/Cb0	Cr0	B4	Cr/Cb4	Cb4
P[3]	G0	—	—	Cb7	B3	Cr/Cb3	Cb3
P[2]	B2	—	—	Cb6	B2	Cr/Cb2	Cb2
P[1]	B1	—	—	Cb5	B1	Cr/Cb1	Cb1
P[0]	B0	—	—	Cb4	B0	Cr/Cb0	Cb0
Falling Edge of CLKI [1]							
IN_MODE[3:0]	**0000**	**0010/0001**	**0101**	**0100**	**1000**	**0110**	**1100**
P[11]	R7	R4	Y7	Y7	R7	—	Cr7
P[10]	R6	R3	Y6	Y6	R6	—	Cr6
P[9]	R5	R2	Y5	Y5	R5	—	Cr5
P[8]	R4	R1	Y4	Y4	R4	—	Cr4
P[7]	R3	R0	Y3	Y3	R3	Y7	Cr3
P[6]	G7	G5[2]	Y2	Y2	R2	Y6	Cr2
P[5]	G6	G4	Y1	Y1	R1	Y5	Cr1
P[4]	G5	G3	Y0	Y0	R0	Y4	Cr0
P[3]	R2	—	—	Cb3	G7	Y3	Y7
P[2]	R1	—	—	Cb2	G6	Y2	Y6
P[1]	R0	—	—	Cb1	G5	Y1	Y5
P[0]	G1	—	—	Cb0	G4	Y0	Y4

FOOTNOTE:

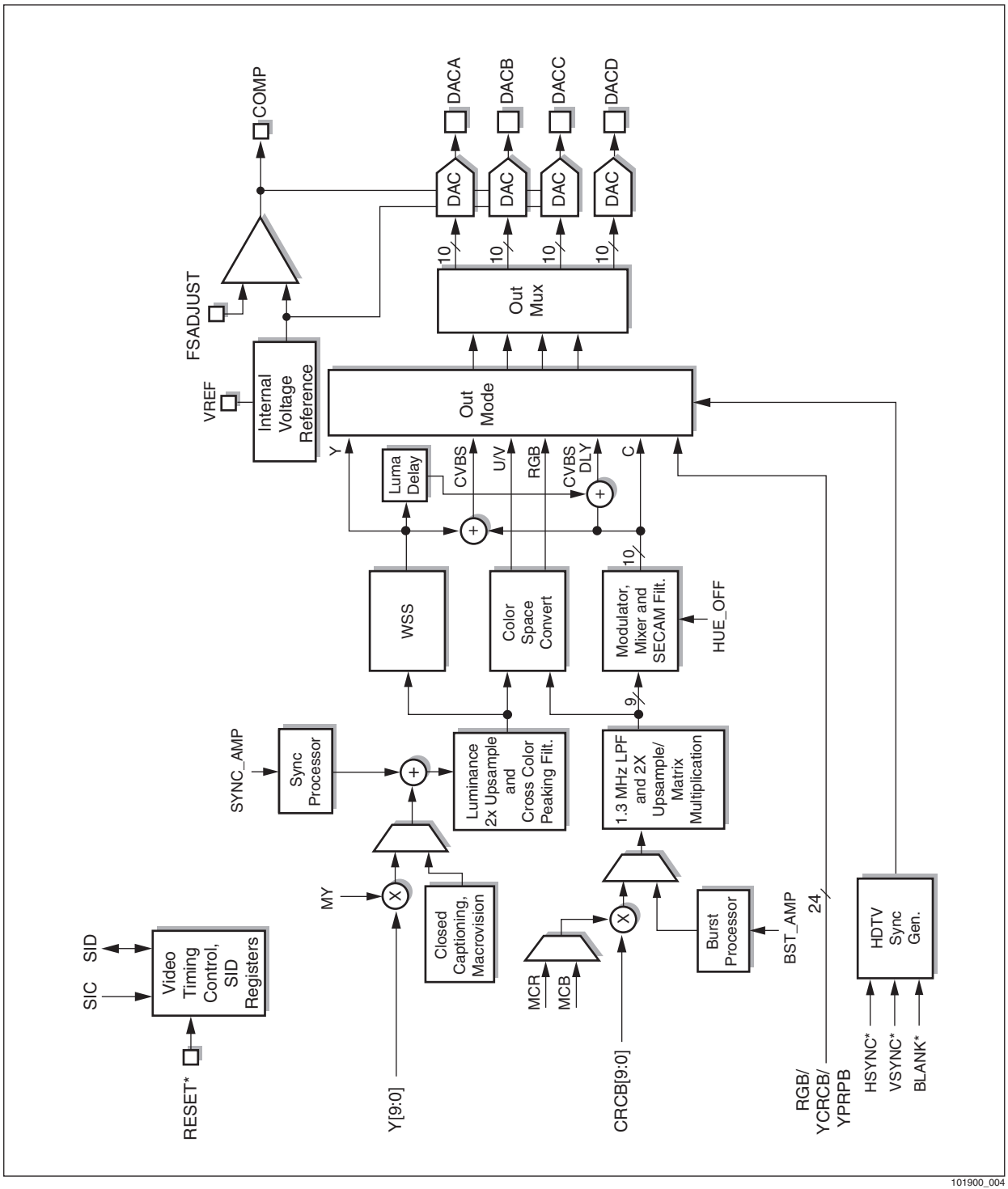
[1] Nonmultiplexed input formats are not supported with CX25874/5. Input formats requiring more than 12 pixel lines should use the CX25890/1/2 DVI encoder or CX25870/1 Video encoder.

[2] G5 is ignored in 15-bit RGB Multiplexed Input Mode.

1.2 Device Block Diagram

Figure 1-2 describes all major internal circuit blocks of the CX25874/5 TV out encoder. Proprietary components of the device are not shown.

Figure 1-2. CX25874/875 Encoder Core Block Diagram



1.3 Device Description

1.3.1 Overview

The CX25874/875 is a video encoder designed for TV output of interlaced and noninterlaced input graphics data. Common applications requiring flicker-filtered TV output include:

- desktop/portable PCs with TV out
- high-definition TVs
- DVD players and set-top boxes
- graphic cards with TV out
- game consoles
- set-top boxes

It incorporates normal and adaptive filtering technology for flicker removal and flexible amounts of overscan compensation for high-quality display of noninterlaced images on an interlaced TV. The CX25874/875 accomplishes this by minimizing the flicker and controlling the amount of overscan so that the entire image is viewable.

The CX25874/875 consists of a Color Space Converter/Flicker Filter engine followed by a digital video encoder. The Color Space Converter/Flicker Filter contains:

- A timing converter
- Various horizontal video processing functions
- Flicker filter and vertical scaler for overscan compensation

The output of this engine feeds into a FIFO for synchronization with the digital video encoder.

The CX25874/875 provides composite (CVBS), S-Video, Component (YC_RC_B or YUV), R/G/B/PAL Euro SCART, VGA R/G/B, or 3-signal analog RGB or YP_BP_R HDTV output. While the encoder is in HDTV output mode, the device will automatically insert trilevel synchronization pulses and vertical synchronizing “broad pulses.” The CX25874/875 is compliant with EIA770-3, SMPTE 274M/293M/296M and supports the most popular ATSC HDTV resolutions including 480p, 720p, and 1080i. Finally, this encoder supports both standard-definition Macrovision® (version 7.1.L1) and high-definition Macrovision (525p copy protection for progressive scan).

1.3.2 Serial Interface

The device includes a 2-wire read and write serial interface for programming the registers in the device. The interface is designed to operate nominally at 3.3 V levels. To ensure that valid serial data is received and transmitted, make sure the VDD_SIO pin is connected to a stable 3.3 V supply, or sub 3.3 V supply matching the low-voltage graphics interface high level. Review Section 3.9 for more details of the encoder’s serial interface.

1.3.3 Low-Voltage Digital Graphics and Serial Interface

The CX25874/5 can receive or transmit signals from/to a graphics controller at any voltage level from 3.3 V (maximum) to 1.1 V (minimum). The most common lower voltage levels are 2.5 V, 1.8 V, 1.5 V, 1.3 V, and 1.1 V. The default input/output voltage preferred amplitude swing for the graphics interface signals (defined as P[11:0], HSYNC*, VSYNC*, CLKI, SLEEP, BLANK*, RESET*, CLKO, XTL_BFO, and FIELD), and serial interface signals (SID, SIC, and ALTADDR) is 3.3 V. This level matches the first and second generation Conexant VGA to TV encoders (Bt868/869 and CX25870/871 respectively) and ensures backwards compatibility. See Table 1-3 for a list of the digital pins that comprise the encoder's low-voltage graphics interface.

For a 3.3 V digital interface, no special configuration steps are necessary. The customer's system should adhere to Figure 3-5. If this is done on power-up, the encoder will automatically expect 3.3 V signal interface.

For a 1.5 V or sub 3.3 V digital interface, several special configuration steps are necessary. First, the customer's system should adhere to Figure 3-6. Second, connect the VDDO (#36 and #11) power supply pins to the lower supply voltage (1.5 V or other). Finally, make sure the graphics controller is configured to send and accept signals at the lower supply voltage.

Adjusting the VDDO pins appropriately controls the input (or output) voltage levels for the P[11:0], CLKI, SLEEP, RESET*, CLKO, XTL_BFO, FIELD and HSYNC*/ VSYNC*, BLANK*, and the GPO [2:0] (in slave interface; EN_BLANKO = 0) digital graphics-related pins.

The VDD_SIO (pin #38) is the supply voltage pin that allows for control of the serial interface signals (SIC, SID, ALTADDR). Since both interface types are independent, it is possible for the data master device to use a 3.3 V serial interface while simultaneously utilizing a sub 3.3 V graphics interface to transfer data to the PC encoder. The REG_IN, REG_OUT pins are associated with the encoder's core voltage and have no influence on the graphics interface nor the serial interface peak-to-peak voltage levels. See Table 1-4 for a list of pins that comprise the encoder's serial interface.

Table 1-3. Digital Pins that Comprise the Encoder's Low-Voltage Graphics Interface

Pin Number	Pin Name	Direction of Pin
1	XTL_BFO	Output
2	Pixel[0]	Input
3	Pixel[1]	Input
4	Pixel[2]	Input
5	Pixel[3]	Input
6	Pixel[4]	Input
7	Pixel[5]	Input
8	Pixel[6]	Input
13	Pixel[7]	Input
14	Pixel[8]	Input
15	Pixel[9]	Input
16	Pixel[10]	Input
17	Pixel[11]	Input
18	HSYNC*	Input or Output
19	VSYNC*	Input or Output
20	FIELD	Output
21	BLANK*	Input or Output
26	SLEEP	Input
27	RESET*	Input
28	GPO [0]	Output
29	GPO [1]	Output
30	GPO [2]	Output
35	CLKI	Input
37	CLKO	Output

Table 1-4. Digital Pins that Comprise the Encoder's Serial Interface

Pin Number	Pin Name	Direction of Pin
39	SID	Input or Output
40	SIC	Input
41	ALTADDR	Input

1.3.4 Reset

There are four reset events possible with this device:

First, if the RESET* pin is held low (between 0.8 V and GND –0.5 V) for a minimum of 20 input pixel clock cycles (equivalent to1 μs if CLKI = 20 MHz), a timing reset and a software reset are performed. This is called a hardware RESET* event. If the RESET* pin is continually held low, the encoder's SIC and SID lines remain high, allowing other devices on the serial bus to receive commands while the CX25874/5 is in its reset state. No serial communication (reads or writes) with the encoder is possible while its RESET* line is held low. In addition, active video from all DACs will completely disappear, and a 27.000 MHz signal will be sent from CLKO while the RESET* line is held down.

Second, a timing reset can be generated by setting the TIMING_RST register bit. In this case, the subcarrier phase is set to zero, and the horizontal and vertical counters are configured to the beginning of VSYNC* of Field 1 (both counters equal to zero).

The third reset event is a software reset. By setting SRESET bit to 1, all registers are configured internally to their default state. The SRESET bit will be cleared back to zero automatically.

The final reset event is a power-on reset occurring immediately after correct VDD, VAA, and ground are first applied to the device. A power-on reset is generated on power-up. The power-on reset generates the same type of reset as the RESET* pin. A time delay circuit is triggered after the supply voltage reaches a value sufficiently high enough for the circuit to operate and then generates the power-on reset. As such, the device may not initialize to the default state unless the power supply ramp rate is sufficiently fast enough. A hardware/pin reset is recommended if the default state is required. This event happens automatically regardless of the type of master device connected to the DENC.

If the CX25874/875 is in the master interface (i.e., encoder sends the syncs to the data master) then after a power-on or pin reset, the encoder and the flicker filter start at line 1, pixel 1 of their respective timing generation. For the encoder this means the odd field is always the first field after a power-on reset, pin reset, or timing reset.

In slave timing interface (encoder is either pseudo-master or pure slave), even though the input is receiving progressive frames that have no field associated with it, the input timing generator keeps track of the frames received. As a result, after every second frame received, a frame sync is sent to the encoder section so that the input and encoder remain synchronized. The frame sync forces the encoder to the beginning of the odd field.

A software reset, which can be generated by setting the SRESET register bit, initializes all the serial interface registers to their default state. As a result, all digital output control pins are three-stated. Registers 0x38 and 0x76 to 0xB4 inclusive are then initialized to autoconfiguration mode 0 (see the Auto Configuration section values). The EN_OUT bit must be set to enable the digital outputs.

A power-on reset, pin reset, or timing reset (register 0x6C, bit 7) causes the input timing generator to send the encoder a frame synchronization pulse setting the encoder to the beginning of the odd field. The first HSYNC*/VSYNC* combination then corresponds to the encoder even field. Then, the second HSYNC*/VSYNC* combination again causes a frame synchronization pulse, and the encoder will start the odd field, and so on and so forth.

NOTE: The GPU (or Data Master device) must issue at least one transition (more preferred) from a 0 to a 1 on CLKI after power-up and before or during the application of the hardware RESET* pulse. Failure to do so will prevent several encoder clocking modes (most notably PLL32CLK) from working properly.

To reiterate, CLKI cannot be left in steady state condition from power-up until after the rising edge of the hardware RESET* pulse. Toggling must occur, and the frequency received at CLKI prior to the end of RESET* must be less than 80 MHz.

1.3.5 Device Initialization

After a non-timing reset event, the CX25874/5 will be configured in autoconfiguration mode 0, pseudo master interface, active video turned off. The device must be programmed through the serial interface to activate a video output (i.e., set EACTIVE bit to 1), and configure the CLKO, HSYNC*, VSYNC*, and FIELD outputs to match the desired interface. The easiest method for accomplishing the initialization phase is to use an appropriate autoconfiguration mode from Appendix C, and switch the interface bits appropriately. (For information on autoconfiguration and interface bits see to Section 1.3.9.)

1.3.6 Clocking Generation and Reference Crystal

Two timing generators control the operation of the encoder. The first generator controls the input timing and processing of image data through the flicker filter and overscan compensation sections to the internal FIFO, which bridges the input and output sections. The output encoder timing block generates the signals for the proper encoding of the video into NTSC, PAL, or SECAM and extracts the processed input pixels from the internal FIFO. The timing generators can receive a clock from either an external crystal oscillator and internal PLL (master, pseudo-master, or slave interface), or from the CLKI pin (slave interface only). The preferred clock source for the timing generation is the internal PLL which uses the XTALIN pin as its reference. The PLL has a main output clock, F_{CLK}, which is defined by the equation that follows later. There is also a secondary output with a different divide ratio so that it is exactly two thirds the frequency of F_{CLK}. Alternately, the pin CLKI can be used as the clock source for the timing generators. Conexant recommends that the encoding clock be generated by an external crystal residing between XTALIN and XTALOUT or a clock oscillator chip driving XTALIN (bias circuit connected to XTALOUT). Register bit EN_XCLK selects the clock source.

Besides the registers that set the various parameters in both the vertical and horizontal direction, the following register bits are used to set the type of video input format.

DIV2—Setting this bit to 1 will change the input from a progressive scan format to an interlaced video format, such as CCIR601. The one exception is for HDTV interlaced format; this bit should remain zero.

DIV2_LATCH—When it is 0, the input data will latch only on the rising edge of clock, as with CCIR601. When it is set to 1, the input data will latch on both edges of the clock, which is useful for a format like interlaced RGB. This bit is only active when DIV2 = 1.

MODE2X—Use this bit for VGA controllers that can only send data on one edge of the input clock. The encoder will only latch pixel data on CLKI's rising edge.

PLL_32CLK—This bit puts the encoder into a clocking mode where the input timing generator still receives the main clock from the PLL, but the output timing now uses the secondary clock. The name derives from the fact that for every three clocks at the input, there are two clocks at the output. This mode is used for standard TV out with all 1024x768 inputs and some 800x600 inputs.

PIX_DOUBLE—This will cause a duplication of each input pixel. This mode is useful for low-resolution formats like 320x240.

EN_XCLK—If set to a logical 0, the internal clock source is selected via the crystal attached to XTALIN/XTALOUT. When the EN_XCLK bit is set to 1, the clock frequency received at the CLKI pin is utilized as the main pixel/encoder clock.

BY_PLL—Setting this bit is not recommended for normal use but only for debug or testing purposes. BY_PLL will bypass the PLL and use the reference clock at the XTALIN pin as the encoder clock source. This bit has a lower precedence than EN_XCLK.

A crystal must be present between XTALIN and XTALOUT pins if the internal clock source is selected. In this case, the CX25874/5's CLK frequency is synthesized by its PLL such that the pixel clock frequency equals

F_{CLK} = Fxtal * {PLL_INT[5:0] + (PLL_FRACT[15:0]/2^{16})}/6

The PLL_LOCK bit is set when the PLL is stable.

When the encoder is the clock master, a delayed version of the clock output from the pin CLKO is returned to the pin CLKI and synchronized with the pixel data. The frequency of this clock is F_{CLK}, except for these two cases:

1. PIX_DOUBLE = 1
2. DIV2 = 1 and DIV2_LATCH = 1.

In these two cases CLKO frequency = ½ F_{CLK}.

The frequency of the video output clock is determined by the mode of operation set by the bits MODE2X and PLL_32CLK. This frequency is used in the SINX/X correction equation detailed in later sections. The following table shows how this clock is derived from the PLL. As mentioned previously, the main PLL output = F_{CLK} and the secondary PLL output = $^2/_3$ $F_{CLK.}$

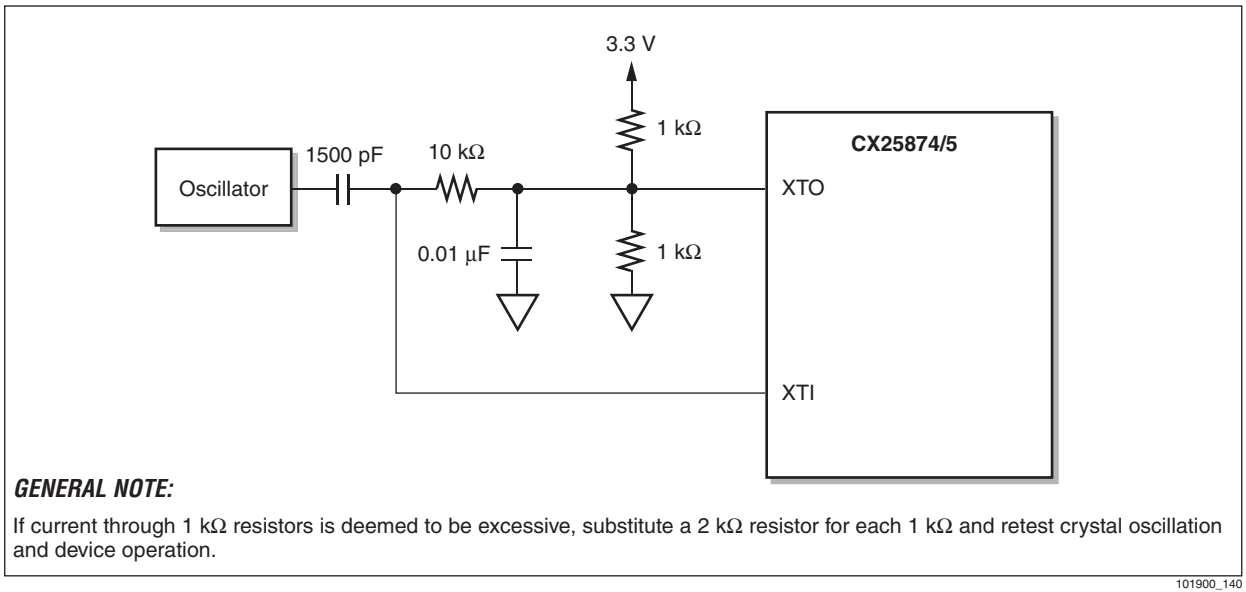
MODE2X	PLL_32CLK	Video Output Clock Frequency
0	0	Main PLL output
0	1	Secondary PLL output
1	0	1/2 main PLL output
1	1	1/2 secondary PLL output

The crystal must be chosen so that the precise line rate for the video standards required can be achieved. This is done to maintain the subcarrier relationship to the line rate and thereby achieve the precise subcarrier frequency required. The crystal oscillator is designed to oscillate from 10 MHz through 25 MHz. A 13.5000 MHz crystal meets the requirements for NTSC, PAL, SECAM, Component YCRCB, SCART, and HDTV video standards. The crystal must be within 50 ppm of the

maximum desired clock rate for NTSC operation, and 25 ppm for any other standard or HDTV video format, across the temperature range (0° to 70° C). If the CX25874/5 is to provide all video outputs selectable through software, the customer must use a crystal with a maximum tolerance across the temperature range of 25 ppm. If a crystal is used, the designer must ensure that the crystal operates with an external load capacitance equal to its specified data sheet listed value (usually C_L). In addition, the external load capacitors used in the crystal circuit must have their ground connections very close to the encoder. Appendix B contains a list of previously tested and recommended crystal vendors.

Optionally, an externally generated 13.5000 MHz clock source may be supplied to the CX25874/5 instead of a crystal. This single-ended clock source can be derived from an external oscillator or dedicated clock generation chip. If an external clock source is used, it should have CMOS label specifications. This 13.5000 MHz clock should be connected to the encoder's XTALIN and XTALOUT pins using the biasing circuit shown in Figure 1-3. Again, the external source must exhibit ±25 ppm or better frequency tolerance. Refer to Section 3.7.5 for more details on clock and color subcarrier stability.

Figure 1-3. Single-Ended Oscillator Biasing Circuit



GENERAL NOTE:

If current through 1 kΩ resistors is deemed to be excessive, substitute a 2 kΩ resistor for each 1 kΩ and retest crystal oscillation and device operation.

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When the PLL_INPUT register bit is set to a logical 1, CLKI is selected as the reference for PLL after it is divided by two. This is a special mode for slave interface with PLL_32CLK = 1. In this mode, set PLL_INT = 12 DEC and PLL_FRACT = 0

If the external clock source is selected (EN_XCLK=1), a clock signal of the desired pixel clock rate must be present at the CLKI pin. The clock must meet the same requirements as above. It is highly recommended that the internal clock be used in order to ensure the output video remains within the specifications defined by the relevant video standard. Any aberration in the source clock is reflected in the color subcarrier frequency of the output video and detracts from the quality of the image on the television.

If the DIV2 register bit is set, this internal clock is divided by two before driving the first timing generator. This is required for interlaced input to interlaced output mode (i.e., CCIR601/DVD and CCIR656 applications).

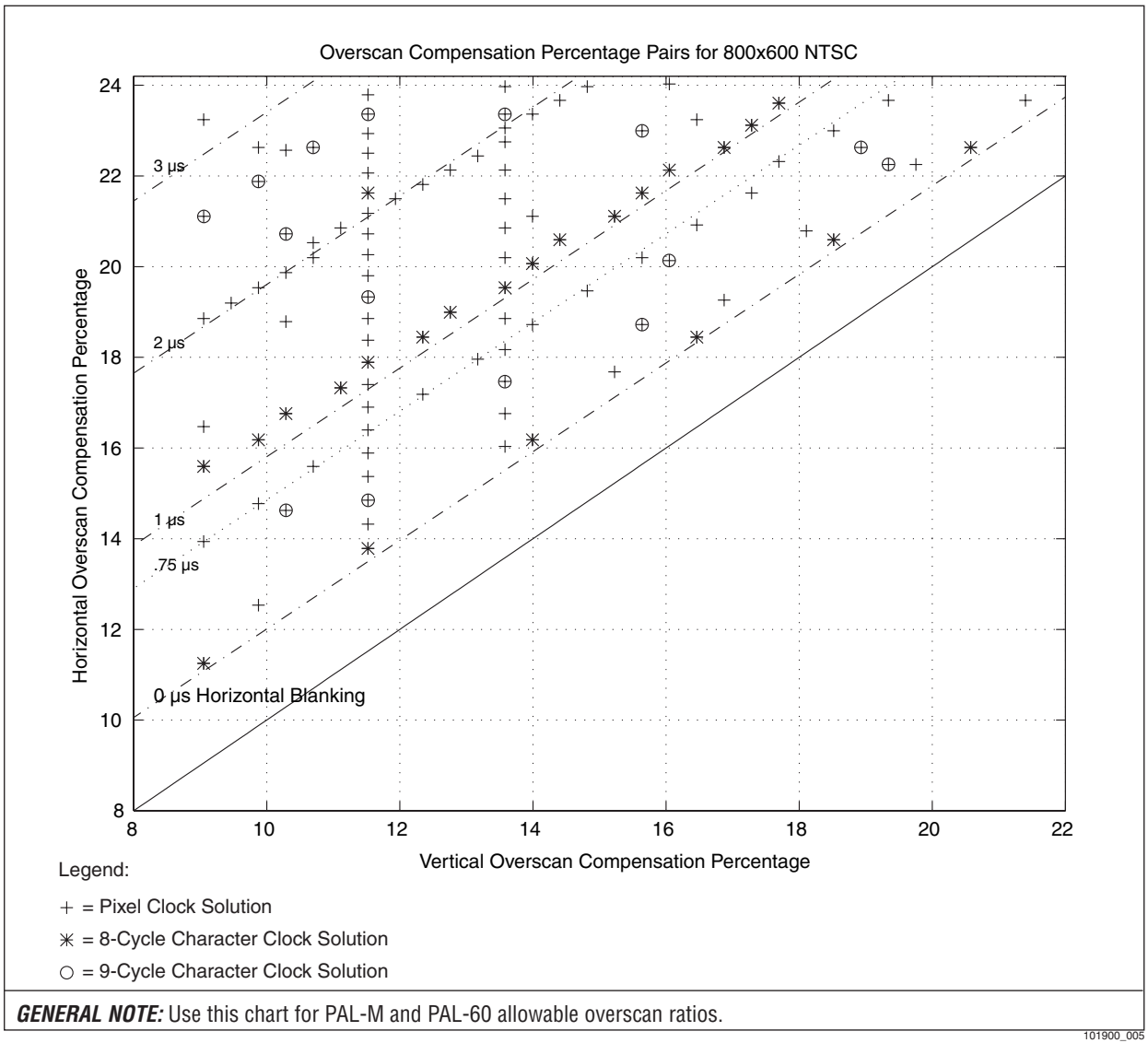
The CLKI pin is the clock used for synchronizing pixel inputs (P[11:0]) with the timing input signals (HSYNC*, VSYNC*, and BLANK*) and normally is a delayed version of the CLKO pin. It can be directly connected to CLKO if desired. Data is registered with this input and re-synchronized to the internal clock. In a multiplexed input mode, both edges of the CLKI input are used. If the MODE2X register bit is set, the internal clock is divided by two, allowing a 2x external clock, and data to be provided on the rising edge only. For proper encoder operation, regardless of the interface chosen, a single-ended oscillator must drive the XTALIN pin (and biasing circuit used, see Figure 1-3) or a crystal must be present between the XTALIN/ XTALOUT ports.

1.3.7 3:2 Clocking Mode for Higher Input Resolutions

All graphics controllers require some finite time for resetting their internal counters to zero, clearing register flags, and any other event that needs to be performed on a line-by-line basis. The sum of time these incidents take are the graphics controller's total horizontal blanking time. The amount of horizontal blanking time varies from one master device to another but it is never less than 0 µs and usually does not exceed 4 µs per digital line.

Figure 1-4 illustrates that when higher active resolutions (i.e., 800x600 or greater), are generated by data master devices that require more horizontal blanking time than the CX25874/5 allows for in standard clocking mode for dual display of certain overscan compensation percentage pairs, a problem can result. For the 800x600 NTSC example, a graphics controller may require a minimum total of 1.25 µs of Horizontal Blanking time per line while clocking a frame with an active resolution of 800x600 to the encoder. If this were the case, the entire set of overscan compensation solutions charted at the 1 µs diagonal plot line (denoted with a dot-dash-dot) and below are made unavailable to the designer. The result is a more limited set of overscan pairs to choose from, and correspondingly less size control for the picture when displayed on a television.

Figure 1-4. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input/NTSC Output



GENERAL NOTE: Use this chart for PAL-M and PAL-60 allowable overscan ratios.

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Since the CX25874/5 contains its unique 3:2 Clocking Mode, the designer does not face this constraint any longer. By choosing an appropriate autoconfiguration mode, which sets the PLL_32CLK bit to 1, and altering the values for various timing registers within the controller and encoder (e.g., H_CLKI = HTOTAL, VLINES_I = VTOTAL, H_BLANKI, V_BLANKI, etc.), the encoder switches into the 3:2 Clock mode. While in this operational state, additional solutions in the overscan-compensation-pairs domain for higher resolutions now exist. In addition, the encoder now allows the data master (e.g., graphics controller) to send digital data to it at a faster rate than is clocked out of the encoder. Specifically, the CX25874/5 begins to transfer pixels out at a rate of [2/3] that of the CLKI input frequency. In other words, the pixel input frequency clocks in data at a ratio of [3:2] or 1½ times faster than the CX25874/5 outputs the analog pixel data. In this mode, the encoder's expansive on-chip FIFO bridges the frequency difference that now exists between the digital-timing input and mixed-signal encoder output blocks of the CX25874/5. The result is a much closer match in the available overscan percentages in the horizontal and vertical

direction for the higher resolutions. This ensures the TV out picture appears more orthogonal where the amount of blanking is nearly equal on all sides of the image.

Since the horizontal blanking time only becomes a critical issue at higher resolutions, the user should use the 3:2 Clocking Mode only when necessary at the 800x600, between 800x600 and 1024x768, and always at the 1024x768 active resolution. For software programming ease, most of the autoconfiguration modes for 800x600 and all for the 1024x768 resolution are 3:2 mode solutions already. The specific modes that use the 3:2 clock feature are contained in Appendix C and summarized in Table 1-5.

Table 1-5. Autoconfiguration Solutions that Utilize 3:2 Clocking Mode

Autoconfiguration Mode #	Active Resolution	Type of Digital Input	Overscan Ratio	Video Output Type
10	1024x768	RGB	Standard	NTSC
11	1024x768	RGB	Standard	PAL-BDGHI
14	1024x768	YCrCb	Standard	NTSC
15	1024x768	YCrCb	Standard	PAL-BDGHI
18	800x600	RGB	Lower	NTSC
22	800x600	YCrCb	Lower	NTSC
26	1024x768	RGB	Lower	NTSC
27	800x600	RGB	Lower	PAL-60
30	1024x768	YCrCb	Lower	NTSC
34	800x600	RGB	Higher	NTSC
40	800x600	RGB	Alternate	NTSC
42	1024x768	RGB	Higher	NTSC
43	1024x768	RGB	Higher	PAL-BDGHI

If the desired overscan ratio is not available via a particular autoconfiguration mode, you should derive a custom 3:2 clock solution via Cockpit (i.e., CX25874/875 register programming tool), or contact your local FAE directly, and ask for a compete register set. If done correctly, a custom higher resolution CX25874/875 register set will have PLL_32CLK (bit 5 of register 0x38) set and adjust its timing registers and signals automatically.

1.3.8 Master, Pseudo-Master, and Slave Interfaces

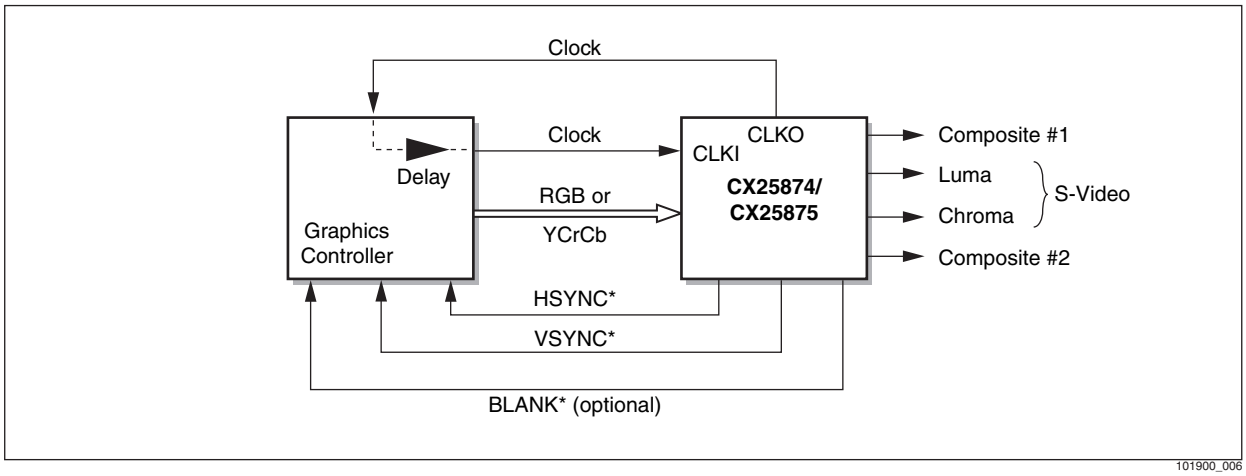
Like its predecessors, the Bt868/869 and the CX25870/1, the CX25874/875 encoders can be operated in three possible interfaces. These connection types are named master, pseudo-master, and slave. The clocking ability of the master device and direction of the timing signals dictate what particular interface is used between the Conexant encoder and graphics controller/data master device.

1.3.8.1 Master Interface

In master interface, CLKO, HSYNC*, VSYNC*, and BLANK*, are generated by the encoder as outputs. These signals' leading edges denote when a new clock period, new line, and new frame starts, respectively. Because the encoder transmits the clock and timing signals, this interface is also referred to as clocking master/timing master.

An illustration of the master interface is shown in Figure 1-5 using the graphics controller as the master device and S-Video and two Composite ports as the video outputs.

Figure 1-5. Operating the Encoder in Master Interface



A minimum of 9 inputs (CLKI and 8 lines for pixel data P[7:0]) and 3 outputs (HSYNC*, VSYNC*, and CLKO) are required for this configuration. The amount of inputs could grow as high as 14 if the 24-bit RGB multiplexed mode with a blank * signal is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

Master interface can only exist if the graphics controller can accept the encoder's reference clock and send back a version of that clock at the same frequency with the pixel data transitions synchronized to CLKI's rising and falling edges. This is accomplished via the VGA encoder's clock output (CLKO) and clock input (CLKI) ports.

1.3.8.2 Reason for BLANK*

If the graphics controller possesses pixel-based resolution (i.e., pixels are only a single pixel clock wide) then the encoder does not have to transmit or receive the BLANK* signal. However, for graphics controllers that are character clock based, a BLANK* signal is necessary.

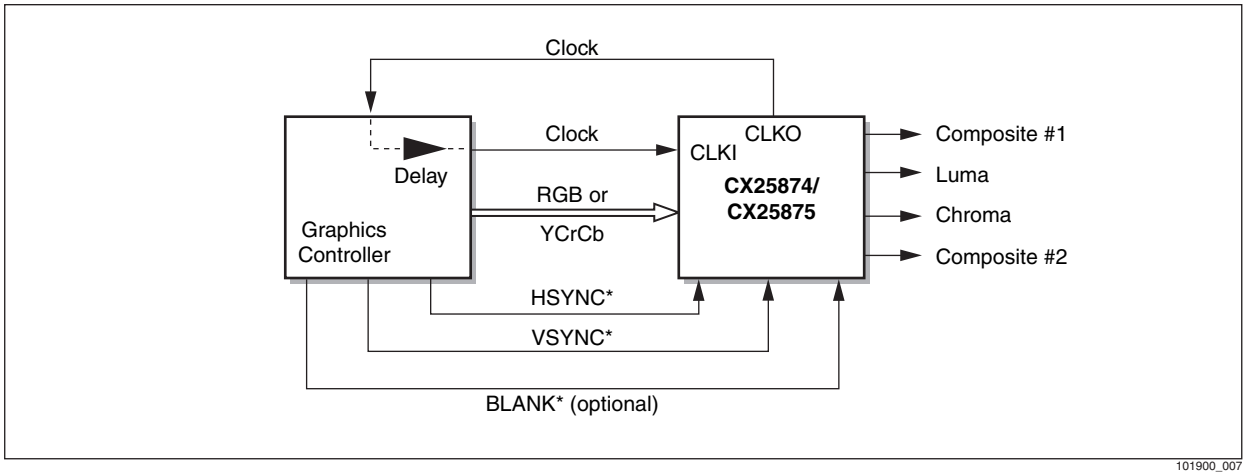
The BLANK line is necessary because a character clock is actually 8 or 9 pixel clocks in duration. This causes several pixel clocks to elapse, resulting in an erroneous delay prior to the next HSYNC* being observed by the encoder and the next line starting. The only method of compensating for this delay is for character clock based controllers to use the BLANK* signal. This signal is required in the physical interface to indicate the exact location of the first active pixel on each line.

1.3.8.3 Pseudo-Master Interface

In pseudo-master interface, the encoder generates a clock reference signal, CLKO as an output. This signal's purpose is to inform the graphics controller the exact frequency at which the data must be sent to the encoder. Timing signals—HSYNC*, VSYNC*, and BLANK*—are received by the encoder as inputs. The leading edges of these signals denote when a new clock period, new line, and new frame starts, respectively. Because this connection scheme shares mastering responsibilities, the interface is also named clocking master/timing slave.

Figure 1-6 provides an illustration of the pseudo-master interface using the graphics controller as the timing master device.

Figure 1-6. Operating the Encoder in Pseudo-Master Interface (Default Interface at Power-Up)



A minimum of 11 inputs (CLKI, HSYNC*, VSYNC*, and 8 lines for pixel data P[7:0]) and 1 output (CLKO) are required for this configuration. The amount of inputs could grow as high as 16 if the 24-bit RGB multiplexed mode is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

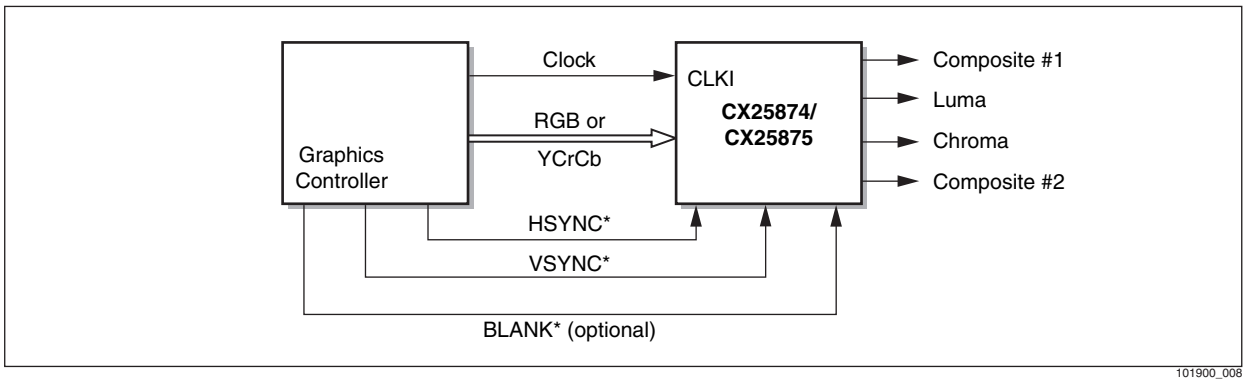
Pseudo-master interface can only exist if the graphics controller can accept the encoder's reference clock and send back a version of that clock at the same frequency with the pixel data transitions synchronized to CLKI's rising and falling edges. This is accomplished via the VGA encoder's clock output (CLKO) and clock input (CLKI) ports.

1.3.8.4 Slave Interface

In slave interface, no output signals are generated by the encoder. The CX25874/875 relies strictly on the graphics controller to send clock and timing signals to trigger when a new clock period, new line, and new frame starts. Because no frequency reference signal is used (CLKO), the master device must pre-program the encoder with an appropriate register set so the encoder expects data at the specific digital pixel rate prior to actually receiving the data. In addition, the timing signals must be shaped so they adhere to the appropriate slave interface timing diagrams illustrated in Section 4.4. Due to the added complexity of this interface, Conexant recommends its use only as a final option.

The slave interface is illustrated in Figure 1-7 using the graphics controller as the master device and S-Video and two Composite ports as the video outputs.

Figure 1-7. Operating the Encoder in Slave Interface



A minimum of 11 inputs (CLKI, HSYNC*, VSYNC*, and P[7:0]) are required for this configuration. The amount of inputs will increase to 15 (without BLANK*) or 16 (with BLANK*) if 24-bit multiplexed RGB mode is chosen as the Input Pixel Mode (i.e., IN_MODE[3:0] = 0000) by the designer.

It is highly recommended that the device operate in master or pseudo-master interface to ensure that the input and output video streams remain synchronized. If either the master device, supplying the HSYNC* and VSYNC* inputs, or the encoder, which receives the data, is not correctly programmed, the output image will lose lock with the input. By running the CX25874/875 in either clock master interface, any timing errors that occur can be absorbed to some extent by the expansive on-board FIFO, and synchronization problems do not occur.

1.3.8.5 Slave Interface Without a Crystal

Since PAL and SECAM televisions are especially strict in terms of accepting color subcarrier frequencies with more than 25 ppm error (i.e., Fsc ± 338 Hz using a crystal of 13.500 MHz), it is critical that the data master maintain a very high level of accuracy and frequency consistency within the incoming pixel clock in slave interface. In numerical terms, this means that the incoming clock (tied to CLKI) should always remain within a window of {ideal CLKI} ± 25 ppm. As an example, for 640x480 PAL autoconfiguration mode #1, CLKI would have to reside in the range [29.499670 MHz < ideal CLKI = 29.500008 MHz < 29.500746 MHz]. NTSC televisions have slightly more tolerance in terms of the color subcarrier frequency deviation. Most consumer NTSC sets can accept pixel clock rates with up to 50 ppm error (i.e., Fsc ± 675 Hz using a crystal of 13.500 MHz) while still maintaining color within the picture. However, it is still important that the data master maintain a high level of accuracy for the incoming clock for this SDTV format as well. In numerical terms, for 640x480 NTSC autoconfiguration mode #0, the pixel clock (CLKI) would have to reside in the range [28.195118 MHz < ideal CLKI = 28.195793 MHz < 28.196468 MHz].

Tight control of the incoming digital clock ensures that the CX25874/5 generates an analog Fsc (color subcarrier) of 4.433618 MHz ± 338 Hz for PAL-BGHI or 4.250000 / 4.406250 MHz ± 338 Hz for SECAM or 3.579545 MHz ± 675 Hz for NTSC. Actual testing has found that excursions outside this range eventually result in a loss of color for PAL, SECAM, and NTSC consumer televisions.

Often, the only reason that slave interface is used is because the data master or GPU driving the encoder is clock-limited and cannot receive and process the incoming clock from the DENC (i.e., CLKO). As a result, the GPU must use its own internal PLL and transmit the pixel clock frequency needed by the encoder for that autoconfiguration or other TV Out mode. Unfortunately, because the encoder's PLL (m/n) ratio and resolution far exceeds the PLL capability of most GPUs, pixel clock frequency mismatches commonly occur in between what the GPU sends versus what the DENC needs for that particular mode. This mismatch often causes color to be lost in an otherwise stable and synchronized TV out picture because the color subcarrier frequency is skewed by an amount proportional to the difference in frequencies.

Fortunately, color can be re-established so long as the GPU can generate a pixel clock (CLKI) frequency within $\pm$ 1 MHz. of the CLKI frequency normally needed by the encoder to support the desired autoconfiguration or other valid custom mode. If this can be done, extra registers (MSC[31:0], PLL_INT[5:0], and PLL_FRACT[15:0]) will also need to be reprogrammed in accordance with the procedures and tables listed in Section 1.3.10, "Adaptations for Clock-Limited Master Devices" of this data sheet. Once these steps have been successfully executed, an accurate color subcarrier frequency will be produced by the CX25874/5 and colorful PAL, SECAM, or NTSC analog output will be seen.

Occasionally, fine-tuning and hand-adjustment of registers 0xAE (MSC[7:0]) and 0xB0 (MSC[15:8]) are required as a final step to fully dial in and remove errors in the color subcarrier frequency. Consult your local Conexant representative for any required technical assistance.

1.3.9 Autoconfiguration and Interface Bits

The default operation of the encoder is tied into its 48 autoconfiguration modes. Autoconfiguring the device occurs when bits CONFIG[5:3] and CONFIG[2:0] in register 0xB8 are programmed to any state from 000000 to 101111. At the conclusion of this serial write, default values are copied from the CX25874/5's internal ROM into the most important timing registers with indices 0x38 and 0x76 to 0xB4, inclusive. All other registers are not changed at the conclusion of an autoconfiguration mode command.

After an autoconfiguration command, the CX25874/5 device remains in the same interface it was in before the command execution. The lone exception to this is autoconfiguration modes #44 and #31, which switch the encoder into pseudo master interface. Depending on which autoconfiguration mode# was initiated, the CX25874/5 will expect to receive either a 320x200, 320x240, 640x400, 640x480, 720x400, 720x480, 720x576, 800x600, or 1024x768 active digital input frame and output a NTSC or a PAL composite and/or S-video signal. See Table 2-5 for a description of CONFIG[5:0] and Appendix C for more detail on each autoconfiguration mode.

Using an autoconfiguration mode is the easiest method for bringing up the most popular desktop, game/Direct X, DOS boot-up screen, and DVD resolutions. This is true regardless of the interface used between the encoder and graphics controller. To turn the direction of the SYNCs around and/or change the interface, simply reprogram the encoder via several serial writes.

The bits that control the interface are SLAVE, EN_BLANKO, EN_DOT, and EN_OUT. Since the abilities of graphics controllers vary greatly, Tables 1-6 through 1-11 have been compiled to explain the relationship between the Interface bits and the actual interface itself. Even more permutations of the following interfaces are possible but Tables 1-6 through 1-11 capture the six most popular architectures and bit settings.

Table 1-6. Master Interface without a BLANK* Signal (Input or Output)

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb[1] of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb[2] of Register 0xC4)
MASTER BLANK* is an output from the encoder or BLANK* is NOT included as part of the interface.	0	1	0	1
FOOTNOTE: (1) MSb = Most Significant Bit (2) LSb = Least Significant Bit				

- The state of the SLAVE bit dictates whether the CX25874/875 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. In other words, SLAVE will determine whether the overall interface is master or pseudo-master. The SLAVE bit allows the graphics controller vendor to switch between master video timing and slave video timing through software.
- EN_BLANKO is high (=1), signifying the CX25874/875's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25874/875 to use its internal counters to determine the active versus the blanking regions.

- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25874/875 and also enables HSYNC* and VSYNC* outputs.

Table 1-7. Master Interface with a BLANK* Input to the CX25874/875

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
MASTER BLANK* SIGNAL transmitted to the encoder and received as an input.	0	0	1	1

- The state of the SLAVE bit dictates whether the CX25874/875 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. In other words, SLAVE will determine whether the overall interface is master or pseudo-master. The SLAVE bit allows the graphics controller vendor to switch between master video timing and slave video timing through software.
- EN_BLANKO is low (= 0), signifying the CX25874/875's BLANK* port is an input.
- EN_DOT = 1 telling the CX25874/875 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and where the blanking region starts (falling edge).
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25874/875 and also enables HSYNC* and VSYNC* outputs.

Table 1-8. Pseudo-Master Interface without a BLANK* Signal (Input or Output) to the CX25874/875 (Default at Power-Up)

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
PSEUDO MASTER BLANK* is NOT included as part of the interface.	1	1	0	1

- SLAVE bit = 1 so the CX25874/875 is the video timing slave. It expects to receive the syncs from the graphics controller.
- EN_BLANKO is high (=1), signifying the CX25874/875's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25874/875 to use its internal counters to determine the active versus the blanking regions.
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25874/875.
- Interface of CX25874/5 encoder after power-up.

Table 1-9. Pseudo-Master Interface with a BLANK* Input to the CX25874/5

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)
PSEUDO MASTER BLANK* SINGAL transmitted to the CX25874/5 and received as an input.	1	0	1	1

- SLAVE bit = 1 so the CX25874/875 is the video timing slave. It expects to receive the syncs from the graphics controller.
- EN_BLANKO is low (= 0), signifying the CX25874/875's BLANK* port is an input.
- EN_DOT = 1 telling the CX25874/875 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and where the blanking region starts (falling edge).
- EN_OUT = 1 ensures there is a clock output (CLKO) from the CX25874/875.

Table 1-10. Slave Interface without a BLANK* Signal (Input or Output)

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)	EN_XCLK (MSb of Register 0xA0)
SLAVE BLANK* is NOT included as part of the interface.	1	1	0	0	1

- After autoconfiguration mode #28 or #29, the CX25874/875 expects active low VSYNC* and HSYNC* signals from the controller. The format of pixels at the input of the encoder needs to be 24-bit YCrCb multiplexed unless modifications are made to the IN_MODE[3:0] 4-bit sequence.
- In addition to Table 1-10, another bit must be programmed manually with this interface. The most significant bit of CX25874/875 register 0xA0 must be set. This guarantees that EN_XCLK is high (=1) which will allow the CX25874/875 to accept CLKI as the pixel clock source.
- SLAVE bit = 1 means the CX25874/875 is the video timing slave. It expects to receive the syncs from the graphics controller. Since the encoder is in slave interface, the HSYNC* and VSYNC* outputs will be three-stated, and the encoder will be set up to receive these timing signals from the graphics controller.
- EN_BLANKO is high (=1), signifying the CX25874/875's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0, telling the CX25874/875 to use its internal counters to determine the active versus the blanking regions.
- EN_OUT = 0, ensures the clock output port (CLKO) is three-stated from the encoder.

Table 1-11. Slave Interface with a BLANK Input to the CX25874/875*

Interfaced Used	SLAVE (Bit 5 of 0xBA)	EN_BLANKO (MSb of Register 0xC6)	EN_DOT (Bit 6 of Register 0xC6)	EN_OUT (LSb of Register 0xC4)	EN_XCLK (MSb of Register 0xA0)
SLAVE BLANK* SIGNAL transmitted to the CX25874/875 and received as an input.	1	0	1	0	1

- After autoconfiguration mode #28 and #29, the CX25874/875 expects active low VSYNC* and HSYNC* signals from the controller. The format of pixels at the input of the encoder needs to be 24-bit YCrCb multiplexed unless modifications are made to the IN_MODE[3:0] 4-bit sequence.
- In addition to Table 1-11, another bit must be programmed manually with this interface. The most significant bit of CX25874/875 register 0xA0 must be set. This guarantees that EN_XCLK will be high (=1) which will allow the CX25874/875 to accept CLKI as the pixel clock source.
- SLAVE bit = 1 so the CX25874/875 is the video timing slave. It will expect to receive the syncs from the graphics controller. Since the encoder is in slave interface, then the HSYNC* and VSYNC* outputs will be three-stated, and the CX25874/875 will be set up to receive these timing signals from the graphics controller.
- EN_BLANKO is low (= 0), signifying the CX25874/875's BLANK* port is an input.
- EN_DOT = 1, telling the CX25874/875 to use the BLANK* signal it is receiving to determine where active video starts (rising edge of BLANK*) and the HACTIVE register to denote where the blanking region starts.
- EN_OUT = 0: This will ensure the clock output port (CLKO) is three-stated from the encoder.

NOTE: Autoconfiguration Mode #28 for NTSC DVD Playback and Mode #29 for PAL DVD Playback place the encoder into slave CCIR601-compliant interface where it expects a BLANK* input and YCrCb digital input format. The EN_XCLK bit = 1 in these modes as well.

1.3.10 Adaptations for Clock-Limited Master Devices

Ideally, the graphics controller or proprietary ASIC, in combination with the CX25874/875, operates in either master or pseudo-master interface. Occasionally, using either of the clock master configurations is not possible because the master device does not have the capabilities of receiving a clock from the encoder, nor can it synchronize the digital data with this clock on its return. If either limitation exists, only slave interface can be used for the system configuration. Often, within the slave interface, the data master can only generate certain discrete clock frequencies. This means the encoder has to make extra accommodations for proper Standard-Definition TV (SDTV) out to be displayed.

Fortunately, the encoder does have the flexibility to adapt to almost any incoming clock frequency in the range from 20 MHz to 80 MHz. All that is required is to follow the procedure in Table 1-12, which forces the encoder to accept a frequency through CLKI that does not match any CX25874/875 autoconfiguration frequency. Once the CX25874/875's 4-byte wide MSC register is reprogrammed accordingly, the result is the generation of the correct color subcarrier frequency for NTSC or PAL and corresponding proper S-Video or Composite TV output.

Tables 1-12 and 1-13 contain the procedures required for the encoder to accept a frequency through CLKI that is not equal but is close to the chosen CX25874/875 autoconfiguration mode clock frequency. Completion of the steps contained in the two tables will modify the MSC register and PLL_INT and PLL_FRACT registers correctly and thus produce an accurate NTSC or PAL analog output.

Table 1-12. Adjustment to the Encoder's MSC Registers

1. What is input frequency to CX25874/875's CLKI input from data master?
2. Depending on answer to step 1, find an autoconfiguration mode that has a frequency close to the incoming input frequency (within 1 MHz is preferred).
3. Look up the clock frequency for the chosen autoconfiguration mode in Appendix C.
4. Determine the scaling factor 'x' where

   x = input frequency to CLKI input (usually from data master) / autoconfiguration mode frequency as specified in Appendix C
5. Determine the autoconfiguration mode's MSC[31:0] value in hex by reading back the CX25874/875's registers; 0xB4(=MSb), 0xB2, 0xB0, 0xAE(=LSb). These register values can also be found by looking them up in Appendix C. The values determined will have to be cascaded together.
6. Convert the MSC[31:0] 4-byte hexadecimal value to decimal.
7. Divide the total found from step 6 by the scaling factor 'x' found from step 4.
8. Convert the answer from step 7 to the hexadecimal format. This value should be comprised of a total of 4 bytes. The most significant byte will likely not change from the previous value in register MSC[31:24]. Other MSC values may not change either but the least significant bytes should have definitely been modified.
9. Program the bytes determined from step 8 into the CX25874/875's MSC[31:0] registers. Write these bytes in order to registers 0xB4 (most significant byte = MSC[31:24]), 0xB2, 0xB0, and 0xAE (least significant byte = MSC[7:0]).

Table 1-13. Adjustment to the PLL_INT and PLL_FRACT Registers

1. What is input frequency to CX25874/875's CLKI input from data master?
2. Depending on answer to step 1, find an autoconfiguration mode that has a clock frequency close to the incoming CLKI frequency (within 1 MHz is preferred).
3. Look up the desired clock frequency for the chosen autoconfiguration mode in Appendix C.
4. Determine the scaling factor 'x' where:
   x = input frequency to CLKI input (usually from data master) / autoconfiguration mode frequency as specified in Appendix C
5. Determine the PLL_INT value in hex by reading back the CX25874/875's register 0xA0 for that autoconfiguration mode. This register value can also be found by looking it up in Appendix C.
6. Convert the PLL_INT register value to decimal.
7. Multiply the answer found in step 6 by $2^{16} = 65536$.
8. Determine the PLL_FRACT value in hex by reading back the CX25874/875's register 0x9E and 0x9C. These two registers cascade to form the PLL_FRACT[15:0] 2-byte value. These register values can also be found by looking them up in Appendix C.
9. Convert the 2-byte PLL_FRACT register value to decimal.
10. From steps 7 and 9, add the PLL_INT and PLL_FRACT decimal values.
11. Multiply the total found from step 10 by the scaling factor 'x' found from step 4.
12. Convert the answer from step 11 to the hexadecimal format. The value should be comprised of a total of three bytes. The most significant byte will likely be the original PLL_INT[7:0] byte from step 2.
13. Program the bytes determined from step 12 into the CX25874/875's PLL_INT[7:0] and PLL_FRACT[15:0] registers. The most significant byte from step 12 is the new PLL_INT value. Write this to register 0xA0. The 2 least significant bytes from step 12 is the new PLL_FRACT value. Write these bytes in order to registers 0x9E and 0x9C respectively.

1.3.11 Input Formats

The device can convert a wide range of input formats to analog standard-definition video TV outputs. The input can be either noninterlaced or interlaced active digital data from a minimum of 320x200 to a maximum of 1024 x 768 pixels per frame for standard TV outputs. Many other nonstandard input formats can be encoded as well. For detailed information on the CCIR601 mode, please refer to the *DVD Movie Playback Architecture and Solutions Application Note*. This application note can be obtained from your local Conexant Systems sales office.

For instructions on how to display nonstandard resolutions on the TV, request the *Supporting TV Out with Non-Standard Graphics Input Resolutions Application Note* from your local Conexant Systems sales office. Your local Conexant FAE can also offer assistance in generation of encoder register sets to support nonstandard resolutions.

1.3.12 Input Pixel Timing

The device can accept the input data in either RGB or YCrCb digital formats. Data can be input either a full pixel at a time clocked in on the rising edge of CLKI only (mode 2x = 1), or in various multiplexed modes, using both edges of CLKI.

In YCrCb format, either 24-bit 4:4:4 data or 16-bit 4:2:2 data can be input. In RGB format, either 15-bit 5:5:5, 16 bit 5:6:5, or 24-bit RGB can be input. In 16-bit 4:2:2 YCrCb input format, multiplexed Y, Cr, and Cb data is input through the P[11:4] or P[7:0] input pins. The Y data is input on the falling edge of CLKI. The Cr/Cb data is input on the rising edge of CLKI. The Cb/Y/Cr/Y sequence begins at the first active pixel. In 24-bit 4:4:4 YCrCb input format, multiplexed Y, Cr, and Cb data is input through the P[11:0] inputs. Both the rising and falling edge of CLKI sample the input data.

In RGB input format, input data is sampled as 12 bits at a time in 24-bit RGB format or 8 bits at a time in 15/16 bit RGB format on both the rising and falling edge of CLKI. Table 1-2 shows the data pin assignments for all available multiplexed input formats.

In addition, several 24-bit and 16-bit alternate multiplexed data formats exist for maximum flexibility. See Table 1-2 for these pin-to-bit assignments.

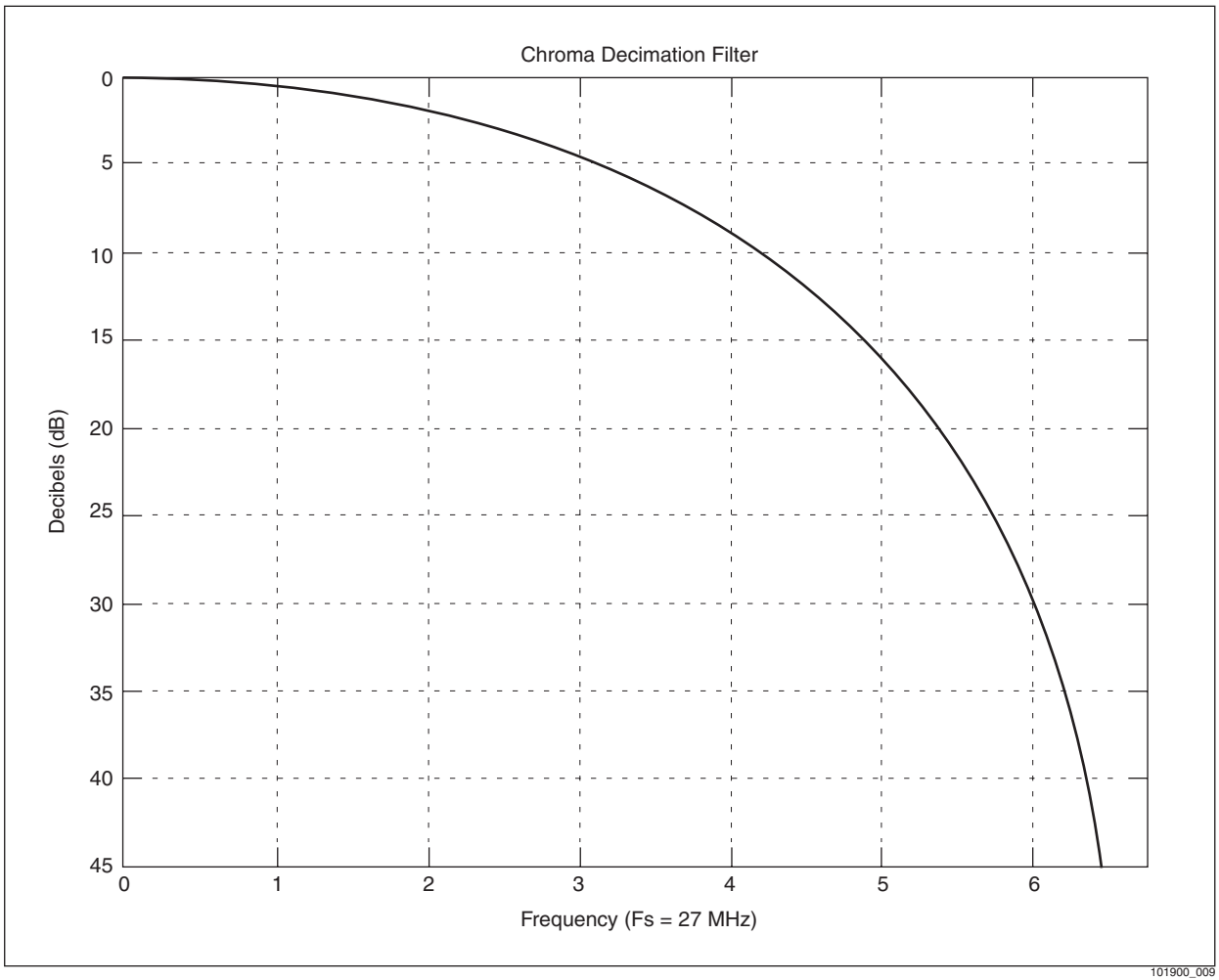
1.3.13 YCrCb Inputs

With the encoder's IN_MODE [3:0] set to YCrCb mode, the encoder must receive digital component YCrCb data as an input. If this occurs, the encoder will convert the YCrCb input to an internal Y/R-Y/B-Y for further processing through the device. Y has a nominal range of 16–235; Cr and Cb have a nominal range of 16–240, with 128 (80 hex) equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

This encoder can also receive either standard YCrCb or HDTV YPrPb digital data for conversion into RGB or YP_RP_B HDTV outputs. It is critical that either pseudo-master or slave interface be used for conversion to HDTV as well.

Figure 1-8 illustrates the frequency response of the sub-sampling process. If 4:4:4 data is input, it is subsampled to 4:2:2 prior to overscan compensation and flicker filtering.

Figure 1-8. Decimation Filter Response at Sampling Frequency (Fs) of 27 MHz



The resulting 4:2:2 output must then be converted to YUV values and then scaled for the output range of the DACs. The MY, MCR, and MCB registers must be programmed to perform this conversion. The scaling equations are as follows:

$MY = (int)\ [V100/(219.0 * V_{FS}) * 2^{16} + 0.5]$

$MCR = (int)[(128.0/127.0) * V_{100} * 0.877/(224.0 * V_{FS} * 0.713 * sinx) * 2^{16} + 0.5]$

$MCB = (int)[(128.0/127.0) * V_{100} * 0.493/(224.0 * V_{FS} * 0.564 * sinx) * 2^{16} + 0.5]$

where: V_{100} *= 100% white voltage (0.661 V for NTSC, 0.7 V for PAL/SECAM)*
V_{FS} *= Full scale output voltage (1.28 V)*

F_{sc} = color subcarrier frequency (see Table A-2)

F_{CLK} *= Analog pixel rate*

$Sinx = Sin\ (\pi \cdot F_{SC}/F_{CLK})/(\pi \cdot F_{SC}/F_{CLK})$

1.3.14 RGB Inputs

With IN_MODE[3:0] set to a RGB mode, the encoder must receive digital gamma-corrected RGB data as an input. If this occurs, the RGB data will be converted to Y/R-Y/B-Y as follows:

$$Y[9:0] = INT(0.299 * 2^{10} * R[7:0]) + INT(0.587 * 2^{10} * G[7:0]) + INT(0.114 * 2^{10} * B[7:0]) + 2^{7}] * 2^{-8}$$
$$0 \leq Y[9:0] \leq 1023$$

For 15- and 16-bit RGB input formats, individual R, G, and B values are left justified to eight bit numbers.

After the initial conversion, the Y/R-Y/B-Y values are sub-sampled to 4:2:2 data prior to overscan compensation and flicker filtering.

The resulting 4:2:2 output must then be converted to YUV values and then scaled for the output range of the DACs. The MY, MCR, and MCB registers must be programmed to perform this conversion. The scaling equations are:

$$MY = (int)[V_{100}/(255 * V_{FS}) * 2^{16} + 0.5]$$
$$MCR = (int)[(128.0/127.0) * V_{100} * 0.877/(127 * V_{FS} * sinx) * 2^{15} + 0.5]$$
$$MCB = (int)[(128.0/127.0) * V_{100} * 0.493/(127 * V_{FS} * sinx) * 2^{15} + 0.5]$$

where: V_{100} = 100% white voltage (0.661 V for NTSC, 0.7 V for PAL)
V_{FS} = Full scale output voltage (1.28 V)

F_{sc} = color subcarrier frequency (see Table A-2)

F_{CLK} = analog pixel rate

$Sinx = Sin\ (\pi\ F_{SC}/F_{CLK})/(\pi\ F_{SC}/F_{CLK})$

For SECAM formulas review the SECAM section.

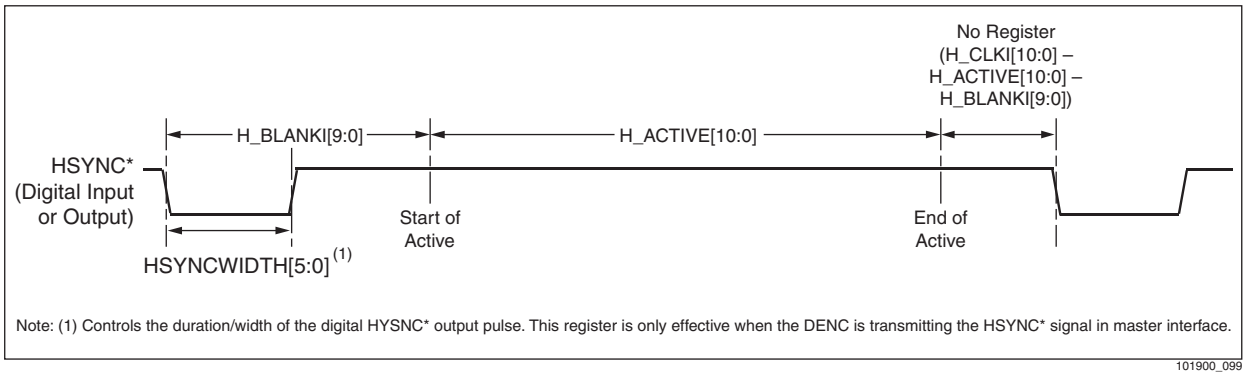
This encoder can also receive RGB digital data for conversion to RGB or YP_RP_B HDTV outputs. It is critical that either pseudo master or slave interface be used for conversion to HDTV as well.

1.3.15 Input Pixel Horizontal Sync

The HSYNC* pin provides line synchronization for the pixel input data. It is an output in master interface and an input in slave and pseudo-master interface. In the master interface, it is a pulse two CLKI cycles (by default) in duration whose leading edge indicates the beginning of a new line of pixel data. The period between two consecutive HSYNC* pulses is H_CLKI CLK cycles. The first active pixel should be presented to the device H_BLANKI minus the internal pipelined clock (5 clock cycles) after the leading edge of HSYNC*. The next H_ACTIVE pixels are accepted as active pixels and used in the construction of the output video. In the slave interface the exact number of clocks per line (H_CLKI) must be provided as calculated for the desired overscan ratio. Only the leading edge of HSYNC* is used, and the low period of the pulse must be at least two CLKI cycles in duration. HSYNC* is clocked into the encoder by the rising edge of CLKI.

The polarity of the HSYNC* signal is changed by the HSYNCI register bit. The default convention is active low. The HSYNCWIDTH register controls the duration/width of the digital HSYNC output pulse when the interface is master. Figure 1-9 illustrates the relationship between all horizontal timing registers. See Figures 4-1 through 4-8 for additional timing details.

Figure 1-9. Horizontal Timing Register Relationship—CX25874/5 Encoder



Note: (1) Controls the duration/width of the digital HYSNC* output pulse. This register is only effective when the DENC is transmitting the HSYNC* signal in master interface.

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1.3.16 Input Pixel Vertical Sync

The VSYNC* pin provides field synchronization for the pixel input data. It is an output in master interface, and an input in the slave and the pseudo-master interfaces.

For noninterlaced input timing in master interface, VSYNC* is a pulse one horizontal line time in duration whose leading edge indicates the beginning of a frame of input pixel data. The leading edge coincides with the leading edge of HSYNC*. The period between two consecutive pulses is V_LINESI horizontal lines. The first line of active data should be presented to the device V_BLANKI lines after the leading edge of VSYNC*. The next V_ACTIVEI lines are accepted as active lines and used in the construction of the output video.

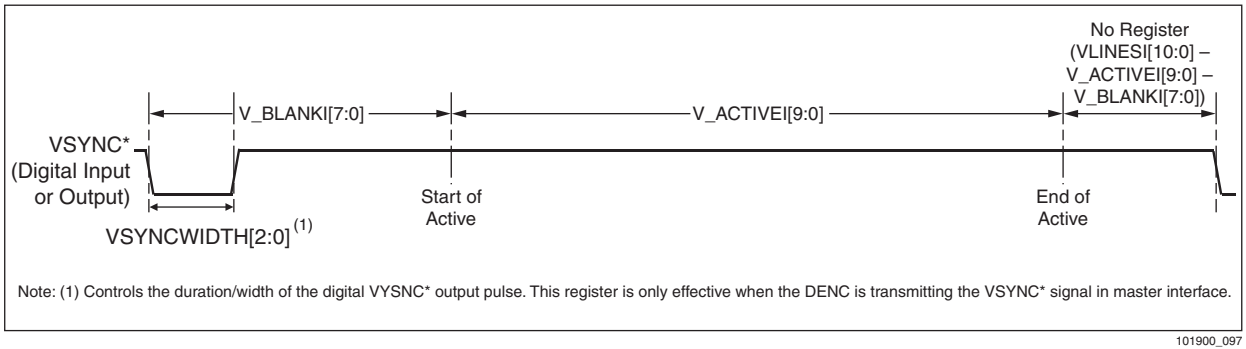
The PC encoder disregards lines after the leading edge of VSYNC* but before VSYNC* + V_BLANKI lines by not encoding them. In slave interface, the period must be exactly the frame rate of the desired video format. Only the leading edge of the VSYNC* is used, and the high and low duration must be at least two CLKI cycles. The beginning of the frame of data is indicated by the next leading edge of HSYNC* coincident with or after the leading edge of VSYNC*.

For interlaced input timing, only the slave interface is supported. The period must be exactly the frame rate of the desired video format. If the leading edge of HSYNC* and VSYNC* are coincident, that indicates the input is in odd field, and the internal line counter is reset to line 1 at the leading edge of VSYNC*. If the leading edges of HSYNC* and VSYNC* are not coincident, and separated by a minimum of two CLKI cycles, this indicates the input is an even field. In this case, the internal line counter is reset to line 2 at the beginning of the next line. Only the leading edge of VSYNC* is used, and the high and low VSYNC* width must be at least two CLKI cycles. VSYNC* is clocked in by the rising edge of CLKI.

The polarity of the VSYNC* input and output can be programmed by the VSYNCI register bit. The default convention is active low. The VSYNCWIDTH register controls the duration/width of the digital VSYNC output pulse when the interface is master. The FLD_MODE bits allow further flexibility in the HSYNC* and VSYNC* timing relationship.

Figure 1-10 illustrates the relationship between all vertical timing registers. See Figures 4-1 through 4-8 for additional timing details.

Figure 1-10. Vertical Timing Register Relationship—CX25874/5 Encoder



1.3.17 Input Pixel Blanking

Input pixel blanking can be controlled by either the BLANK* pin or by the internal registers. Blanking can be programmed independently of master or slave interface using the EN_BLANKO register bit. As an output (EN_BLANKO = 1), pixel blanking is generated based on the active area defined by the H_BLANKI, H_ACTIVE, V_BLANKI, and V_ACTIVEI registers. With EN_BLANKO = 1, the BLANK* pin is output in the proper relationship to the syncs to indicate the location of active pixels. As an input (EN_BLANKO = 0), when the BLANK* pin goes high, it indicates the start of active pixels at the pixel input pins. If the blanking area is determined internally, the H_BLANKI and V_BLANKI registers must be programmed properly, as they define the amount of pixels (or lines) that elapse between the leading edge of SYNC and the first active pixel (line). This area is commonly referred to by Graphic Processing Units (GPUs) as the "back porch." There is no register in the DENC that defines the time between the end of active and the leading edge of SYNC ("front porch" area). This parameter is obtained by subtracting H_ACTIVE and H_BLANKI from HCLKI (HTOTAL). The same concept applies vertically. The duration of active data is still determined by the H_ACTIVE register. The BLANK* signal is clocked in by the rising edge of CLKI.

An additional function for the BLANK* pin is used if the EN_DOT register bit is set. If EN_DOT = 1, the BLANK* pin becomes an input whose rising edge defines the data master's character clock boundary. This is used internally by the encoder to keep track of the exact pixel count for controllers that cannot operate at pixel clock rates but instead operate at VGA character clock rates.

The polarity of the BLANK* input/output can be programmed by the BLANKI register bit. The default convention is active low. The BLNK_IGNORE bit only has an effect if the encoder is receiving data in the CCIR656 format.

Table 1-14 summarizes the direction of the BLANK* signal in each interface. For more information refer to Section 1.3.18.

Table 1-14. Allowable BLANK* Signal Directions by Interface

Encoder Interface	Allowable Direction of BLANK*
Master	Input or Output
Pseudo-Master	Input
Slave	Input

1.3.18 Overscan Compensation

Overscan compensation is the process by which the encoder converts the digital input lines to the appropriate number of output lines for producing a full-screen image on the television receiver. This conversion is done in accordance with the Vertical Scaling Ratio (VSR). VSR is the ratio of the number of input lines received to number of output lines per field generated by the encoder (i.e., 262.5 lines/field for NTSC and 312.5 lines/field for PAL-BDGHI and SECAM). Using the correct amount of compensation in both the horizontal and vertical dimensions (at least 10 percent) will ensure that the entire digital image normally seen on the PC monitor is satisfactorily mapped to the analog television without any pixels or lines hidden in unviewable or blanked areas.

Increasing the Horizontal Overscan Compensation (HOC) percentage while keeping the Vertical Overscan Compensation (VOC) percentage the same will have several effects on the VGA Encoder. First, the number of output clocks per line (H_CLKO) will increase. Correspondingly, the clock frequencies shared between the data master and the encoder (i.e., CLKO = CLKI) will increase. Therefore, the original number of active pixels will be squeezed into a smaller analog video display region because the frequency at which input data is clocked into the CX25874/875 has increased. Since the CX25874/875 now processes active data at a faster rate than CCIR601-only compatible encoders, the graphics controller will need to transmit more blank pixels per line (i.e., HTOTAL must increase to match CX25874/875's H_CLKI) to make up the difference.

Increasing the (VOC) percentage while keeping the Horizontal Overscan Compensation percentage the same will have several different effects on the VGA Encoder. First, the H_CLKO total will stay the same as will the pixel rate (i.e., CLKI = CLKO). These parameters are dictated by the HOC value only. Second, the number of total vertical input lines (V_LINESI = data master's VTOTAL) will increase, which will increase the internal VSR. The net result is that more active pixels and more active lines will be used to generate each output line. The only way for the graphics controller to transmit these additional input lines with the same clock frequency as before is to decrease the amount of blanked pixels per line.

To support a custom overscan ratio, an entire set of overscan compensation calculations is required. This results in as many as 25 new register values for the VGA Encoder. For ease of use, these equations are embedded into Conexant's Windows™-based programming application called Cockpit. Each computation is somewhat interdependent on the others but the basic overscan equations are as follows:

(*) VSR = (V_LINESI) / (# of total output lines per field)

and

(**) # Blanked Pixels = {[H_CLKO / VSR] – H_ACTIVE}

For illustrative purposes, the calculations used to generate the 13.785 percent HOC percentage for Autoconfiguration Mode 0–640x480 RGB in, H_CLKO = 1792, NTSC output, are shown below:

From Appendix C:

Number of clocks necessary to latch in the V.S.R. # of input lines for every 1 analog output line = 1792 CLKs [i.e., H_CLKO]

Encoder must ensure input is 2X upsampled.

Therefore:

active CLKs per analog line = 2*(H_ACTIVE)

active CLKs per analog line = 1280 active CLKs per analog line

percent of input used to create active video area = {1280 active CLKs / 1792 total CLKs} = 71.4286 percent

Therefore:

(x) = active region percent of analog output line = 71.4286 percent

(y) = active region percent of typical analog video for NTSC = 52.65556 µs / 63.55556 µs = (y) = 82.4945 percent of line is active

Ratio of [x/y] = {71.4286 percent / 82.4945 percent} = 0.862147

HOC percentage = 1–{Ratio of [x/y]}

HOC percent = 1–0.862147 = 13.785 percent = HOC percentage for Autoconfiguration Mode 0

As a result, 13.785 percent of the horizontal active region within each line of an NTSC signal will be forcibly blanked by the encoder. For most TVs, this will resize the upsampled digital image properly so all of the pixels fit horizontally within the bezeled area of North American or Japanese TVs. The 13.785 percent overscan percentage is equally distributed on either side of the horizontal active region (i.e., 13.785 percent / 2 = 6.89 percent extra blanking for the beginning and end of the line). The original 640 active pixels (i.e., H_ACTIVE) will then be squeezed into the remaining analog active region with the faster pixel rate.

The explanation of the vertical overscan percentage value is similar. For autoconfiguration mode #0, V_ACTIVEO is 212, which means there are 210 full active lines per field. The first and last lines are filtered lines that assist in smoothing the transitions into and out of the active region to avoid flickering and are not counted. Any NTSC standard calls for 243 active lines per field, so 210/243 = 0.864198 of the vertical active region is used. This calculation yields a vertical overscan compensation percentage of 100–86.4198 = 13.5802 percent.

Flicker filtering, vertical overscan compensation, and horizontal overscan compensation are NOT SUPPORTED in any interlaced RGB or YCrCb input format sent to the VGA Encoder. Interlaced input data is commonly used as a DVD output format from a MPEG2 Decoder chip. Because of the data and image content types, flicker filtering and overscan compensation are not necessary in this case. Before and after effects of overscan compensation are illustrated in Figures 1-11 and 1-12.

Figure 1-11. Windows Desktop TV Out Image from Encoder without Overscan Compensation

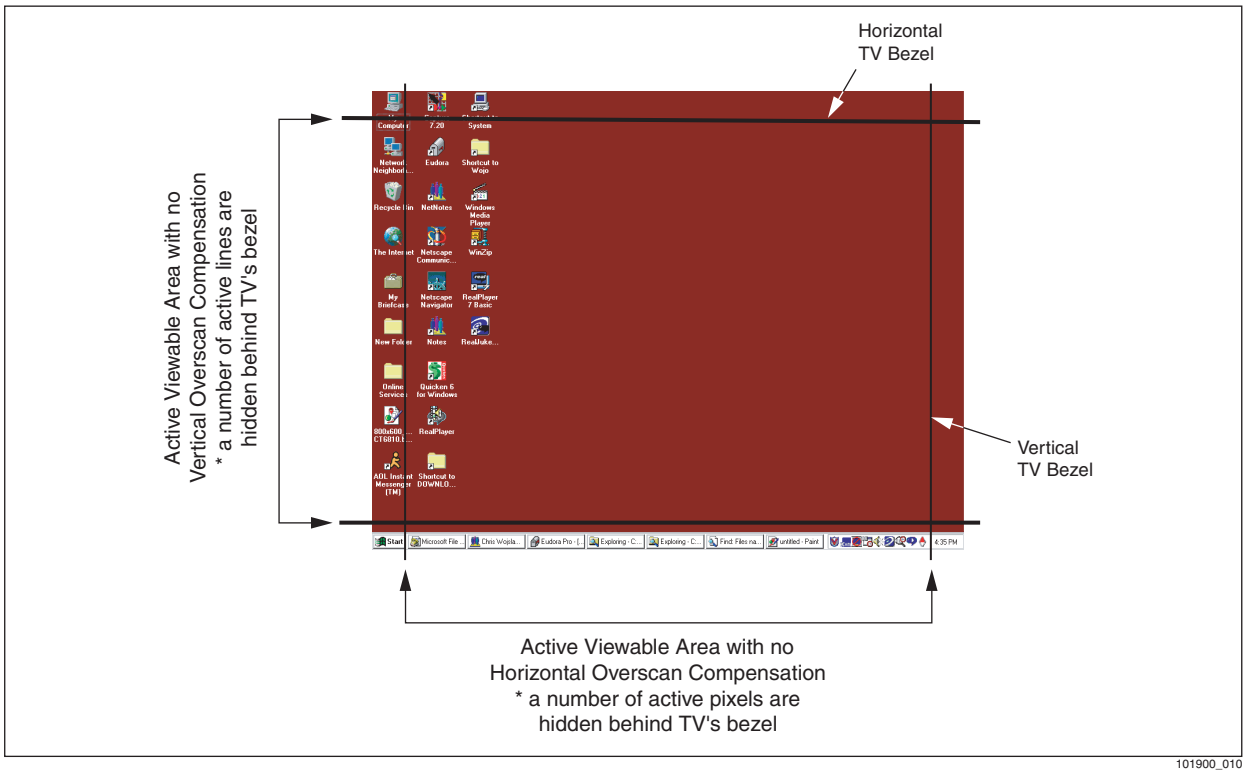
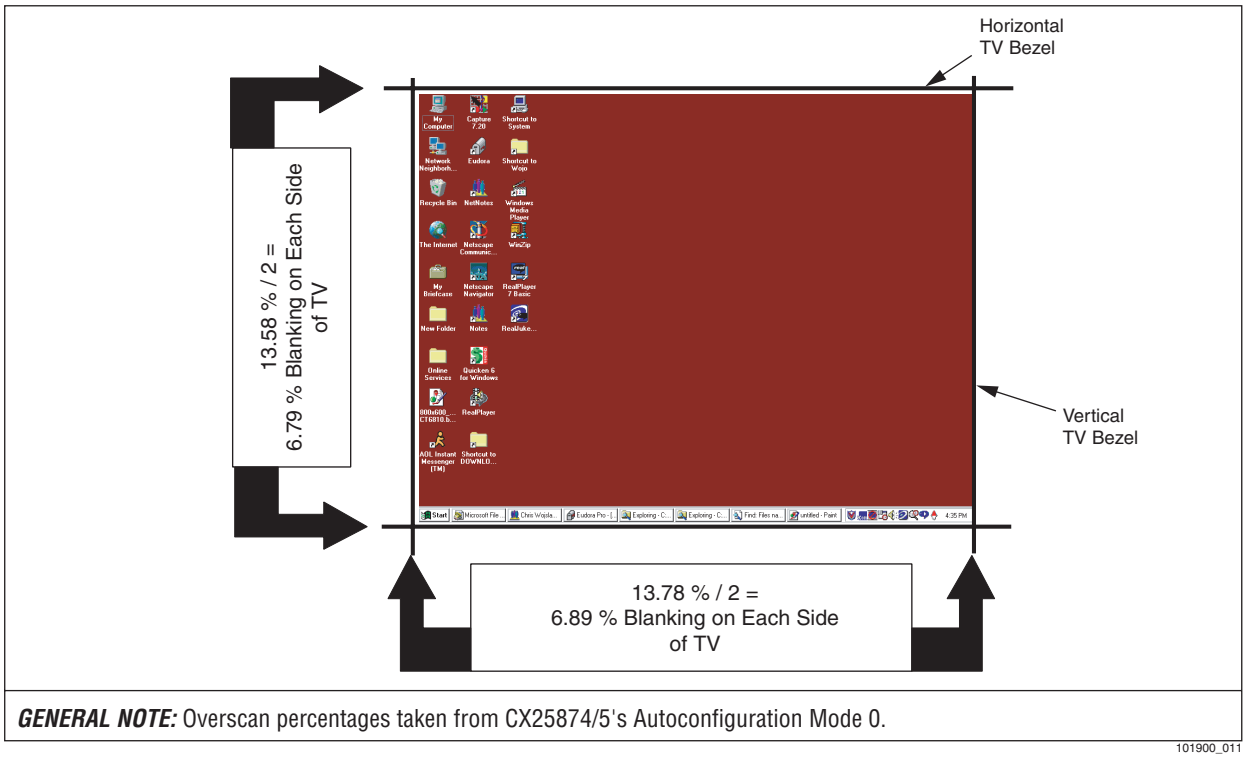


Figure 1-12. Windows Desktop TV Out Image from CX25874/875 with Overscan Compensation



GENERAL NOTE: Overscan percentages taken from CX25874/5's Autoconfiguration Mode 0.

In Figure 1-12, the VGA Encoder overscan compensated the 640 horizontal active pixels of data to fit within the viewable video region. With 13.78 percent HOC, the active data is contained within a 45.397 µs. portion of time within each active line while the remaining 7.26 µs (52.65556 µs.–45.397 µs.) part of the active region is blanked by the encoder.

The net result of overscan compensation will be an interlaced NTSC, PAL, or SECAM video image that fits within the bezel area of a TV Monitor. Correct choice of the HOC and VOC percentages is important so that no regions of the active input image will be hidden behind the plastic of the TV unit. Various TVs require different HOC and VOC values to fully utilize the entire viewable area of the TV. For the user's convenience, Conexant has included Appendix A in the CX25874/875 data sheet which lists the best overscan ratios for the most popular active resolutions (320x200, 320x240, 640x400, 640x480, 720x480, 720x576, 800x600, or 1024x768) and the two most common video outputs (NTSC and PAL). Varying amounts of blanking would be required depending on the HOC and VOC percentages and active input resolutions.

Ultimately, the blanked regions are dictated by the BLANK* signal itself and/or the internal pixel counter for the CX25874/875. Actual transmission of null or blanked pixels is not necessary since the encoder ignores any data sent to it via the pixel input port within the blanked regions. Only the active pixels need to be sent to the encoder from the controller during the digital active period.

Figures A-1 through A-8 illustrate many of the allowable overscan compensation percentage pairs for the major desktop resolutions and the most popular video outputs. These figures illustrate the minimum horizontal blanking times the data master must possess along with overscan compensation plots for pixel based data masters as well as 8- and 9-cycle character clock based graphics controllers.

1.3.19 Standard Flicker Filtering

To understand what flicker filtering is, one must understand two of the primary differences between the analog video standards used by TVs and the technology used in today's computer monitors.

First, computer monitors receive their video signal in a more basic, pristine form than TVs do. As discussed earlier, the video signal sent by a computer to its monitor is broken into multiple electrical components (red, green, blue, and sync) while a TV signal has all necessary information combined into a single composite signal or separate Luma and Chroma analog channels (S-Video). In order to process this composite signal, a TV must break it up into its original components, inevitably degrading the picture's brightness, saturation, and hue quality and creating distortions.

A second factor contributing to the decreased quality of images displayed on TV monitors is interlacing, a technique by which a complete TV picture is drawn in two passes from the top to the bottom on the picture tube. In interlacing, the first pass paints all the odd lines, and the second pass paints the even lines. Noticeable flicker occurs when the images in the odd lines are very different from the images in the even lines. As the odd and even lines are alternately displayed, the eye perceives the quick appearing and disappearing of visual information. This results in the irritation called flicker. Flicker is especially noticeable when viewing thin horizontal lines that only take up a single row within the odd or even field. If, for example, the line happens to be on an odd row, it totally disappears every time the even rows are displayed, resulting in that item appearing and disappearing at the field rate on the TV.

Unlike TV monitors, computer monitors paint an entire image in one pass from top to bottom, in a display format called noninterlaced or progressive. Images displayed in a noninterlaced format do not suffer from the same flicker problems.

For improved image quality and reduced flickering, the Conexant PC Encoder contains a 5-tap or 5-line flicker filter for both the Luma (F_SELY[2:0]) channel and Chroma (F_SELC[2:0]) channel. Conexant's standard flicker-filter works by applying a mathematically weighted, user-selected 2, 3, 4, or 5-line averaging algorithm to the incoming pixels of data. This slightly alters the digital information that is processed for eventual conversion to the odd and even lines of a TV picture so that the alternating lines are more similar to each other. This way, when the lines appear and disappear in the interlacing process, the flicker is less noticeable. The more similar the lines are made to appear, the less flicker is visible.

As the flicker artifact is reduced further and further, more and more information is being altered by the encoder and potentially lost from the original picture. Vertical resolution is therefore sacrificed and text clarity suffers, especially for small fonts below 10 points (10/72 of an inch) in size. For this reason, the amount of flicker filtering is programmable and should be controlled by the end user. Finding an optimal standard flicker filter setting for Luma and Chroma is somewhat subjective in nature and ensures that a pleasing image is seen on the television.

Unlike other vendors' encoder products, the CX25874/875 integrates both a standard flicker filter and additional adaptive flicker filter. This implementation allows for the preservation of small font text clarity and other tiny video details lost with only one filtering step. The adaptive feature eliminates more flicker with less loss of resolution because it is able to selectively apply a more aggressive flicker reduction level only to those portions of an image where the effect will be beneficial. Encoders lacking this adaptive filter apply the standard flicker filtering process to the entire screen. Small

text and icons often become unreadable, and thin, horizontal lines often completely disappear. The CX25874/875's adaptive flicker filter prevents this from happening and is described in Section 1.3.20.

As long as progressive RGB or YCrCb data is received in encoder mode, the CX25874/875's flicker filter is effective with any active resolution from 320x200 to a maximum of 1024 x 768. The flicker reduction is present on any interlaced standard-definition video output such as NTSC, PAL, or SECAM. The DIS_FFILT register bit turns off the standard flicker filter. The vertical scaling can be disabled by setting the internal V_SCALE register to 4096 for a noninterlaced input. Finally, the CX25874/875 supports up to 24-bit color processing, meaning that the converted image will feature the same depth of color as the original computer picture.

While the CX25874/5 is generating a VGA style RGB or a YP_RP_B or RGB HDTV set of outputs, the standard flicker filter cannot be utilized. This is the case regardless of the resolution (480p, 720p, 1080i, etc.) received by the Conexant device.

1.3.20 Adaptive Flicker Filter

Adaptive Flicker Filtering is an enhanced feature included with the CX25874/875. It allows the encoder to automatically alter the amount of flicker filtering based on the image being processed. The result is a higher-quality optimized image because a superior balance between vertical resolution and flicker reduction has been achieved. The adaptive flicker filter is enabled via the ADPT_FF bit. There are four possible settings ranging from 2-line (most observable flicker, greatest vertical resolution) to 5-line (minimal observable flicker, moderate vertical resolution). The luminance and chrominance outputs are independent in terms of the level of adaptive flicker filtering. When the adaptive flicker filter is on, the manual flicker filter is off and vice versa.

Vertical filtering in the PC Encoder serves three purposes:

- Vertical polyphase interpolation filtering to upsample the image data vertically. This increases the resolution and accuracy of the subsequent vertical downsampling required to fit the entire image into the visible region of the television.
- Anti-alias filtering to reduce aliasing artifacts when downsampling vertically.
- Flicker filtering to reduce the flicker produced when vertical high-frequency content is displayed on an interlaced device.

The vertical interpolation filtering and vertical anti-alias filtering requirements are driven by the amount of vertical down scaling required, and do not vary substantially with image content. The flicker filtering requirement, however, is dependent upon the image content.

Regions of the image with vertical high-frequency content will flicker in proportion to the amplitude of that high-frequency content. Regions with high-amplitude, vertical-high frequency content require substantial flicker filtering, but regions with low amplitude or no vertical high-frequency content require little or no flicker filtering.

For this reason, the CX25874/875 provides adaptive flicker filtering. It analyzes the image content to detect areas that require strong flicker filtering, and adjusts its vertical filtering to apply stronger flicker filtering to those regions. This analysis and adjustment occurs on a pixel by pixel basis, so each pixel in the output line has the optimal amount of flicker filtering applied to it.

The Adaptive_FF1 and Adaptive_FF2 registers (0x34 and 0x36) configure the adaptive algorithm. The Y_ALTFF[1:0] and C_ALTFF[1:0] fields allow the selection of the alternative (i.e., usually stronger) flicker filter level to combine with the standard flicker filter level selected by fields F_SELY[1:0] and F_SELC[1:0] (register 0xC8). This creates an array of flicker filters for the Y channel and C channel respectively. The actual flicker filter amount applied for a given pixel output depends on the detection and location of any high-amplitude vertical high-frequency content within the input samples that creates that output pixel.

The amplitude of the high-frequency content that triggers an adaptation of the flicker filter can be adjusted via the Y_THRESH[2:0] and C_THRESH[2:0] bit fields. The FFRTN bit offers two ways to combine the standard and alternate flicker filters to generate an array of flicker filters. The YSELECT bit allows the Chroma channel flicker filter to be adapted based on the Chroma channel or the Y (i.e., Luminance) channel content.

NOTE: Neither standard nor adaptive flicker filtering is supported by the CX25874/875 in noninterlaced video output formats (VGA style RGB or YUV, HDTV 480p, 525p, 540p, 625p, or 720p), or interlaced HDTV (1035i or 1080i).

Table 1-15 summarizes recommended configurations of the adaptive flicker filter for various types of image content and resolutions. Figure 1-13 illustrates the standard and adaptive flicker filter control registers and their control levels. The internal low-pass filter, brightness, saturation, and coring control levels are also shown.

Table 1-15. Optimal Adaptive and Standard Flicker Filter Settings for Common PC Applications and Resolutions

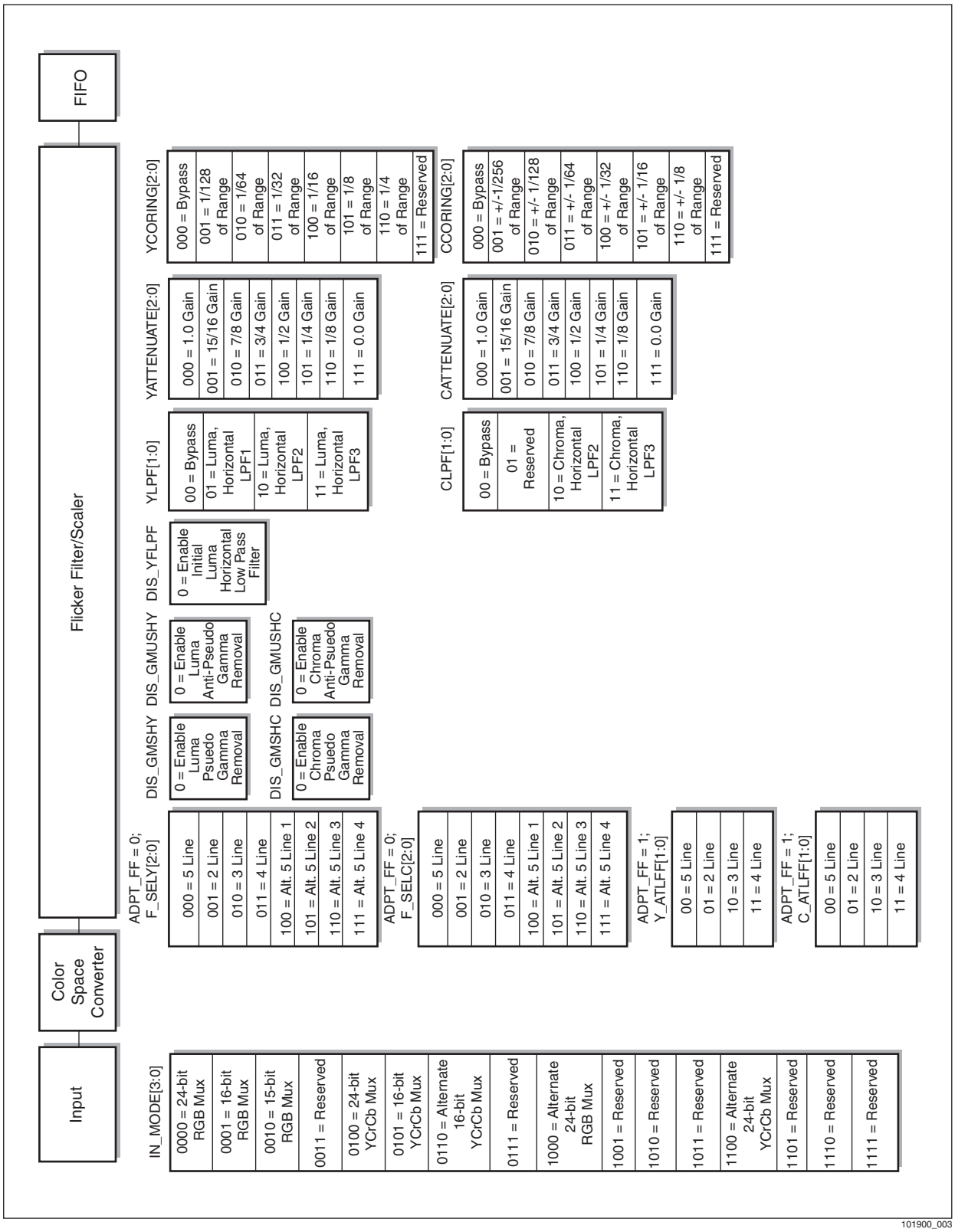
	Standard FF settings		CX25874/5 Adaptive FF settings								
Desktop Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**Y_SELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	3-line	3-line	On	4-line	4-line	000	000	On(2)	On(2)	1	0
640x480 in, PAL-BDGHI out(3)	3-line	3-line	On	4-line	4-line	100	100	On(2)	On(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	010	010	Off(2)	On(2)	1	0
800x600 in, PAL-BDGHI out(3)	4-line	4-line	On	5-line	5-line	010	010	On(2)	On(2)	1	0
1024x768 in, NTSC out(1)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0
1024x768 in, PAL-BDGHI out(3)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0
Web Page Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**Y_SELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	4-line	3-line	On	4-line	4-line	100	100	Off(2)	Off(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	010	010	Off(2)	Off(2	1	0
1024x768 in, NTSC out(1)	5-line	5-line	On	5-line	5-line	110	110	On(2)	Off(2)	1	0

Table 1-15. Optimal Adaptive and Standard Flicker Filter Settings for Common PC Applications and Resolutions

	Standard FF settings		CX25874/5 Adaptive FF settings								
Word Processing Resolution/ Video Output Type	**FSEL_Y**	**FSEL_C**	**ADPT_FF**	**Y_ALTFF**	**C_ALTFF**	**Y_THRESH**	**C_THRESH**	**Y_SELECT**	**FFRTN**	**BYYCR**	**CHROMA_BW**
640x480 in, NTSC out(1)	3-line	3-line	On	4-line	4-line	010	010	Off(2)	On(2)	1	0
800x600 in, NTSC out(1)	4-line	4-line	On	5-line	5-line	100	100	On(2)	Off(2)	1	0

FOOTNOTE:
(1) NTSC-J, PAL-M, and PAL-60 video outputs should use the NTSC standard and Adaptive FF settings.
(2) On denotes a 1 bit setting. Off denotes a 0 bit setting.
(3) PAL-N, PAL-M, and PAL-60 video outputs should use the PAL-BDGHI standard and Adaptive FF settings.

Figure 1-13. Flicker Filter and Video Adjustment Control Diagram



1.3.21 VGA Registers Involved in the TV Out Process

Timing constraints for the Conexant encoder are driven by the timing requirements of the analog video output (NTSC, PAL, or SECAM) together with the active resolution and overscan compensation ratio (i.e., amount of blanking in the active region) of the television image. To explain what specific CRTC or VGA registers within the graphics controller need to be involved in displaying a nonstandard or desktop format on both a TV and CRT, one can work backwards from those output signal timing requirements to determine the input timing requirements.

Each output field has a vertical blanking region and an active region. These regions are defined relative to the vertical sync pulse, horizontal sync pulse, given format (i.e., number of lines per field), and a given pixel clock frequency (i.e., number of pixel clocks per line). Within each line of the active region there is a horizontal blanking period (that includes a horizontal sync pulse) and an active period (where the image data is located). Given those parameters, at least six registers within every generic graphics controller need to be changed for display of each active and total resolution.

Table 1-16 lists the VGA/CRTC registers of the data master involved in the TV out process.

Table 1-16. VGA/CRTC Registers Involved in TV Out Process

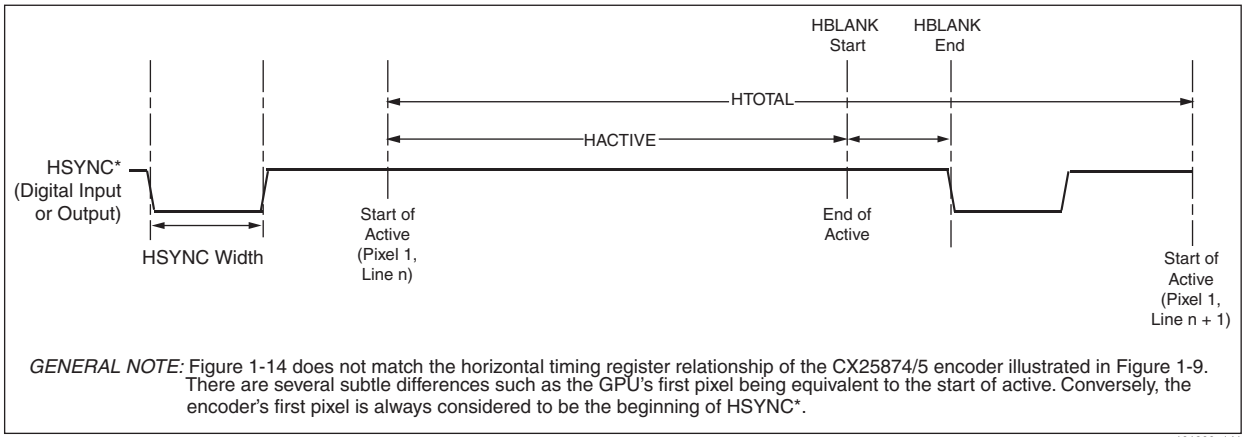
Register Name	Description
Start VBLANK/VSYNC* and End VBLANK/VSYNC*	These VGA registers work in combination with each other to control the scan line at which the vertical blanking period begins and the point at which it ends. This register pair correlates closely to the encoder's V_BLANKI value.
VACTIVE (or Vertical Display End)	Dictates the specific number of active lines for the present digital frame. VACTIVE should equal the encoder's V_ACTIVEI value.
VTOTAL	Specifies the number of scan lines from one VSYNC* active to the next VSYNC* active pulse. The difference between VTOTAL and VACTIVE is the amount of blanked lines. VTOTAL should equal the encoder's V_LINESI value.
Vertical Retrace Start(1) and Vertical Retrace End(1)	Controls the start of the vertical retrace pulse which signals the display to move up to the beginning of the active display. This field contains the value of the vertical scanline counter at the beginning of the first scanline where the vertical retrace signal is asserted. The end of this pulse is contorlled by the Vertical Retrace End register. The Vertical Retrace Start register is always greater than HACTIVE and Start VBLANK, but less than Vertical Retrace End. The Vertical Retrace End register is always less than VTOTAL and less than or equal to End VBLANK.
HBLANK/HSYNC* Start and HBLANK/HSYNC* End	This VGA register set works in combination with each other to control the value of the pixel or character clock counter where the HSYNC* signal becomes active and the position at which HSYNC* becomes inactive. This register pair correlates closely to the encoder's H_BLANKI value.
HACTIVE (or Horizontal Display End)	Dictates the specific number of active pixels per line. HACTIVE should equal the encoder's H_ACTIVE value.
HTOTAL	Specifies the number of pixel clocks or character clocks from one HSYNC* active to the next HSYNC* active pulse. In other words, this is the total time required for both the displayed and non displayed portions of a single scan line. The difference between HTOTAL and HACTIVE is the amount of blanked pixels per line. HTOTAL should equal the encoder's H_CLKI value.
Horizontal Retrace Start(1) and Horizontal Retrace End(1)	Specifies the pixel clock at which the GPU begines sending the horizontal synchroniation pulse to the display which signals the VGA monitor to retrace back to the left side of the screen. The end of this pulse is controlled by the End Horizontal Retrace register. This pulse may appear anywhere in the scan line, as well as set to a position beyond the Horizontal Total register which effectively disables the horizontal synchronization pulse. The Horizontal Retrace Start register is always greater than HACTIVE and HBLANK Start, but less than Horizontal Retrace End. The Horizontal Retrace End register is always less than HTOTAL and less than or equal to HBLANK End.

FOOTNOTE:

(1) These registers affect timing and the image on a VGA monitor much more so than the timing required by the encoder for TV out. For some GPUs, these registers might not have any effect on the digital timing required for TV out.

Figure 1-14 illustrates the relationship between all horizontal timing registers in a generic GPU. This timing diagram may not reflect the functionality of all GPUs including those for notebook PCs, set-top boxes, or other types of consumer systems. The designer is strongly urged to consult the data sheet of other vendors' products to confirm their timing relationships and CRTC register functionality.

Figure 1-14. Horizontal Timing Relationship—Generic GPU



GENERAL NOTE: Figure 1-14 does not match the horizontal timing register relationship of the CX25874/5 encoder illustrated in Figure 1-9. There are several subtle differences such as the GPU's first pixel being equivalent to the start of active. Conversely, the encoder's first pixel is always considered to be the beginning of HSYNC*.

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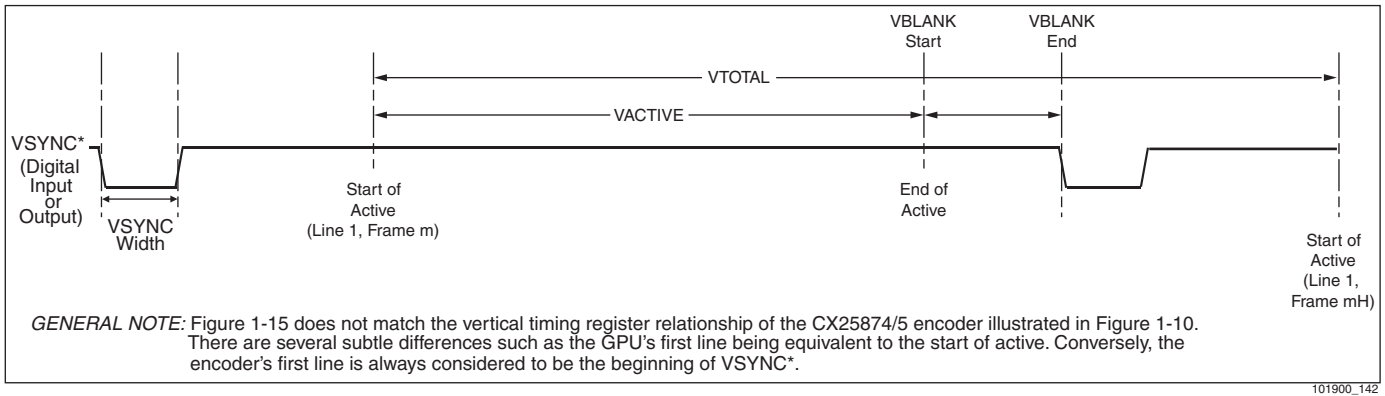
Figure 1-15 illustrates the relationship between all vertical timing registers in a generic GPU.

Figure 1-15. Vertical Timing Relationship—Generic GPU



GENERAL NOTE: Figure 1-15 does not match the vertical timing register relationship of the CX25874/5 encoder illustrated in Figure 1-10. There are several subtle differences such as the GPU's first line being equivalent to the start of active. Conversely, the encoder's first line is always considered to be the beginning of VSYNC*.

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To achieve VGA compatibility, the controller must manipulate some of its own VGA register settings in order to produce a hi-quality dual display on both the computer monitor and TV. It should be noted that the encoder has no way of knowing that a different VGA mode has been selected. As a result, it relies on the serial bus master device to reconfigure it via an autoconfiguration mode or complete register set rewrite to make adjustments in its timing.

When the two devices are programmed correctly, (i.e., matching HTOTAL, VTOTAL, HACTIVE, VACTIVE) regardless of the interface, the required input HSYNC*/ VSYNC* to first input active pixel or line spacing matches the output HSYNC*/ VSYNC* to first output active pixel or line spacing. When this occurs, the graphics controller always transmits active data at the time the CX25874/875 expects to receive it. Superior TV out quality is achieved only when this type of timing symmetry exists.

1.3.22 Output Modes

The CX25874/5 encoder can generate following types of video outputs: Composite (CVBS), S-Video (separate Luma [Y] and Chroma [C] channels), YUV, Component 480i YC_RC_B, VGA-style RGB, Euro SCART, Component (YP_RP_B) for HDTV, or RGB for HDTV. These outputs are selected by the OUT_MODE[1:0] register bits in combination with the HDTV_EN and EN_SCART bits.

While the encoder is in VGA style RGB, no color space conversion is possible from input to output. Analog RGB is transmitted from a digital RGB input and analog YUV is output from a digital YCrCb input.

When outputting standard-definition RGB, the device outputs VGA/SVGA analog RGB with a bilevel sync. In this mode, the R, G, and B input data is fed to the DACs after the addition of a horizontal sync and, if the SETUP bit is 1, a setup pedestal is added. The output currents are scaled so that the DACs output the proper 1 V full-scale (sync tip to peak white) levels for driving a CRT monitor. The graphics controller must provide all the timing control (including separate HSYNC and VSYNC signals) for the monitor, which results in the encoder operating as a slave in this case. Only the P[11:0], BLANK*, HSYNC*, and VSYNC* input pins and the RGB analog output pins are active. The BLANK*, HSYNC*, and VSYNC* pins are automatically enabled as inputs in this mode.

Each of the four video signals generated by the OUT_MODE[1:0] field can be multiplexed to any DAC using the OUT_MUXA[1:0], OUT_MUXB[1:0], OUT_MUXC[1:0], and OUT_MUXD[1:0] register bits. To do this, program the 2-bit value representing the desired type of output into the appropriate OUT_MUXx[1:0] register. As an example, suppose a system requires Composite video (i.e., 00 binary) to be output from DAC_A, chroma (10) on DAC_B, luma (01) on DAC_C, and Composite video (00) on DAC_D. This scheme could be accomplished by programming register 0xCE with 0001 1000 binary or 18 hex.

The LUMADLY[1:0] register bits control the amount of delay for the Y_DLY (11 binary) analog output. The allowable delay ranges from 0 (no delay) to 3 pixel clocks.

All digital-to-analog converters are designed to drive standard video levels into a combined RLOAD of 37.5 Ω (doubly-terminated 75 Ω loads to ground). Unused outputs should be disabled by setting the corresponding DACDISx bit to minimize the supply current or left as a no connect. Disabling unused DAC outputs reduces cross chroma distortion and improves overall picture quality.

1.3.23 Analog Horizontal Sync

The HSYNC_WIDTH[7:0] register determines the duration of the horizontal sync pulse embedded within each standard-definition analog line. The beginning of the horizontal sync pulse corresponds to the reset of the internal horizontal pixel counter. The horizontal line rate is determined by the H_CLKO[11:0] register. The internal horizontal counter is reset to 1 at the beginning of the horizontal sync and counts up to H_CLKO.

The sync rise and fall times are automatically controlled. The sync peak-to-peak amplitude is programmable over a range of values by SYNC_AMP[7:0]. Incrementing the SYNC_AMP by 1 increases the sync amplitude of the analog sync pulse by 30 mV.

1.3.24 Analog Vertical Sync

The analog vertical sync duration is selectable as either 2.5 total lines or 3 total lines by the register bit VSYNC_DUR. If VSYNC_DUR = 1, 3 lines are selected; if VSYNC_DUR = 0, 2.5 lines are selected.

The device automatically blanks the video from the start of the horizontal sync interval through the end of the color burst, as well as the vertical sync to prevent erroneous video timing generation.

1.3.25 Analog Video Blanking

Analog video blanking is controlled by the H_BLANKO, V_BLANKO, and V_ACTIVEO registers. Together they define an active region where pixels are displayed. V_BLANKO defines the number of lines from the leading edge of the analog vertical sync to the first active output line per field. V_ACTIVEO defines the number of active output lines. H_BLANKO defines the number of output pixels from the leading edge of horizontal sync to the first active output pixel. H_ACTIVE defines the number of active output pixels.

The device automatically blanks video from the start of the horizontal sync interval through the end of the burst, as well as the vertical sync interval to prevent erroneous video timing generation.

1.3.26 Video Output Standards Supported

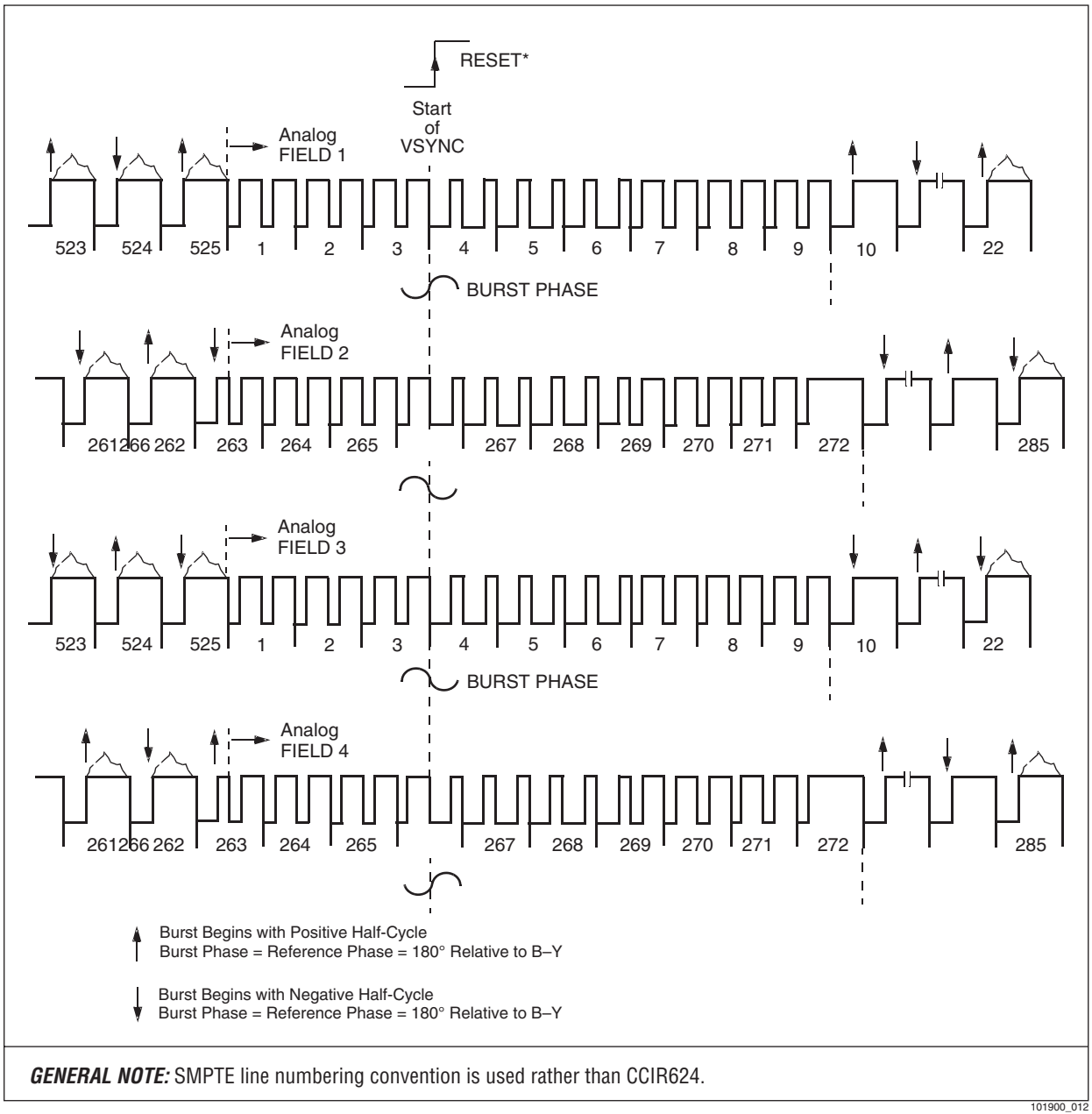
Several bits (625LINE, SETUP, VSYNC_DUR, PAL_MD, FM, DIS_SCRST) and various autoconfiguration modes control the generation of standard-definition video standards. They allow the generation of all the different NTSC, PAL, and SECAM standard-definition video standards. The aforementioned bits control the specific encoding process parameters. It is likely other registers may need to be modified to meet all the video parameters of the particular video standard. The most important bit settings for generation of standard-definition video inputs are shown in Table 1-17. Other CX25874/5 registers and bits must be reprogrammed to generate different video output.Video timing modes supported by the Conexant encoder are illustrated in Figures 1-16 through 1-27. These show typical events that occur for each type of video format.

Table 1-17. Important Bit Settings for Generation of Standard-Definition Video Outputs

Video Output Bit	NTSC-M	NTSC-Japan	PAL-BDGHI	PAL-N	PAL-Nc	PAL-M	PAL-60(1)	SECAM-B, G, H(2)	SECAM-D, K, K1(3)	SECAM-L(4)
VSYNC_DUR	1	1	0	1	0	1	1	0	0	0
625LINE	0	0	1	1	1	0	0	1	1	1
SETUP	1	0	0	1	0	1	0	0	0	0
PAL_MD	0	0	1	1	1	1	1	0	0	0
DIS_SCRST	0	0	0	0	0	0	0	1	1	1
FM	0	0	0	0	0	0	0	1	1	1

FOOTNOTE:
(1) PAL-60 used primarily in China.
(2) SECAM-B, G, H used primarily in the Middle East.
(3) SECAM-D, K, K1 used primarily in Russia and Eastern European nations.
(4) SECAM-L used primarily in France.

Figure 1-16. Interlaced 525-Line (NTSC) Video Timing



GENERAL NOTE: SMPTE line numbering convention is used rather than CCIR624.

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Figure 1-17. Interlaced 525-Line (PAL-M) Video Timing

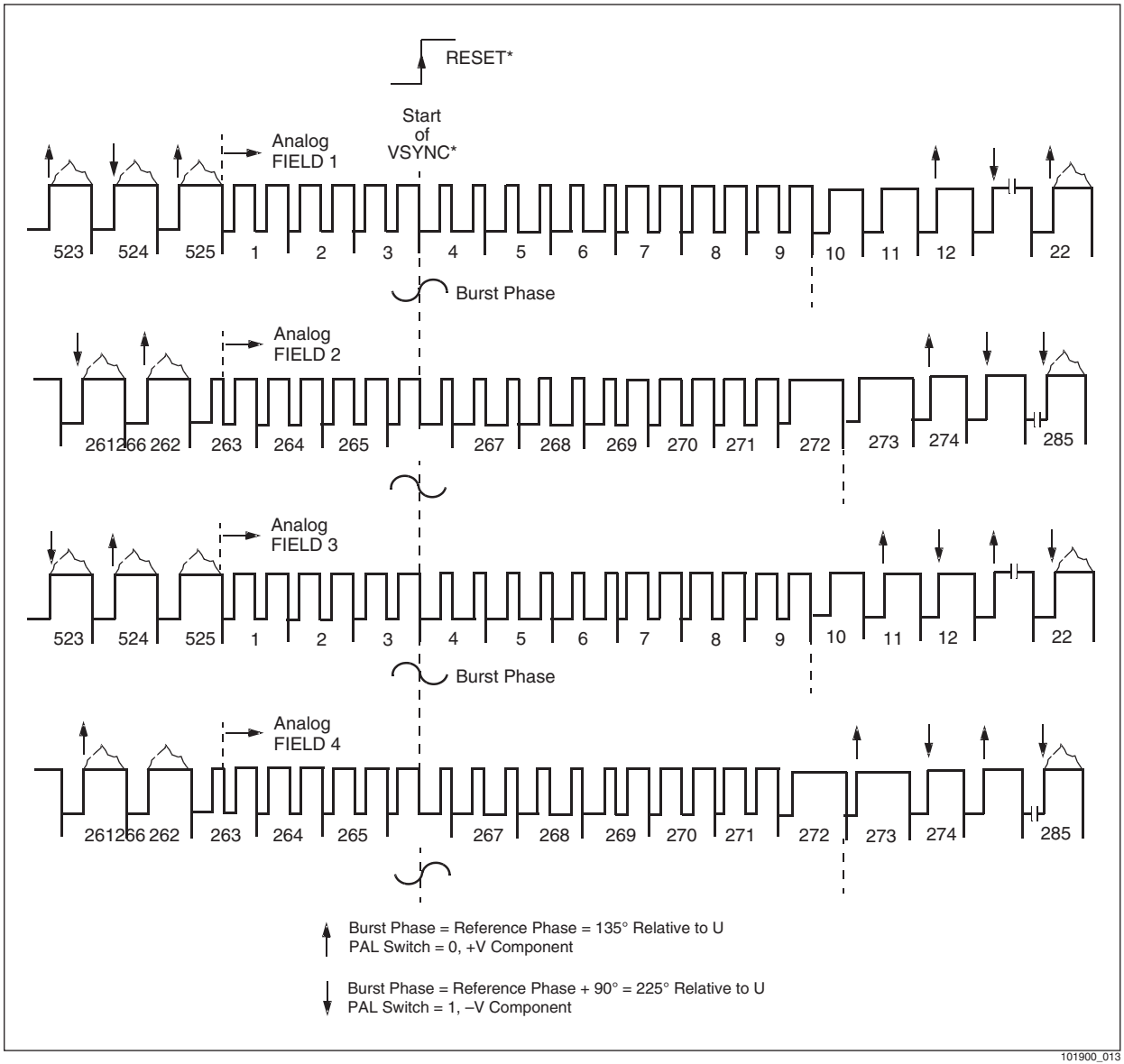


Figure 1-18. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 1–4)

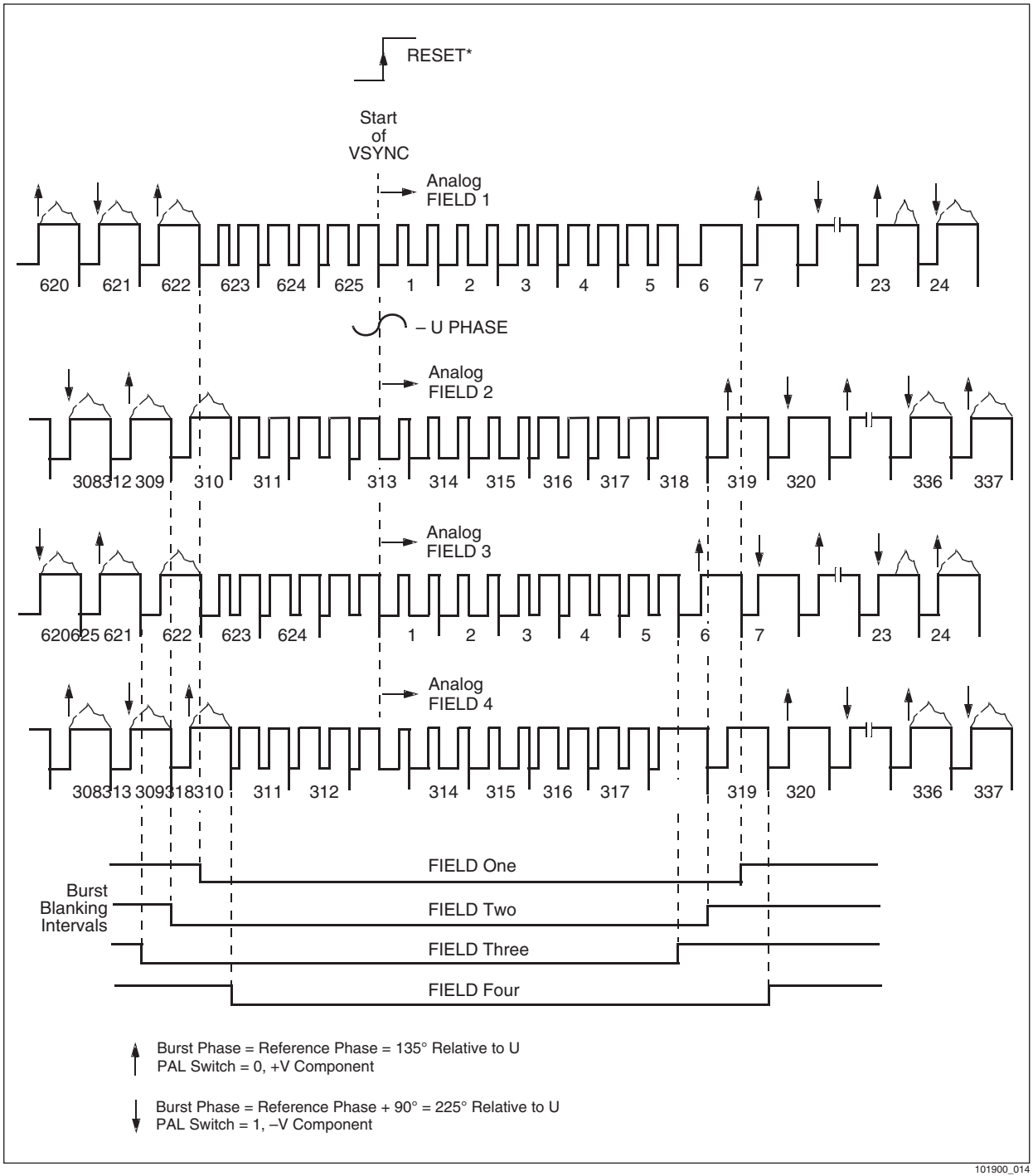


Figure 1-19. Interlaced 625-Line (PAL-B, D, G, H, I, Nc) Video Timing (Fields 5–8)

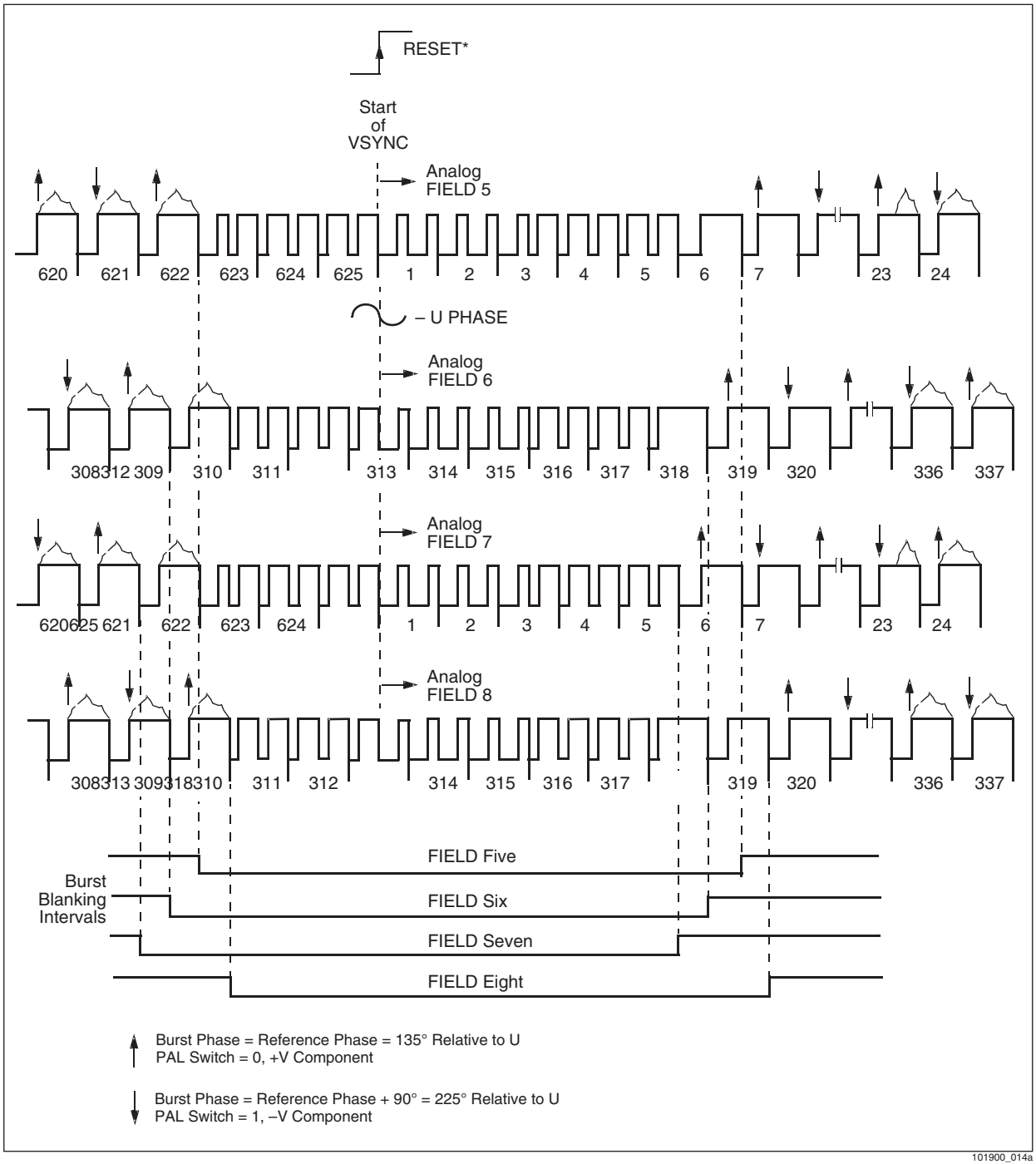


Figure 1-20. Interlaced 625-Line (PAL-N) Video Timing (Fields 1–4)

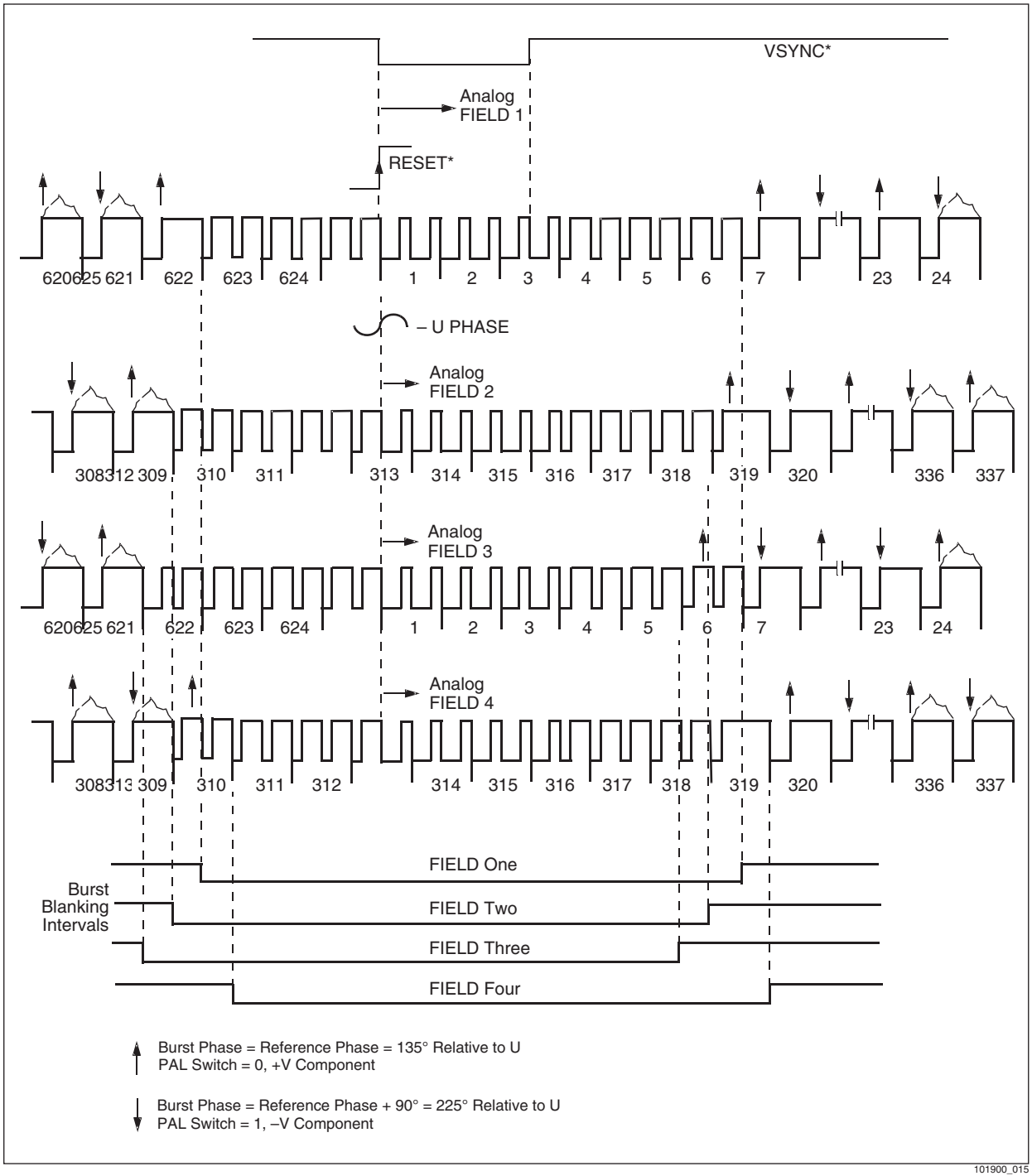


Figure 1-21. Interlaced 625-Line (PAL-N) Video Timing (Fields 5–8)

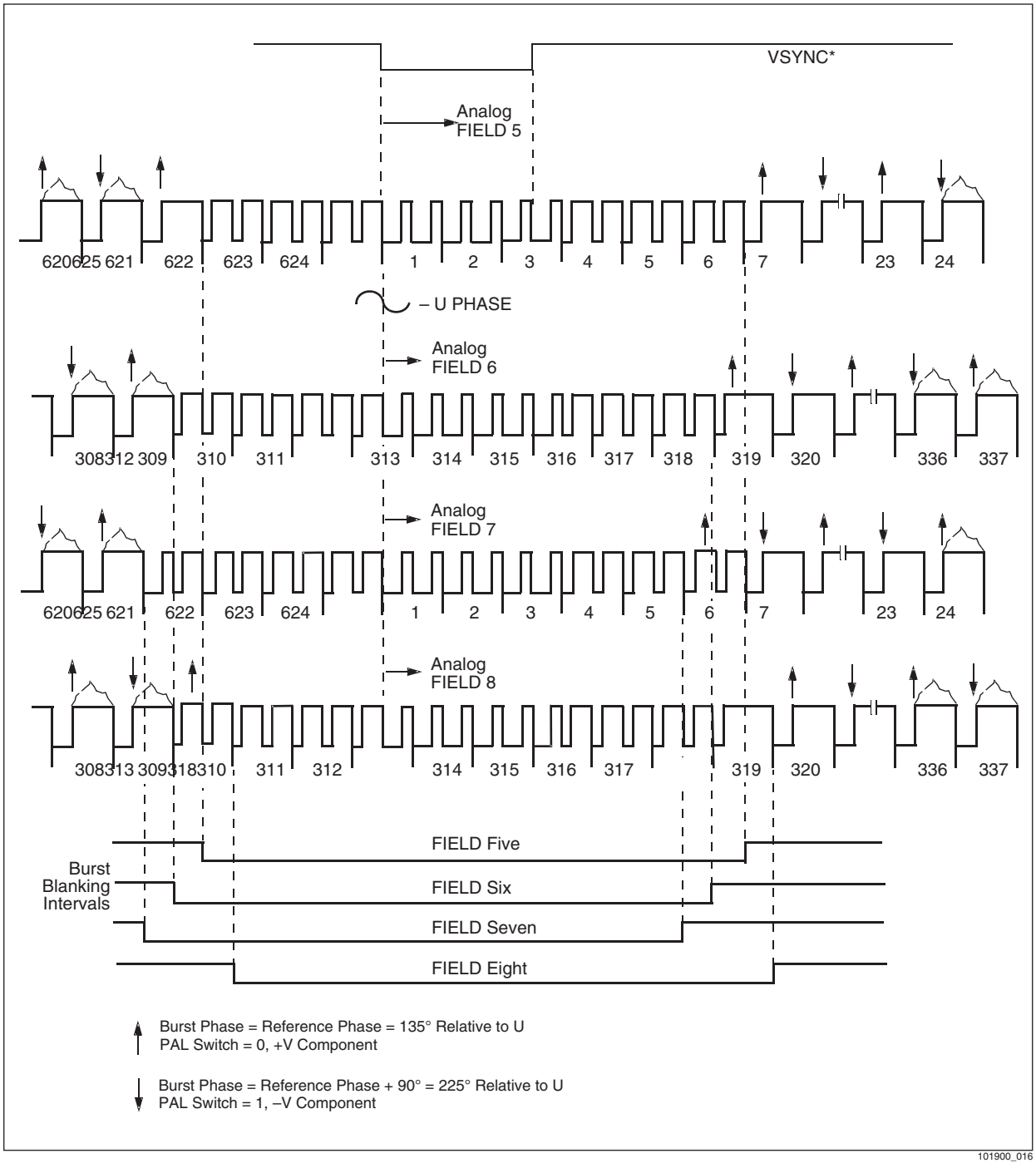


Figure 1-22. Noninterlaced 262-Line (NTSC) Video Timing

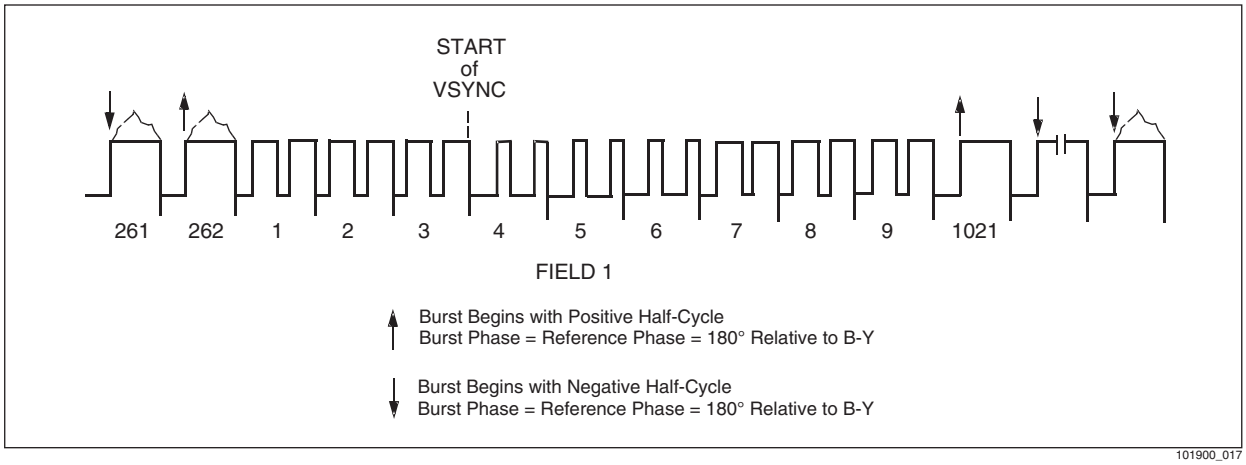


Figure 1-23. Noninterlaced 262-Line (PAL-M) Video Timing

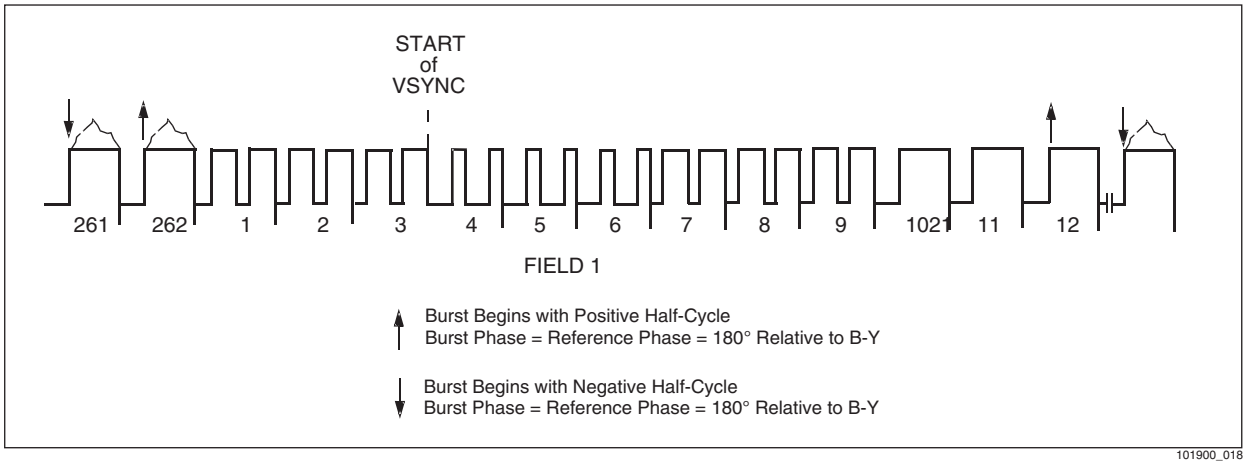


Figure 1-24. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, Nc) Video Timing

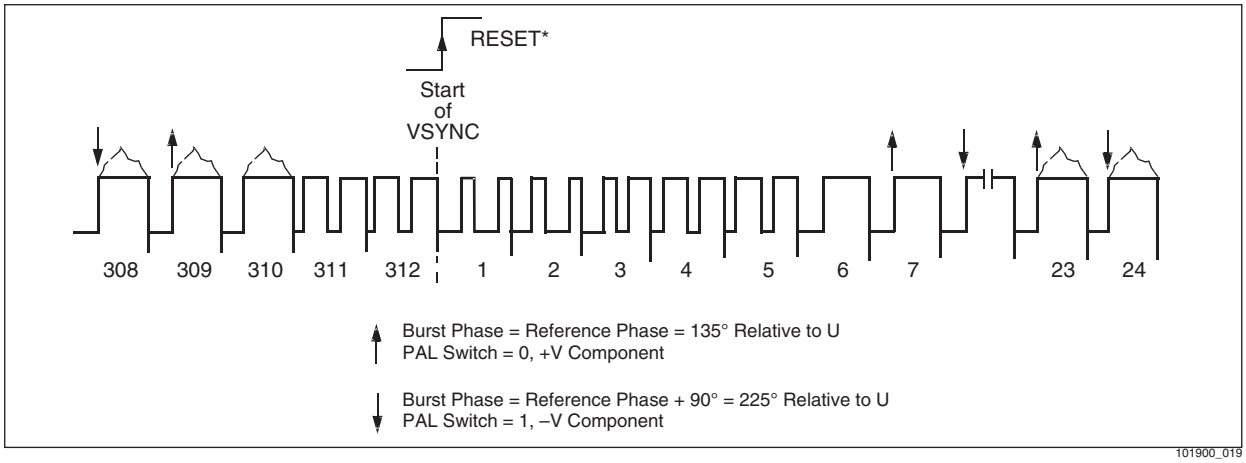
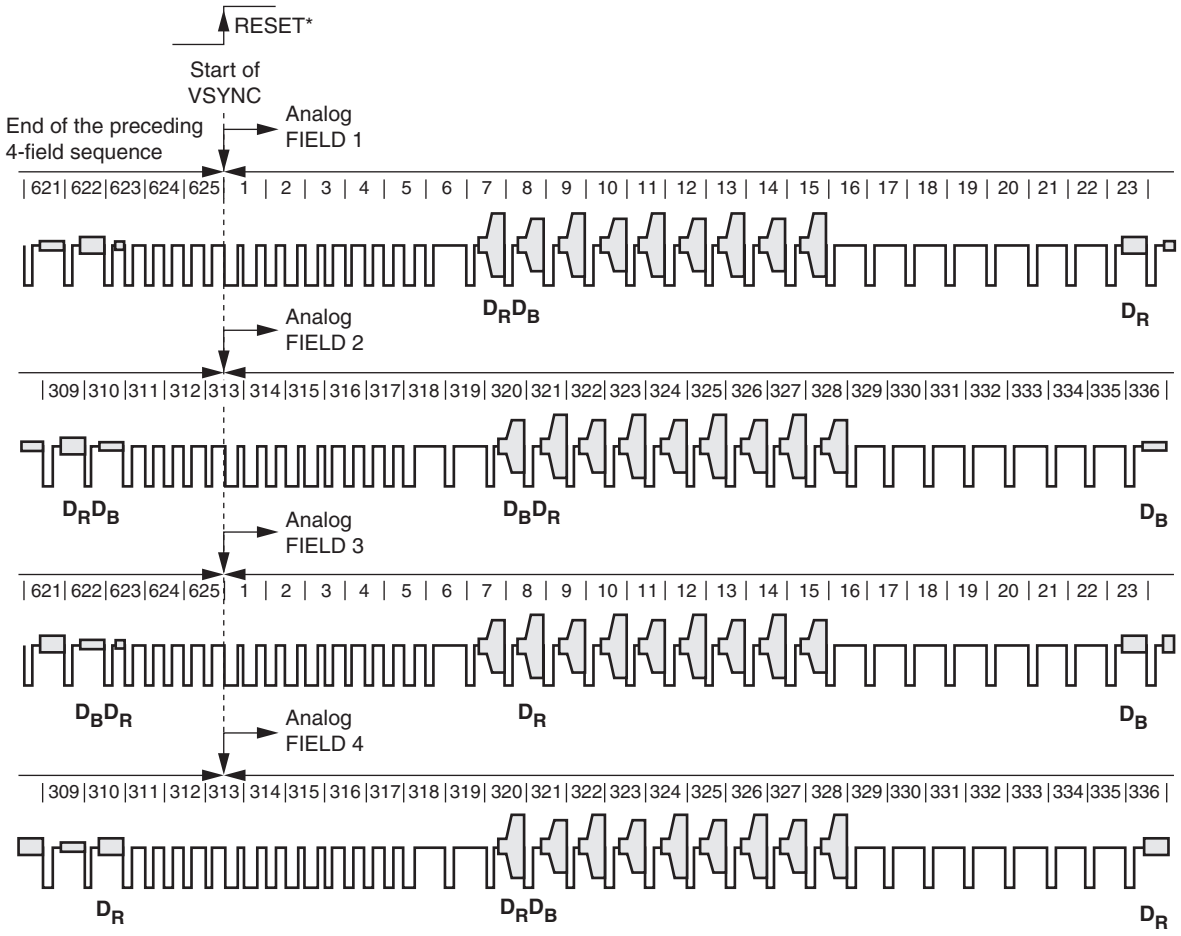


Figure 1-25. Interlaced 625-Line (SECAM-B, D, G, K, K1, L, M) Video Timing (Fields 1-4)



GENERAL NOTE:

1. D_R and D_B color subcarrier signal sequences over four consecutive fields shown above.
2. D_R color subcarrier frequency is 4.406250 MHz.
3. D_B color subcarrier frequency is 4.250000 MHz.

101900_020

1.3.27 Subcarrier Generation

The device uses a 32-bit-word to synthesize the subcarrier. The value of the subcarrier increment required to generate the desired subcarrier frequency is found with the following equations:

NTSC:

$MSC[31:0] = int ((455/(2 * H\_CLKO)) * 2^{32} + 0.5)$

PAL:

$MSC[31:0] = int (((1135/4+1/625)/H\_CLKO) * 2^{32} + 0.5)$

PAL-M (Brazil):

$MSC\ [31:0] = int ((909/(4 * H\_CLKO)) * 2^{32} + 0.5)$

PAL-Nc (Argentina):

$MSC[31:0] = int (((917/4 + 1/625)/H\_CLKO) * 2^{32} + 0.5)$

SECAM:

$MSC\_DB[31:0] = int (272/(H\_CLKO) * 2^{32} + 0.5)$

$MSC\_DR[31:0]^{(1)} = int (282/(H\_CLKO) * 2^{32} + 0.5)$

where: H_CLKO is the number of output clocks/line (this is register 0x76 and the low nibble of 0x86).

NOTE: When generating SECAM, the MSC register becomes the MSC_DR register.

This allows the generation of any desired color burst subcarrier frequency for any desired standard-definition video standard. The 32-bit subcarrier increment must be loaded by the serial interface before the subcarrier is enabled. The device is reset to disable chroma until the last byte of the 32-bit increment loads, at which time the chroma is enabled, unless the DCHROMA bit is set.

In order to prevent any residual errors from accumulating, the subcarrier DTO (Discrete Time Oscillator) is reset every four fields for NTSC formats and every eight fields for PAL formats. For best quality in SECAM, the DIS_SCRST bit should be set preventing a subcarrier phase reset at the beginning of each color field sequence. Furthermore, the SECAM subcarrier is generated on lines 23-310 and 336-623 automatically unless disabled by the PROG_SC bit.

1.3.28 Subcarrier Phase Reset/Offset

In order to maintain correct SC-H phasing, the subcarrier phase is set to 0 degrees on the leading edge of the analog vertical sync every four (NTSC) or eight (PAL) fields, unless the DIS_SCRST (bit four of register 0xA2) is set to a logical 1. This is true for both interlaced and noninterlaced outputs. The subcarrier phase can be adjusted from the nominal 0 degrees phase by the PHASE_OFF[7:0] register, where each LSb change corresponds to a 360/256 = 1.406 degrees change in the phase.

Setting DIS_SCRST to 1 may be useful in situations where the ratio of CLK/2 to HSYNC* edges in a color frame is noninteger, which could produce a significant phase impulse by resetting to 0.

1.3.29 Burst Generation

The subcarrier burst generation is a function of the video standard (e.g., NTSC, PAL, or SECAM), the subcarrier frequency increment (MSC[31:0]), and the burst horizontal begin and end register settings (HBURST_BEGIN[7:0] and HBURST_END[7:0]). To calculate the value of HBURST_END[7:0] subtract 128 from the desired location in clock cycles. The burst will automatically be blanked during the horizontal sync preventing invalid sync pulses from being generated. Burst blanking is automatically controlled by the selected video format. Burst rise and fall times are automatically generated by the device. The burst amplitude is controllable through the BST_AMP[5:0] field.

1.3.30 Video Amplitude Scaling and SINX/X Compensation

Both the luminance and chrominance video amplitudes can be scaled by the MY, MCR, and MCB registers. This allows various colorimetry standards to be achieved, and can also be used to boost the chroma to compensate for the sin x/x loss of the DACs. Appendix A shows the range of values achievable and values for various video formats.

The DAC output response is a typical sinx/x response. For the composite video output, this results in a slightly lower than desired burst and chroma amplitude value. This is compensated for, to some extent, by choosing an output filter that boosts the frequency response slightly. Conexant includes this type of low-pass filter in Section 3.4. Another method which can be used effectively, and is used by default in the auto configuration modes, is to boost the burst and chroma gain as programmed by the BST_AMP and MCR/MCB register values by a factor of (x/sinx). The amount of sinx/x amplitude reduction is calculated by:

$sinx/x = sin\ (\pi * Fsc/F_{CLK}) / (\pi * Fsc/F_{CLK})$ *[in radians]*

Fsc = desired subcarrier burst frequency

F_{CLK} *= analog pixel rate*

1.3.31 Chrominance Disable

The chrominance subcarrier can be turned off by setting the DCHROMA bit to a logical 1. This disables the subcarrier burst as well, providing luminance-only signals on the CVBS output and a static blank level on the chrominance output.

1.3.32 FIELD Pin Output

Like its predecessors, the Bt868/869 and the CX25870/871, this PC encoder includes a FIELD pin output. This signal is output only and is accessed through pin #20. The frequency of the FIELD pin is 30 Hz during an NTSC video output, and 25 Hz throughout a PAL or SECAM video output. The only programming step required to obtain the FIELD output is to serially write the EN_OUT bit to 1.

The purpose of this signal is to provide a digital TTL compatible output which tracks the analog interlaced field presently being transmitted by the CX25874/875 DACs. The peak-to-peak amplitude of this output will be from 0 V to the level present on the VDDO pins. If these pins are tied to 3.3 V, then the FIELD high state is transmitted at

a 3.3 V level. If these pins are tied to 1.5 V or lower voltage, then the FIELD high state is transmitted at a 1.5 V or lower level. The logical 0 level from FIELD will always be GND/VSS regardless of the logical 1 voltage.

The FIELD output transitions after the rising edge of CLKI, two clock cycles following the leading edge of the digital HSYNC* input or output. Figure 1-26 shows the relationship between the FIELD and Composite (CVBS) outputs and VSYNC* input for NTSC. Figure 1-27 illustrates this same relationship for PAL.

Figure 1-26. FIELD Pin Output Timing Diagram: NTSC-M, J, 4.43, PAL-M, 60

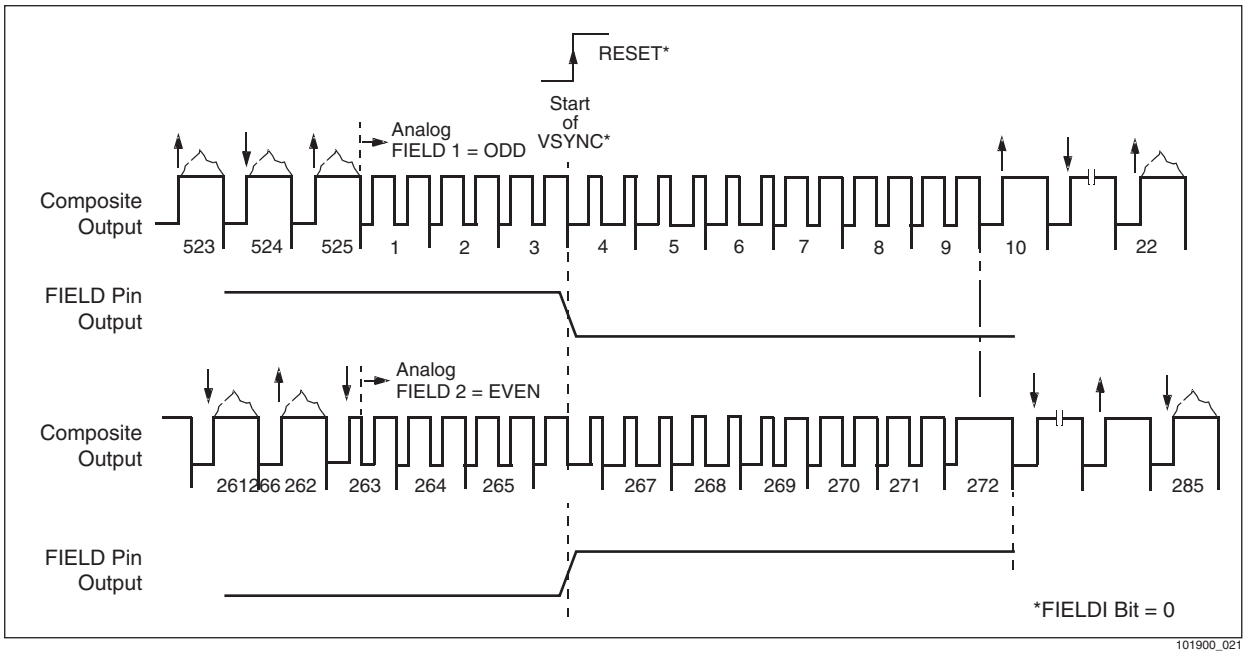
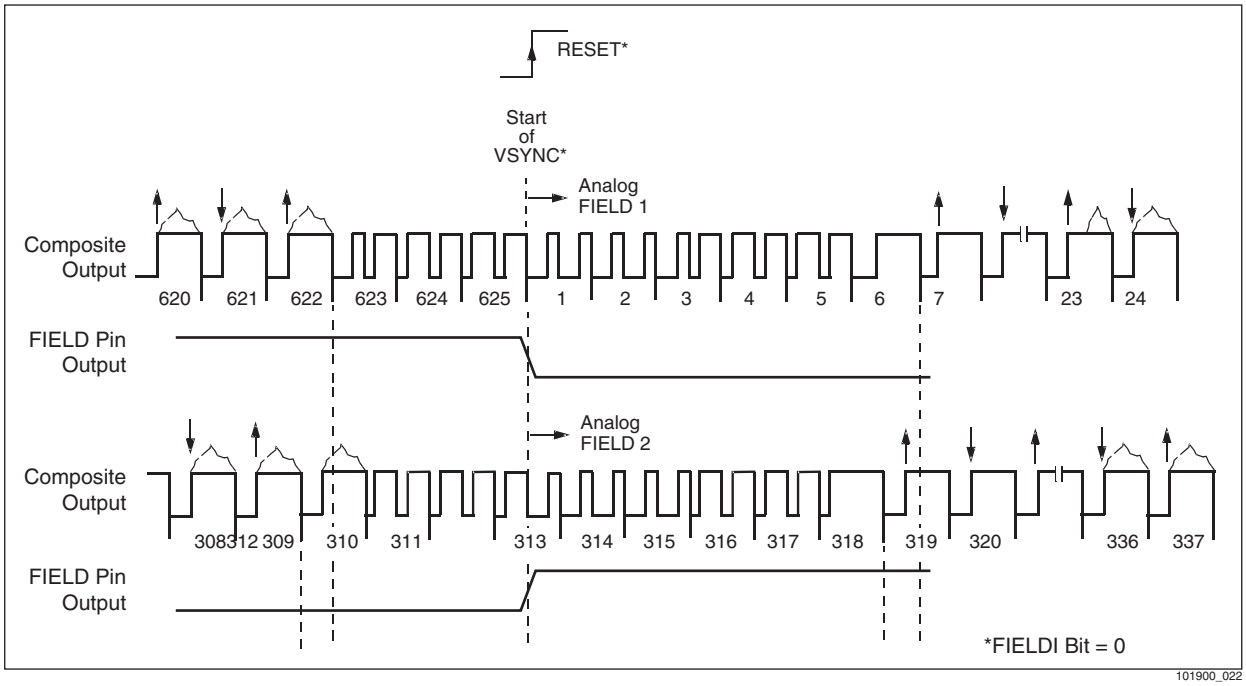


Figure 1-27. FIELD Pin Output Timing Diagram (PAL-B, D, G, H, I, N, Nc)



By default, the internal FIELDI bit will be 0 which forces the encoder to transmit a logical 1 during transmission of an EVEN field and logical 0 for the period of an ODD field. To change the FIELD polarity, reprogram the FIELDI bit.

If the encoder is the timing master and sends out HSYNC* and VSYNC*, then after a power-on, pin, or timing reset (setting of bit 7, register 0x6C), the encoder and the flicker filter portions of the device start at line 1, pixel 1 of their respective timing generation. For the CX25874/875, this means the ODD field is always the first field conveyed after a power-on reset, pin reset, or timing reset.

When the CX25874/875 receives an interlaced data format, its FIELD pin represents only the output field presently being generated by the on-chip DACs. When the CX25874/875 receives progressive (i.e., noninterlaced) frames which have no field associated with it, the CX25874/875's input timing generator still keeps track of frames received. As a result, after the entire second frame has been received, the input and encoder sections become resynchronized. This re-synchronization is done through an internal frame sync signal. This action, in turn, forces the CX25874/875 to the beginning of the odd field and changes the FIELD pin back to its odd state.

If the CX25874/875 is the timing slave (i.e., it accepts HSYNC* and VSYNC*) receives pin reset or timing reset (register 0x6C, bit 7) this causes the input timing generator to send the encoder the aforementioned frame sync. This sets the encoder to the beginning of the odd field, which is conveyed through the FIELD pin. The first digital HSYNC* and VSYNC* combination then corresponds to the encoder's EVEN output field. The second digital HSYNC* and VSYNC* combination will again cause a frame sync and the encoder will start sending the ODD field both from its DACs and FIELD pin. This ODD–EVEN–ODD–EVEN … field sequence continues indefinitely.

1.3.33 Buffered Crystal Clock Output

The buffered crystal clock output (XTL_BFO) pin provides a buffered output (0 V to the voltage on the VDDO pin peak-peak) of whatever frequency is found between the encoder's XTALIN and XTALOUT pins. This signal can then be used as a much more accurate input clock to the graphics controller because controllers typically utilize clock sources with errors between 75–150 ppm. This implementation ultimately results in better VGA picture quality because the clock driving the data master is within the same tolerance (i.e., 25 ppm) as the TV out encoder. This can also lead to a considerable savings in cost, component count, and PC board space because the crystal attached to the data master has been completely eliminated.

On power-up, the encoder will transmit a 0 to 3.3 V signal (or whatever voltage is received by the VDDO pins) at a frequency equal to the frequency of the crystal found between the XTALIN and XTALOUT ports. The tolerance of the XTL_BFO signal will match the tolerance found within the encoder's crystal. The CX25874/875 was designed to expect a 13.500 MHz ± 25 ppm crystal. As a result, all the PLL_INT and PLL_FRACT register values found within each CX25874/875 autoconfiguration mode possess this set of default values.

The CX25874/875 also has the flexibility to support an alternate 14.31818 MHz crystal with a tolerance of ± 25 ppm. To switch the encoder to operate with this crystal frequency, install an appropriate crystal and crystal circuit between the XTALIN and XTALOUT ports. After any autoconfiguration mode has been set, the PLL_INT and PLL_FRACT registers must be manually programmed in accordance with the equations in Section 1.3.6.

For CX25874/875 designs, a small (e.g., 33 Ω) series resistor should be added to XTL_BFO, as close as possible to the signal source device. This reduces overshoot and undershoot on this signal as it changes states. The buffered crystal clock output pin should be floated if not used. Disabling the XTL_BFO pin is possible through the XTL_BFO_DIS bit.

1.3.34 Noninterlaced Output

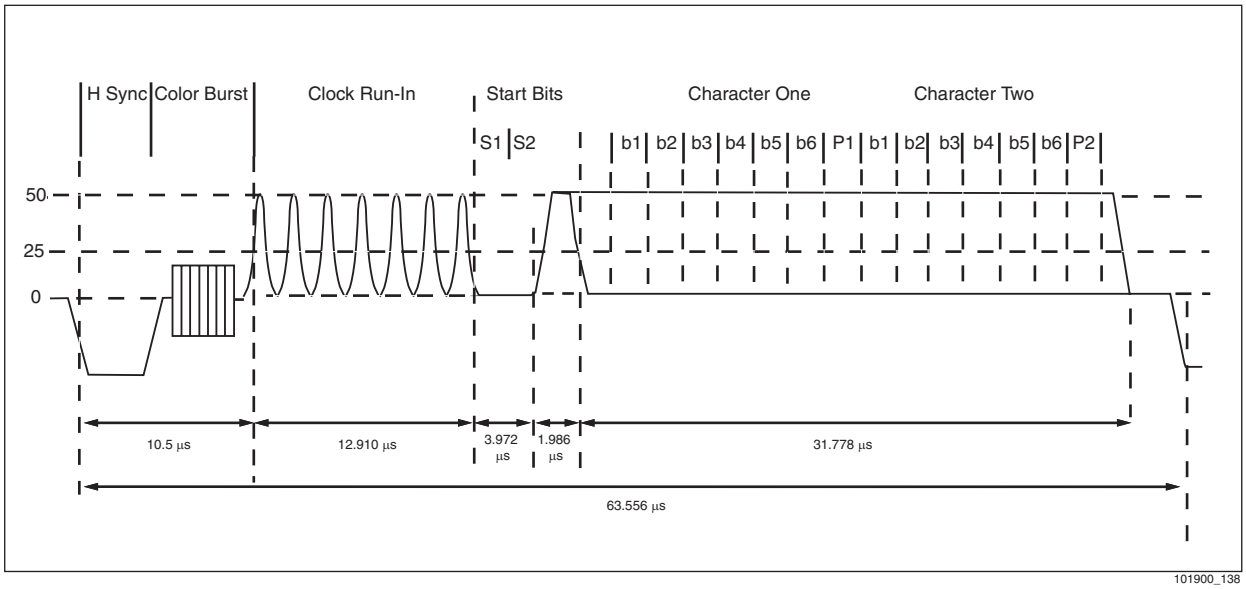
This is a legacy video output mode, continued for backward compatibility to the Bt868/869 encoders. It is not recommended for new designs. The CX25874/875 is programmed for noninterlaced video out via the NI_OUT bit, and it is recommended that the DIS_SCRST bit be set to a one. Although only the odd field will be transmitted, the FIELD pin will continue to change state on the leading edge of the analog vertical sync. A 30 Hz offset should be subtracted from the color subcarrier frequency while in NTSC mode so that the color subcarrier phase is inverted from field to field. The transition from interlaced to noninterlaced in master interface occurs during odd fields to prevent synchronization disturbance.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan >2x) may not function properly.

1.3.35 Closed Captioning

The CX25874/875 encodes NTSC/PAL–M Closed Captioning (CC) on scan line 21, and NTSC/PAL–M extended data services on scan line 284, in accordance with the EIA-608B (CEA-608B) standard shown if Figure 1-28. The bit rate for CC-encoded data is 0.5035 MHz for 525-line video systems. For 625-line systems, this bit rate falls to 0.500 MHz. Four 8-bit registers (CCF1B1, CCF1B2, CCF2B1, and CCF2B2) provide the data while bits ECCF1 and ECCF2 enable display of the data. A logical 0 corresponds to the blanking level of 0 IRE, while a logical 1 corresponds to 50 IRE above the blanking level.

Figure 1-28. EIA-608B (CEA-608B)-Compliant Line 21 Waveform (NTSC)



NOTE: Figure 1-28 reprinted courtesy of EIA/CEA-608B specification.

Closed captioning for PAL–B, D, G, H, I, N, Nc is similar to that for NTSC. Closed-caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC system, except that encoding is provided on lines 22 and 335, for closed captioning and extended data services, respectively.

The CX25874/875 generates the clock run-in start bits and appropriate timing automatically. The user must control the 2 bytes of data for each field. Each of these 2 bytes is a 7-bit and odd parity ASCII character, which represents text or control characters for positioning or display control. For the purposes of CC or EPS, only the Y signal for S-video or Component YCrCb outputs is used. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47 Section 15.119 (10/91 edition or later) for programming information. The EIA608 standard describes ancillary data applications for Field 2 Line 21 (line 284).

When CCF1B2 is written, CCSTAT_O is set; when CCF2B2 is written, CCSTAT_E is set. After the CC bytes for the odd field are encoded, CCSTAT_O is cleared; after the CC bytes for the even field are encoded, CCSTAT_E is cleared. If the ECCGATE bit is set, no further encoding is performed until the appropriate registers are written again; a null is transmitted on the appropriate CC line in that case. If the ECCGATE

bit is not set, the user must rewrite the CC registers prior to reaching the CC line; otherwise the last bytes are re-encoded. The CC data bytes are double-buffered to prevent loss of data during the encoding process.

The equations governing CCR_START and CC_ADD registers are listed below.

CCR_START:

- For NTSC:
  *((H_CLKO*10.003*27) / 1716) + 60*
- For PAL, SECAM:
  *((H_CLKO*10.003*27) / 1728) + 60*

CC_ADD:

- For NTSC:
  $2^{22}/H\_CLKO$
- For PAL, SECAM:
  $(2^{22}*1728) / (1716*H\_CLKO)$

Pseudo-code that can be used to create a software routine for Closed Caption Encoding is included as Appendix D.

1.3.36 Copy Generation Management System-Analog

The Copy Generation/Guard Management System (CGMS) is a copy control system for DVD recorders that either prevents copies or controls the number of copies that can be made. CGMS can be added to either analog (CGMS-A) or digital signals (CGMS-D). DENCs such as CX25874/5 encoders only output analog TV, so, for the purposes of this data sheet, CGMS-A is discussed. CGMS-D protection is not possible with CX25874/5 encoders.

CGMS is a copy control system consisting of two bits in the MPEG-2 compressed video stream that indicate whether copying of the content is permitted or not. For CGMS to work, the bits must be set during the authoring process. Next, the DVD player or other system adds CGMS data to its analog video output stream through the encoder. Lastly, the DVD recorder recognizes and responds correctly to the CGMS bit setting.

When the DENC is generating NTSC, CGMS-A is identical to closed captioning in that it embeds data in the field blanking interval on line 21. Line 20 can also be used for CGMS-A in 525-line analog formats. Whereas closed captioning uses 16 bits or 2 bytes worth of data, CGMS-A uses only 2 bits of this overall sequence. The analog timing provided by the CX25874/5 will match the waveform shown in Figure 1-28 for both CGMS-A and CC.

Most standards for CGMS-A copy protection are unclear in terms of PAL output, so these standards will be minimally discussed in this section. Refer to Section 1.3.37.1 for this encoder's PAL Wide-Screen Signaling (WSS) capabilities.

In summary, for NTSC, all aspects of CGMS-A can be supported with CX25874/5 encoders, because the timing and waveform for CGMS-A matches that timing and waveform required for support of NTSC closed captioning which also adheres to the EIA-608 standard.

When line 21 is utilized for other purposes, CX25874/5 can place closed-caption content (whose waveform and timing are defined in the EIA/CEA-608-B standard) within one of the following lines in the Vertical Blanking Interval (VBI): line 19, line 20, line 21, or line 22 of 525-line NTSC systems. The CCSEL[3:0] bit field in the

CX25874/5 controls which line receives the CC/CGMS-A content. The CC and CGMS-A bits must reside on the same line.

When the DENC is generating HDTV 720p and 1080i Y PR PB outputs, the device transmits a data waveform for HDTV signals compliant with the EIAJ CPR-1204-2, CEA-770.3-C and CEA 805A-TYPEA standards, because, in terms of timing and the analog waveforms, they are identical. The display/pixel clock is 74.25 MHz at VSYNC = 60 Hz for each supported standard. The start symbol and data symbol width are the same and equal to 1.038 µs (for 1080i) and 0.782 µs (for 720p). The start symbol position (from 0H, start of line to bit 0 of the header) is 4.15 µs (for 1080i) and 3.13 µs (for 720p). The number of data bits encoded per symbol is 1 or bilevel. A logical high level is nominally 70 percent of peak white (i.e., 490 mV), and logical low is nominally 0 percent of peak white (0 mV).

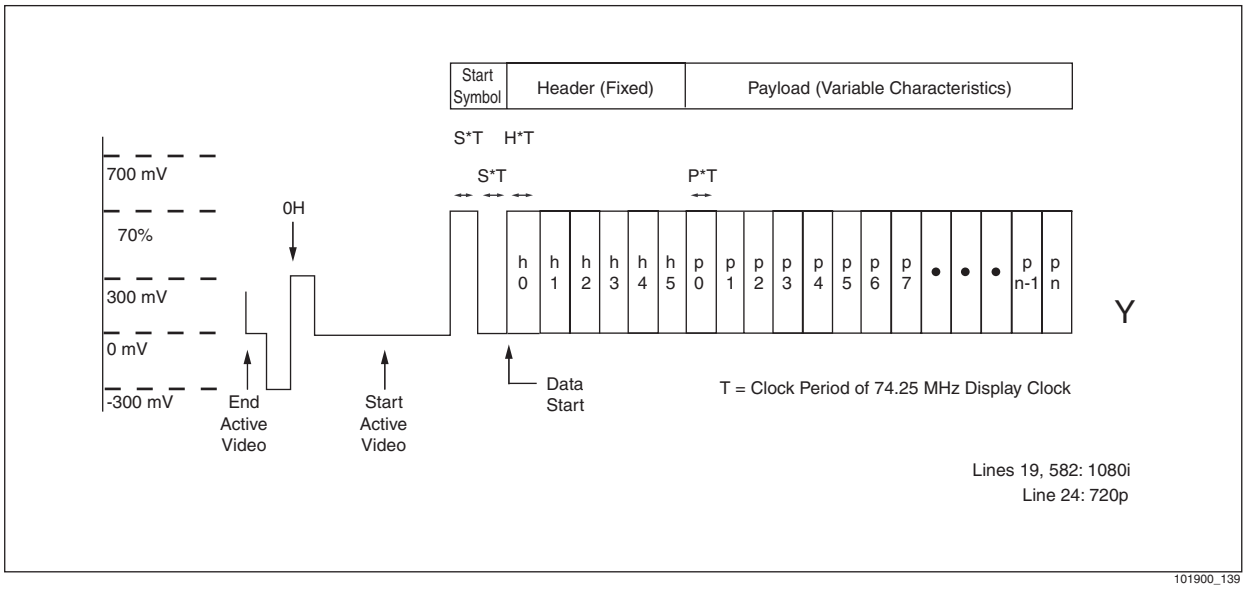
Like SDTV, CGMS-A HDTV 720p and 1080i are just two specific data bits in the larger Type A Packet Payload Data sequence within the vertical blanking interval. The CX25874/5 encoder does not support the CEA 805A-TYPEB standard in 720p and 1080i for a number of reasons:

1. First, and most importantly, the position of Type A packet for 720p format must be in VBI line 24. Position of Type B Packet for 720p format must be in VBI line 23. The position of Type A packet for 1080i format must be in VBI lines 19 and 582. Position of Type B Packet for 1080i format must be in VBI lines 18 and 581. This DENC cannot place CGMS-A and WSS data on alternate lines within the HDTV VBI for 720p or 1080i.
2. Second, the Type B payload data symbol width (i.e., each analog bit interval) is different from the Type A payload data symbol width, along with other timing parameters.
3. Third, Type B Packet payload data is placed in 128 bits (16 bytes) versus only 14 bits for Type A Packet payload data.

In summary, for 720p and 1080i, CX25874/5 supports EIAJ CPR-1204-2, CEA-770.3-C, and CEA 805A-TYPEA standards. Since CGMS-A is a subset of CEA-770.3-C and CEA 805A-TYPEA, then CX25874/5 transmits compliant CGMS-A in accordance with these standards.

The CX25874/875 encodes CGMS-A bits as two bits of the overall data payload in the TYPEA data sequence in accordance with the CEA 805A-TYPEA waveform shown in Figure 1-29.

Figure 1-29. CEA 805A-TYPEA-Compliant HDTV 1080i, 720p Waveform



NOTE: Figure 1-29 reprinted courtesy of CEA 805A-TYPEA specification.

For HDTV 480p Y PR PB outputs, the CX25874/5 encoder transmits a data waveform for HDTV signals compliant with the EIAJ CPR-1204-1, CEA-770.1-C, CEA-770.2-C, and CEA 805A-TYPEA standards, because, in terms of timing and the analog waveform, they are identical. The display/pixel clock is 27.000 MHz at VSYNC = 60 Hz for each supported standard. The start symbol and data symbol width are the same and equal to 0.963 µs. The start symbol position (from 0H, start of line to bit 0 of the header) is 5.778 µs. The number of data bits encoded per symbol is 1 or bilevel. A logical high level is nominally 70 percent of peak white (i.e., 490 mV), and logical low is nominally 0 percent of peak white (0 mV).

The CX25874/5 encoder does not support the CEA 805A-TYPEB standard in 480p for the following reasons:

1. First, and most importantly, the position of Type A packet for 480p format must be in VBI line 41. Position of Type B Packet for 480p format must be in VBI line 40. This DENC cannot place CGMS-A and WSS data on alternate lines within the HDTV VBI for 480p.
2. Second, the Type B payload data symbol width (i.e., each analog bit interval) is different from the Type A payload data symbol width, along with other timing parameters.
3. Third, Type B Packet payload data is placed in 128 bits (16 bytes) versus 14 bits for Type A Packet payload data.

The four possible states of the CGMS bits are listed below:

- No more copies (one generation copy has been made).
- No copying is permitted.
- Copying is permitted without restriction.
- One generation of copies may be made.

1.3.37 Wide Screen Signaling—Standard-Definition TV

Ratios of 16:9 and other non-4:3 aspect ratios within SDTV are being adopted in increasing numbers. To assist in the management of this type of program material received by TVs, a WSS set of standards have recently been developed. These documents have allowed broadcasters, consumer equipment makers, and encoder vendors to a display 16:9 and other non-4:3 programs in their correct aspect ratio while simultaneously increasing their control over copyrighted media.

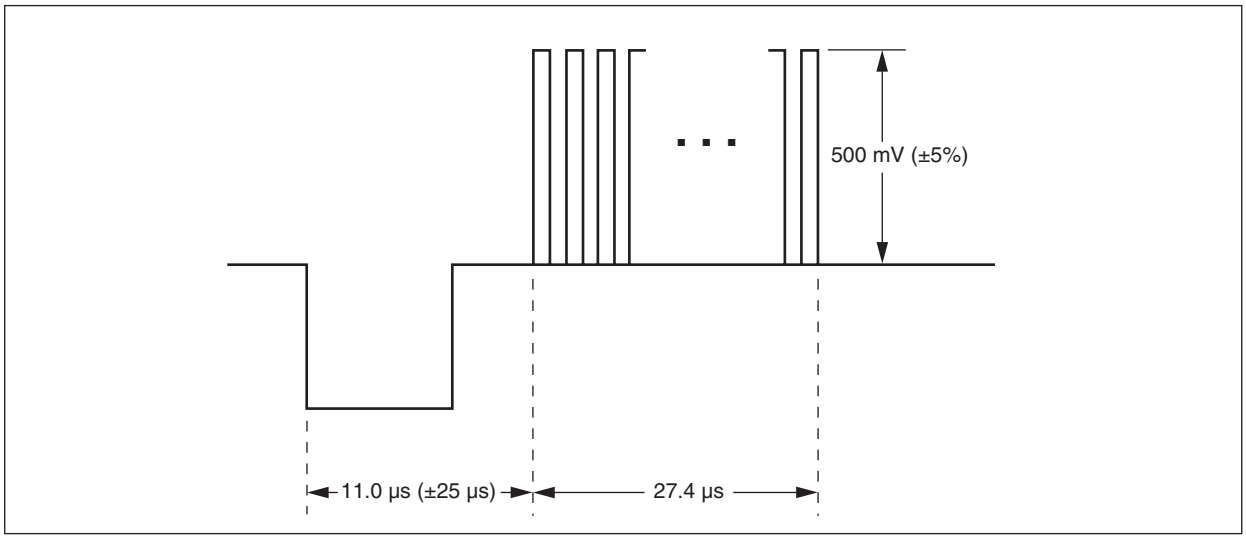
It is the intention of Macrovision to eliminate pirated copies. On the other hand, copyright management, a subset of WSS described in the EN 300 294 specification, is used to control the amount of legal copies allowed. For this type of copyright management to work, the equipment making the copy (e.g., VCR) must recognize and respond to the data being broadcasted. The WSS based encoder within the DVD player or game console transmits the data on the first part of PAL, line 23, and for NTSC, lines 20 and 283.

The CX25874/5 supports the most popular WSS standards for encoding of data into analog PAL or analog NTSC video signals. The PAL encode process for WSS is accomplished by using approximately the first 40 microseconds of Field 1's line 23 as described in the EN 300 249 (version 1.3.2) standard while the copyright management information is transmitted using a portion of these same bits. The 525-line NTSC composite and S-Video outputs comply with the EIAJ CPR-1204, IEC 61880-1 standards. For analog YUV video signals, WSS information will be present only on the Luma (Y) signal. For HDTV 480p Y PR PB outputs, the CX25874/5 encoder adheres to the EIAJ CPR-1204-1, CEA 805A-TYPEA only, CEA 770.1-C, and CEA 770.2-C (2H) standards, respectively. For HDTV 720p/1080i Y PR PB outputs, the CX25874/5 encoder adheres to the EIAJ CPR-1204-2 standard.

1.3.37.1 WSS for PAL-B, D, G, H, I, N, Nc Outputs (CGMS-A PAL)

For 625-line systems such as PAL, the first portion of line 23 is used to transmit the all the WSS information. An illustration of an encoded PAL Composite or Luma video signal from the CX25874/5 that contains WSS data is shown in Figure 1-30.

Figure 1-30. Horizontal Timing for PAL Output-Line 23 that Contains WSS Data



The peak-to-peak amplitude of the pulses present on line 23 is 500 mV with a tolerance of 5 percent. The signal's shape will be a sine-squared pulse based waveform. When WSS encoding is turned on, the clock frequency for WSS data encoded onto line 23 by the CX25874/5 is 5 MHz. The data is encoded using a format called biphase L coding. Basically, this means the encoder will output a sequence of three 500 mV. (above blanking level) pulses for a duration of 200 ns ±10 ns each then transmit three elements of the video blank level for a duration of 200 ns ±10 ns each. This 111 000 sequence comprises any 1 data bit written to the WSSDAT registers. Writing a 0 data bit to WSSDAT would force the CX25874/5 to output the opposite element sequence of 000 111. Consult your particular WSS standard for additional details on the biphase L coding format and the significance of each data bit to a WSS-compliant television.

The WSS sequence for PAL present on line 23 is normally comprised of a run-in code, a start code, and 14 bits of data unique to the broadcast content itself. The run-in code consists of seven hexadecimal elements plus a single bit (1 F 1C 71 C7 Hex) at 5 MHz. The start code consists of exactly six hexadecimal elements (1E 3C 1F Hex) also at 5 MHz. These two initial codes are generated by the CX25874/5 automatically. These codes are detected by enhanced PALplus TVs as a trigger mechanism to change the TV's Aspect Ratio, display enhanced services content, display subtitles, or respond to the reserved bits that get encoded after the initial codes.

The aspect ratio data consists of 4 data bits (b3 through b0) that specify the aspect ratio that should be used by the television if it has WSS and/or copyright management capability. Data bit b0 is considered the LSb. Descriptions of the four aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with black bars on the left and the right sides.

Option #2—14:9 aspect ratio: This content is best displayed with a 14:9 aspect ratio picture. The 14:9 aspect ratio picture should be centered on the display, with black bars on the left and the right sides.

Option #3—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

Option #4—greater than 16:9 aspect ratio: This content is best displayed with an aspect ratio exceeding 16:9. The >16:9 aspect ratio picture should be displayed as in Option #3 or use the full height of the display by zooming in.

For actual data bit assignments (e.g. b3, b2, b1, b0), and specific usage information (formats, positions, and number of active lines) for the Aspect Ratio, consult the ITU-R BT.1119 standard.

The enhanced services content that follows the Aspect Ratio information consists of a single data bit that turns on either camera mode or film mode. This data bit is denoted as b4.

The next 3 bits are all assigned a value of 0 since they are reserved. This bit field is comprised of b5, b6, and b7.

The subtitles data follows the three consecutive zeros. It consists of three data bits (b8 through b10) that specify whether or not subtitles are present and the position and/or appearance of the subtitles themselves. Data bit b8 is considered the LSb and controls whether or not subtitles exist within Teletext.

NOTE: A separate IC is required for transmission of Teletext-encoded data since the CX25874/5 does not have this capability. The combination DENC + DVI transmitter, CX25890/1/2, has an integrated Teletext encoder.

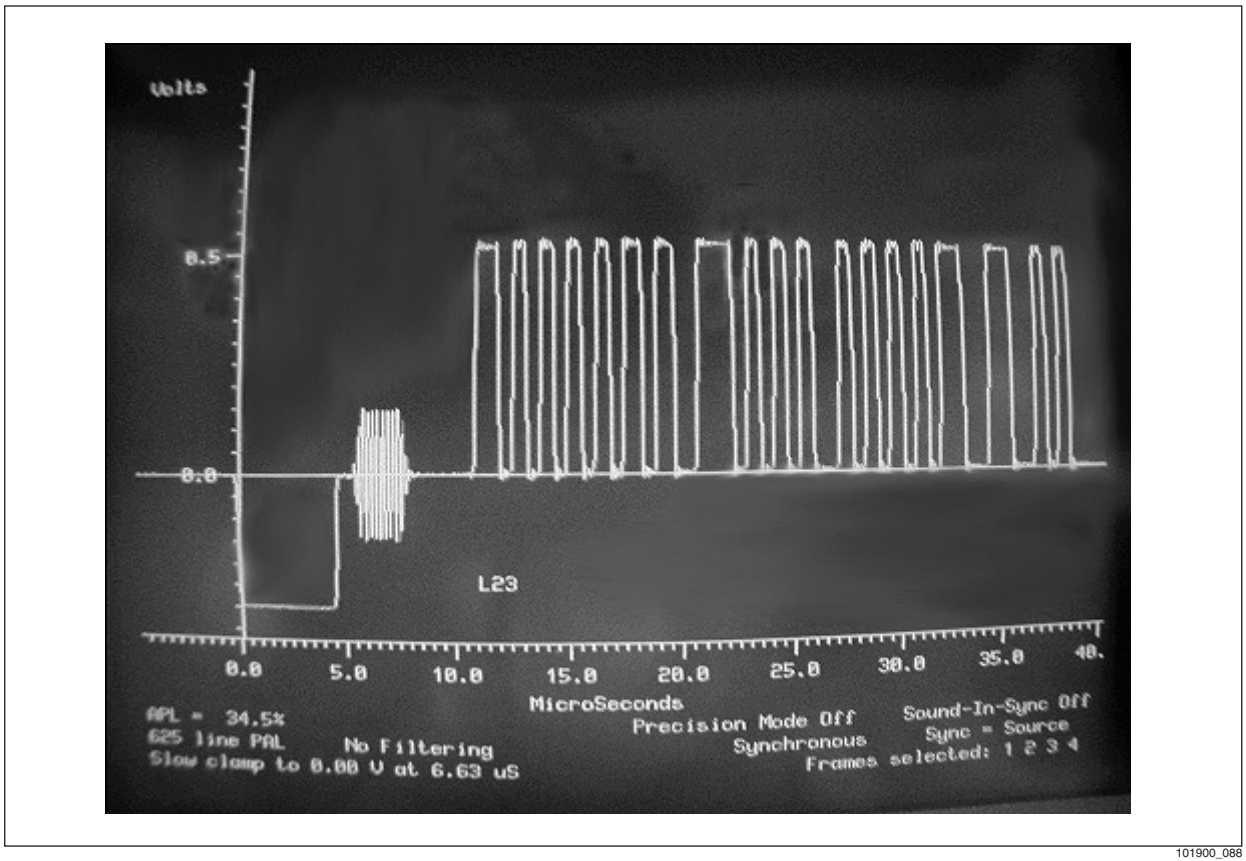
Bits b9 and b10 work in tandem to dictate the position of subtitles within Teletext. The allowable positions of teletext subtitles are inside the active image, outside the active image, or no open subtitles.

The final 3 bits are all assigned a value of 0 since they are reserved. This bit field is comprised of b11, b12, and b13.

An oscilloscope photo of an actual 625-line WSS signal from the CX25874/5 is shown in Figure 1-31. In this photo, the Conexant encoder has already been programmed into autoconfiguration mode #1 for a 640x480 input resolution and PAL-I output with roughly 16.5 percent overscan compensation. The input and output clock frequency of 29.50008 MHz in combination with the WSSINC equation below dictates a final WSSINC value of 2 B6 3D hex. For the WSS data, 4F hex has previously been written to register 0x60, A0 hex to register 0x62, and 00 hex to register 64 hex. This data has been encoded into the WSS PAL Composite signal, shown in Figure 1-31. Remember, all WSS (and/or copyright management) data registers must be filled with appropriate bit information for that standard. The data bits encoded below have no particular significance and are only meant as an illustration.

The CX25874/5 will not transmit new WSS data within line 23 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has been programmed. This byte of information can be the same value as before, or not, but it must be written to via the serial bus. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded.

Figure 1-31. WSS PAL Composite Signal from the CX25874/5



101900_088

In summary, to enable WSS within line 23 of the PAL Composite signal (or Luma channel within a PAL S-Video output) perform the sequence of serial writes found in Table 1-18.

Table 1-18. Switching Conexant Encoder into PAL WSS Output Operation

Step	Procedure
A	Configure the encoder so it generates a standard PAL-B, D, G, H, or -I output with the desired overscan compensation percentage. This can be done through the use of a standard PAL autoconfiguration mode (Appendix C) or a custom register set.
B	Probe or look up the input clock frequency to the encoder. This frequency can be found in Appendix C for all autoconfiguration modes and almost always matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 625-line formats: WSSINC (decimal) = 2^{20} / ($200*10^{-9}$ * F_{CLK})*(1)*
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66.
E	Program the CX25874/5's register 6A through 66 with the hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to 4 hex. The EWSSF2 bit has no effect with WSS or CGMS since Field 2-line 23 may not contain any encoded elements with the PAL output.
G	Write the WSSDAT registers with correct data per the ITU-R BT.1119 and EN 300 294 standards. The encoder generates the PAL WSS run-in and start code automatically but the data is under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal. WSSDAT[1], least significant bit of register 60, contains the data bit b0 as described in the standards, and WSSDAT[14] contains the most significant data bit, b13. Any information written to WSSDAT[20:15], in register 64, will be ignored for PAL WSS.
H	Use an oscilloscope or VM700 from Tektronix to verify WSS data is present on line 23 of Field 1 within the PAL video signal. Use 75 Ω termination.

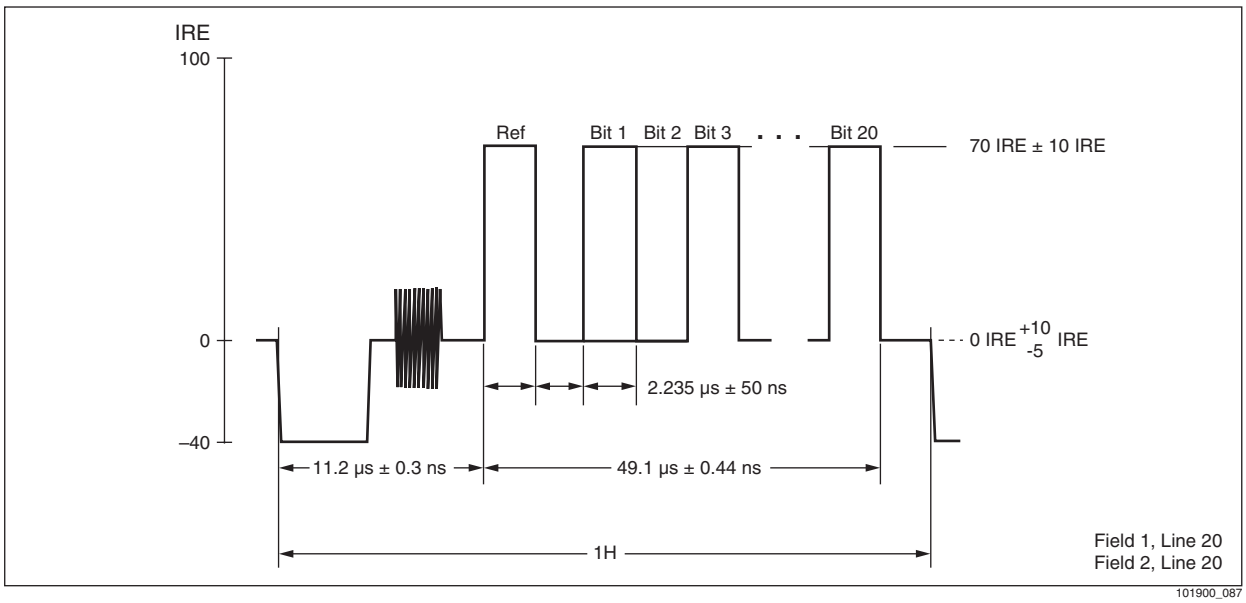
FOOTNOTE:
(1) The F_{CLK} term will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated.

The CX25874/5 is compliant with both major standards governing Wide Screen Signaling within 625-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *ITU-R BT.1119* and *EN 300 294 standard*s.

1.3.37.2 WSS for NTSC -M, J Outputs

For 525-line systems such as NTSC, lines 20 and 283 are used to transmit the all the WSS information required by the enhanced television receiver. An illustration of a typical NTSC video output Composite or Luma signal containing WSS data from the CX25874/5 is shown in Figure 1-32.

Figure 1-32. Typical WSS NTSC Analog Waveform Compatible to EIAJ CPR-1204 and IEC 61880-1



The bit frequency of each WSS bit encoded within line 20 and/or line 283 is the NTSC color subcarrier frequency divided by 8 (i.e., FSC / 8) or about 447.443 kHz. The peak-to-peak amplitude of the waveform present on line 23 is 490 mV with a tolerance of 14 percent. The signal's shape will be a sine-squared, pulse-based waveform. The data format utilized for CPR-1204 based information is standard binary whereby a 1 is denoted by a waveform level of 70 IRE (~490 mV) and a 0 as 0 IRE (video blank level).

The NTSC WSS sequence present on lines 20/283 is comprised of a start code, a data payload, and a Cyclic Redundancy Check (CRC) sequence. The total sequence of 22 bits takes up approximately 49.1 microseconds of line 20 or line 283. Each WSS bit therefore has a period of 2.235 µs $\pm$ 50 ns, as shown in Figure 1-32. The start code consists of 2 consecutive bits—a 1 and then a 0 transmitted in this order. The Conexant video encoder automatically generates the start code. This is a reference signal used as a trigger mechanism by Japanese-enhanced WSS TVs to change features such as the aspect ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25874/5 will not transmit new WSS data within lines 20 or 283 until the final WSSDAT register, address 0x64–WSSDAT[20:13], has be programmed. This byte of information can be the same value as before, or not, but it must be written to via the serial bus. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, without the presence of black bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the NTSC image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the program's 3D information, source information, signal format, category code, control code, character code, or the fact that Word 2 simply contains no additional data. This bit field is comprised of b3, b4, b5, and b6, where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the *EIAJ (Electronic Industries Association of Japan) CPR-1204 standard (March 1997), page 3.*

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the length and time remaining of the broadcast or the 3D signal format or audio and pull-down information or data pertaining to the consumer equipment package ID and code. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the *EIAJ CPR-1204 standard (March 1997) pages 4–9.*

The final six bits (b20, b19, b18, b17, b16, b15) comprise the error check code called CRC. The CRC used for NTSC WSS EIAJ CPR-1204 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 20/283 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25874/5 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204 standard (March 1997) page 10.*

In summary, to enable WSS within line 20 or line 283 of the NTSC Composite signal (or Luma channel within a NTSC S-Video output), perform the sequence of serial writes found in Table 1-19.

Table 1-19. Serial Writes Required to Switch Conexant Encoder into NTSC WSS Output Operation

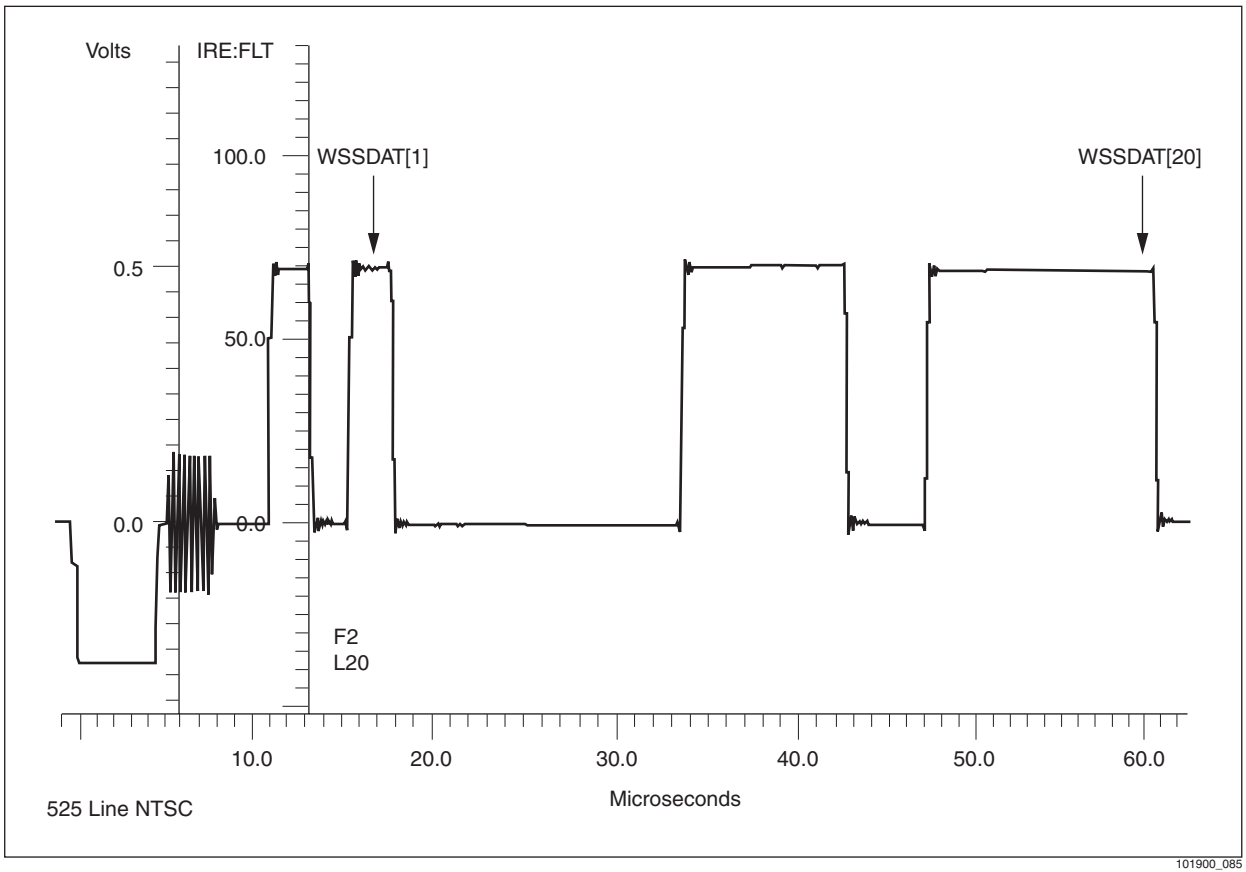
Step	Procedure
A	Configure the encoder so it generates a standard NTSC-M or NTSC-J output with the desired overscan compensation percentage. This can be done through the use of a standard NTSC autoconfiguration mode (Appendix C) or a custom register set.
B	If a NTSC-M (North America, Taiwan) output is desired, leave the SETUP bit set to 1. If a NTSC-J output is desired, reset the SETUP bit to 0.
C	Probe or look up the input clock frequency to the encoder. This frequency can be found in Appendix C for all autoconfiguration modes and almost always matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
D	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 525-line formats: WSSINC (decimal) = 2^{20} / (2.234*10^{-6}* F_{CLK})(1)
E	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For autoconfiguration mode #0, with F_{CLK} equal to 28.195793 MHz, WSSINC converts to 0 41 06 hex.
F	Program the CX25872/873's register 6A through 66 with the five hexadecimal nibbles from the previous step.
G	Set the EWSSF2 bit and EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to 0x0C. These bits have the effect of turning on WSS encoding for Field 2 (EWSSF2 bit) and Field 1 (EWSSF1).
H	Write the WSSDAT registers with correct data per the EIAJ CPR 1204 standard. The encoder generates the NTSC WSS start code automatically but the data and CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
I	Use an oscilloscope to verify WSS data is present on line 20 and/or line 283 within the NTSC video signal. Figure 1-33 shows the CX25874/5 encoder's Field 1, line 20 NTSC output after the encoder was previously programmed into autoconfiguration mode #0 and WSS enabled. The data encoded onto line 20 is FC F0 1 hex. WSSDAT[20:13] (register 0x64) has been written with FC, WSSDAT[12:15] (register 0x62) equals F0, and WSSDAT[20:13] (lowest nibble of register 0x60) has been written with C1. Register 0x60 also turned on WSS on Fields 1 and 2.

FOOTNOTE:

(1) The F_{CLK} term will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated.

An illustration of a WSS NTSC waveform with WSSDAT = FC F0 1 hex from the CX25874/5 is shown in Figure 1-33.

Figure 1-33. CX25874/5 WSS NTSC Line 20 Analog Waveform; WSSDAT = FC F0 1 hex



WSSDAT[2:0] = FC F0 1 hex in Figure 1-33 is just sample data. It has no correlation to the CRC or other required Word 1 and 2 values to actually enable WW/CGMS-A. This data was used to illustrate that WSSDAT[1] is placed at the beginning of line 20, and WSSDAT[20] is placed at the end of line 20.

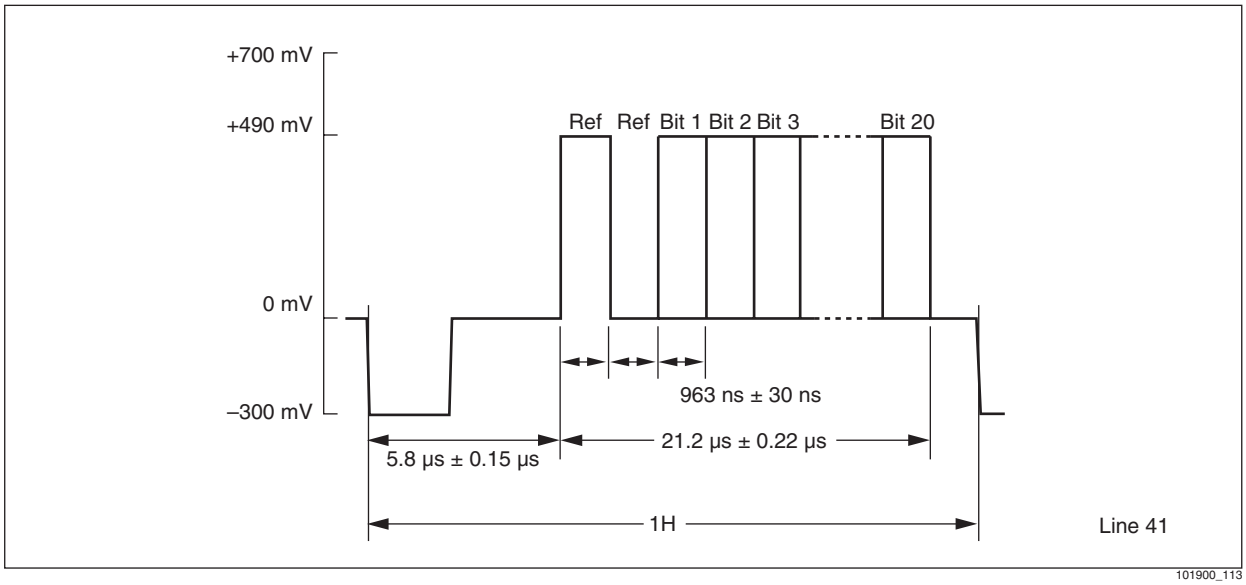
The CX25874/5 is compliant with Japan's *EIAJ CPR 1204* standard and the world IEC 61880-1 standard governing Wide Screen Signaling within 525-line television systems. For exact bit settings, definitions, timing, and other requirements, consult these documents.

1.3.38 Wide Screen Signaling (WSS)—High-Definition TV

1.3.38.1 WSS for 480p (525p) HDTV Outputs

For HDTV systems that receive the progressive 480p (525p in Japan) resolution, line 41 is used to transmit all the WSS information required by the enhanced television receiver. An illustration of a typical 480p (525p) Luma (Y) video signal containing WSS data from the CX25874/5 is shown in Figure 1-34.

Figure 1-34. Typical WSS 480p (525p) Luma Analog Waveform



NOTE: Figure 1-34 is compatible with EIAJ CPR-1204-1 and CEA 805A_TYPEA.

The bit frequency of each WSS bit encoded within line 41 is the horizontal scanning frequency multiplied by a factor of 33 which equates to 1038.5 kHz. The peak-to-peak amplitude of the waveform present on line 41 is 490mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 41. The data format used for CPR-1204-1 based information is standard binary, whereby a 1 is denoted by a waveform level of 490 mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 480p (525p) HDTV WSS sequence present on line 41 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 21.2 µs of this line. Each WSS bit therefore has a period of 0.963 µs ±30 ns as shown in Figure 1-34. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX258874/875 video encoder. This is a reference signal used as a trigger mechanism by Japanese-enhanced WSS 480p (525p) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25874/5 will not transmit new WSS data within line 41 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has been programmed. This byte of information can be the same value as the previous WSS data payload, or not, but it

must be written to via the serial bus to trigger a new WSS encode operation. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 480p (525p) image appears without horizontal black stripes (no letterbox), or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the program's 3D information, source information, signal format, category code, control code, character code, or the fact that Word 2 simply contains no additional data. As of the print date of this data sheet, only Word1 values between 0001 and 1010 binary are defined. This bit field is comprised of b3, b4, b5, and b6, where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the *EIAJ (Electronic Industries Association of Japan) CPR-1204-1 standard (March 1998) page 2*.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the *EIAJ CPR-1204 standard (March 1997) pages 4–9* and *EIAJ CPR-1204-1 standard (March 1998) pages 2–4.*

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-1 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 41 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25874/5 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204-1 (March 1997) page 10* and/or CEA 805A_TYPEA (CEA 770-1-C and CEA 770-2 (2H) 480p) standards.

To summarize, to enable WSS within line 41 of the 480p (525p) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 1-20.

Table 1-20. Serial Writes Required to Switch Conexant Encoder into HDTV 480p (525p) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 480p (525p) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set.
B	The input clock frequency to the encoder must be 27.00000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 480-line HDTV formats: WSSINC (decimal) = 2^{20} / ($963*10^{-9}* F_{CLK}$)(1) = 104856/26.001 = 40328
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 480p HDTV Y PR PB, with F_{CLK} equal to 27.00000 MHz, WSSINC converts to 0 9D 88 hex.
E	Program the CX25874/5's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit (bit 6) to 1 by programming the upper nibble of register 0x60 to 4 hex. Do not bother setting the EWSSF2 bit since the output will be progressive and there is no even (second) field. The EWSSF1 bit has the effect of turning on WSS encoding within the 480p (525p) HDTV Y analog output.
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 41 within the HDTV video signal. Some multiformity HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore a single gray line which will be the WSS-encoded data.

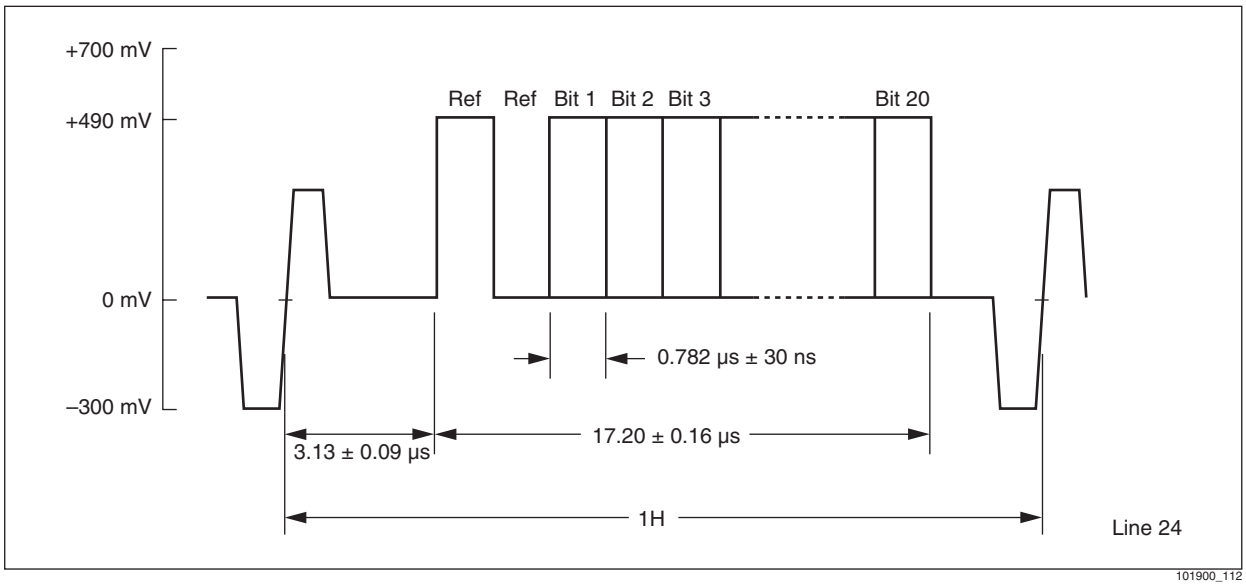
FOOTNOTE:
(1) The F_{CLK} term will remain the same for 480p HDTV. However, F_{CLK} will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of HDTV and standard-definition formats.

The CX25874/5 is compliant with Japan's *EIAJ CPR 1204-1 standard* governing Wide Screen Signaling within 525-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-1 standard* itself.

1.3.38.2 WSS for 720p (750p) HDTV Outputs

For HDTV systems that receive the progressive 720p (750p in Japan) resolution, line 19 (per *SMPTE 296M standard*) or line 24 (per Japan's *EIAJ CPR-1204-2*) is used to transmit all the WSS information required by the enhanced television receiver. An illustration of a typical 720p (750p) Luma (Y) video signal containing WSS data from the CX25874/5 is shown in Figure 1-35.

Figure 1-35. Typical WSS 720p (750p) Luma Analog Waveform



NOTE: Figure 1-35 is compatible with EIAJ CPR-1204-2.

The bit frequency of each WSS bit encoded within line 24 is the horizontal scanning frequency multiplied by (1650 / 58) which equates to 1278.8 kHz. The peak-to-peak amplitude of the waveform present on line 24 is 490 mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 24. The data format utilized for CPR-1204-2 based information is standard binary whereby a 1 is denoted by a waveform level of 490 mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 720p (750p) HDTV WSS sequence present on line 24 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 17.2 microseconds of this line. Each WSS bit therefore has a period of 0.782 µs ± 30 ns as shown in Figure 1-35. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX258874/875 video encoder. This is a reference signal used as a trigger mechanism by Japanese enhanced WSS 720p (750p) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25874/5 will not transmit new WSS data within line 24 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has be programmed. This byte of information can be the same value as the previous WSS data payload, or not, but it must be written to via the serial bus to trigger a new WSS encode operation. Using

register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 720p (750p) image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the time remaining in the program, or the fact that Word 2 simply contains no additional data. Word 1's bit field is comprised of b3, b4, b5, and b6 where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g. b3, b4, b5, b6), consult the EIAJ (Electronic Industries Association of Japan) *CPR-1204-2 standard (January 2000) page 3*.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of al

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-2 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 24 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25874/5 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204 standard (March 1997) page 10*.

To summarize, to enable WSS within line 24 of the 720p (750p) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 1-21.

Table 1-21. Serial Writes Required to Switch Conexant Encoder into HDTV 720p (750p) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 720p (750p) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set.
B	The input clock frequency to the encoder must be 74.25000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 720-line HDTV formats: WSSINC (decimal) = 2^{20} / ($0.782*10^{-6}*$ F_{CLK})[(1)] = 104856/58.0635= 18059
D	Once WSSINC has been solved for, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 720p HDTV Y PR PB, with F_{CLK} equal to 74.25000 MHz, WSSINC converts to 0 46 8B hex.
E	Program the CX25874/5's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set the EWSSF1 bit (bit 6) to 1 by programming the upper nibble of register 0x60 to 4 hex. Do not bother setting the EWSSF2 bit since the output will be progressive and there is no even (second) field. The EWSSF1 bit has the effect of turning on WSS encoding within the 720p (750p) HDTV Y analog output.
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 24 within the HDTV video signal. Some multi-format HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore a single gray line which will be the WSS encoded data.

FOOTNOTE:

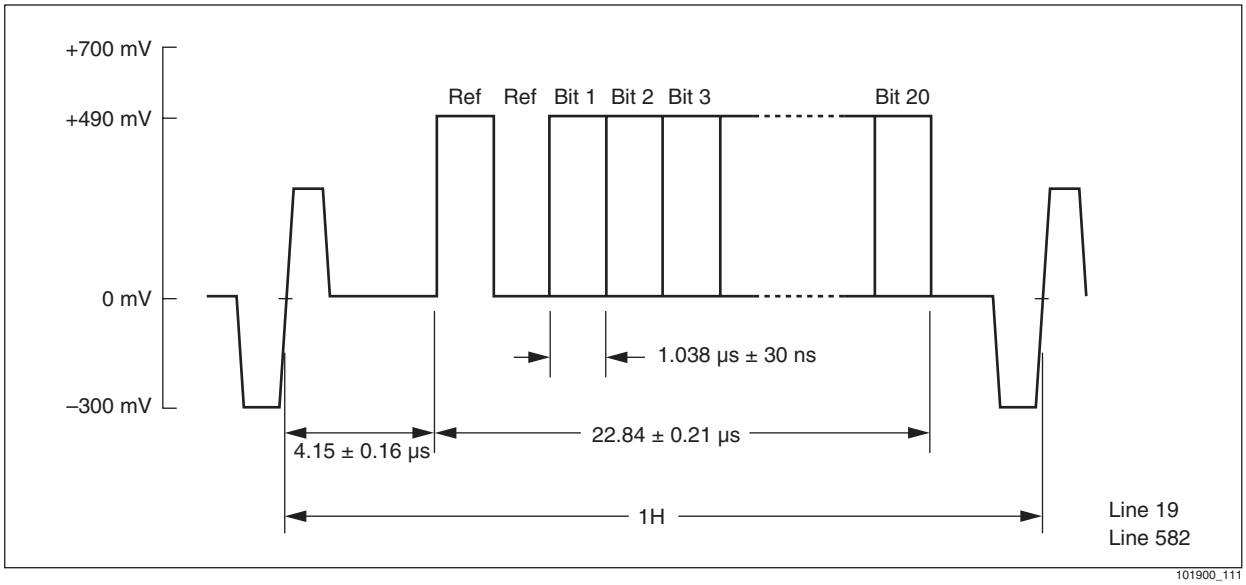
(1) The F_{CLK} term will remain the same for 720p HDTV. However, F_{CLK} will change every time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of other HDTV and standard-definition formats.

The CX25874/5 is compliant with Japan's *EIAJ CPR 1204-2 standard* governing Wide Screen Signaling within 750-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-2 standard* itself.

1.3.38.3 WSS for 1080i (1125i) HDTV Outputs

For HDTV systems that receive the interlaced 1080i (a.k.a. 1125i in Japan) resolution, lines 17 and 579 per the SMPTE 274M standard are used to transmit all the WSS information required by the enhanced television receiver. According to Japan's EIAJ CPR-1204-2 standard, lines 19 and 582 are used to transmit this same WSS information required by the enhanced television receiver. An illustration of a typical 1080i (1125i) Luma (Y) video signal containing WSS data from the CX25874/5 is shown in Figure 1-36.

Figure 1-36. Typical WSS 1080i (1125i) Luma Analog Waveform



NOTE: Figure 1-36 is compatible with EIAJ CPR-1204-2.

The bit frequency of each WSS bit encoded within line 19/582 is the horizontal scanning frequency multiplied by (2200 / 7) which equates to 963 kHz. The peak-to-peak amplitude of the waveform present on line 19/582 is 490 mV with a tolerance of ±49 mV. The signal's shape will be a pulse-based waveform embedded within line 19 or 582 or both. The data format utilized for CPR-1204-2 based information is standard binary whereby a 1 is denoted by a waveform level of 490mV and a 0 as 0 mV (video black level). Only the Y (luma) channel of the HDTV Y PR PB output will contain the WSS data.

The 1080i (1125i) HDTV WSS sequence present on line 19 or 582 is comprised of a start code and a data payload with a CRC sequence. The two reference bits (1 and then 0) and 20-bit data payload takes up approximately 22.8 µs of this line. Each WSS bit therefore has a period of 1.038 µs ±30 ns as shown in Figure 1-36. The two reference bits (a 1 and then a 0) transmitted in this order is automatically generated by the Conexant CX258874/875 video encoder. This is a reference signal used as a trigger mechanism by Japanese enhanced WSS 1080i (1125i) HDTVs to change features such as the Aspect Ratio, letter-box appearance, 3D information, and pull-down configuration based on the bits that get encoded after the initial start code.

The CX25874/5 will not transmit new WSS data within line 19/582 until the final WSSDAT register, address 0x64—WSSDAT[20:13], has be programmed. This byte of

information can be the same value as the previous WSS data payload, or not, but it must be written to via the serial bus to trigger a new WSS encode operation. Using register 0x64 as a WSS activation mechanism prevents partial incorrect sequences of information from being encoded into the luma channel.

The first data bit is called b1. It specifies the aspect ratio that should be used by the NTSC television if it has WSS capability. Descriptions of the two aspect ratio choices are as follows:

Option #1—4:3 aspect ratio: This content is best displayed with a 4:3 aspect ratio picture. The picture should be centered on the display, with or without the presence of black letterbox bars.

Option #2—16:9 aspect ratio: This content is best displayed with a 16:9 aspect ratio picture like most HDTVs. The 16:9 aspect ratio picture should be displayed using the full width of the display without the presence of black bars.

The second bit, b2, controls whether or not a letterbox is visible. The letterbox appears visually as a set of horizontal black stripes on the top and bottom of the screen. The letterbox is most commonly seen when a widescreen format DVD with a 16:9 ratio is played back on a TV with a standard 4:3 aspect ratio. Only two choices are possible with this bit: Either the HDTV 1080i (1125i) image appears without horizontal black stripes (no letterbox) or a letterbox is present.

The next four bits comprise Word 1. Word 1 is basically a header field that forces Word 2 into one of sixteen different configurations. Examples of these dissimilar configurations for Word 2 include the original broadcast's record date, its record time, the time remaining in the program, or the fact that Word 2 simply contains no additional data. Word 1's bit field is comprised of b3, b4, b5, and b6 where b3 is the MSb, and b6 is considered the LSb. For actual data bit assignments (e.g., b3, b4, b5, b6), consult the EIAJ (Electronic Industries Association of Japan) CPR-1204-2 standard (January 2000), page 3.

The subsequent eight bits that comprise Word 2 (b7, b8, b9, b10, b11, b12, b13, b14) contain different types of information depending on Word 1's value. Bit 7 is considered the LSb, and b14 is considered the MSb. This bit field could signify the time remaining in the broadcast or the record date. Other possibilities exist. Again, the information contained in Word 2 carries different meaning depending on the Word 1 bit values. For the definitions of all Word 2 values, consult the EIAJ CPR-1204 standard (March 1997) pages 4–9.

The final six bits (b20, b19, b18, b17, b16, b15) of the data payload comprise the error check code called CRC. The CRC used for WSS EIAJ CPR-1204-2 compliance is the following polynomial: {X6 + X + 1}, where X is preset to 1. This means that the final six bits of the line 19/582 sequence must all be received as 1 or the TV receiver may judge the incoming data as erroneous. CRC data is not encoded by the CX25874/5 automatically and must instead be inserted via the appropriate serial registers by the designer. For additional information on the CRC code, consult the *EIAJ CPR-1204 standard (March 1997) page 10.*

To summarize, to enable WSS within line 19 or line 582 of the 1080i (1125i) HDTV Luma (Y) signal perform the sequence of serial writes found in Table 1-22.

Table 1-22. Switching Conexant Encoder into HDTV 1080i (1125i) WSS Output Operation

Step	Instruction
A	Configure the encoder so it generates a standard 1080i (1125i) HDTV Y PR PB output by following the instructions contained in Appendix E using a custom register set. Make certain that the HSYNCI and VSYNCI bits in register C6 are programmed properly to match the polarity of the incoming HSYNC and VSYNC signals. Failure to do so will prevent 1080i WSS from being enabled.
B	The input clock frequency to the encoder must be 74.25000 MHz. This frequency matches the frequency being transmitted from the encoder's CLKO pin. This frequency is equivalent to F_{CLK}.
C	Taking the F_{CLK} term from the previous step and using the following equation, determine the clock incrementing factor, WSSINC in decimal, for 1080-line HDTV formats: WSSINC (decimal) = 2^{20} / (1.038*10^{-6}* F_{CLK})(1) = 104856/77.0715= 13605
D	Once WSSINC has been solved, perform a decimal to hexadecimal conversion to ascertain the five nibbles that comprise WSSINC[19:0]. The most significant nibble of this number becomes WSSINC[19:16] which is part of register 6A. The next two nibbles comprise register 68 which is WSSINC[15:8], and the final 2 nibbles form WSSINC[7:0] which is register 66. For 1080i HDTV Y PR PB, with F_{CLK} equal to 74.25000 MHz, WSSINC converts to 0 35 25 hex.
E	Program the CX25874/5's register 6A through 66 with the five hexadecimal nibbles from the previous step.
F	Set both the EWSSF2 bit and EWSSF1 bit to 1 by programming the upper nibble of register 0x60 to C hex. These bits have the effect of turning on WSS encoding for Field 2 (EWSSF2 bit) and Field 1 (EWSSF1).
G	Write the WSSDAT registers with correct data per the EIAJ CPR 1204-2 standard. The encoder generates the WSS start code automatically but the 14-bits of data and 6-bit CRC fall under the control of the designer. WSSDAT[14:1] will correspond to the 14 data bits of the WSS signal while WSSDAT[20:15} will correspond to the six bits required for the CRC sequence. WSSDAT[1], least significant bit of register 60, contains the data bit b1 as described in the standard, and WSSDAT[14] contains the most significant data bit, b14. Any information written to WSSDAT[20:15], in register 64, will be encoded as the CRC.
H	Use an oscilloscope to verify WSS data is present on line 19 and/or line 582 within the HDTV video signal. Some multi-format HDTVs can be placed into H/V delay mode, which allows for viewing of the entire Vertical Blanking Interval and therefore one or two gray lines which will be the WSS encoded data.

FOOTNOTE:

(1) The F_{CLK} term will remain the same for 1080i HDTV. However, F_{CLK} will change very time the active resolution, video output type, or horizontal overscan compensation percentage changes. As a result, WSSINC will need to be recalculated for support of HDTV and standard-definition formats.

The CX25874/5 is compliant with Japan's *EIAJ CPR 1204-2 standard* governing Wide Screen Signaling within 1125-line television systems. For exact bit settings, definitions, timing, and other requirements, consult the *EIAJ CPR 1204-2 standard* itself.

1.3.39 Chrominance and Luminance Processing

The CX25874/5 accepts digital pixels in either a YCrCb or RGB format. After receipt, these pixels are sent through an internal multiplexer and then 2x sampled. Next, the input data is converted to an internal YUV format. After that, the Y and UV components are filtered and finally upsampled to the system clock frequency.

The luminance signal is always low-pass filtered using the upsampling filter response illustrated in Figure 1-37. Additional peaking or reduction filters can be enabled (see Figures 1-38, 1-39, and 1-40), using the PKFIL_SEL[1:0] register field. The peaking filters are optimized for high bandwidth frequency response, and optimal picture quality.

The default chrominance filter response is illustrated in Figure 1-41. An alternate wide bandwidth response can be selected using register bit CHROMA_BW, as illustrated in Figure 1-42.

Figure 1-37. Digital Luminance Upsampling Filter

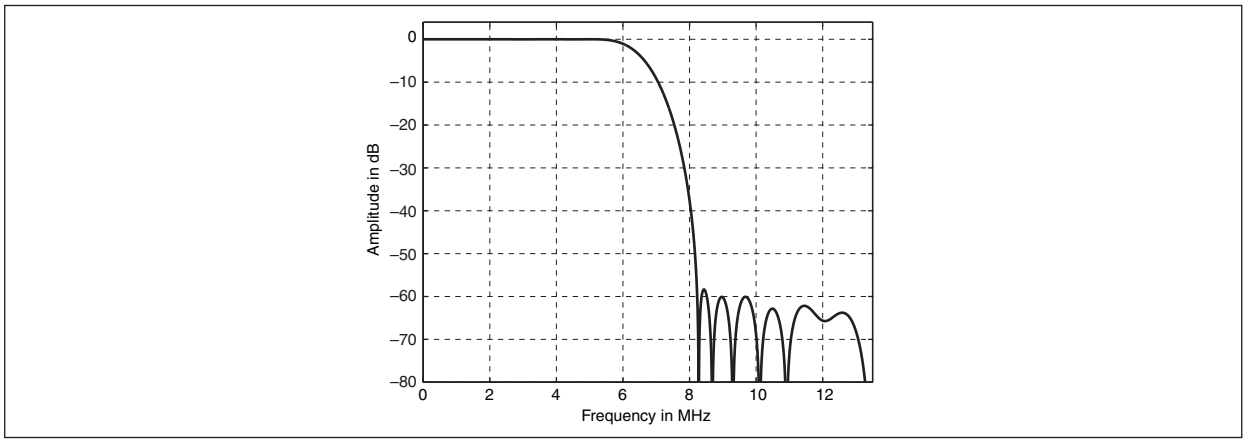


Figure 1-38. Text Sharpness (Luminance Upsampling) Filter with Peaking Options

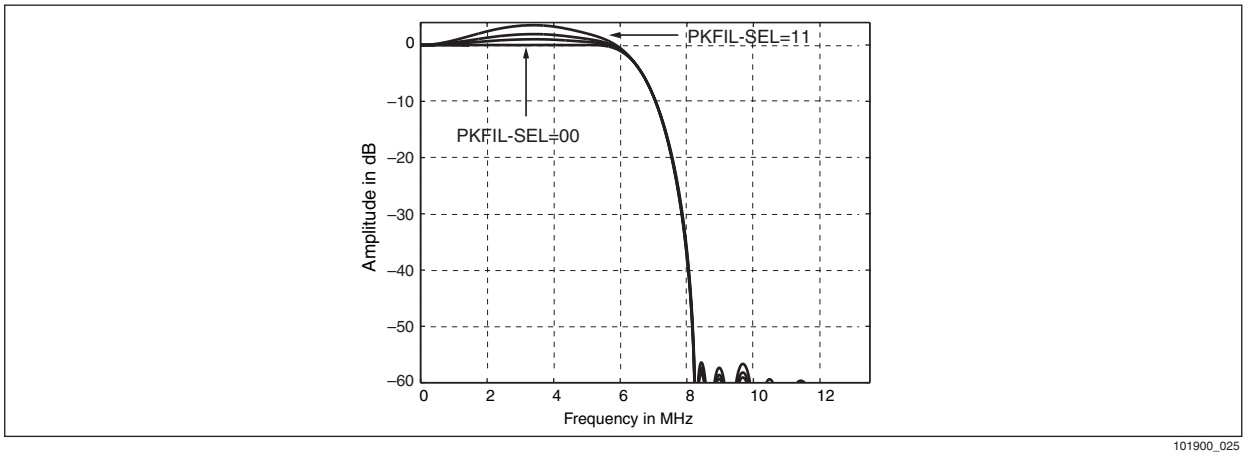
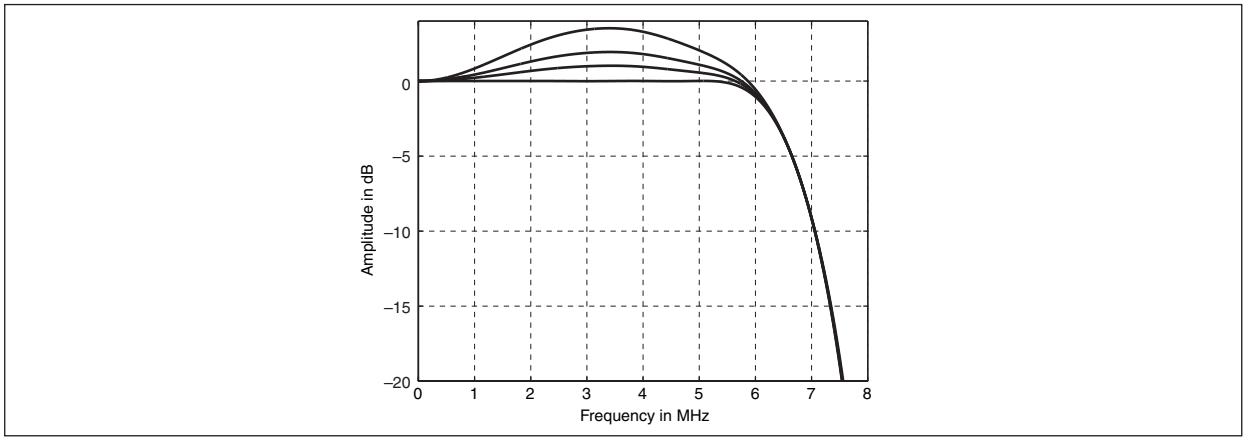
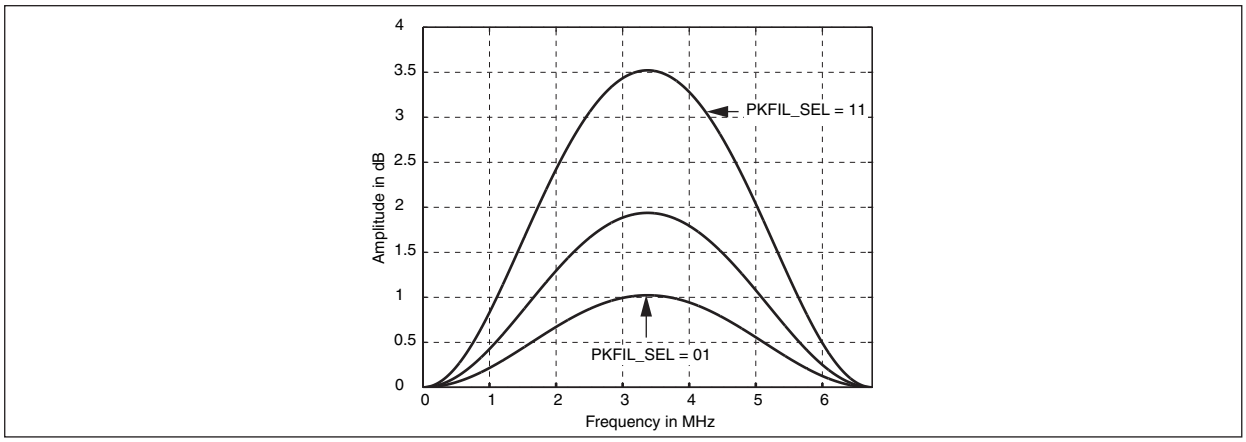


Figure 1-39. Close-Up of Text Sharpness (Luminance Upsampling) Filter with Peaking and Reduction Options



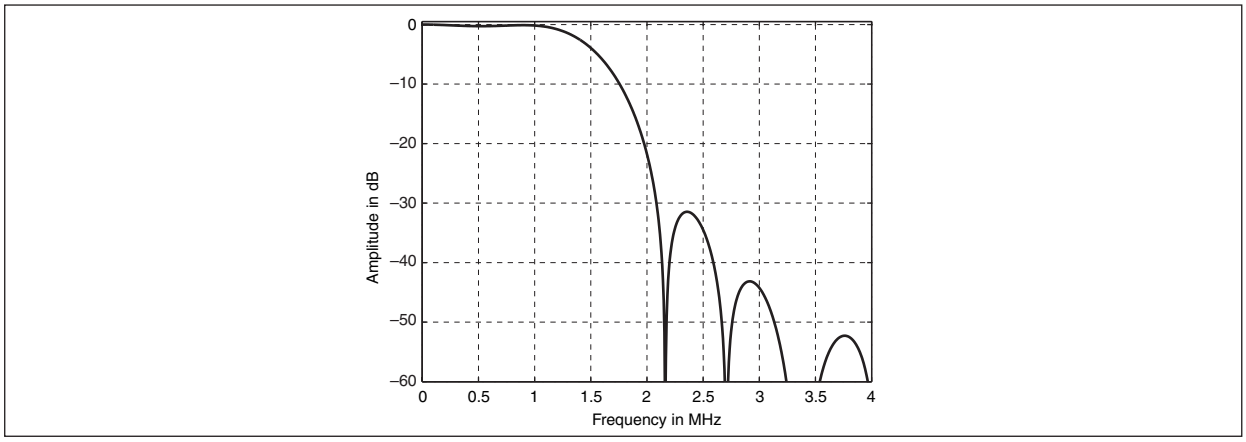
101900_026

Figure 1-40. Zoom-In of Text Sharpness (Luminance Peaking) Filter Options



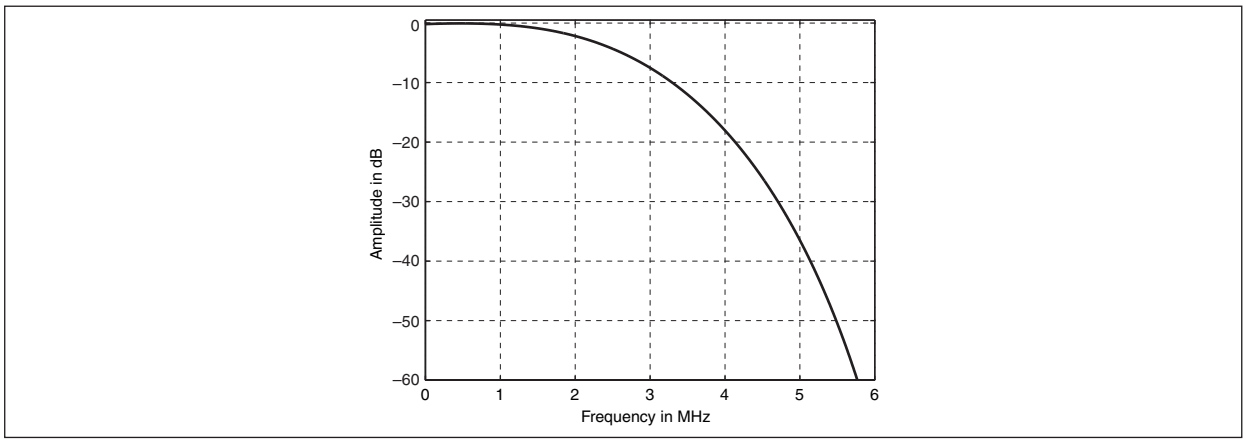
101900_027

Figure 1-41. Digital Chrominance Standard Bandwidth Filter (CHROMA_BW = 0—Default)



101900_028

Figure 1-42. Digital Chrominance Wide Bandwidth Filter (CHROMA_BW = 1)



1.3.40 Color Bar and Blue Field Generation

This encoder has two internal color bar generators. Preflicker HDTV filter color bars are enabled by setting the FFCBAR bit to a logical 1. Postflicker SDTV filter color bars are enabled by setting the ECBAR bit to a logical 1. The SDTV color bars have 100 percent amplitude levels and 75 percent chroma levels.

FFCBAR color bars are optimized for RGB input mode and ECBAR color bars are optimized for YCrCb input mode.

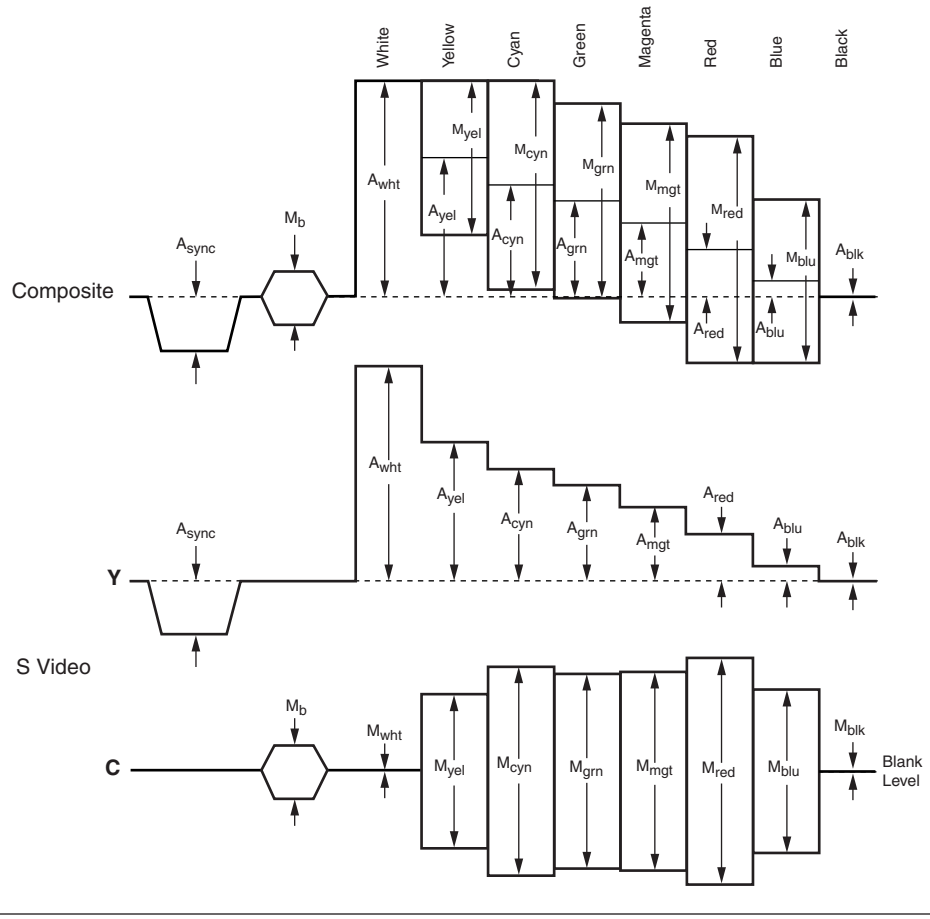
The device uses the H_BLANKO register value to determine the starting point of the color bars, and the H_ACTIVE register value to determine the width. Eight bars are displayed, with the colors and amplitudes being generated internally. The pixel inputs (P11–P0) are ignored in color bar mode. The CX25874/875 must be programmed with the appropriate MY, MCR, and MCB register values for the desired input format, RGB or YCrCb. This can be done through an autoconfiguration mode.

The CX25874/875 also produces a SDTV blue field by setting register bit BLUEFLD to 1. Pixel inputs are ignored while any of the color generation wave forms are being produced.

While SDTV color bars (ECBAR =1) or blue field are generated, the DENC does not need to receive the HSYNC*, VSYNC*, BLANK*, or CLKI input signals. The only requirement for these patterns is the presence of the main encoder clock found between the XTALIN and XTALOUT ports (master, pseudo-master interface).

Figure 1-43 and Tables 1-23 and 1-24 illustrate the voltage amplitudes for the different color bar outputs from the Conexant encoder.

Figure 1-43. Composite and S-Video Analog Voltage Levels (SDTV Color Bars)



GENERAL NOTE:
1.A $_x$ is the DC (luminance) amplitude referenced to black, except for A_{blk} and A_{sync}, which are referenced to blank.
2.M $_x$ numbers are the peak-to-peak amplitudes of the subcarrier waveform.

101900_031

Table 1-23. Composite and Luminance Color Bar Amplitudes

Y and Composite Amplitudes	A_{sync}	A_{wht}	A_{yel}	A_{cyn}	A_{grn}	A_{mgt}	A_{red}	A_{blu}	A_{blk}
NTSC-M (V)	–0.286	0.661	0.441	0.347	0.292	0.203	0.149	0.054	0.0536
NTSC-J (V)	–0.286	0.714	0.477	0.375	0.316	0.220	0.161	0.059	0
PAL-B (V)	–0.300	0.700	0.465	0.368	0.308	0.217	0.157	0.060	0
GENERAL NOTE: A_x is the DC (luminance) amplitude referenced to black, except for A_{blk} and A_{sync}, which are referenced to blank.									

Table 1-24. Composite and Chrominance Color Bar Magnitudes

C and Composite Magnitudes	M_b	M_{wht}	M_{yel}	M_{cyn}	M_{grn}	M_{mgt}	M_{red}	M_{blu}	M_{blk}
NTSC-M (V)	0.286	0	0.444	0.630	0.589	0.589	0.629	0.444	0
NTSC-J (V)	0.286	0	0.480	0.681	0.636	0.636	0.681	0.480	0
PAL-B (V)	0.300	0	0.470	0.663	0.620	0.620	0.664	0.470	0
GENERAL NOTE: M_x numbers are the peak-to-peak amplitudes of the subcarrier waveform.									

1.3.41 CCIR656 Mode Operation

Data transmitted from MPEG2 video decoders or various multimedia processors is often done in a format called CCIR656. This format is similar to CCIR601 in many ways but is unique in that the video sync information is embedded as codes in the data stream. As a result, no digital HSYNC or VSYNC signals are required as part of the physical interface between the timing master and slave devices. Applications for CCIR656 typically include consumer appliances such as Video CD players, DVD players, set-top boxes, and MPEG add-in cards where pin counts are limited.

The actual digital CCIR656 input data delivered to the CX25874/875 is interlaced 4:2:2 YCrCb over eight physical lines. In addition, there are two timing reference codes, one at the beginning of each video data block (Start of Active Video, SAV) and one at the end of each video data block (End of Active Video, EAV). These timing reference values consist of a unique 4-word sequence that conveys when the active video starts and ends. The CCIR656 compliant master device embeds both SAV and EAV codes into the stream where appropriate.

While in CCIR656 Mode, the CX25874/875 acts as the timing slave device. An illustration of a correct connection scheme for the slave interface is shown in Figure 1-44.

All data between the EAV code and SAV code are automatically inserted by the Conexant encoder. An 80 hexadecimal number is inserted for Cb and Cr samples and 10 hexadecimal for Y samples. This blanking data and SAV/EAV codes are the only differences between the CCIR656 mode and CCIR601 mode operation.

NOTE: Both EAV and SAV codes contain a prefix of FF0000 prior to the unique "XY" event code.

Pertinent SAV and EAV codes are contained in Table 1-25.

Figure 1-44. CX25874/875 Connection to CCIR656-Compatible Master Device

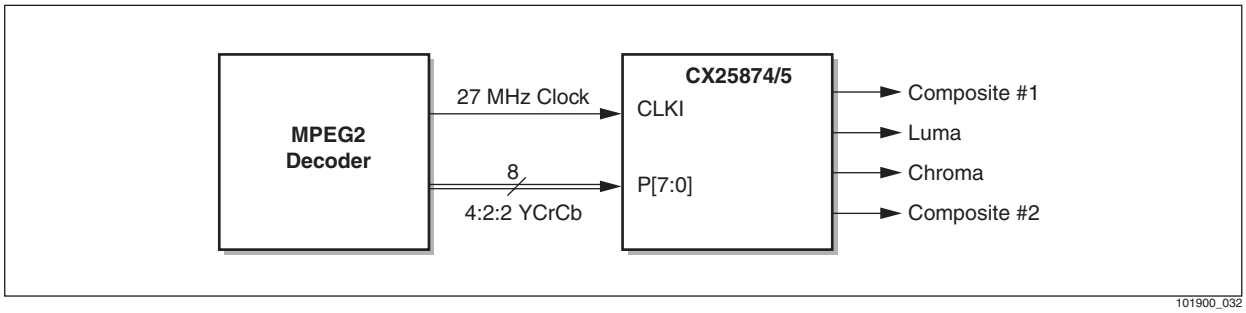


Table 1-25. CCIR656 "XY" Events

"XY" Event	SAV	EAV
Odd Field Vertical Blanking Lineq	0xAB	0xB6
Odd Field Active Video Line	0x80	0x9D
Even Field Vertical Blanking Line	0xEC	0xF1
Even Field Active Video Line	0xC7	0xDA

While in CCIR656 Mode, the encoder adheres to all input guidelines specified in the ITU-R BT.656-3 standard. This specification was developed for the transmission of color video signals in YCrCb format at a pixel rate of 27.000 MHz without the use of dedicated timing reference signals.

To display a DVD movie on a TV and computer monitor simultaneously, CCIR656 data must be sent from a MPEG2 decoding master device directly to the CX25874/875 encoder. Finally, various software steps are necessary so the encoder is set up to accept the interlaced YCrCb data and video timing reference codes.

The first programming step is to configure the CX25874/875 to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x480 and output a standard NTSC video output. The pertinent set of conditions for this option are:

- Type of Digital Video Input: Interlaced 4:2:2 YCrCb
- Active Resolution (HorizontalxVertical): 720 pixels x 480 lines
- Overscan Compensation: None. Horizontal = 0%; Vertical = 0%
- Interface: Pseudo-master or slave
- Pixel Rate 27.000 MHz
- Type of Analog Video Output: Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 28 is a perfect fit. As a result, simply use the MPEG2 decoders' serial bus mastering ability to program the CX25874/875s CONFIG[5:3] and CONFIG [2:0] fields with a binary value of 011 100. This translates into writing a hexadecimal number of 0x34 to register 0xB8, since both bits 7 and 3 are reserved, and therefore 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4, including register 0x38. The exact data transferred into these registers is contained in Appendix C.

After completion of the autoconfiguration command, the encoder expects to receive interlaced 4:2:2 YCrCb data from the clock and timing master device at a rate of 27.000 MHz with blanking regions being defined by HSYNC* and VSYNC*. Since these external signals, by definition, do not exist in CCIR656 mode, a second and final programming step is required.

After enabling autoconfiguration mode 28, the programmer must make sure to set the E656 bit to 1. This is bit 6 of register 0xD6 and enables a CCIR656 input to be received via the CX25874/875's P[7:0] port or P[11:4] port, depending on the state of the IN_MODE[3:0] field. Once this is done, the encoder disregards the synchronization signals.

Only after the completion of these steps will a DVD stream be properly encoded and rendered onto the television by the VGA Encoder.

For CCIR656 Mode operation with a PAL Composite or S-Video output, use Autoconfiguration Mode 29 instead of autoconfiguration mode 28 and program the master device to send a digital frame with an active resolution of 720x576.

1.3.42 CCIR601 Mode Operation for DVD Playback

Data coming from a DVD is often decoded by a MPEG2 decoder or graphics controller into a format called CCIR601. CCIR601 is the more common name for 4:2:2 YCrCb data at a 27 MHz pixel rate, as specified in the ITU-R BT.601 standard. This specification was developed specifically for the digitalization of color video signals.

To play a DVD movie on a television in addition to a CRT monitor, CCIR601 data must be sent from a MPEG2 decoding master device directly to the CX25874/875 encoder. This can be either a dedicated MPEG2 decoder chip or a graphics controller with this functionality. Various software steps are necessary so that the encoder enters slave or master interface and is set up to accept the interlaced YCrCb data or noninterlaced RGB digital format. After all of these steps have been executed properly, a DVD movie stream is properly encoded and rendered onto the television by the VGA encoder.

There are different capabilities among graphics controllers, MPEG2 decoders, and proprietary ASICs that impact the particular DVD implementation. This section seeks to cover the most common hardware/software configurations and the trade-offs associated with each. If the reader has an interface idea about the routing of data from the CCIR601 source to encoder that is not discussed here, please contact your local Conexant Field Applications Engineer for further technical support.

1.3.42.1 CCIR601 Data In/NTSC Out

The first option to playing a DVD movie via the CX25874/875 is to send the digital video CCIR601 data directly to the encoder from the MPEG2 decoder. In this case, the graphics controller does not have any effect on the CCIR601 digital stream arriving at the input of the encoder because it bypassed the data or the data was routed around the controller. In either case, the CX25874/875 must be configured to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x480 and output a standard NTSC video output. The pertinent set of conditions for this option are:

- Type of Digital Video Input: Interlaced 4:2:2 YCrCb
- Active Resolution (HorizontalxVertical): 720 pixels x 480 lines
- Overscan Compensation: None. Horizontal = 0%; Vertical = 0%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.000 MHz
- Type of Analog Video Output: Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 28 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011100. This translates into writing a hexadecimal number of 0x34 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate value for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix C.

After completion of the autoconfiguration command, the encoder expects to receive interlaced CCIR601 data from the clock and timing master device at a rate of 27.000 MHz. If this occurs, approximately 40 clocks later (i.e., pipeline delay through the decoder), the CX25874/5 begins transmitting a NTSC-compatible S-Video or Composite Video signal containing the DVD movie.

1.3.42.2 CCIR601 Data In/PAL Out

The second option is very similar to the first. In this scenario, the interlaced CCIR601 video data is transmitted directly to the encoder from the MPEG2 decoder. However, instead of generating a NTSC signal, the encoder produces a PAL-BDGHI compatible DVD movie output. The active resolution changes as well for this alternative by increasing to 720x576.

To enable DVD playback in this scenario, the CX25874/875 must be configured to accept interlaced 4:2:2 YCrCb data with an active resolution of 720x576 and output a standard PAL video output. The pertinent set of conditions for this option are:

- Type of Digital Video Input: Interlaced, 4:2:2 YCrCb
- Active Resolution (HorizontalxVertical): 720 pixels x 576 lines
- Overscan Compensation: None. Horizontal = 0%; Vertical = 0%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.000 MHz
- Type of Analog Video Output: Standard PAL[PAL-BDGHI]

Given this set of conditions, autoconfiguration mode 29 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011 100. This translates into writing a hexadecimal number of 0x35 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate value for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix C.

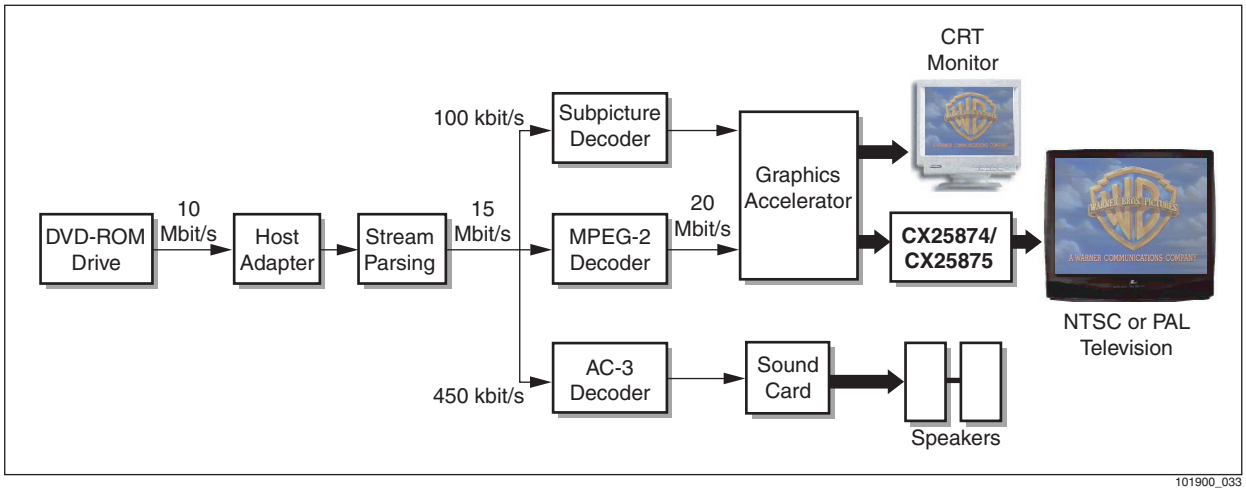
After completion of the autoconfiguration command, the encoder expects to receive interlaced CCIR601 data from the clock and timing master device at a rate of 27.000 MHz. If this occurs, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.3.42.3 VGA-Compatible RGB Data In/NTSC Out

The third option for DVD playback is unlike the previous two methods. In this case, the MPEG2 decoder's 4:2:2 YCrCb interlaced data is sent as an input to the graphics controller. In turn, the controller deinterlaces and color space converts the CCIR601 data into a noninterlaced RGB format. The encoder finally ends up receiving this standard VGA digital data from the graphics controllers digital output port for generation into an analog TV signal.

This design is illustrated in Figure 1-45.

Figure 1-45. DVD Playback Utilizing Graphics Controller for Color-Space and Progressive Scan Conversion



To enable DVD playback with this architecture, the graphics controller must be able to deinterlace and color space convert the CCIR601 input data from the MPEG2 decoding source. Furthermore, since the pixel clock frequency is not 27.000 MHz any longer, the graphics controller must have the ability to synchronize the pixel data to the clock rate dictated by the CX25874/875's CLKO signal. Finally, the controller must be able to function as the clocking master and timing slave as described in Section 1.3.8.

The recommended interface for the CX25874/875 for this option is master and the encoder must be programmed to accept noninterlaced RGB data and output a standard NTSC video output. The pertinent factors for the NTSC option are:

- Type of Digital Video Input: Progressive Scan/Noninterlaced; 24-bit RGB per pixel Multiplexed Input Format
- Active Resolution (HorizontalxVertical): 720x480
- Overscan Compensation Ratio: Minimal; Horizontal = 1.24%; Vertical = 1.23%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.6923 MHz
- Type of Analog Video Output: Standard NTSC[NTSC-M]

Given this set of conditions, autoconfiguration mode 44 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 101100. This translates into writing a hexadecimal number of 0x54 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers is contained in Appendix C.

After completion of the autoconfiguration command, the encoder enters master interface. In addition, the CX25874/875 will expect to receive digital frames with an active resolution of 720x576 comprised of noninterlaced RGB data at a pixel rate of 27.6875 MHz. If these events occur, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.3.42.4 VGA-Compatible RGB Data In/PAL Out

The CX25874/5 can also be programmed to accept noninterlaced RGB data and output a standard PAL video output with ultra-low overscan compensation. The pertinent factors for this PAL option are:

- Type of Digital Video Input: Progressive Scan/Noninterlaced; 24-bit RGB per pixel Multiplexed Input Format
- Active Resolution (HorizontalxVertical): 720x576
- Overscan Compensation Ratio: Minimal; Horizontal = 0.017%; Vertical = 1.00%
- Interface: Master, pseudo-master, or slave
- Pixel Rate 27.6875 MHz
- Type of Analog Video Output: Standard PAL [PAL-B, D, G, H, I]

Given this set of conditions, autoconfiguration mode 31 is a perfect fit for this architectural option. As a result, simply use the MPEG2 decoder's serial bus mastering ability to program the CONFIG[5:3] and CONFIG[2:0] field with a binary value of 011100. This translates into writing a hexadecimal number of 0x37 to register 0xB8, since both bits 7 and 3 are reserved and therefore, 0. Once the encoder acknowledges this write to its autoconfiguration register, it automatically loads the appropriate values for this type of DVD configuration into its register indices from 0x76 to 0xB4 including 0x38. The exact data transferred into these registers in contained in Appendix C.

After completion of the autoconfiguration command, the encoder enters master interface. In addition, the CX25874/5 will expect to receive digital frames with an active resolution of 720x576 comprised of noninterlaced RGB data at a pixel rate of 27.6875 MHz. If these events occur, approximately 40 clocks later (i.e., pipeline delay), the encoder will begin transmitting a PAL-compliant S-Video or Composite video signal containing the DVD movie.

1.3.43 SECAM Output

Unlike the Bt868/869, the CX25874/875 now includes an encoder block for conversion of digital video data into a SECAM Composite (CVBS) and/or a SECAM S-Video signal.

Like other standard-definition video outputs, any active resolution from 320x200 to 1024x768 can be supported with the SECAM encoder block. The circuit accepts RGB or YCrCb data in a variety of multiplexed input formats, reformats the digital data, and finally routes the stream through the four on-chip Digital-to-Analog Converters (DACs). The encoder supports all variations of the SECAM analog video standard including those commonly used in France (SECAM-L), Eastern Europe/Russia (D, K, K1), and Greece/Middle East (B, G, H).

The SECAM specific processing is achieved in this block by pre-emphasizing the color difference signals. Once data is received, it is converted to an internal YUV format. Next, the Y component is filtered and then upsampled to the system clock frequency while the UV components are used to frequency modulate the two subcarrier frequencies appropriately.

For information on the luminance signal, peaking and reduction filters, and default chrominance filter, see Section 1.3.39.

The color subcarrier frequencies, 4.25000 MHz for Db and 4.40625 MHz for Dr, are controlled by a number of registers, chiefly MSC_DB[31:0] for Db and MSC[31:0] for Dr. Figure 1-46 illustrates the SECAM pre-emphasis filter response at higher (>3 MHz) frequencies within the standard-definition television passband. The figure illustrates the SECAM-specific, pre-emphasis filter response for the modulated chrominance signal.

Table 1-26 lists three complete register sets for the most common desktop input resolutions with the SECAM output. This output adheres to the SECAM target video parameters included in Table A-1. Correct timing occurs only if the Conexant encoder is programmed correctly with the register values listed in Table 1-26, the master device provides the RGB data at the listed clock frequency (CLKI and CLKO), and the interface bits are modified to match the desired connection type.

Figure 1-46. SECAM High Frequency Pre-emphasis Filter

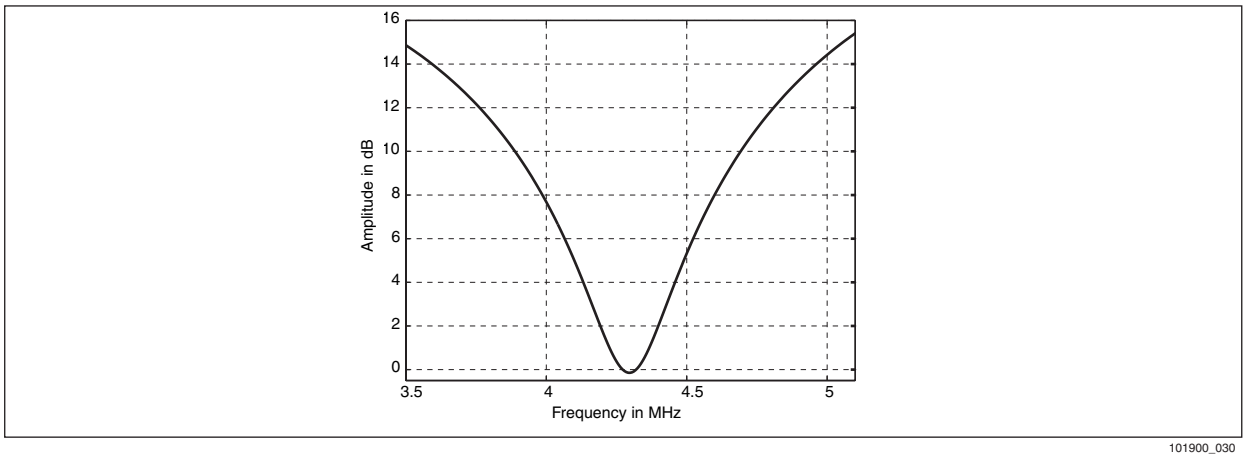


Table 1-26. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(1 of 4)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	**800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%**	**1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%**
CLKI and CLKO Frequency	29.500007 MHz	36.000000 MHz	67.687489 MHz
State of PLL_32CLK bit	0	0	1
Internal Pixel Clock Frequency	29.500007 MHz	36.000000 MHz	45.124993 MHz
Register Address	**CX25874/5 Register Values**	**CX25874/5 Register Values**	**CX25874875 Register Values**
0x00	00	00	00
0x02	00	00	00
0x04	00	00	00
0x06	00	00	00
0x2E	00	00	00
0x30	00	00	00
0x32	00	00	00
0x34	00	00	00
0x36	00	00	00
0x38	00	00	20
0x3A	00	00	00
0x3C	80	80	80
0x3E	80	80	80
0x40	80	80	80
0x42*(1)*	8B	8E	9B
0x44*(1)*	A0	E3	5D
0x46*(1)*	E1	38	1C
0x48*(1)*	24	1E	18
0x4A*(1)*	28	3A	5F
0x4C*(1)*	3B	77	C4
0x4E*(1)*	25	1C	13
0x50*(1)*	28	3A	5F
0x52*(1)*	3B	77	C4
0x54*(1)*	25	1C	13

Table 1-26. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(2 of 4)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
Register Address	**CX25874/5 Register Values**	**CX25874/5 Register Values**	**CX25874/5 Register Values**
0x56[(1)]	AC	18	7A
0x58[(1)]	20	27	31
0x5A	00	00	00
0x5C	00	00	00
0x5E	00	00	00
0x60	00	00	00
0x62	00	00	00
0x64	00	00	00
0x66	3C	E3	D9
0x68	00	00	00
0x6A	00	00	00
0x6C[(2)]	46	46	46
0x6E	00	00	00
0x70	0F	0F	0F
0x72	00	00	00
0x74	01	01	01
0x76	60	00	48
0x78	80	20	00
0x7A	8A	AA	D4
0x7C	A6	CA	FC
0x7E	68	9A	E2
0x80	C1	0D	79
0x82	2E	29	28
0x84	F2	FC	FE
0x86	27	39	4B
0x88	00	00	00
0x8A	B0	C0	91
0x8C	0A	8C	5E
0x8E	0B	03	0D

Table 1-26. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out *(3 of 4)*

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
Register Address	**CX25874/5 Register Values**	**CX25874/5 Register Values**	**CX25874/5 Register Values**
0x90	71	EE	B6
0x92	5A	5F	76
0x94	E0	58	00
0x96	06	0A	3F
0x98	00	66	A4
0x9A	50	96	A0
0x9C	72	0	55
0x9E	1C	0	15
0xA0	0D	10	1E
0xA2	8C	8C	24
0xA4	F0	F0	F0
0xA6	58	57	56
0xA8*(1)*	76	5F	4B
0xAA*(1)*	4D	3E	31
0xAC	8C	8C	8C
0xAE*(1)*	EA	55	76
0xB0*(1)*	BE	55	4A
0xB2*(1)*	3C	55	FF
0xB4*(1)*	26	1F	18
0xB6	00	0	0
0xB8	01	3	33
0xBA	00	0	0
0xBC	00	0	0
0xBE	00	0	0
0xC0	00	0	0
0xC2	00	0	0
0xC4*(3)*	01	1	1
0xC6*(4)*	03	3	3

Table 1-26. Register Values for 640x480 / 800x600 / 1024x768 RGB In, SECAM-L Out (4 of 4)

	640x480 RGB in, SECAM-L out HOC = 16.55%, VOC = 16.66%	800x600 RGB in, SECAM-L out HOC = 14.52% VOC=13.19%	1024x768 RGB in, SECAM-L out HOC = 12.72% VOC = 12.15%
Register Address	**CX25874/5 Register Values**	**CX25874/5 Register Values**	**CX25874/5 Register Values**
0xC8	1B	1B	1B
0xCA	C0	C0	C0
0xCC	C0	C0	C0
0xCE(5)	24	24	24
0xD0	00	0	0
0xD2	00	0	0
0xD4	00	0	0
0xD6	00	0	0
0xD8	40	40	40

FOOTNOTE:
(1) This is a SECAM specific register.
(2) Register 0x6C contains the TIMING_RESET bit. Set this bit as your last programming step and the CX25874/5 will clear it automatically later.
(3) Register 0xC4 contains the EN_OUT bit. Adjust according to your design's interface as necessary.
(4) Register 0xC6 contains the EN_BLANKO, EN_DOT, and IN_MODE[2:0] bits. Adjust according to your design's interface as necessary.
(5) Register 0xCE contains the OUT_MUXD[1:0], OUTMUXC[1:0], OUTMUXB[1:0], and OUTMUXA[1:0] bit fields for output routing. Adjust according to your design's interface as necessary.

The procedure required to obtain a SECAM output with an overscan compensation percentage that differs from those solutions in Table 1-26 is fairly simple. First, configure the encoder so it generates a standard PAL-B, D, G, H, I output with the desired overscan compensation percentage. This can be done through the use of a PAL-B, D, G, H, I autoconfiguration mode, a hand-generated, or a predefined register set. Second, perform a full register read-back from the CX25874/875. Carefully note the value for register 0xA2. Third, program the bits found in Table 1-27 to their new state within the CX25874/875.

Table 1-27. Vital SECAM Bit Settings–Register 0xA2

Bit Name	Location	State for PAL-BDGHI	State for SECAM
FM	Bit 7 of register 0xA2	0	1
PAL_MD	Bit 5 of register 0xA2	1	0
VSYNC_DUR	Bit 3 of register 0xA2	0	0

Finally, calculate the values, found in Table 1-28, for the MSC_DB[31:0], MCR[7:0], MCB[7:0], FILFSCONV[5:0], FIL4286INCR[7:0], and MSC[31:0] registers for the particular SECAM overscan solution. To accomplish this task, readback both values that comprise the HCLKO[11:0] register, convert it to decimal (base 10), and use it in the equations below. After solving each SECAM register equation, perform a conversion back to a hexadecimal number and program the appropriate registers with their new SECAM specific values. Refer to Table 1-28.

The equations for generation of a SECAM output based on a RGB input only are:

- MSC_DB[31:0] = int ((272 / H_CLKO[11:0]) * 2^{32} + 0.5)
- DR_LIMITP[10:0] = ((4.756 MHz/ Internal Pixel Clock Frequency)*2^13)
- DR_LIMITN[10:0] = ((3.9 MHz/ Internal Pixel Clock Frequency)*2^13)
- DB_LIMITP[10:0] = ((4.756 MHz/ Internal Pixel Clock Frequency)*2^13)
- DB_LIMITN[10:0] = ((3.9 MHz/ Internal Pixel Clock Frequency)*2^13)
  - If PLL_CLK32 is 0, then Internal Pixel Clock Frequency = CLKI = CLKO.
  - If PLL_CLK32 is 1(for some overscan ratios in 800x600 and all 1024x768 resolutions), then Internal Pixel Clock Frequency = (2/3) * CLKI
- FIL4286INCR[7:0]: Six equations required to find hex value
  - SCINCR_OFF = int(8192 * 4.286 * 1728 / (27 * H_CLKO[11:0]) + 0.5)
  - SCINCR_OFFh = dec2hex(SCINCR_OFF)
  - SCINCR_OFFb = hex2bin(SCINCR_OFFh)
  - SCINCR_INTb = SCINCR_OFFb and (bitwise AND operator) with 111111111(binary)
  - SCINCR_INTnot = NOT[SCINCR_INTb]
  - FIL4286INCR[7:0] = [BIN2DEC{SCINCR_INTnot}]/2
- FILFSCONV[5:0] = int((27 * H_CLKO[11:0] * 1.087) / 1728 + 0.5)

For RGB input only:

- MCR[7:0] = int ((920.26) / (288036.0 * H_CLKO[11:0] * SINX) * 2^{26} + 0.5)

where SINX = [sin (2π * Fsc / CLKI)] / (2π * Fsc / CLKI)

- MCB[7:0] = int ((598.15) / (288036.0 * H_CLKO[11:0] * SINX) * 2^{26} + 0.5)

where SINX = [sin (2π * Fsc / CLKI)] / (2π * Fsc / CLKI)

- MSC[31:0] = int ((282 / H_CLKO[11:0]) * 2^{32} + 0.5)
- MY = same as PAL, no change required for SECAM

For YCrCb input only:

- MCR[7:0] = int (1.902/(224*0.713)*(0.28/F_{CLK})/(84*SINX)*2^{27}+0.5)
- MCB[7:0] = int (1.505/(224*0.564)*(0.28/F_{CLK})/(84*SINX)*2^{27}+0.5)
- MY = same as PAL, no change required for SECAM

Table 1-28. SECAM Specific Registers within the Conexant VGA Encoder

Register Address	Description	Value for PAL-BDGHI	Value for SECAM
0x42	MSC_DB[7:0]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x44	MSC_DB[15:8]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x46	MSC_DB[23:16]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x48	MSC_DB[31:24]	Not Used for PAL-BDGHI	Use MSC_DB[31:0] equation
0x4A	DR_LIMITP[7:0]	Not Used for PAL-BDGHI	Use DR_LIMITP[10:0] equation
0x4C	DR_LIMITN[7:0]	Not Used for PAL-BDGHI	Use DR_LIMITN[10:0] equation
0x4E	DR_LIMITN[10:8] and DR_LIMITP[10:8]	Not Used for PAL-BDGHI	Use DR_LIMITN[10:0] equation Use DR_LIMITP[10:0] equation
0x50	DB_LIMITP[7:0]	Not Used for PAL-BDGHI	Use DB_LIMITP[10:0] equation
0x52	DB_LIMITN[7:0]	Not Used for PAL-BDGHI	Use DB_LIMITN[10:0] equation
0x54	DB_LIMITN[10:8] and DB_LIMITP[10:8]	Not Used for PAL-BDGHI	Use DB_LIMITN[10:0] equation Use DB_LIMITP[10:0] equation
0x56	FIL4286INCR[7:0]	Not Used for PAL-BDGHI	Use FIL4286INCR[7:0] equation
0x58	Bits 5–0 are FILFSCONV[5:0]	Not Used for PAL-BDGHI	Use FILFSCONV[5:0] equation
0xA8	MCR[7:0]	Overscan Ratio Dependent	Use MCR[7:0] equation
0xAA	MCB[7:0]	Overscan Ratio Dependent	Use MCB[7:0] equation
0xAE	MSC[7:0]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB0	MSC[15:8]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB2	MSC[23:16]	Overscan Ratio Dependent	Use MSC[31:0] equation
0xB4	MSC[31:24]	Overscan Ratio Dependent	Use MSC[31:0] equation

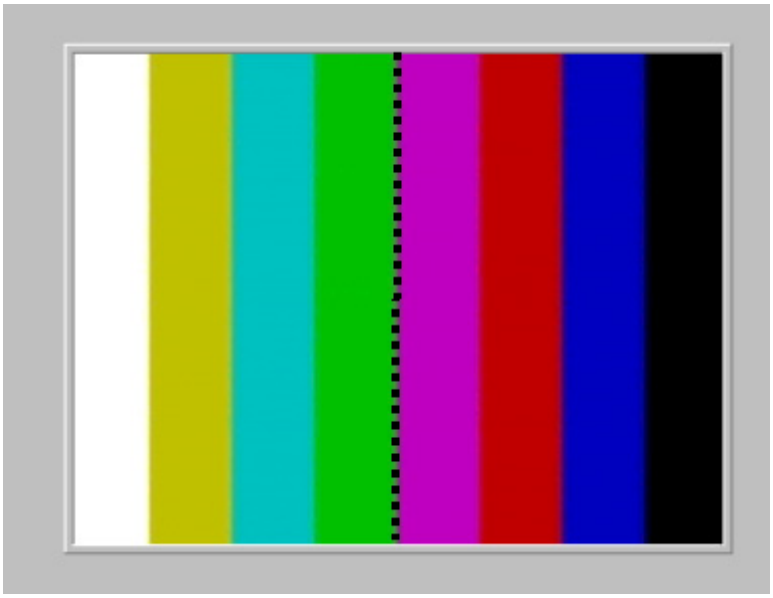
1.3.44 Elimination of Dot Crawl in Composite NTSC Output

One of the possible types of analog video outputs the CX25890/1/2 can generate is composite (abbreviated CVBS) video. With this sort of output, all video data is carried in a single signal that combines chrominance (hue and saturation) and luminance (brightness) information. Generally, this signal is transferred between video devices using a single interconnect cable with an RCA connector on both ends.

Composite video differs versus S-Video, which separates the color and brightness information into two separate signals. S-Video (also known as Y/C-Video) transfers chrominance (color portion of video signal denoted C) and luminance (brightness portion of the video signal denoted Y) information separately resulting in a higher picture quality than Composite video. Since Composite video joins the chrominance and luminance signals together into one unified signal, the two components must be divided out from each other at the television by a comb filter or other method. This process naturally results in some distortion and picture degradation and exhibits the worst image quality as compared to other forms of video connection.

One of the most common distortion artifacts seen with Composite video is an annoyance called dot crawl. Another name for this is vertical zipper. Due to the nature of the color subcarrier-switching pattern found in NTSC, dot crawl only occurs when the CX25874/5 is generating NTSC-M or NTSC-J Composite and not PAL, SECAM, or any other analog interlaced video standard. Because it is somewhat content dependent, dot crawl is sometimes difficult to see. This artifact is most noticeable when the video image contains a sharp color separation in adjacent vertical lines or pixels. For instance, in standard 75-percent or 100-percent color bars, there is a region of that test image from left to the right where the green bar ends and the magenta bar begins. This is shown in Figure 1-47 along with an example of the dot crawl artifact.

Figure 1-47. NTSC Composite Output: Standard 75 Percent Color Bars With Dot Crawl Artifact

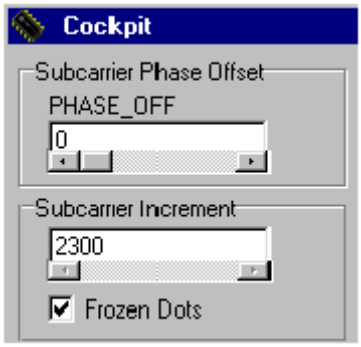


Green-to-magenta is a difficult region to encode because these colors have almost completely opposite hues (green's chrominance phase is 240°, whereas magenta's is 61°). Hence, when the drastic phase shift transition occurs, a line of continuously moving dots rolling vertically through the transition region can be seen. There are a

number of circuit-based fixes that can be implemented to marginally improve this artifact, such as improving the chrominance/luminance filtering in the TV and refining the low-pass filters used for each of the CX25874/5's analog signal output lines.

Ultimately though, the best solution for minimizing dot crawl is to create a checkbox on the TV out page, as shown in Figure 1-48, and embed the source code for the Frozen Dots' algorithm behind it that allows the end-user the ability to turn NTSC Composite dot crawl on or off. Sample source code for freezing and eliminating the dot crawl is listed in Table 1-29.

Figure 1-48. Frozen Dot Checkbox from Conexant's Cockpit Application



This source code will execute the algorithm that lessens the zipper effect and appear to freeze the dots comprising the zipper in NTSC Composite video. The algorithm and corresponding source code have already been embedded in various internal programming tools (Cockpit) and thus, are proven solutions. The algorithm basically deceives the television by altering the NTSC color subcarrier offset amount generated by the CX25890/1/2 device's Composite output.

Table 1-29. Source Code for Elimination of Dot Crawl in NTSC Composite Video *(1 of 2)*

```
//  Assumptions:
//
//      - We only freeze dots when using NTSC CVBS out
//      - TTO and ATO are same for 525-line and 625-line modes
//      - NTSC is always 525-line
//      - 2^32 == 0x100000000 hex
//      - 2^31 ==  0x80000000 hex
//      - TTO - 'Total Time per Output Line' = 63.55556E-6 (.00006355556 sec.) for NTSC
//      - ATO - 'Active Time per Output Line' = 52.65556E-6 (.00005265556 sec.) for NTSC
//      - HOC = Horiz. Overscan Compensation = 13.79 / 100 (.1378530858) (or some other input)
//                2^32 x (1 - HOC) x ATO x (455 + 1/525)
//           MSC = ----- + .5
//                        (4 x H_ACTIVE x TTO)

//  Determining the MSC expression:
//
// DWORD  dwMSC = (348948560744.3 / H_ACTIVE) + .5;
//           = ( ( pow(2,32) * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 4 * H_ACTIVE * TTO ) ) + 0.5;
//             reduce
//           = ( ( pow(2,31) * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 2 * H_ACTIVE * TTO ) ) + 0.5;
//             re-express equation
//           = ( ( 0x80000000 * ( 1 - HOC ) * ATO * ( 455 + 1/525 ) ) / ( 2 * H_ACTIVE * TTO ) ) + 0.5;
//             substitute
//           = ( ( 0x80000000 * ( 1 - HOC ) * .00005265556 * ( 455.0 + 1/525 ) ) / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//             reduce
//           = ( ( 0x80000000 * ( 1 - HOC ) * .00005265556 * 455.001919 ) / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//             substitute
//           = ( ( 0x80000000 * ( 1 - .1378530858 ) * .00005265556 * 455.001919 ) / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//             reduce
//           = ( ( 2147483648 * .8621469142 * .00005265556 * 455.001919 ) / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//             reduce
//           = ( 44357657.97721 / ( H_ACTIVE * .00012711112 ) ) + 0.5;
//             lose the rounding-up
//           = 44357657.97721 / ( H_ACTIVE * .00012711112 );
//             reduce
//           = 348967564578.2 / H_ACTIVE;
```

Table 1-29. Source Code for Elimination of Dot Crawl in NTSC Composite Video *(2 of 2)*

```
// Assumptions:
//          lose the insignificant decimal point.
//          the only problem is that the number on top is greater than 32 bits.
//          so, we either have to use large integers, floats, or expand/simplify
//          the expression.
//        = 348967564578 / H_ACTIVE;
//          expand
//        = ( 348967564578 / 128 ) / ( H_ACTIVE / 128 );
//          reduce and re-express.  we're done.
//        = 0xA2802CEA / ( H_ACTIVE / 128 );
//          or, reduce and re-express with a GCD of 640 and 800.
//          expand
//        = ( 348967564578 / 160 ) / ( H_ACTIVE / 160 );
//          reduce and re-express.  we're done.
//        = 0x820023EE / ( H_ACTIVE / 160 );

// Frozen dots only works with NTSC Composite
if( bNTSC )
{
   // To get frozen dots, calculate MSC with increment.
DWORD      dwMSC = 0x820023EE / ( H_ACTIVE / 160 );
regAE.ucMSC = dwMSC & 0x000000FF;
regB0.ucMSC = ( dwMSC & 0x0000FF00 ) >> 8;
regB2.ucMSC = ( dwMSC & 0x00FF0000 ) >> 16;
regB4.ucMSC = ( dwMSC & 0xFF000000 ) >> 24;
}
```

GENERAL NOTES:

1. Frozen Dots only functions with an NTSC Composite video output and either a 640X480 or 800X600 digital input coming from the graphics controller. Modifications required to above source code to enable frozen dots with a 1024x768 active digital input coming from the graphics controller.
2. For optimal visual quality of the NTSC CVBS image, Frozen Dots should be disabled during multimedia applications such as playing a game or watching a DVD Movie. Frozen Dots should be enabled during nonmultimedia applications such as e-mailing, word processing, presentations, and other scenarios where menus and small graphics will be frequently displayed.
3. H_ACTIVE is the number of digital pixels per horizontal input line. Make sure a case statement or some other line of code is included for turning on this feature when the user's desired video output is NTSC (NTSC-M video standard is used in USA, NTSC-J in Japan, most of Southeast Asia, etc.) and turning the feature off when the user's desired video output is PAL (different variations used in Western and Central Europe, South America, etc.).
4. The only marked improvement between this set of equations and the set that was embedded in older versions of Cockpit is that Conexant was able to further solve for the MSC[31:0] value, successfully deriving an equation which will stay within 32 bits. It works fine for 640x480, and 800x600 because 160 divides both 640 and 800 evenly.

Manual adjustment of register 0xB6 = PHASE_OFF in the CX25874/5 and/or manual adjustment of register 0xAE = MSC[7:0] can also have the same type of special effects as the algorithm in Table 1-29. By increasing or decreasing these values slowly, the subcarrier phase and subcarrier increment will change, and with certain register combinations, the crawling dots will appear at certain points to stand still.

1.3.45 Macrovision Copy Protection

The CX25875 device supports Version 7.1.L1 of the Macrovision specification for copy protection for all NTSC, PAL, and SECAM video outputs. The CX25874 does not support the Macrovision feature whatsoever.

NOTE: The CX25875 will power-up with Macrovision copy protection enabled as required by Macrovision Version 7.1.L1.

The CX25875 device also provides Macrovision 525p (480p) copy protection for progressive scan outputs. Another term for this technology is the DVD 1.03 Macrovision copy protection scheme. This type of HDTV copy protection turns on automatically after a power on reset and after the CX25875 begins transmitting 480p YP_RP_B. The designer only needs to program HDTV copy protection specific registers if Macrovision was off previously.

For detailed instructions and lists of default register values for the CX25875 obtain a Macrovision license and then ask for the *Macrovision Process Supplement Application Note* from your local Conexant salesperson or field application engineer.

1.3.46 HDTV Output Mode

The CX25874/875 includes an HDTV Output Mode that generates the analog RGB or analog YP_BP_R component video outputs necessary for driving a Japan D-type or generic HD input port. To drive the Japan D connector with required 0 V, 2.2 V, and 5 V signal lines to express the type of format and whether the timing is progressive or interlaced requires the integration of an external device such as a PLD.

While generating HDTV outputs, the device accepts RGB, YCrCb, or YPrPb digital data in a 480p, 720p, or 1080i ATSC resolution.

In addition, the 576p (625p) resolution defined in the ITU-R BT.1358 standard and the 1035i resolution defined in the ITU-R BT.709-4 standard are supported. Finally, many custom HD resolutions such as 540p, used by RCA set-top boxes, are acceptable as well.

After a pipeline delay, it outputs either analog RGB or analog YP_BP_R signals and automatically inserts trilevel synchronization pulses (when necessary) and vertical synchronizing broad pulses. The output waveforms, input data requirements, register values, and configuration details are explained in Appendix E. The device complies with most major SMPTE, EIA, and ITU standards governing HDTV resolutions, as explained in Appendix E.

1.3.47 SCART Output

In this mode of operation, the CX25874/875 can be used successfully to provide one full Red/Green/Blue/CSYNC (or optionally, a 2-signal Luminance and Chrominance) SCART/Peritel output to drive SCART-compatible televisions or VCRs. Many PAL/European TVs being manufactured now have SCART compatible sockets, that allows the television and the set top box, graphics card, or game console driving it to work in RGB color instead of the standard composite. The picture quality for full SCART is significantly better due to the individual RGB Composite signals being sent directly to the TV color guns. This is opposed to the TV having to modulate and decode the RGB signals from another color format. This ultimately yields a crisper picture.

On power-up, the CX25874/875 will output NTSC standard-definition television outputs. To switch the device into SCART Output Mode with three sync-less Red/Green/Blue (RGB) analog outputs and a single Composite Video output from pin #59, program the encoder into a satisfactory PAL output mode and then perform the serial writes listed in Table 1-30.

Table 1-30. Serial Writes Required to Switch CX25874/875 into SCART Output Operation

Bit Name	Location	Value	Comment
EN_SCART	Bit 3—Register 0x6C	1	Enables SCART Output mode. DACs will transmit Video[0-3] as SCART compatible RGB/CVBS outputs. By default, in SCART Output mode, the encoder will transmit: DACA = Video[0] = Red DACB = Video[1] = Green DACC = Video[2] = Blue DACD = Video[3] = Composite Video signal
OUT_MUXD[1:0] OUT_MUXC[1:0] OUT_MUXB[1:0] OUT_MUXA[1:0]	Bits 7:0—Register CE	E4	By configuring the DAC routing register, the encoder will now transmit: DACA = Video[0] = 00 = Red DACB = Video[1] = 01 = Green DACC = Video[2] = 10 = Blue DACD = Video[3] = 11 = Composite Video signal
OUT_MODE[1:0]	Bits 3:2—Register D6	11	Forces encoder to generate SCART (R/G/B/CVBS) output mode.

NOTE: No change to the incoming or outgoing HSYNC* and VSYNC* signal frequencies are necessary for SCART generation. The sync rates should continue to match those found with PAL-BDGHI transmission.

While the CX25874/875 is in SCART output mode, the composite sync output (Video[3]) contains a standard bilevel analog sync along with all other components that comprise a standard PAL-BDGHI video signal. The sync pulse has an amplitude of 0 mV to 300 mV peak-to-peak and a duration of 4.70 µs by default. The amplitude can only be adjusted through the use of external passives, but its width can be adjusted through serial writing of the CX25874/875 HSYNC_WIDTH register.

The CX25874/875's PAL Composite Signal should be used by the subsystem to provide the positive-going Video output/sync output expected by SCART-compliant display devices. In other words, the Composite Sync output should be fed into the Video Input (Contact #20-CEI IEC 933-1) on the SCART connector.

SCART_CSYNC will possess the same bandwidth and time delays as the CX25874/875 RGB primary color signals.

The RGB primary color signals generated in SCART mode will not contain any embedded syncs. For each output, the difference between the peak value (pure white) and blanking level is 0.7 V (± 3 dB). Therefore, the blanking level will reside at GND (0 mV) and the maximum level is 700 mV for RGB. The HSYNC* and VSYNC* digital inputs received by the CX25874/875 continue to act as a trigger to start a new line and new frame respectively as is the case with Composite and SVHS outputs. The RGB signals are blanked in accordance with the values contained in the H_BLANKO and V_BLANKO registers, with H_CLKO and H_ACTIVE playing a lesser role.

The primary color signals expect a 75 Ω load from the display device. Correct RGB amplitudes are generated when the CX25874/875's SCART outputs each see an equivalent impedance of 37.5 Ω between the source and destination.

By default, the RGB positive-going signals are transmitted from the CX25874/875 in the manner shown in Table 1-31.

Table 1-31. Default SCART Outgoing Signal Assignments

Pin # on CX25874/875	SCART Output
60 = DACA	Video[0] = Red Primary Color
61 = DACB	Video[1] = Green Primary Color
62 = DACC	Video[2] = Blue Primary Color
59 = DACD	Video[3] = Composite Video Signal
GENERAL NOTE: Video[0-3] can be routed out of any of the 4 on-chip DACs by adjusting the appropriate OUT_MUXA/B/C/D[1:0] bits.	

Other major characteristics of the CX25874/875 SCART Output Mode are:

- DAC detection possible in this mode for R, G, and B outputs.
- Acceptable digital RGB inputs include 24/16/or 15 bits per pixel multiplexed, noninterlaced RGB.
- Acceptable digital YCrCb inputs include 24/16 bits per pixel multiplexed, noninterlaced YCrCb.
- CX25874/875 can operate in master, pseudo-master, or slave interface.
- Pixel sampling rate in this mode is determined based on the incoming and outgoing clock frequencies (CLKI and CLKO).
- DAC resolution for all DACs = 10-bits.
- Compliance with the European EN50-049 SCART connector standard. Blue should be received as Pin #7, Green as Pin #11, Red as Pin #15, and CVBS Out from the CX25874/875 as Composite Out at Pin #19 (Display Side of Connector).
- Compliance with the CEI IEC Publication 933-1 standard. Blue should be received as Pin #7, Green as Pin #11, Red as Pin #15, and CVBS Out from the CX25874/875 as Composite Out at Pin #19 (Display Side of Connector).

The CX25874/875 is compliant with the major standards and technical reports governing the SCART interface. Table 1-32 summarizes the pins to be used for transmission of SCART RGB/CVBS video with this Conexant device.

Table 1-32. CX25874/875 SCART Outputs for Different SCART Standards

RGB Standard	Red	Green	Blue	Composite/Blanking
European EN50-049 SCART(1) connector	Pin 15	Pin 11	Pin 7	Pin 19 -Composite Sync Out (To Display)
CEI IEC 933-1: (1) BBC SCART Arrangement #1	Pin 15	Pin 11	Pin 7	Pin 19 - Composite Sync Out (To Display)
Y- C Standard	**Chroma**	**x**	**Luma**	**x**
Luminance - Chrominance(2) SCART: BBC SCART Arrangement #2	Pin 15	—	Pin 20	—

FOOTNOTE:
(1) Red/Green/Blue signals levels are from 0 V + 0.7 V peak-to-peak with 75 Ω load impedance.
(2) The Luminance – Chrominance Outputs for SCART are equivalent to PAL-BDGHI S-Video. Therefore, OUTMODE[1:0] should be programmed to 00, the EN_SCART bit should be reset to 0, and the OUTMUXA/B/C[1:0] bits adjusted according to which DACs must transmit Luminance(Video[1]) and Chrominance(Video[2]).

A specialized cable and connector are required to connect the CX25874/875's RGB/CSYNC or Y/C outputs to the TV's SCART input. This cable can be procured from various European electronic stores and comes in at least two different arrangements. Consult the CEI IEC 933-1 specification (*Audio, Video, and Audiovisual systems-Interconnections and Matching Values*) for a precise illustration of their 21-contact SCART connector, video signal peak-peak values, and cordset types.

The most common types of SCART connectors are the so-called Type I and Type II variety. Figures 1-49 and 1-50 illustrate the recommended Type I and Type II SCART connector pinout arrangements.

Figure 1-49. CX25874/5 Driving a Type I SCART Connector (EN 50-049 and IEC 933-1 Compliant)

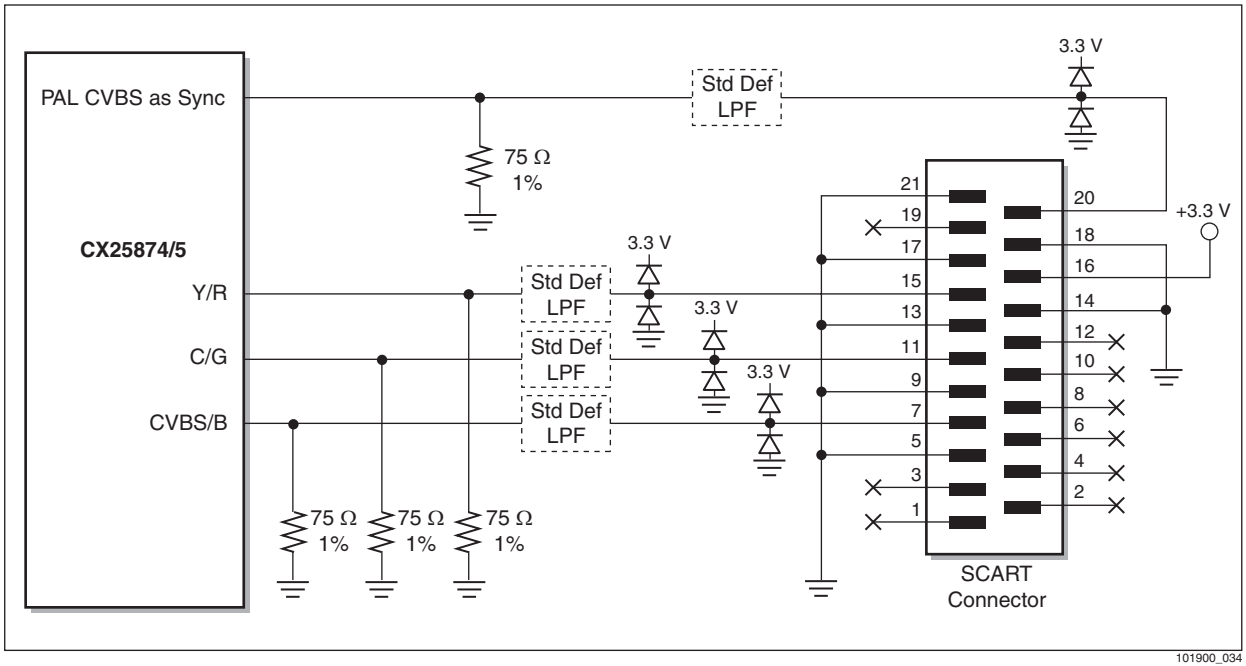
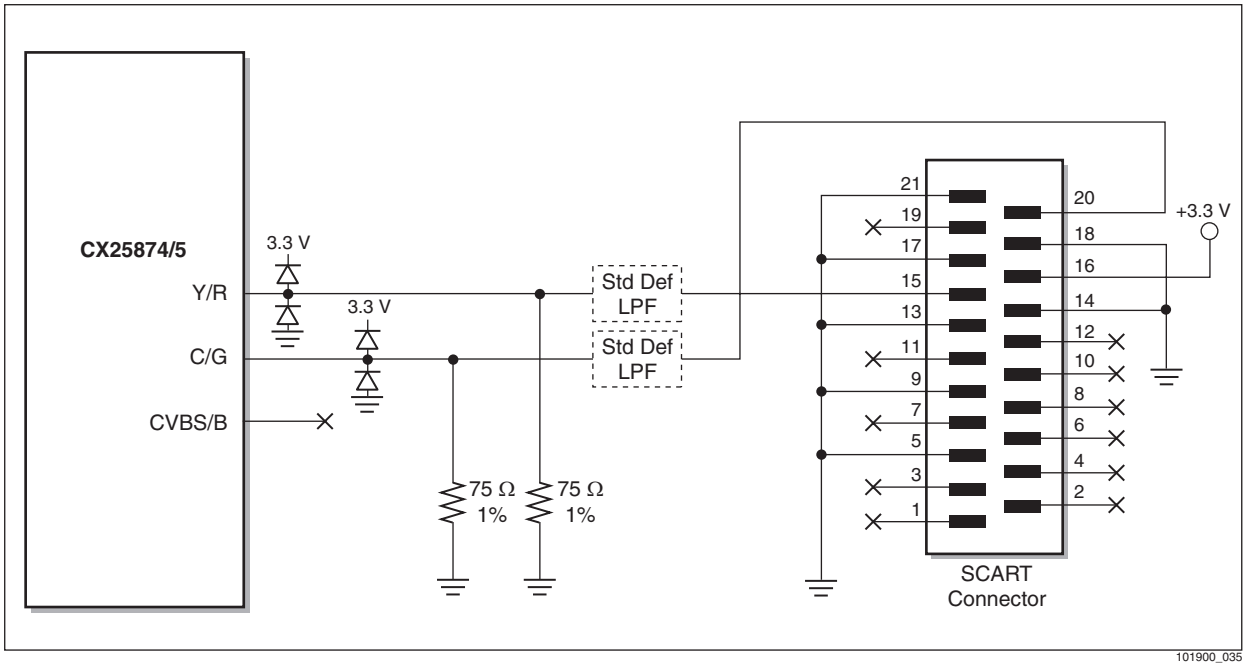


Figure 1-50. CX25874/5 Driving a Type II SCART Connector (Y/C and BBC SCART Compliant)



Conexant recommends that any designer utilizing the CX25874/875 with either type of SCART output utilize the same DAC low-pass filters used for standard-definition TV outputs listed in Section 3.3.

1.3.48 Y CR CB 480i (YUV) Standard-Definition Component Video Outputs

In this mode of operation, the CX25874/25875 provides a set of Component Video Y, CB (B–Y), CR (R–Y) outputs based on a 480 line interlaced RGB or YCrCb digital input format. Some DVD players, such as those made by Toshiba and Panasonic, call the Component Video Output format by their branded name, ColorStream. Others refer to the two EIA standards governing this video format–EIA-770.1 and EIA-770.2-A, and state this video type as Interlaced Component Video, 480i Component Video, or Component YUV. Regardless of the different names, the video format remains the same. For instructions on how to configure the CX25874/5, to generate progressive 480p Component Video (or Color Stream Pro), refer to the HDTV sections. The CX25874/5 and CX25870/871 are the only encoders that can supply HDTV outputs.

The designer can enable ColorStream by using three of the CX25874/5's DACs to generate two color difference signals (P_R and P_B sometimes referred to as C_R and C_B) and a single luminance signal (Y). These three channels allow the video generating device to bypass the TV's internal Y/C separator and color decoder circuits. The analog information therefore gets routed directly into the TV's matrix decoder. By sending the pure component video signal directly to a Component Video or ColorStream input-equipped television or video projector, the input signal forgoes the extra processing that normally would degrade the analog image.

The advantage of this type of video is increased image quality combined with more lifelike colors and crisper detail. Because the video information is transferred over three separate connecting cables instead of two (for S-Video) or one (for Coaxial or RCA/Composite), 480i Component Video yields the best standard-definition TV quality available. However, because we are still dealing with standard 480 line interlaced resolutions, this format remains inferior to High-Definition TV.

Output devices that require generation of this format include, but are not limited to, Digital TV set top boxes, Satellite DBS Receiver Decoders, and DVD players. Input media capable of decoding ColorStream include television receivers and/or professional monitors.

While in the Component Video mode, all 10 bits of the CX25874/5's D/A converters are available for encoding. This results in a D/A conversion more accurate than conventional 8-or 9-bit based MHz systems. The end result is a more artifact-free and clear image.

Some major characteristics governing the interlaced standard-definition television analog component video interface are as follows:

Pixels per Active Line	Active Lines per Frame	Frame Rate (Hz)	Output Scanning Format	Total Samples per Line	Total Lines per Frame
720	480	30 / 1.001	Interlaced	858	525

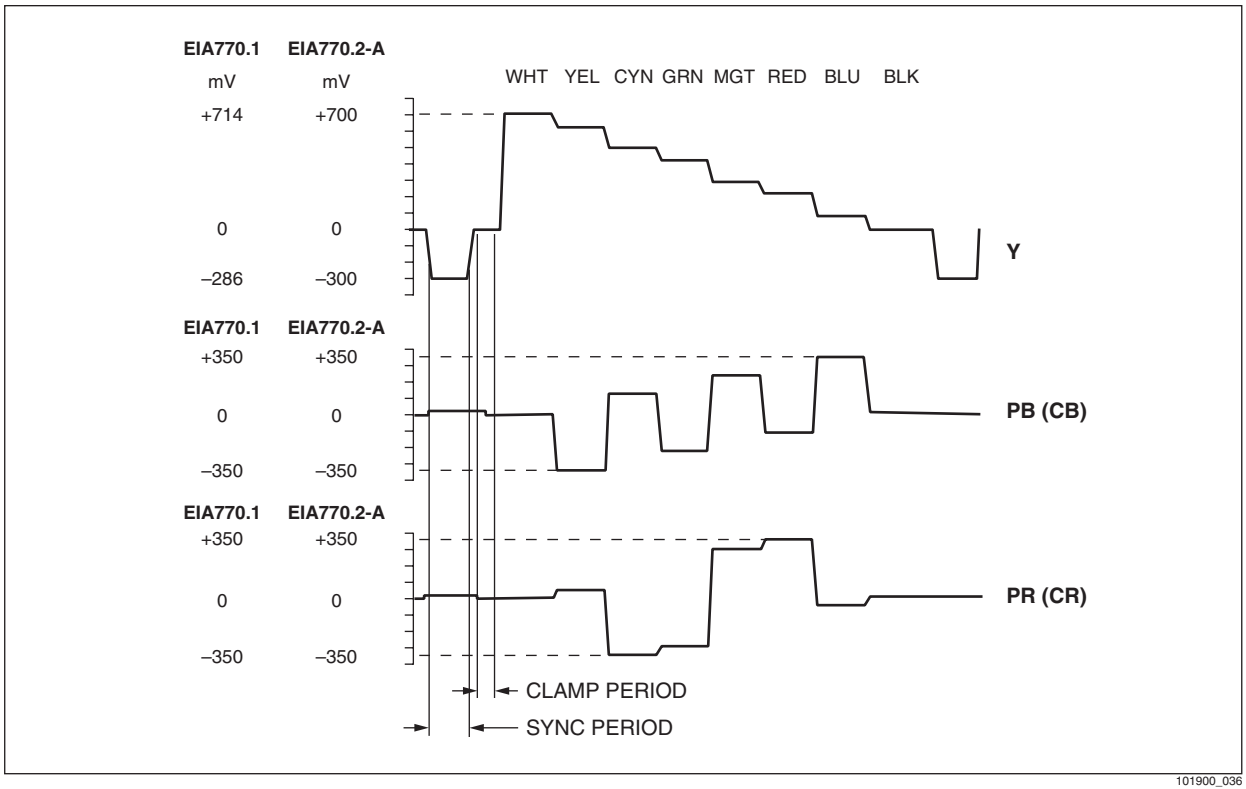
- The digital input stream can be received in a progressive (i.e., noninterlaced) format or interlaced format. Interlaced data must be transmitted as ODD–EVEN–ODD … fields. The fields carry every other scan line in succession with succeeding fields carrying the lines not scanned by the previous field.
- Each field will be divided into an active picture area and a VBI. Similarly, each line will be divided into an active pixel area and a horizontal blanking interval.
- The 480i video output will be capable of either a 4:3 or 16:9 aspect ratio through embedding of Wide Screen Signaling (WSS) bits into the appropriate lines in the VBI. Review the WSS and CGMS sections for more details.

If configured properly, the CX25874/5's EIA 770.2-A compliant Component Video luminance signal has a peak amplitude of 700 mV from the blanking level, with zero setup. A negative-going bilevel sync pulse of 300 mV, conforming to the timing requirements in Figure 1-51, is added to the Luma signal as the only timing reference for the complete Y P_R P_B (YC_RC_B) set of signals.

Neither P_R (C_R) nor P_B (C_B) will contain an embedded sync pulse. Both will have a maximum peak amplitude of ±350 mV. The DC level of P_R and P_B during the horizontal line shown in Figure 1-51 will be at reference black with a voltage of 0 V. It will be generated in conformance with the EIA 770.2-A and EIA770.1 standards. The only differences between these standards are the presence of the 7.5 IRE setup pedestal and slightly different luminance levels. Check Tables 1-33 and 1-34 for complete programming instructions for either standard.

The three component video signals Y, P_B (C_B), and P_R (C_R)will be coincident with respect to each other within ± 5.0 ns. Any filtering that introduces group delay exceeding 5.0 ns should be discarded and redesigned.

Figure 1-51. Y P_R P_B Component Video Signals using 100/0/100/0 Color Bars as the Digital Input Signal (Courtesy– EIA-770.2-A standard, page 8 and EIA-770.1 standard)



To switch the device into 480i Component Video Output Mode with bilevel syncs embedded into each of the three Y P_R P_B analog outputs, first, program up the CX25874/5 into a fully functional NTSC over-scan solution where Composite and/or S-Video is being generated out of at least three of the encoder's outputs. Next, change the registers listed in Table 1-33 to the indicated values.

Table 1-33. Common Registers Required to Switch CX25874/25875 into EIA-770.2-A- or EIA-770.1-Compliant Component Video Outputs

Register/Bit Name	Location	Value	Comment
MCOMPY[7:0]	Bits 7:0—Register 3C	80 (hex)	Gain multiplication factor for Y analog output.
MCOMPU[7:0]	Bits 7:0—Register 3E	90 (hex)	Gain multiplication factor for P_B (C_B) analog output.
MCOMPV[7:0]	Bits 7:0—Register 40	66 (hex)	Gain multiplication factor for P_R (C_R) analog output.
SETUP	Bit 1—Register A2	1 (binary)	Required for EIA770.1 compliance. Enables 7.5 IRE pedestal normally present within NTSC-M active video lines.
OUT_MODE[1:0]	Bits 3:2—Register D6	10 (binary)	Enables Component Video output mode. CX25874/5 DACs will transmit Video[0-3] as EIA-770.2-A or 770.1 compliant Y PR (C_R), PB (C_B), and Y_DELAY outputs
OUT_MUXA[1:0] OUT_MUXB[1:0] OUT_MUXC[1:0] OUT_MUXD[1:0]	Bits 1:0—Register CE Bits 3:2—Register CE Bits 5:4—Register CE Bits 7:6—Register CE	00 (binary) 01 (binary) 10 (binary) 11 (binary)	By default, in Component Video output mode, the CX25874/5 will transmit: DACA = Video[0] = PR (C_R) = V DACB = Video[1] = Y DACC = Video[2] = PB (C_B)= U DACD = Video[3] = Y_DELAY (not used with this type of output)

For EIA-770.1 compliant Component Video out, no other programming steps are required for the CX25874/5 beyond Table 1-33.

For the more common EIA-770.2-A compliant Component Video out, a few additional programming steps are required. These are listed in Table 1-34.

Table 1-34. Unique Registers Required to Switch CX25874/25875 into EIA-770.2-A- Compliant Component Video Outputs

Register/Bit Name	Location	Value	Comment
SETUP	Bit 1—Register A2	0 (binary)	Required for EIA770.2-A compliance. Removes 7.5 IRE pedestal normally present within NTSC-M active video lines.
SYNC_AMP[7:0]	Bits 7:0—Register A4	F0 (hex)	Multiplication factor for adjusting the analog sync amplitude tip to –300 mV for EIA-770.2-A.
MY[7:0]	Bits 7:0—Register AC	85 (hex)	Additional gain multiplication factor for Y EIA-770.2-A analog output. This register needs to be increased by 6 percent of its nominal value. For a NTSC output based on a RGB digital input, this register would be increased 6 percent to 8C (hex) from a nominal value of 85 (hex).

The analog Y, PB (C_B), and PR (C_R)- Video[0-3] outputs can be routed out of any of the four on-chip DACs by adjusting the appropriate OUT_MUXA/B/C/D[1:0] bits. All of the OUT_MUX bits are contained in register 0xCE.

Because the CX25874/5 device has four DACs and only three are needed for Component Video, the designer can choose to use the fourth output, usually from DACD, for any purpose deemed necessary. This output can be configured to either the Y P_R (C_R), P_B (C_B), or Y_DELAY output via OUT_MUXD. If the output is not going to be used whatsoever, Conexant recommends DAC_D be disabled by setting DACDISD (bit 3, Register BA). This saves on power dissipation.

The Component Video output signals expect a 75 Ω load to ground from the display medium. Correct Y, P_R, P_B amplitudes will be generated only when each CX25874/5 output sees an equivalent impedance of 37.5 Ω between the source and destination.

The CX25874/5 is compliant with the major standards and technical reports governing the Standard-Definition TV Analog Component Video interface. The name of these standards are as follows:

- EIA 770.2-A–Standard-Definition TV Analog Component Video Interface
- EIA 770.1–Standard-Definition TV Analog Component Video Interface
- ANSI/SMPTE Standard 170M (1994) (M/NTSC) for Television–Composite Analog Video Signal–NTSC for Studio Applications

To obtain any of these specifications, visit Global Engineering Documents at:

http://global.ihs.com/

Conexant recommends that any designer utilizing the CX25874/5 with a Component Video output utilize the same DAC low-pass filters used for standard-definition TV outputs shown in Figure 3-2.

1.3.49 VGA(RGB)—DAC Output Operation

In this mode of operation, the CX25874/875 acts as a general-purpose triple high-speed D/A converter used to drive video receivers, such as PC monitors. The encoder accomplishes this by bypassing most of the encoder blocks utilized for television outputs, such as the Flicker Filter and FIFO and instead routing the RGB or YCrCb digital data straight through to the on-chip 10-bit DACs. Once the data arrives at the DACs, it is quickly converted to a set of 700 mV peak-to-peak analog outputs, streamed through the respective DAC_X output pins, and routed within the rest of the graphics system according to the PCB layout.

Optimal performance is achieved when the CX25874/875's current controlled DACs are terminated into appropriate resistive loads to produce voltage outputs. The chip's DAC outputs are specifically designed to produce video output levels with a total peak-peak active-region amplitude of 700 mV when directly connected to a single-ended, doubly terminated (Req = 37.5 Ω) load. With the recommended loading of two 75 Ω ± 1 percent resistors (one each for the transmitting and receiving side), the full-scale video amplitude is from 286 mV (blanking) to 986 mV (maximum luminance) and synchronization pulses from 0 mV (negative sync tip) to 286 mV (blanking) respectively. The analog synchronization pulse is generated by the CX25874/875 every time it receives a falling edge on either the HSYNC* or the VSYNC* input by default. These sync pulses can be disabled for the RGB outputs by performing the serial writes listed in Table 1-35.

On power-up, the CX25874/875 will output NTSC standard-definition television outputs. To switch the device into VGA-DAC Output Mode with bilevel syncs embedded on every Red/Green/Blue (RGB) analog output, perform the serial writes listed in Table 1-36 only.

Table 1-35. Serial Writes Required to Remove Bilevel Syncs from all VGA/DAC Outputs

Bit Name	Location	Value	Comment
RGB2PRPB	Bit 6—Register 0x28	0	Default state. No need to reprogram.
BPB_SYNC_DIS	Bit 3—Register 0x28	1	Disables sync on Blue output
GY_SYNC_DIS	Bit 4—Register 0x28	1	Disables sync on Green output
RPR_SYNC_DIS	Bit 5—Register 0x28	1	Disables sync on Red output
GENERAL NOTE: When all bits in Tables 1-35 and 1-41 are programmed correctly, the active video level range will be from +286 mV to +986 mV.			

Table 1-36. Serial Writes Required to Switch CX25874/875 into VGA/DAC Output Operation

Bit Name	Location	Value	Comment
SLAVE	Bit 5—Register 0xBA	1	Ensures CX25874/5 in slave or pseudo-master interface
EN_XCLK	Bit 7—Register 0xA0	1	CLKI used as pixel clock source.
SETUP	Bit 1—Register 0xA2	0	Setup off. The +56 mV pedestal setup is disabled for active video lines.
OUT_MODE[1:0]	Bits 3:2—Register D6	11	Video[0-3] = 11 = VGA Output Mode: DAC_A = Video[0] = Red DAC_B = Video[1] = Green DAC_C = Video[2] = Blue
DAC_DISD	Bit 3—Register 0xBA	1	Disables DACD output. Current is set to 0 mA. Output voltage goes to 0 V.

Of course, the master device's timing signals (HSYNC*, VSYNC*, CLKI) and the digital data sent to the CX25874/875 must also be adjusted to ensure the proper operation of this mode.

Some applications, such as VESA compliant PC Monitors, dictate that the embedded bilevel syncs be completely absent from the RGB analog outputs. Fortunately, the CX25874/875 can provide VESA's syncless outputs as long as the additional set of bits found in Table 1-35 are programmed as shown in this table. Complete all serial writes listed in Tables 1-35 and 1-36.

The outputs generated from the serial writes listed in Table 1-35 and Table 1-36 will not contain any embedded syncs, nor will they contain the positive DC offset voltage present with the CX25874/5 in VGA out mode. Therefore, the blanking level will reside at 0 mV, and the maximum luminance level is 700 mV for the three different outputs. The HSYNC* and VSYNC* digital inputs received by the CX25874/875 will continue to cause blanking, but this is irrelevant since the data itself is blanked at these times.

The VESA Video Signal Standard specification requires that the DAC analog output stay between 0.0 Vdc and 0.700 Vdc +.07 V (or -.03 V) with no excursions at all times. Clearly, the blank and maximum luminance levels for the CX25874/875 are in compliance with this specification.

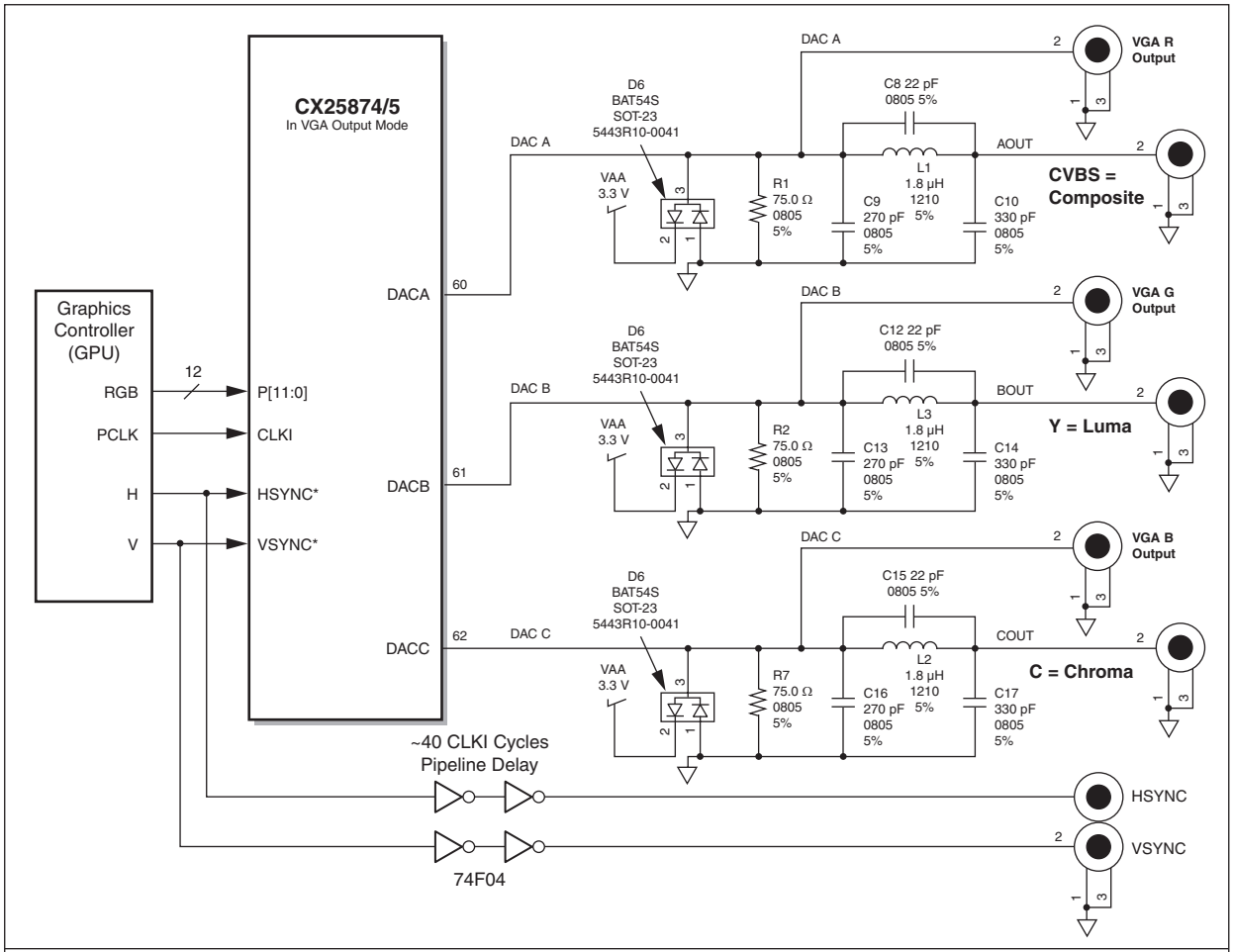
Other major characteristics of the CX25874/875 VGA—DAC Output Mode are:

- Maximum active input resolution = 1024 x 768 or any other active resolution that ensures less than an 80 MHz pixel clock rate
- Acceptable digital RGB inputs include 24/16/ or 15 bits per pixel multiplexed RGB
- Acceptable digital YCrCb inputs include 24/16 bits per pixel multiplexed YCrCb
- CX25874/875 can only be a slave to the data master in this type of operation
- Sampling rate in this mode is determined based on the incoming clock frequency (CLKI)
- DAC resolution for all DACs = 10-bits

Conexant recommends that any designer utilizing the CX25874/875 in this mode circumvent the three capacitors and one inductor found in the DAC low-pass filters used for standard-definition TV outputs. Figure 1-52 illustrates one method of bypassing the capacitors and inductor. Note that an additional RCA (or other type) of connector is recommended in this case for the Red. Green, and Blue VGA Outputs.

Finally, since the encoder cannot transmit analog HSYNC and VSYNC signals directly to the VGA monitor, digital sync signals must be taken from the GPU, buffered (e.g., with a pair of 74F04 inverters) and level-shifted. An additional delay of approximately 40 input pixel clocks must also be imparted on both HSYNC and VSYNC as well to compensate for the pipeline delay of R/G/B through the encoder. Figure 1-52 shows this concept. In VGA modes where embedded syncs in the R/G/B outputs are used, the buffers are not necessary.

Figure 1-52. Filterless DAC Outputs for VGA (RGB) DAC Output with Sync Buffers



GENERAL NOTE:

1. Make sure to have only one of the paired outputs plugged in simultaneously.
2. The VGA R/G/B HSYNC*/VSYNC* outputs can drive either a standard DB15 female connector or 5 separate male BNC connectors.
3. The 74F04 buffers help isolate any noise generated from the monitor, including reflections from coupling into the encoder sync inputs.

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1.3.50 TV DAC Detection Procedures

This encoder can determine whether or not the DAC output is connected to a monitor by verifying that the output is doubly-terminated in VGA, NTSC/PAL/SECAM, SCART, Component Video (YCRCB), or HDTV out modes. The MONSTATx bit for the corresponding DAC is set to 1 if both of the following conditions occur: the device senses a double-terminated load and the CHECK_STAT register bit is set. While CHECK_STAT is set, the output is forced to 2/3 of VREF when terminated and 4/3 of VREF if unterminated. The MONSTATx bit reflects the condition when the DAC output is less than or equal to VREF. The CHECK_STAT bit is automatically cleared after ten clock cycles.

The status of each of the three CX25874/5's DACs can be checked at any time using two different methods. The first method is called Standard serial read-back. To perform a check of each MONSTATx bit and in turn, gather correct information about the connection status of each D-A converter, and follow the Standard DAC detection algorithm procedure in Table 1-37.

Table 1-37. Standard DAC Detection Algorithm for the CX25874/5

1. Set the SRESET bit of the 0xBA register to 1. This usually means register 0xBA will need to be written with 80 hex (for master interface) or A0hex for (for pseudo-master or slave interface). This will force the encoder into its default configuration mode 640x480 RGB in NTSC out video off.
2. Set both the EN_REG_RD and EACTIVE bits to 1. This usually means register 0x6C will need to be written with 44 hex (for all video output modes except SCART). The state of the EACTIVE bit will not impact DAC detection results.
3. Set the CHECK_STAT bit of register 0xBA to 1. This usually means register 0xBA will need to be written with 40 hex (for CX25874/5 in master interface) or 60 hex (for pseudo-master or slave interface).
4. Read register 0x06, which contains the MONSTAT_A, MONSTAT_B, MONSTAT_C, and MONSTAT_D bits in the upper nibble. Bit 7 (MSb) of register 0x06 contains the monitor detection status for DAC_A (MONSTAT_A) while bit 4 contains the monitor detection status for SCART_CSYNC (MONSTAT_D).
5. Check to see if any of the MONSTAT_x bits are 1. If any true result is obtained, at least one television has been detected and therefore connected to the CX25874/5.
6. If all MONSTAT_x bits are 0, repeat step 4 and step 5 again. Read register 0x06 and check the MONSTAT_x bits again. After the 64th iteration, if none of the MONSTAT_x bits are 1, a TV is not connected. Algorithm ends with a null result.

NOTE: If the SRESET, EN_REG_RD, and EACTIVE bits were set previously prior to the start of this TV detection algorithm, there is no need to set these again. Bypass steps 1 and 2, and begin the routine at step 3.

NOTE: Monitor status detection cannot be performed on a disabled DAC (DACOFF = 1 or DACDISx = 1)

Sample C code for the Standard TV Detection Algorithm is listed below for assistance. Sixteen different permutations of the upper nibble of register 0x06 are possible. Each of these results signifies different MONSTAT_x and therefore DAC connection schemes.

```
BOOLEAN IsTvConnected()
{
Register* reg;

reg = OurTvEncoder->GetRegister(0xba);
reg->Write(0x80); // SRESET is set to one

reg = OurTvEncoder->GetRegister(0x6c);
reg->Write(0x44); // EN_REG_RD = 1 and EACTIVE = 1

BYTE val;
reg = OurTvEncoder->GetRegister(0xba);
val = reg->Read();
val |= 0x40; // CHECK_STAT is set to one

BYTE status;
BYTE count = 64;  // if TV connected to any DAC, loop usually
requires no more than 25 iterations
// before returning TRUE
reg = OurTvEncoder->GetRegister(0x06);
do {
status = reg->Read();
} while( ((status & 0xF0) == 0) && (--count > 0) );

if( count > 0 )
return TRUE; // tv is connected

return FALSE; // tv is not connected
}
```

NOTE: DAC detection can be performed while the DENC generates SDTV or HDTV outputs.

The second method that can be used to readback from the encoder is called the ***Legacy*** method. This is because the procedure that follows was the only manner in which Conexant's first generation encoder (i.e., Bt868/869) could be read from. For compatibility purposes, this method was carried forward and exists in this third-generation encoder.

The Legacy procedure to follow for serial read-back and TV detection purposes is shown in Table 1-38. The ESTATUS[1:0] Read-Back Bit Map for the Legacy Algorithm is provided in Table 1-39.

Table 1-38. Legacy DAC Detection Algorithm

1. Write 01 to the ESTATUS[1:0]{bits D7=msb and D6 of register 0xC4}bit field. This sets up the encoder to read the MONSTAT data and check if the DACs have a TV connected.
2. Wait 2 ms to allow the analog nodes to reach their operating point.
3. Write the CHECK_STAT register bit to a one (bit D6 of register BA). This will latch the MONSTAT data internally and then clear itself.
4. Read the MONSTAT data by issuing 0x89 or 0x8B for the CX25874/875's device address. This ensures the least significant bit of the device write portion of the transaction is 1, which indicates to the encoder that it must send a byte of data on the next serial transaction. Do not write a subaddress to the encoder (this is not necessary since the first generation encoder only had one read register) and then read the next byte after the ACK. The 8-bit read in Step 1 contains either the CX25874/5's ID&VERSION (if ESTATUS was written to 00) or the CX25874/5's Monitor Detection for DACs C, B, and A + Closed Caption Status info and the FIELD # (if ESTATUS = 01). If ESTATUS was written to 10 in Step 1, the read byte will contain the PLL_LOCK, FIFO status bits, PAL bit, and BUSY bit.
5. If ESTATUS = 01, the serial master should receive one byte of information telling it the following information in this order:
   a. Monitor Connection Status for DACA output (MONSTAT_A = most significant bit).
   b. Monitor Connection Status for DACB output (MONSTAT_B).
   c. Monitor Connection Status for DACC output (MONSTAT_C).
   d. CCSTAT_E, CCSTAT_O.
   e. FIELD2, FIELD1, FIELD0 (least significant bit). The FIELD[2:0] bits indicate the field number that was last encoded. 000 indicates the 1st field.
6. The serial master must issue a STOP condition to finish the Read transaction. An ACK is not necessary before closing the transaction because the CX25874/5 just ignores the ACK anyway. In reality, the CX25874/875 does not really care about ending a transaction properly as long as a proper START condition is used to start the next transaction. In the read mode when the CX25874/5 is driving the SDA port, ending the transaction cannot take place until the encoder releases control of the SID line. This happens during the transition from when the last bit of the register is output to the receiving of the ACK.
7. The graphics controller, acting as the serial master, should clear the CHECK_STAT register bit back to 0 (bit D6 of register BA) by writing zero to the CHECK_STAT register bit (bit D6 of register BA) to display standard video again from the CX25874/875 VGA encoder.

Table 1-39. ESTATUS[1:0] Read-Back Bit Map for Legacy Algorithm

ESTATUS [1:0]	7	6	5	4	3	2	1	0
00	ID[2:0]			VERSION[4:0]				
01	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_O	FIELD[2:0]		
10	Reserved	SECAM	PLL_RESET_OUT	PLL_LOCK	FIFO_OVER	FIFO_ UNDER	PAL	RESERVED
GENERAL NOTE: Descriptions of these bits are found in Table 2-4.								

To reiterate, a START condition needs to be issued by the serial master to start the next transaction. In the read mode, when the CX25874/875 is driving the SID port, an end to the transaction cannot take place until the encoder releases control of the SID line. This event happens during the transition from when the last bit of the register is output to the receiving of the ACK.

1.3.51 Sleep/Power Management

There are a number of sleep/power down options for the CX25874/875. These options can be grouped into three different categories. The first category pertains to power management during normal operation.

- DIS_PLL bit:
  In nonsleep mode, when an external clock is being used, and the PLL is not needed, this bit will disable the PLL function.
- XTL_BFO_DIS bit:
  This disables the crystal buffer when it is not needed.
- DIS_CLKO bit:
  This will disable the CLKO output pin when not needed, i.e., an external clock is used in slave interface or to reduce sleep current.
- DACDISx/DACOFF bits:
  Each individual DAC can be powered down by setting its corresponding DACDISx bit. This is useful only if some of the DACs are not being utilized by the graphics system. The entire analog subsection of the device can be powered-down with the DACOFF bit, allowing digital operations to continue while reducing the power in the analog circuitry. This will achieve a significant reduction in power while maintaining all digital functionality.

The second category pertains to software enabled sleep operation.

- SLEEP_EN bit:
  Shuts down all internal clocks except the serial port interface clock. Disables all digital I/O pins except these: SLEEP, ALTADDR, CLKO, XTAL_IN, and XTAL_OUT. Disables the PLL. Turns off all DACs and VREF; the SLEEP and RESET* pins are never disabled.
- PLL_KEEP_ALIVE bit:
  When the PLL is used to provide a system clock, this bit keeps it functioning if the rest of the chip is slept through either the sleep pin or sleep bit. This bit has no affect if DIS_PLL is set.

The third category relates to the pin driven sleep operation.

- SLEEP pin:
  In addition to what the SLEEP_EN bit does, the sleep pin shuts down the serial port interface, shuts down the crystal, and disables the ALTADDR pin. If the SLEEP pin = 1, the only way the encoder can return to normal operation is by resetting the SLEEP pin in 0. The encoder will return to normal operation by performing a power on reset. This means the encoder will enter autoconfiguration mode 0 and expect a 640x480 RGB input, pseudo-master interface, and provide an NTSC output.

To achieve additional power savings, all the power management options available in normal operation are also available in software or pin driven sleep operation.

For the lowest possible power consumption, set the XTL_BFO_DIS and DIS_CLKO bits in order, then pull the SLEEP pin (#26) high.

1.4 Programming Methodology

There are four recommended programming methods for determining the valid CX25874/5 encoder register set required to generate your desired SDTV or HDTV output. Each one of these methods requires acquisition of the following design-specific input and output variables:

1.4.52 Input Variables

- Desired number of horizontal active pixels shown on the TV display: HACTIVE
- Desired number of vertical active lines shown on the TV display: VACTIVE
- Type of input data timing sent from GPU or data master device: Digital input can be either noninterlaced (progressive) or interlaced. Progressive timing is most common and preferred for SDTV outputs.
- Type of pixel input format for data sent from GPU or data master device: RGB and YCrCb are supported for SDTV outputs. RGB is most common. RGB and YPrPb are supported for HDTV outputs. RGB is again most common.
- Type of input clocking provided by master device: Pixel-clock based, 8-character-clock based, and 9-character-clock based master are only options. Pixel-clock master is by far the common and preferred for both SDTV and HDTV outputs.

1.4.53 Output Variables

- Desired output TV Standard: SDTV options include NTSC-M, NTSC-J, PAL-B -D -G -H -I (standard PAL), NTSC- 4.43, PAL-M, PAL-N, PAL-Nc, PAL-60, SECAM, Component YCRCB 480i, and SCART RGB. HDTV options include HDTV YPRPB 1080i, HDTV YPRPB 720p, HDTV YPRPB 480p, and HDTV YPRPB 625p.
- Desired amount of HOC, i.e., left and right side blanking in the active region...must always be 0 percent (largest TV picture size) for HDTV outputs: HOC value should be from 0 percent to 25 percent (letter-box TV picture size) for SDTV outputs. The overscan percentages, horizontally and vertically, are independent of each other.
- Desired amount of VOC, i.e., top and bottom directional blanking in the active region must always be 0 percent for HDTV outputs: VOC value should be from 0 percent (largest TV picture size) to 25 percent (letter-box TV picture size). The overscan percentages, horizontally and vertically, are independent of each other.

1.4.54 Choosing a Programming Method

Once these input and output variables are known about the desired mode, either a specific autoconfiguration mode can be used, or a complete SDTV register set (in Appendix F or HDTV register set listed in Appendix C can be used, or a custom generated register set and associated mode from the Cockpit programming application can be calculated, or direct contact to your local Conexant Field Applications Engineer (FAE) can be initiated because the first three options were unsuccessful. If the last option must be pursued, provide your mode's input and output variables to the Conexant FAE. The FAE will then determine whether a SDTV or HDTV out solution is even possible. If a solution does exist, the appropriate custom generated register set will be generated, tested, and returned to you for uploading into your platform containing CX25874/5.

1.4.54.1 Autoconfiguration Modes

The easiest and most preferred method for TV output programming is through the autoconfiguration process and 48 popular autoconfiguration modes built into the CX25874/5's internal memory. Autoconfiguring the device occurs when bit fields CONFIG[5:3] and CONFIG[2:0] in register 0xB8 are programmed to any state from 000|000 to 101|111. At the conclusion of this serial write, default values are copied from the CX25874/5's internal ROM into the most important encoder timing registers with indices 0x38 and 0x76 to 0xB4, inclusive. All other registers are not changed at the conclusion of an autoconfiguration mode command and retain their original state. Appendix C in this data sheet contains all register values and all pertinent input timing parameters for each of the 48 modes.

The flow chart illustrated in Figures 1-53 through 1-70 will allow you to determine the exact autoconfiguration mode that is appropriate for your design. Each path through this chart is based on the set of input and output variables for the desired mode. It is possible that your desired TV output configuration does not correspond to one of the 48 autoconfiguration modes, and alternative actions will be given at the conclusion of the diagram.

Prior to tracing through the flow chart that follows, understand these following points:

- Some active resolution and video output combinations (640x480 NTSC, 640x480 PAL-B -D -G -H-I (standard PAL), 800x600 NTSC, etc.) have more than one autoconfiguration mode associated with it. For these cases, each autoconfiguration mode changes the HOC and VOC percentage by approximately 3 percent from its closest related mode.
- Lowering the HOC or VOC percentage equates to less blanking in the active region of the TV picture, and accordingly, a larger television picture size in that direction. The higher the HOC or VOC percentage, the smaller the TV picture size, because the encoder imparts more blanking in the active region.
- The vertical refresh rate for the 525-line (NTSC, PAL-M, Component YCRCB 480i) standard-definition formats, PAL-60, and HDTV YPRPB 1080i, HDTV YPRPB 720p, HDTV YPRPB 480p output modes must be 60 Hz.
- The vertical refresh rate for 625-line (PAL-B -D -G -H-I (standard PAL), PAL-N, PAL-Nc, SECAM, SCART RGB) and HDTV YPRPB 625p output modes must be 50 Hz.
- Only active resolutions of 320x200 (pixel double), 320x240 (pixel double), 640x400, 640x480, 720x400, 720x480, 720x576, 800x600, and 1024x768 can be supported with an Autoconfiguration mode.

With your input and output variables in hand, trace through the flow chart, and determine which autoconfiguration solution, if any, fits your analog TV out requirements.

If you find an autoconfiguration mode somewhere at the conclusion of Figures 1-53 through 1-70, follow the guidelines set forth in Section 1.3 of this data sheet to fully program the CX25874/5 encoder register bank. In addition, consult Appendix C for timing parameters and programming details that the master device must generate for that particular mode.

Figure 1-53. Autoconfiguration Mode Programming Flow Chart—Main Program

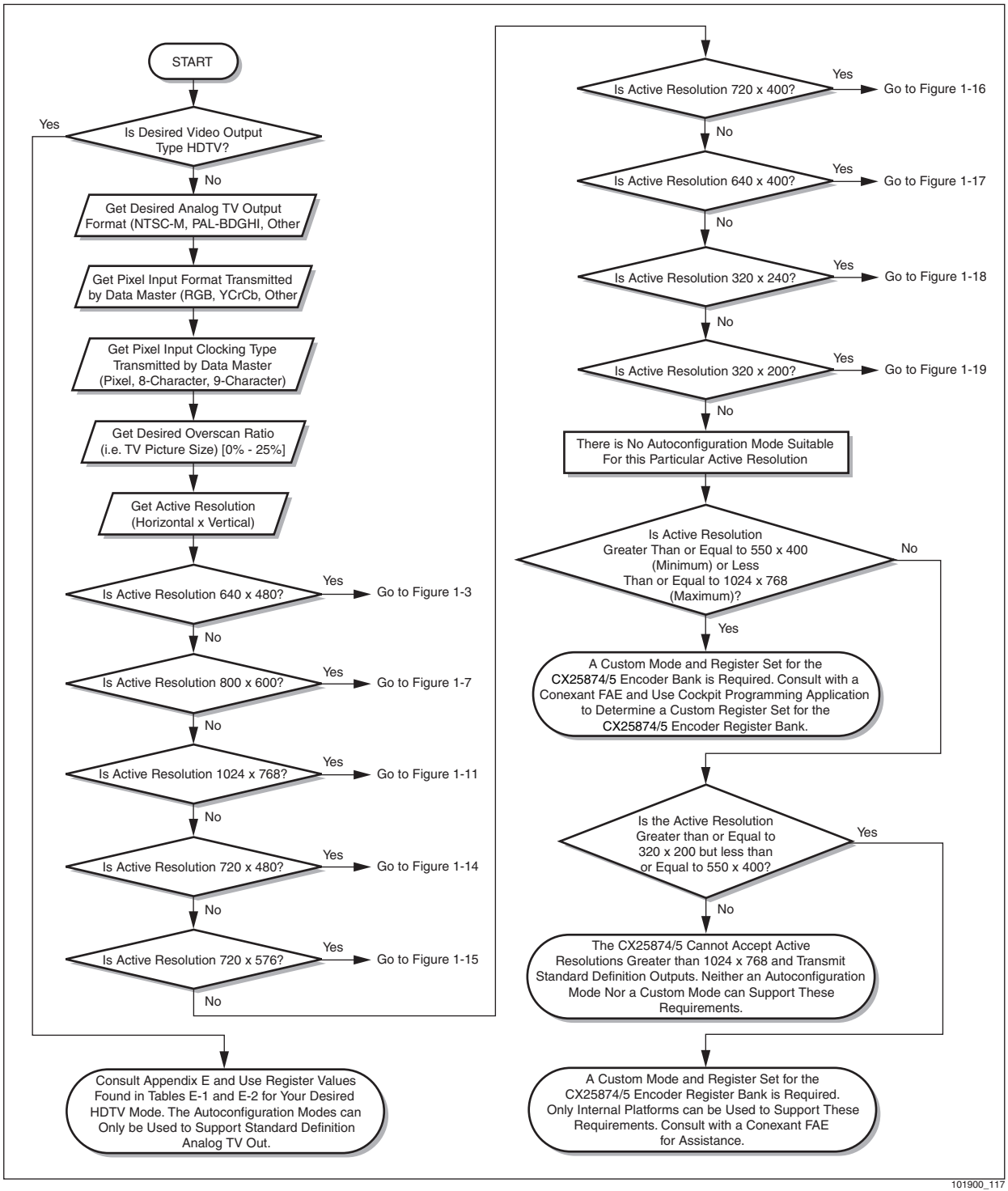


Figure 1-54. Autoconfiguration Mode Programming—640x480

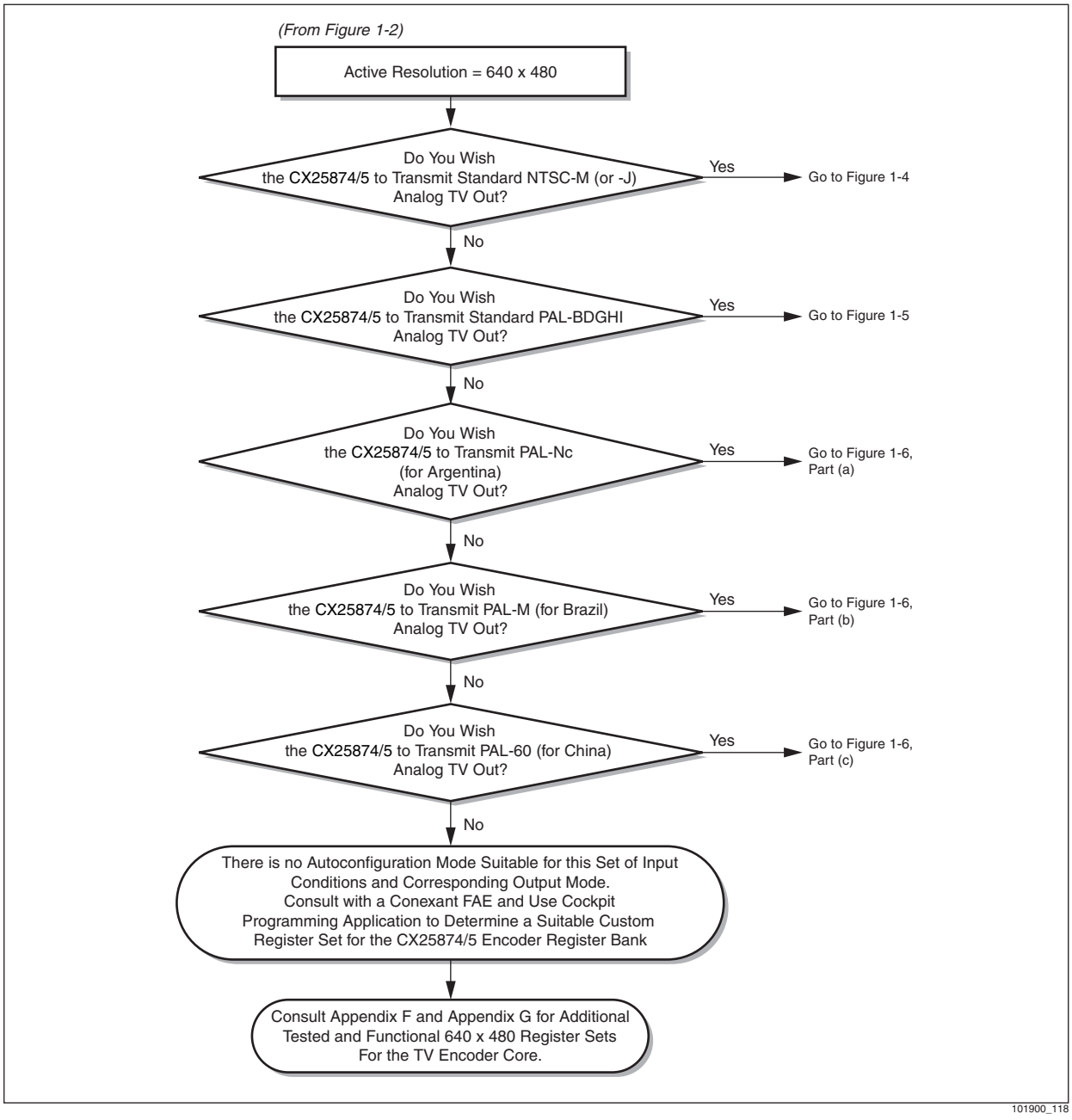


Figure 1-55. Autoconfiguration Mode Programming—640x480; NTSC

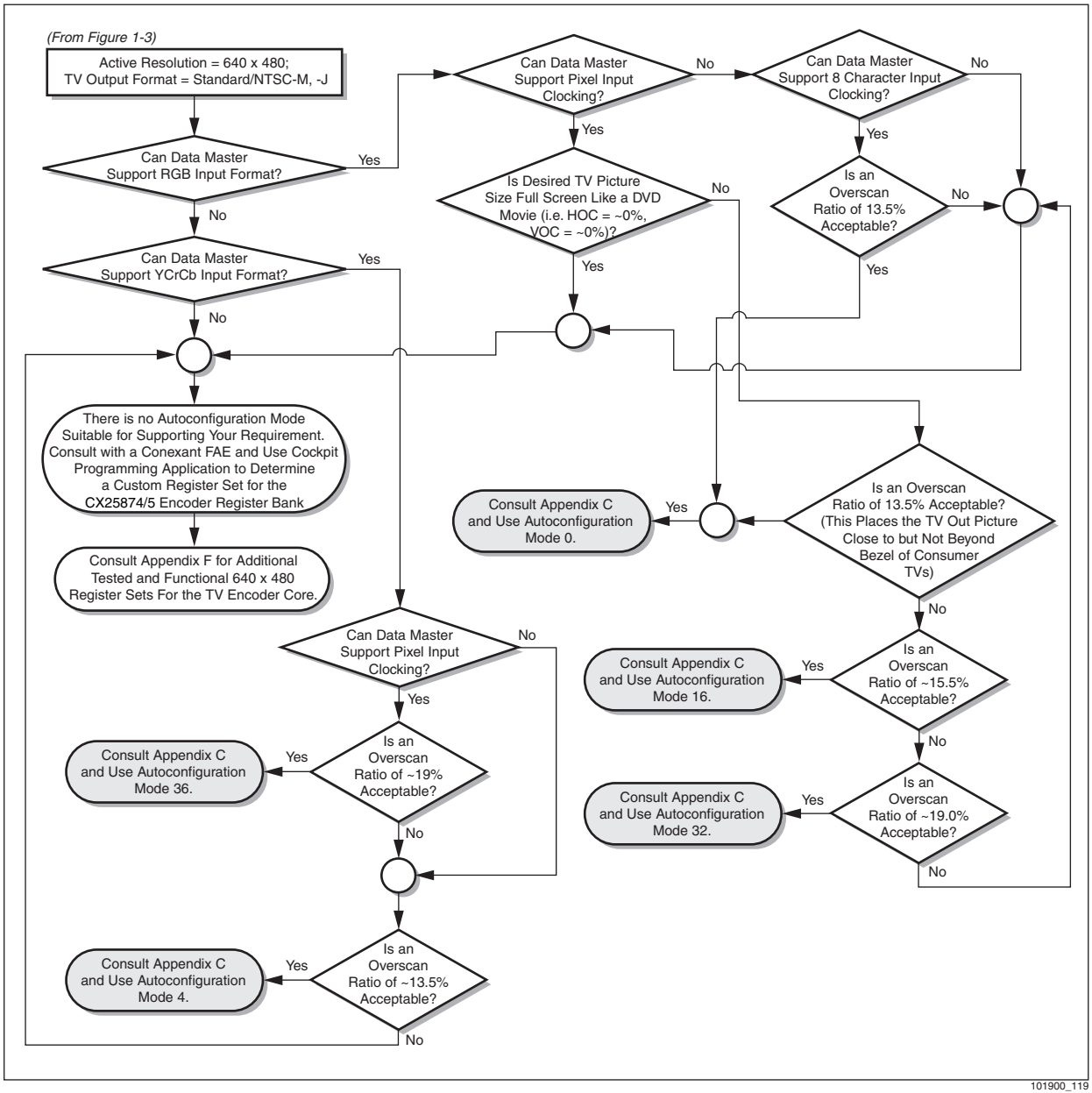


Figure 1-56. Autoconfiguration Mode Programming—640x480; PAL-BDGHI

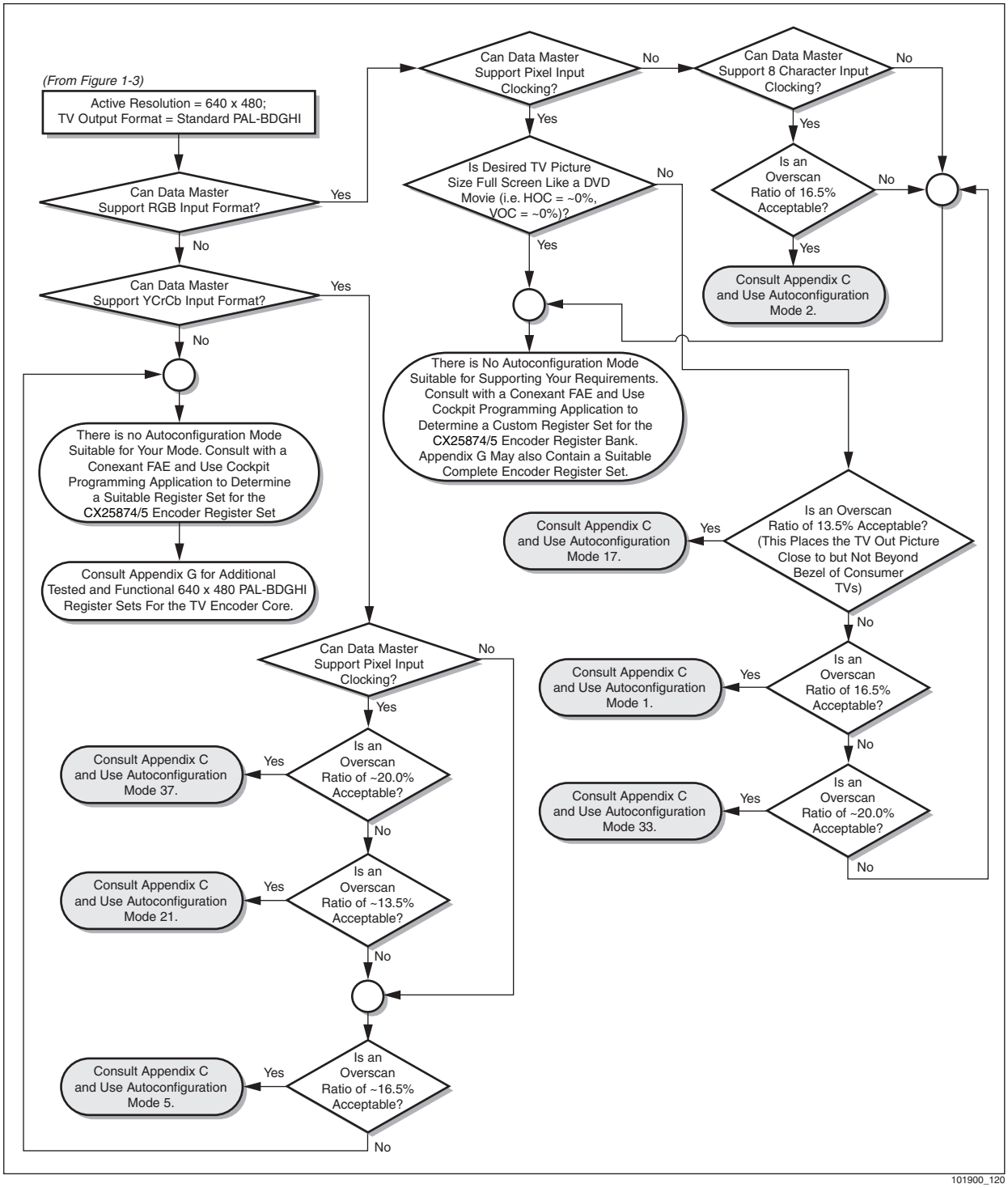


Figure 1-57. Autoconfiguration Mode Programming—640x480; PAL-M, Nc, 60

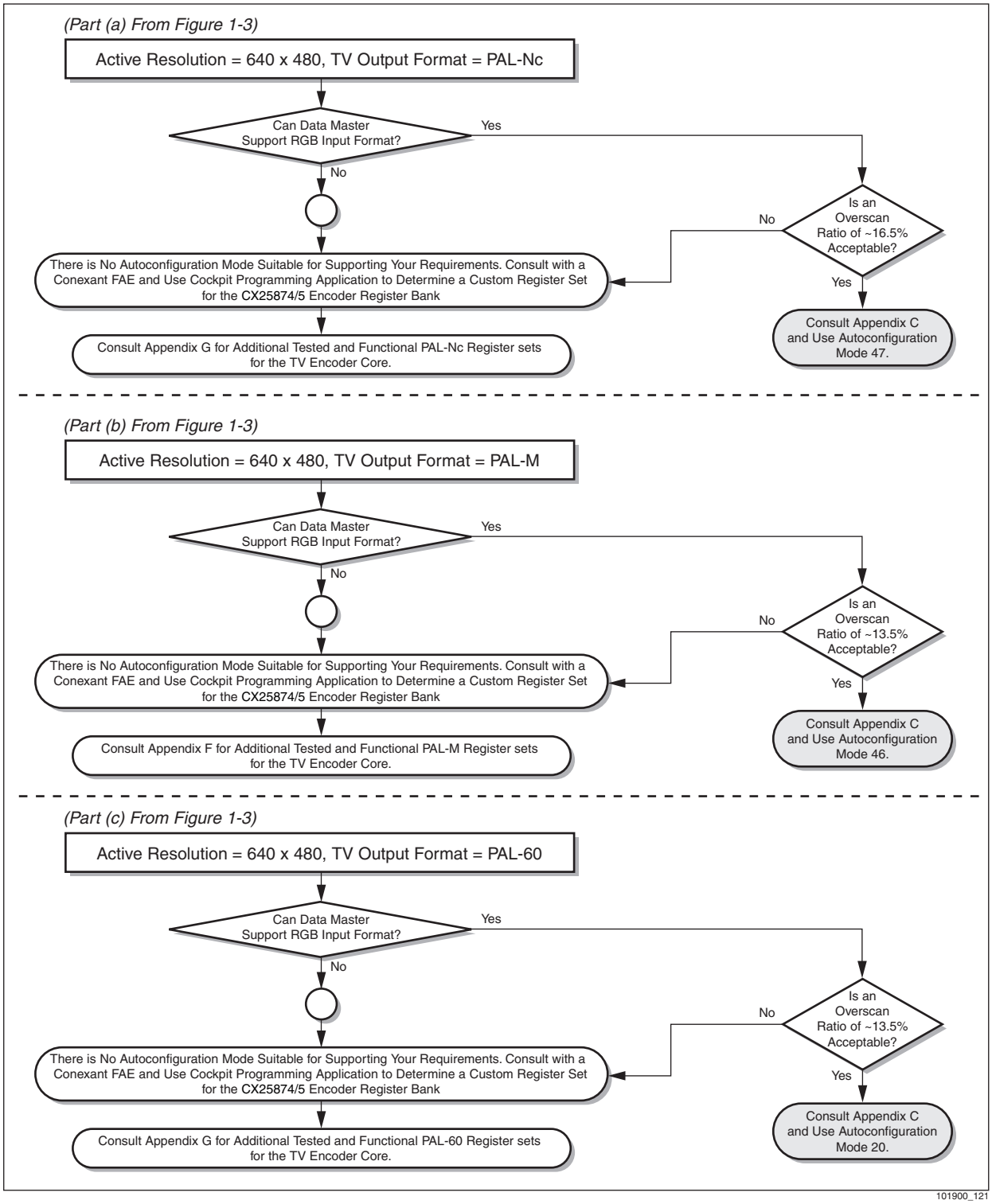


Figure 1-58. Autoconfiguration Mode Programming—800x600

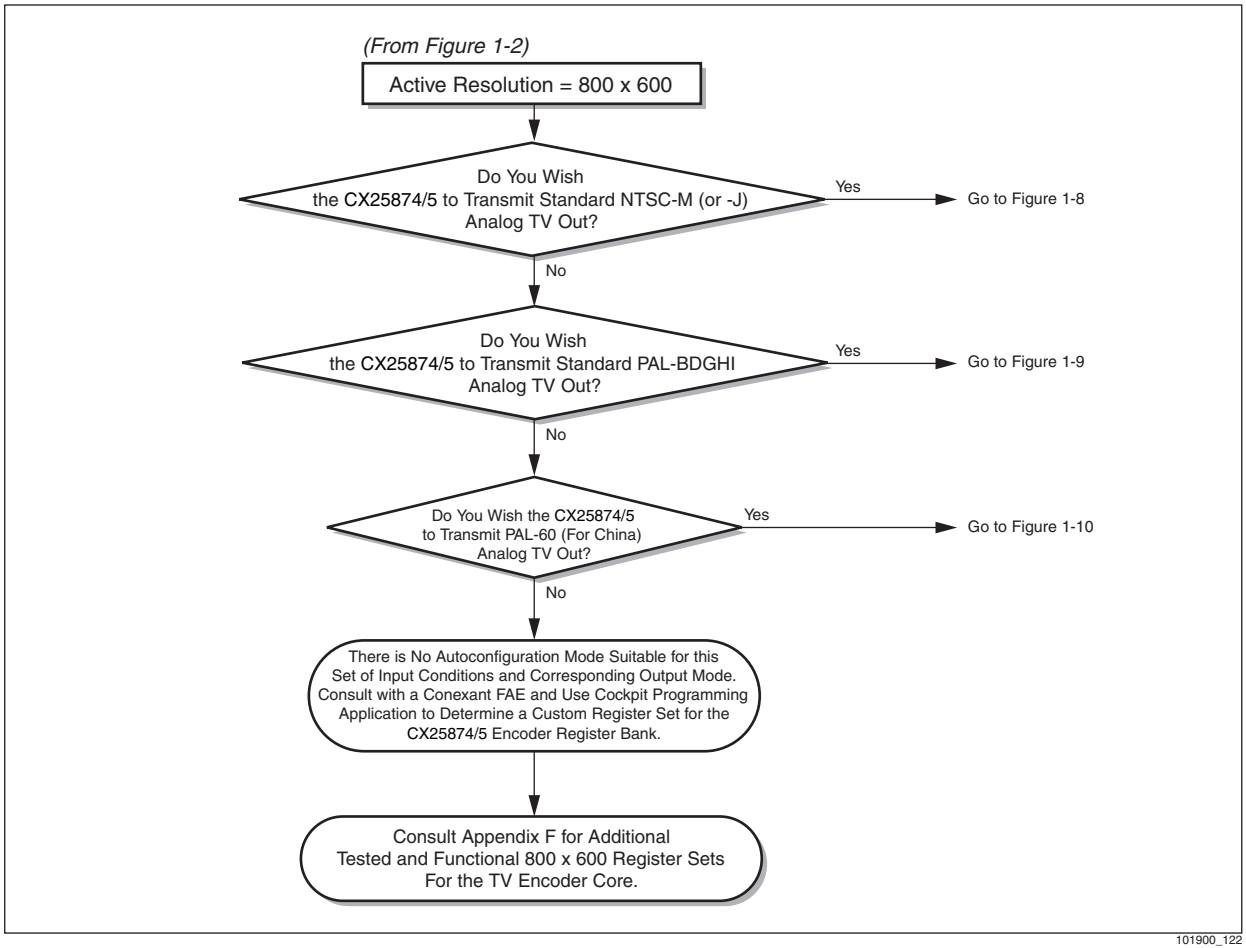


Figure 1-59. Autoconfiguration Mode Programming—800x600; NTSC

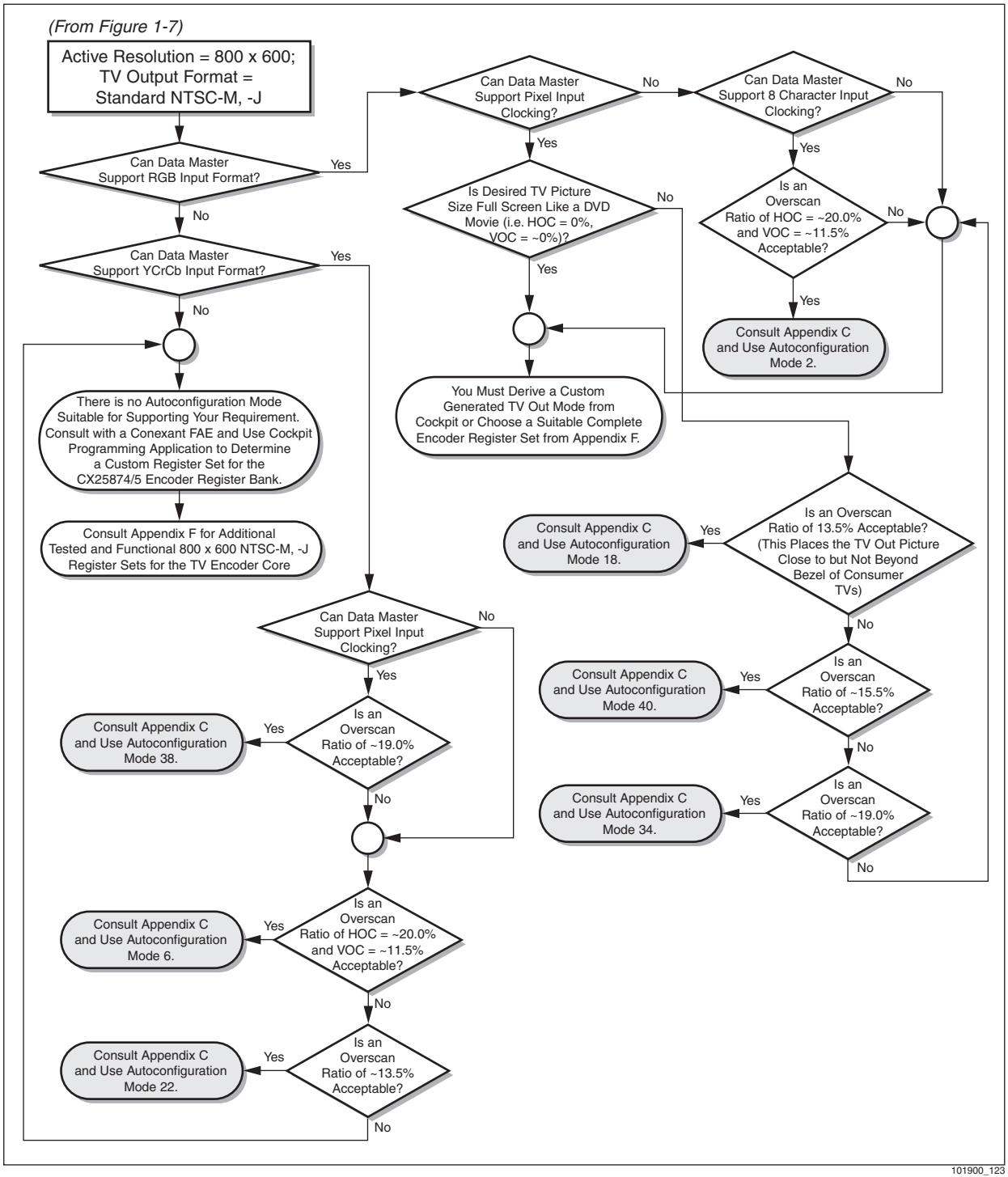


Figure 1-60. Autoconfiguration Mode Programming—800x600; PAL-BDGHI

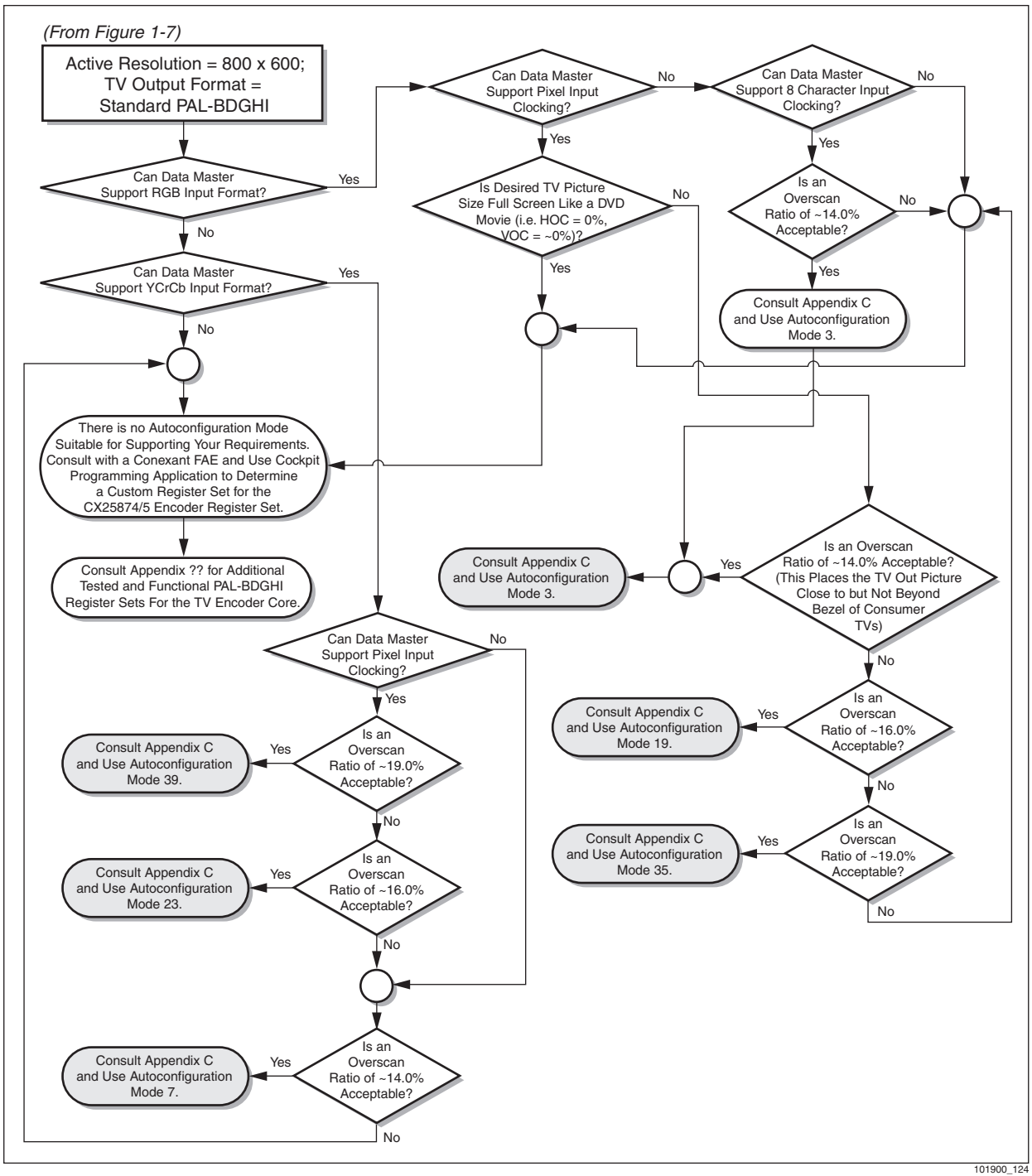


Figure 1-61. Autoconfiguration Mode Programming—800x600; PAL-60

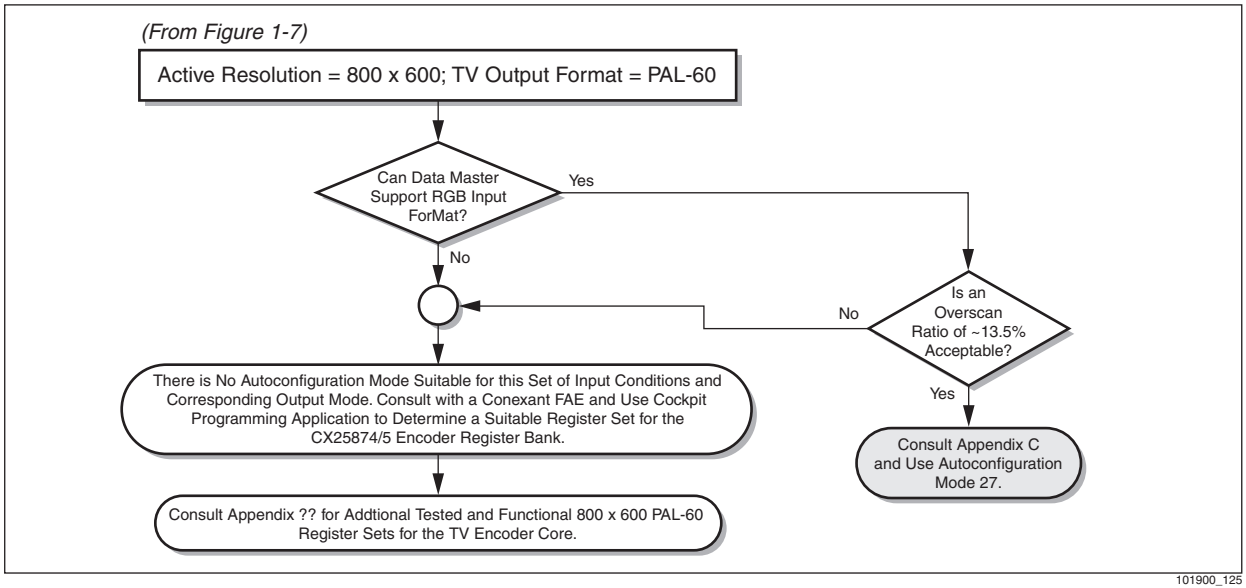


Figure 1-62. Autoconfiguration Mode Programming—1024x768

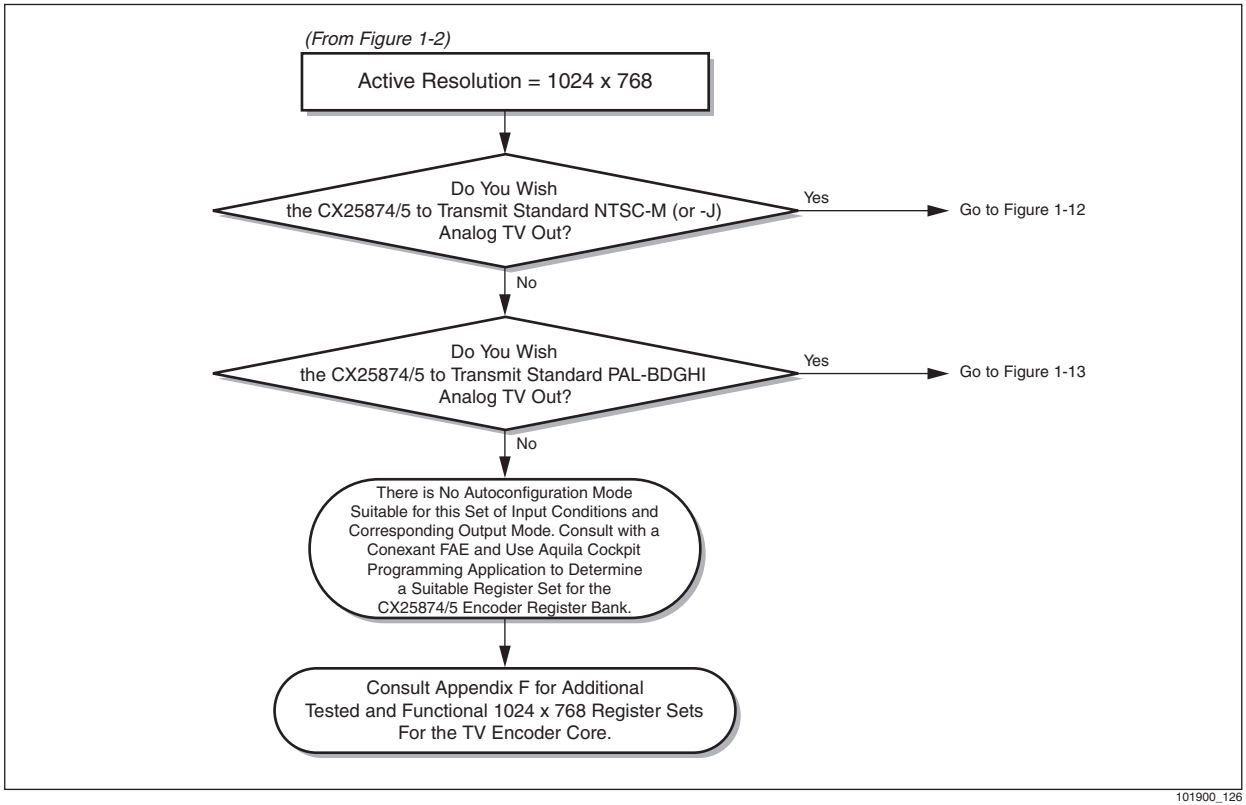


Figure 1-63. Autoconfiguration Mode Programming—1024x768; NTSC

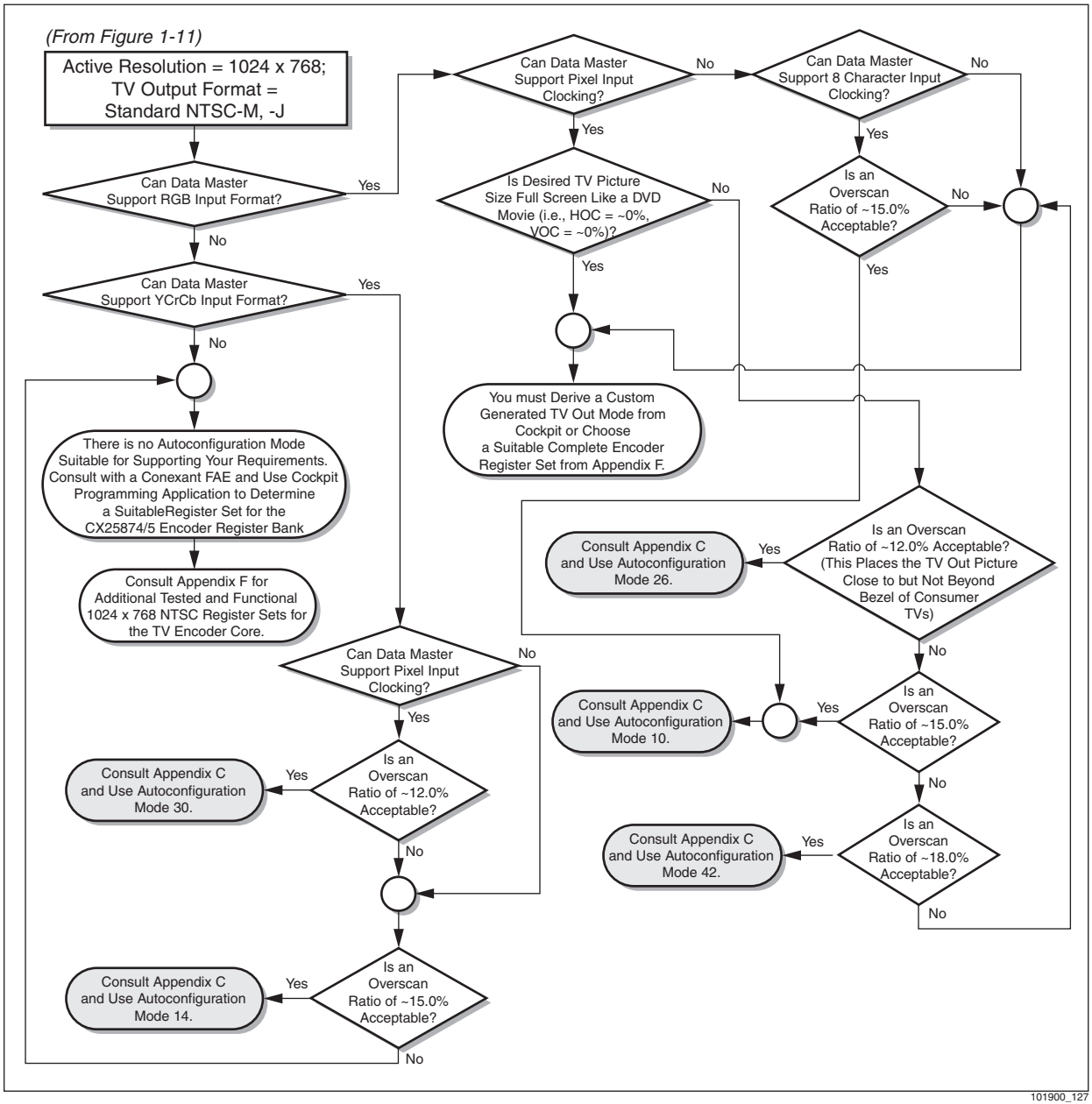


Figure 1-64. Autoconfiguration Mode Programming—1024x768; PAL-BDGHI

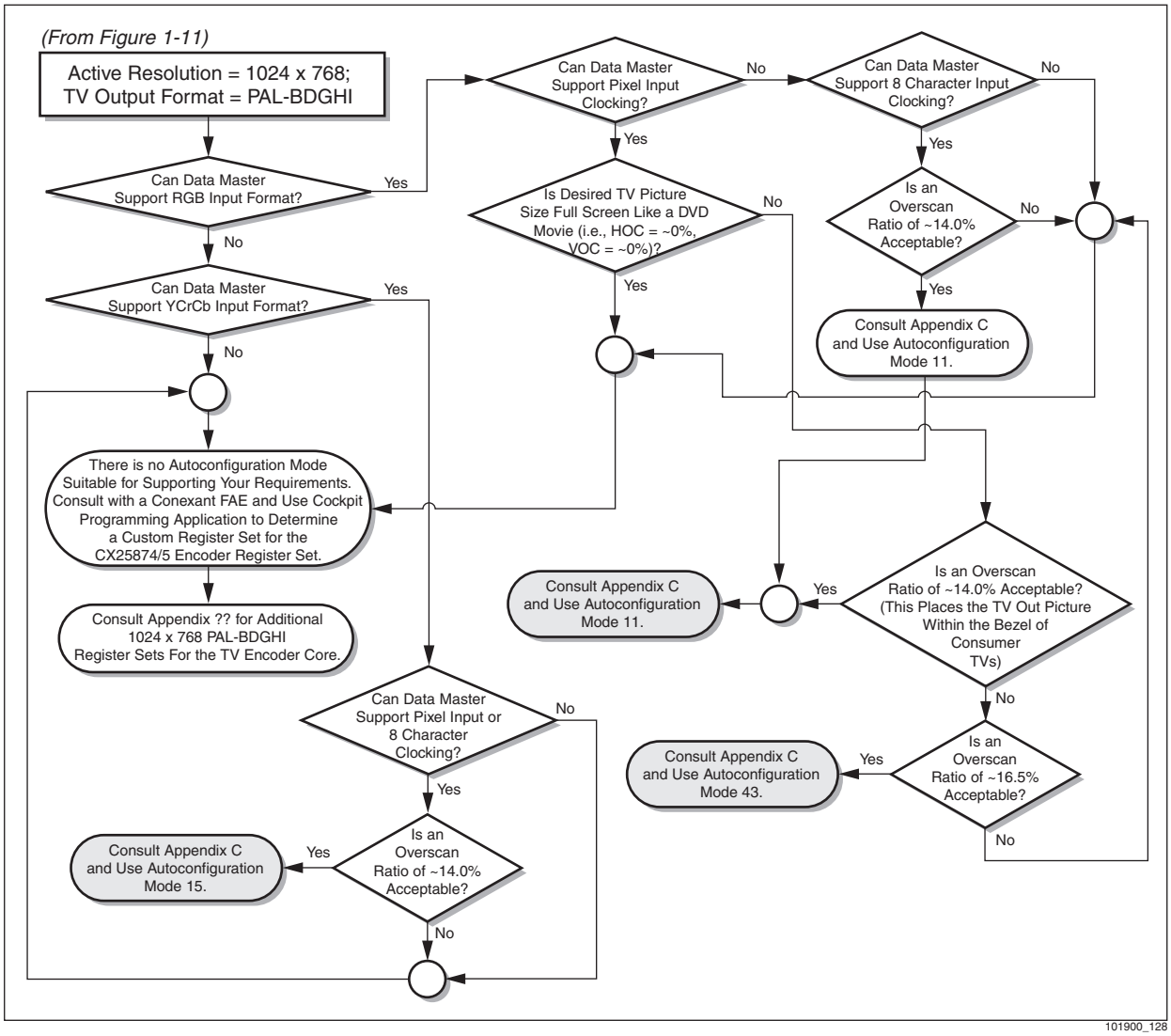


Figure 1-65. Autoconfiguration Mode Programming—720x480

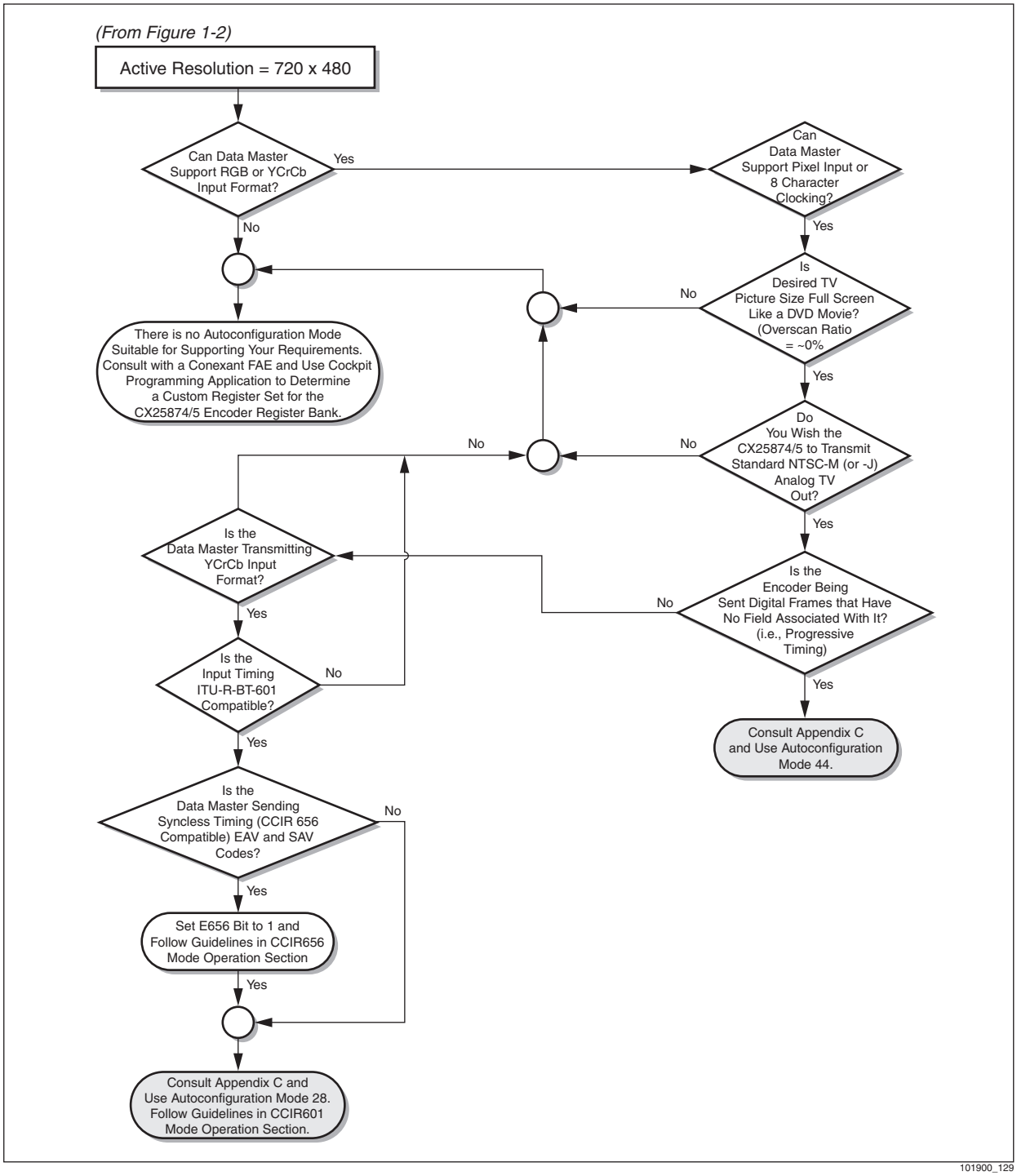


Figure 1-66. Autoconfiguration Mode Programming—720x576

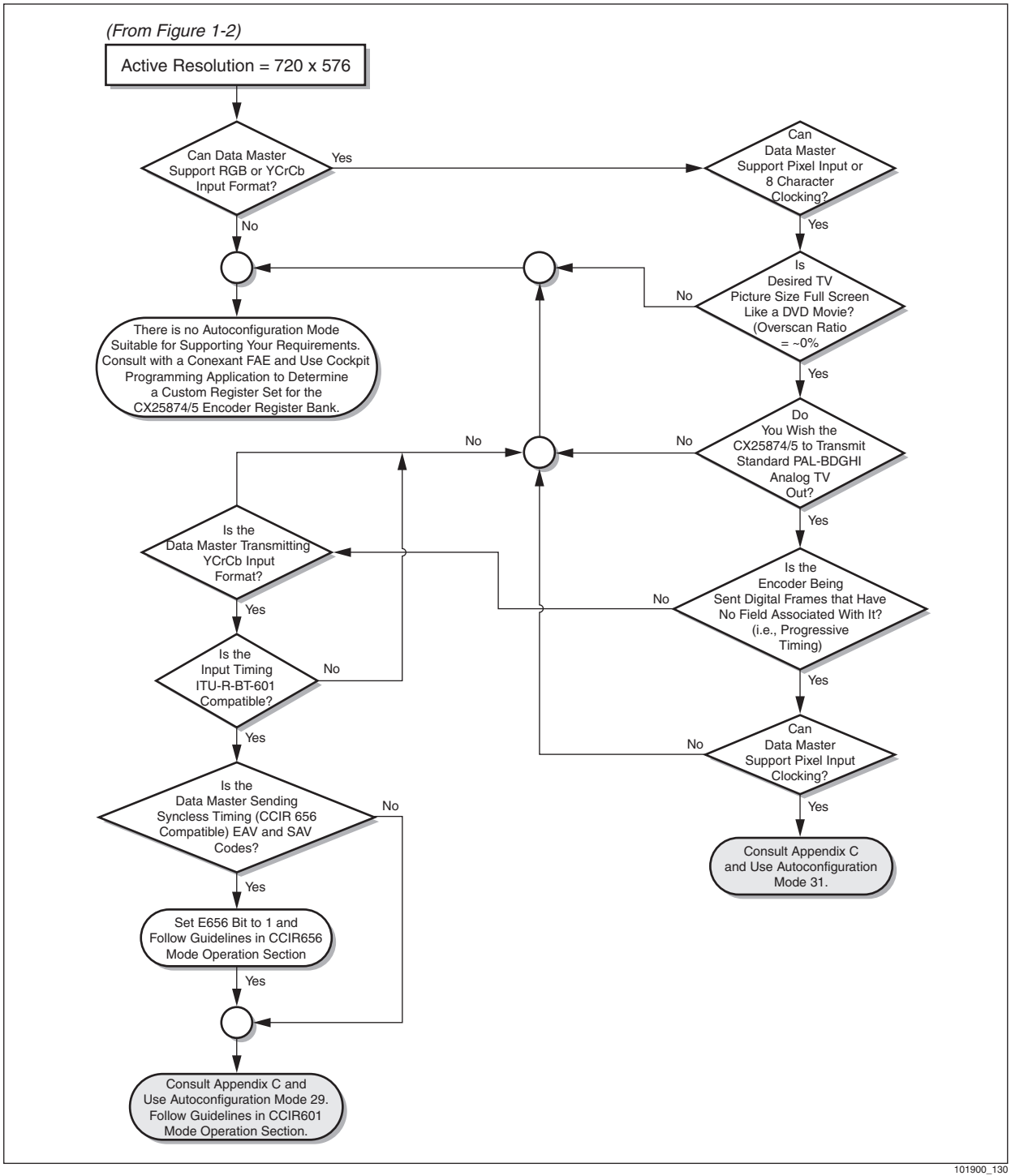


Figure 1-67. Autoconfiguration Mode Programming—720x400

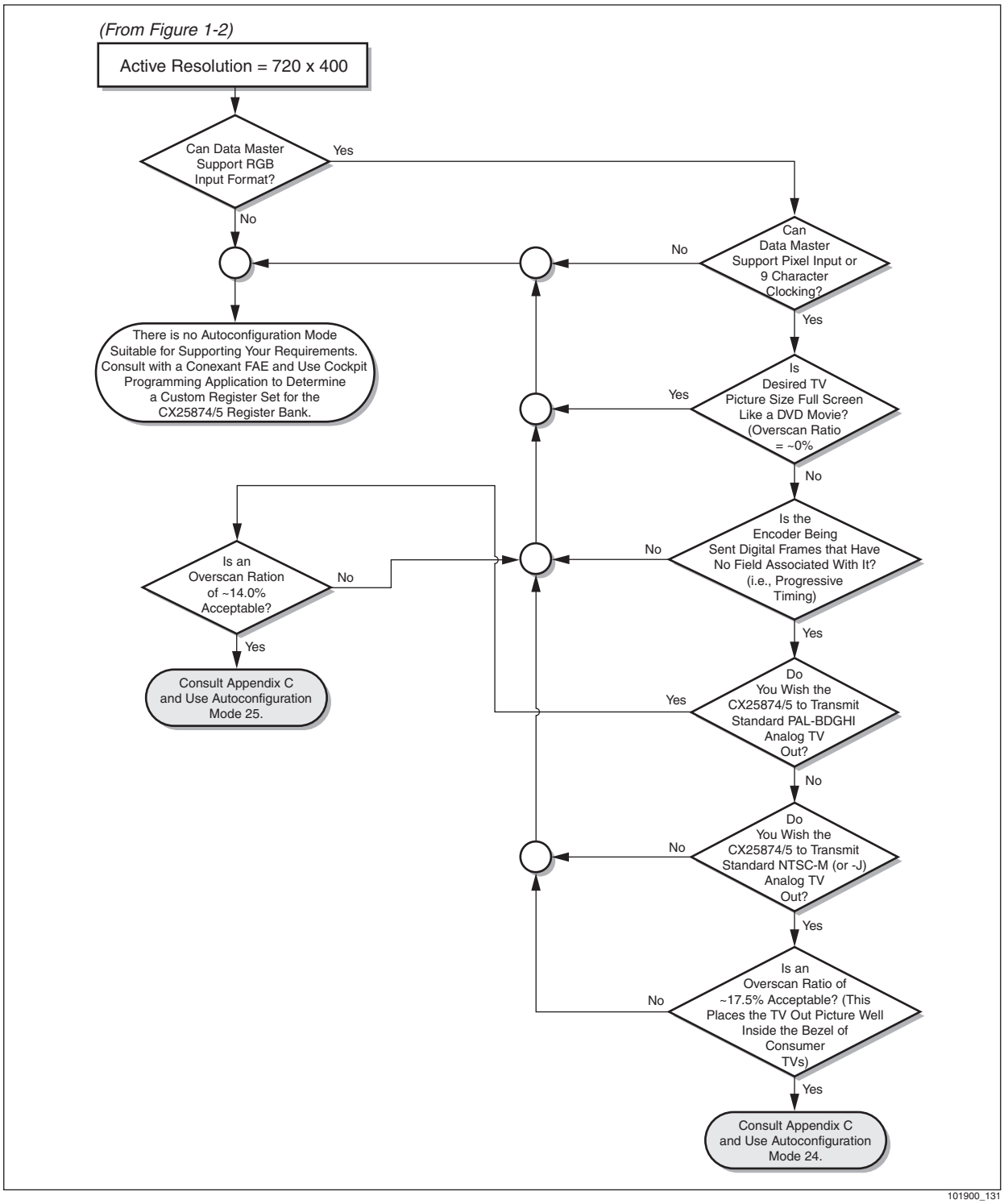


Figure 1-68. Autoconfiguration Mode Programming—640x400

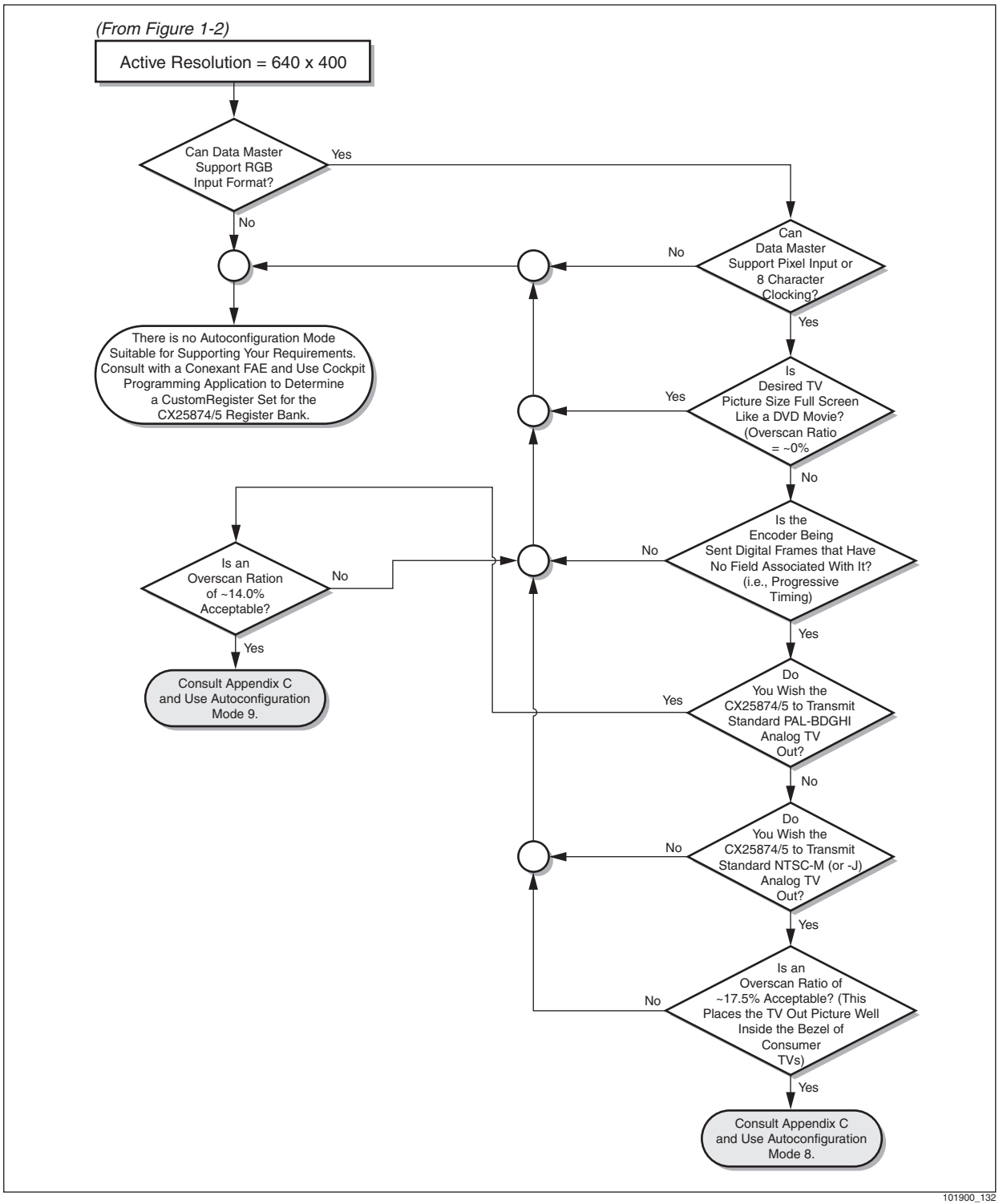


Figure 1-69. Autoconfiguration Mode Programming—320x240

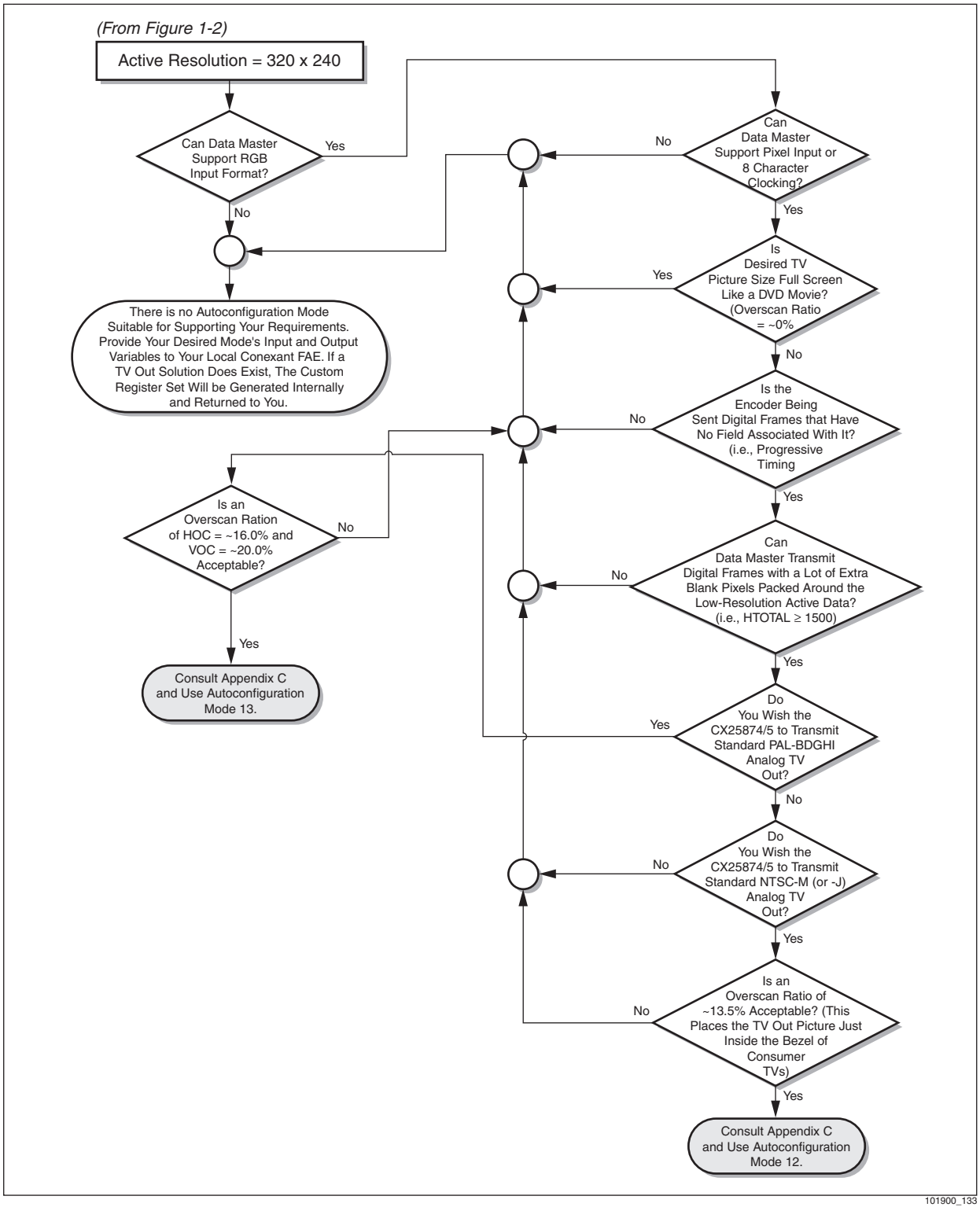
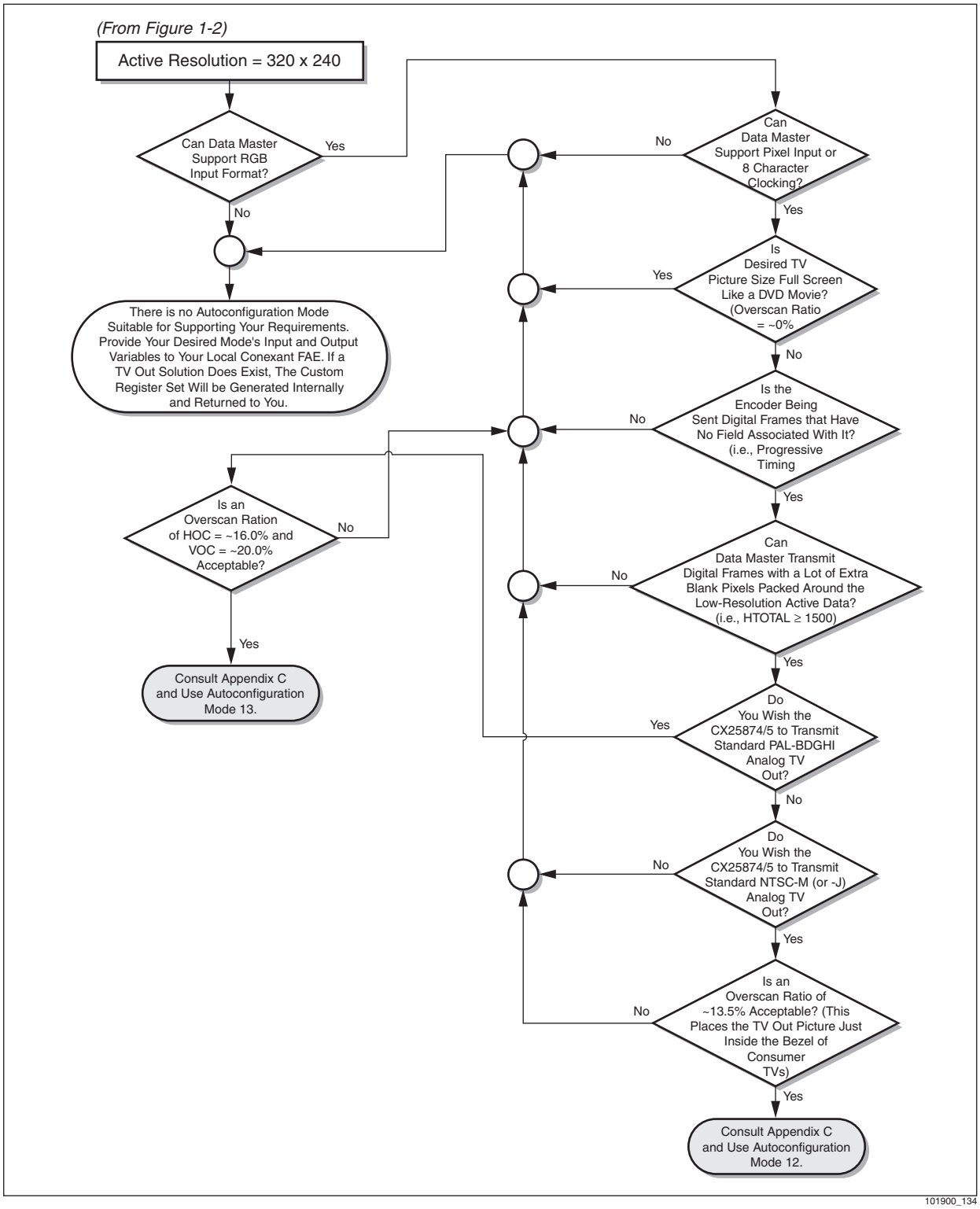


Figure 1-70. Autoconfiguration Mode Programming—320x200



Undoubtedly, the autoconfiguration modes are most popular and most frequently used for programming purposes. However, they are not the only TV output modes that the encoder can possibly support. In fact, many other TV out sizes and solutions are

possible when just considering the desktop resolutions. Desktop resolutions are defined to be the 640x480, 800x600, and 1024x768 active frames used frequently within the Windows desktop environment and popular Windows-compatible application programs.

1.4.54.2 Complete Register Sets—Appendix F

The second recommended programming method is to consult Appendix F of this data sheet. These appendices contain complete encoder register sets for all the aforementioned desktop resolutions and SDTV output video formats. If you wish to display a TV output based on a 640x480, 800x600, and 1024x768 input, and find that the overscan ratios available through various autoconfiguration modes are not sufficient for your design, choose a custom register set with a different overscan ratio found in Appendix F (525-line TV output formats).

If you wish to display a TV output based on an active resolution that is not 640x480, 800x600, and 1024x768, but is between 550x400 and 1024x768 active, jump to the next subsection to the third recommended programming method—Custom Mode Generation with Cockpit.

For support of 640x480, 800x600, and 1024x768, all tables in Appendix F contain fully tested and working NTSC-M, -J, and PAL-M register sets and working PAL-B, -D, -G, -H, -I, -N, Nc, and -60 register sets. Some of these register sets are based on autoconfiguration modes (due to an ideal overscan ratio) but most are purely custom solutions. Each desktop resolution is supported with no less than four register sets in the appendix corresponding to slightly different overscan ratios that vary by approximately 2–3 percent overscan compensation.

Appendix F assumes that the default digital input format will be IN_MODE[3:0] = 0000 = 24-bit RGB multiplexed, and this is reflected in the tables. Changing the encoder over to expect a different input format requires that the designer write a non-0 value to the IN_MODE[3:0] field. If this is necessary, perform this step after the entire register set has been programmed into the encoder.

Other settings shared by register sets in the appendices are as follows:

- The physical interface used by the encoder is the Master Interface with a BLANK* Input. This is not the default pseudo-master interface commonly used with the CX25874/5 encoder DACs. The different interfaces are explained in Section 1.3.9, Autoconfiguration and Interface Bits.
- SLAVE bit = 0. The state of the SLAVE bit dictates whether Port A or Port B associated with the TV out encoder core will be a timing master or timing slave. SLAVE controls the direction of the HSYNC* and VSYNC* ports. Since SLAVE = 0, the syncs will be generated by the DVI encoder and sent to the master device.
- EN_OUT = 1 ensuring the pixel clock reference signal, CLKO, is enabled from the encoder to the data master.
- EN_BLANKO is high (=1), signifying the CX25874/5's BLANK* line is an output or that no BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25874/5 to use its internal counters to determine the active versus the blanking regions.
- Standard and adaptive flicker filter both have been programmed optimally for the specific input resolution.
- DAC routing configures DACD (CX25891/2 only) as Composite, DAC C as Luma, DAC B as Chroma, and DACA as Composite outputs. The DAC routing through register 0xCE will probably need to be adjusted for each customer's particular set of outputs.

When using a complete register set from Appendix F, do not program register 0xB8 (autoconfiguration register) or you will mistakenly overwrite registers 0x38 and 0x76 to 0xB4 with new, unwanted values. Furthermore, the end user of any of these register sets may need to change various interface bits to make the CX25874/5 operate with the particular GPU or master device it is connected to. If you wish the encoder to be in pseudo-master or slave interface, as explained in Section 1.3.8, you will need to reprogram the SLAVE (bit 5 of 0xBA), EN_BLANKO (MSb of register 0xC6), EN_DOT(bit 6 of register 0xC6), and EN_OUT (LSb of register 0xC4) bits to the required bit settings.

1.4.54.3 Custom Mode Generation with Cockpit

As mentioned earlier, depending on the desired mode's input data timing and other conditions, often more than twenty different custom SDTV out solutions can be generated for each active resolution from 550x400 (HACTIVExVACTIVE) to 1024x768. These custom solutions are derived using a proprietary set of digital and analog timing equations and related video parameters and calculations whose end results are hexadecimal values that map directly into new data bytes for register 38 and registers 76 through B4 inclusive found within the CX25874/5 encoder register bank.

Because of the difficulty in understanding these core equations and the proprietary nature of this intellectual property, Conexant does not publish them anywhere in this document or in separate application notes. Instead, these equations are embedded into a Windows-compatible application called Cockpit created by Conexant. Customers that cannot or choose not to use an autoconfiguration mode or a complete register set found in Appendix F should immediately obtain a CX875EVK hardware Evaluation Kit (EVK) and associated installation software. After installing the package via the .exe file, the Cockpit tool will be accessible. Cockpit is a basic development tool for displaying nonstandard resolutions and different overscan compensation ratios. Using the aforementioned mode input and output variables and guidelines found in the application's user manual, use Cockpit's Custom Mode Generation Graphical User Interface (GUI) page to derive a custom solution, display the video on the TV, and save the necessary and correct register set to a text file. To summarize, acquiring Cockpit, following the manual's documented guidelines, and making use of Cockpit's Custom Mode Generation GUI is the third recommended programming method.

Cockpit has many other purposes, such as reading from any register or writing to any register within the DVI encoder or allowing the user to manipulate pertinent pull-down menus, check boxes, and other graphical features found on different pages and see immediately changes in the TV picture or DVI display. However, its most powerful feature for programming purposes is its ability to determine new CX25874/5 encoder register sets and exhibit new TV out solutions based on custom requirements for use with a new data master.

NOTE: When writing an entirely new custom register set to the CX25874/5 encoder bank from a new GPU for TV out, make sure to skip register 0xB8, the autoconfiguration register. Writing any value to it after having loaded values into other registers will replace desired data with unwanted data in indices 0x38 and 0x76–0xB4.

1.4.54.4 Field Applications Support—Internal Hardware Platforms

In rare cases, neither of the three previously mentioned programming methods are suitable for determination of a register set for your desired TV output mode. In this case, Conexant urges you to make a direct request to your local Conexant sales office for additional programming support. This will often be necessary if any of these unusual conditions are true:

- Active resolution is *less than* 550 horizontal active pixels x 400 vertical active lines per frame.
- Active resolution is *less than* 400 horizontal active pixels x 300 vertical active lines per frame and *requires* pixel doubling by the encoder.
- Active resolution is *greater than* 1024 horizontal active pixels x 768 vertical active lines per frame and TV out is standard definition.
- Type of input data timing sent from GPU is INTERLACED and the timing is not compliant with CCIR601/ITU-R BT.601 (i.e., 720 x 480i for 525/60 video systems and 720 x 576i for 625/50 video systems) or CCIR656/ITU-R.BT.601 syncless compatible input standards or HDTV EIA770-3 or SMPTE274M (for 1080i), or ITU-R.BT.709-4 (for 1035i). (Remember, CX25890 does not support HDTV out.)
- Type of pixel input format for data sent from GPU is not RGB or YCrCb for SDTV outputs.
- Type of pixel input format for data sent from GPU is not RGB or YPrPb for HDTV outputs.
- Desired amount of overscan compensation percentage horizontally or vertically is GREATER THAN 25 percent.
- Desired amount of overscan compensation percentage horizontally or vertically is LESS THAN 0 percent.
- HDTV output mode is *not* based on industry-accepted standards such as SMPTE274M/296M/293M or EIA770-2/770-3 1080i (Japan 1125i), 720p (Japan 750p), 480p (Japan 525p) ATSC resolutions.

Conexant field support will consult with internal engineering and provide them your design-specific data and input and output variables. Factory engineering will then attempt to obtain a solution using several specialized internal hardware platforms (such as DVT). If a solution can be found, Conexant will provide a custom register set to you along with timing parameters and any other pertinent technical recommendations for that mode. However, it is possible at this point that no TV out solution can be found using CX25874/5. If this is the case, an alternate Conexant device, if possible, will be proposed as a solution.

1.4.54.5 Programming Conclusion

For more programming instructions, review Section 1.3.21. It is never possible to reprogram only the encoder to enable a new TV out solution. To achieve a high-quality display on the TV, internal GPU registers in the data master must be reprogrammed so this device outputs the new frame timing required by the encoder. Parameters such as HTOTAL, VTOTAL, HACTIVE, VACTIVE, HBLANK, and VBLANK sometimes change significantly when only small changes are made to the input and output variables that comprise the mode. It should be noted that the encoder has no way of knowing that a different TV output mode is desired by the user. As a result, it relies on the serial bus master device to reconfigure it via an autoconfiguration mode or complete register set rewrite to make adjustments in its timing.

When both the GPU and CX25874/5 encoder register bank are programmed correctly, regardless of the interface (pseudo-master, slave, or master), the required input HSYNC* to first input active pixel spacing matches the output HSYNC* to first output active pixel spacing. In addition, the required input VSYNC* to first input active line spacing matches the output VSYNC* to first output active line spacing. When this occurs, the graphics controller always transmits active data at the time the CX25874/5 expects to receive it. Superior TV out quality is achieved only when this type of timing symmetry exists.

2 Internal Registers

A complete register bit map CX25874/5 is displayed in Table 2-1. All registers are read/write unless denoted otherwise. For bit descriptions and detailed programming information, follow the guidelines found in the remaining sections of Chapter 2. All registers are set to their default state following a software reset. A software reset is always performed at power-up. After power-up, a reset can be triggered by writing to the SRESET register bit.

Table 2-1. Register Bit Map for CX25874/5 *(1 of 4)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
00[1]	ID[2:0]			VERSION[4:0]				
02[1]	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_0	FIELD_CNT[2:0][2]		
04[1]	Reserved	SECAM	PLL_RESET_OUT	PLL_LOCK	FIFO_OVER	FIFO_UNDER	PAL	Reserved
06[1]	MONSTAT_A	MONSTAT_B	MONSTAT_C	MONSTAT_D	FIELD_CNT[3:0][2]			
26	YC2YP	Reserved	Reserved	Reserved	GPO_OE	GPO[2]	GPO[1]	GPO[0]
28	SERIALTEST[7:0]							
2E	HDTV_EN	RGB2YPRPB	RPR_SYNC_DIS	GY_SYNC_DIS	BPB_SYNC_DIS	HD_SYNC_EDGE	RASTER_SEL[1:0]	
30	SLEEP_EN	Reserved	XTL_BFO_DIS	PLL_KEEP_ALIVE	Reserved	DIS_PLL	DIS_CLKO	Reserved
32	AUTO_CHK	Reserved	Reserved	Reserved	IN_MODE[3]	DATDLY_RE	OFFSET_RGB	CSC_SEL
34	ADPT_FF	Reserved	Reserved	C_ALTFF[1:0]		Reserved	Y_ALTFF[1:0]	
36	FFRTN	YSELECT	C_THRESH[2:0]			Y_THRESH[2:0]		
38[3]	Reserved	PIX_DOUBLE	PLL_32CLK	DIV2[2]	HBURST_END[8]	HBURST_BEGINS[8]	V_LINESI[10]	H_BLANKI[9]
3A	RAND_EN	Reserved	Reserved	Reserved	HALF_CLKO	Reserved	PLL_INPUT	DIV2_LATCH
3C	MCOMPY[7:0]							
3E	MCOMPU[7:0]							
40	MCOMPV[7:0]							
42	MSC_DB[7:0]							

Table 2-1. Register Bit Map for CX25874/5 *(2 of 4)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
44	MSC_DB[15:8]							
46	MSC_DB[23:16]							
48	MSC_DB[31:24]							
4A	DR_LIMITP[7:0]							
4C	DR_LIMITN[7:0]							
4E	Reserved	Reserved	DR_LIMITN[10:8]			DR_LIMITP[10:8]		
50	DB_LIMITP[7:0]							
52	DB_LIMITN[7:0]							
54	Reserved	Reserved	DB_LIMITN[10:8]			DB_LIMITP[10:8]		
56	FIL4286INCR[7:0]							
58	Reserved	Reserved	FILFSCONV[5:0]					
5A	Y_OFF[7:0]							
5C	HUE_ADJ[7:0]							
5E	XDSSEL[3:0]				CCSEL[3:0]			
60	EWSSF2	EWSSF1	Reserved	Reserved	WSDAT[4:1]			
62	WSDAT[12:5]							
64	WSDAT[20:13]							
66	WSSINC[7:0]							
68	WSSINC[15:8]							
6A	Reserved	Reserved	Reserved	Reserved	WSSINC[19:16]			
6C	TIMING_ RST	EN_REG_RD	FFCBAR	BLNK_IGNORE	EN_SCART	EACTIVE	FLD_MODE[1:0]	
6E	HSYNOFFSET[7:0]							
70	HSYNOFFSET[9:8]		HSYNWIDTH[5:0]					
72	Reserved							
74	DATDLY	DATSWP	Reserved			VSYNWIDTH[2:0]		
76*(3)*	H_CLKO[7:0]							
78*(3)*	H_ACTIVE[7:0]							
7A*(3)*	HSYNC_WIDTH[7:0]							
7C*(3)*	HBURST_BEGIN[7:0]							
7E*(3)*	HBURST_END[7:0]							
80*(3)*	H_BLANKO[7:0]							

Table 2-1. Register Bit Map for CX25874/5 *(3 of 4)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
82[3]	V_BLANKO[7:0]							
84[3]	V_ACTIVEO[7:0]							
86[3]	V_ACTIVEO[8]	H_ACTIVE[10:8]			H_CLKO[11:8]			
88[3]	H_FRACT[7:0]							
8A[3]	H_CLKI[7:0]							
8C[3]	H_BLANKI[7:0]							
8E[3]	Reserved	Reserved	Reserved	VBLANKDLY	H_BLANKI[8]	H_CLKI[10:8]		
90[3]	V_LINESI[7:0]							
92[3]	V_BLANKI[7:0]							
94[3]	V_ACTIVEI[7:0]							
96[3]	CLPF[1:0]		YLPF[1:0]		V_ACTIVEI[9:8]		V_LINESI[9:8]	
98[3]	V_SCALE[7:0]							
9A[3]	H_BLANKO[9:8]		V_SCALE[13:8]					
9C[3]	PLL_FRACT[7:0]							
9E[3]	PLL_FRACT[15:8]							
A0[3]	EN_XCLK	BY_PLL	PLL_INT[5:0]					
A2[3]	FM	ECLIP	PAL_MD	DIS_SCRST	VSYNC_DUR	625LINE	SETUP	NI_OUT
A4[3]	SYNC_AMP[7:0]							
A6[3]	BST_AMP[7:0]							
A8[3]	MCR[7:0]							
AA[3]	MCB[7:0]							
AC[3]	MY[7:0]							
AE[3]	MSC[7:0]							
B0[3]	MSC[15:8]							
B2[3]	MSC[23:16]							
B4[3]	MSC[31:24]							
B6	PHASE_OFF[7:0]							
B8[4]	Reserved	CONFIG[5:3]			Reserved	CONFIG[2:0]		
BA	SRESET	CHECK_STAT	SLAVE	DACOFF	DACDISD	DACDISC	DACDISB	DACDISA

Table 2-1. Register Bit Map for CX25874/5 *(4 of 4)*

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
BC	CCF2B1[7:0]							
BE	CCF2B2[7:0]							
C0	CCF1B1[7:0]							
C2	CCF1B2[7:0]							
C4	ESTATUS[1:0]		ECCF2(EXDS)	ECCF1(ECC)	ECCGATE	ECBAR	DCHROMA	EN_OUT
C6	EN_BLANKO	EN_DOT	FIELDI	VSYNCI	HSYNCI	IN_MODE[2:0]		
C8	DIS_YLPF	DIS_FFILT	F_SELC[2:0]			F_SELY[2:0]		
CA	DIS_GMUSHY	DIS_GMSHY	YCORING[2:0]			YATTENUATE[2:0]		
CC	DIS_GMUSHC	DIS_GMSHC	CCORING[2:0]			CATTENUATE[2:0]		
CE	OUT_MUXD[1:0]		OUT_MUXC[1:0]		OUT_MUXB[1:0]		OUT_MUXA[1:0]	
D0	CCR_START[7:0]							
D2	CC_ADD[7:0]							
D4	MODE2X	DIV2(2)	Reserved	CCR_START[8]	CC_ADD[11:8]			
D6	CCR_ START[9]	E656	BLANKI	BLUEFIELD	OUT_MODE[1:0]		LUMADLY[1:0]	
D8	CHROMA_ BW	BY_YCCR	PKFIL_SEL[1:0]		FIELD_ID	CVBSD_INV	SC_ PATTERN	PROG_SC

FOOTNOTE:

(1) This register is read-only.

(2) These bits are repeated in other registers. The value of these bits will always match those with the same name. Any redundancy of bits have been done for backwards register compatibility.

(3) This register is reprogrammed by the autoconfiguration process.

(4) ***When sequentially writing a new register set to the CX25874/875, make sure to skip register 0xB8***. This is the autoconfiguration register and writing to it will overwrite registers 0x76 through 0xB4 and 0x38 with autoconfiguration values.

2.1 Power-Up State

The power-up state of this encoder will be black burst video in autoconfiguration mode 0 (640 x 480 RGB in IN_MODE[3:0] = 0000, EN_REG_RD = 0, NTSC-M out). A TV out picture will not appear on the screen unless the encoder is sent Mode 0 digital timing. By default, the CX25874/875 will be in pseudo-master interface with serial readback of all registers turned off. To turn off black burst and enable register feedback and active video, the EACTIVE register bit and the EN_REG_RD bit must be set. To accomplish this write register 0x6C to 0x46.

2.2 Device Address

The serial device address for the CX25874/875 is configurable by the state of the ALTADDR pin at reset. Table 2-2 lists how the ALTADDR pin switches the device's serial slave address. The ALTADDR pins state should only be changed during power-up.

Table 2-2. Serial Address Configuration—8 Bit

ALTADDR State	Device Address for Writing	Device Address for Reading
0	0x88	0x89
1	0x8A	0x8B

For 7-bit writing and reading, the serial device address is 0x44 when ALTADDR = 0 and 0x45 when ALTADDR = 1.

2.3 Reading Registers

Following a start condition, writing 0x89 and then the desired subaddress initiates the read-back sequence. The next eight bits of information, returned by the CX25874/875, can be read from the SID pin, most significant bit first. Alternative address 0x8B is required if the ALTADDR pin is high. Registers 0x00 through 0x06 are read only. All other registers can be read from or written to.

The ID[2:0] bits of register 0x00 indicate the part type. The lower five bits (VERSION[4:0]) indicate the version number of that particular encoder. Table 2-4 for all the data details.

For software detection of a connected TV monitor on each DAC output, the MONSTAT_x bits (found in both the 0x06 register and 0x02 register for legacy purposes) should be read accordingly after writing to CHECK_STAT. For a description of this process follow the guidelines and algorithm contained in the TV DAC Detection Procedures section.

To check the status of the monitor connections at the DAC output automatically once per frame during the vertical blanking interval, set the AUTO_CHK bit.

The following pseudocode sample should be used for properly reading registers within the CX25874/5.

First, there are some basic action assignments:

S_ACK	The slave device generates the acknowledge (i.e., the CX25874/5)
M_ACK	The serial master generates the acknowledge.
NACK	No acknowledge is generated by either device.
START	Serial start condition; falling edge of SID occurs when SIC is high.
STOP	Serial stop condition; rising edge of SID occurs when SIC is high.
D_ADDR	The device address is 88 hex with ALTADDR = 0, 8A when it is a 1.

- Next, load 46 hex into register 6C. This will write the EN_REG_RD bit to 1. This enables the serial master to readback all encoder registers.

Perform the following transaction with the serial master:

- START/D_ADDR/S_ACK/6C/S_ACK/46/S_ACK/STOP

- Next, use the serial master to write the register address from which read-back will occur:
  - START/D_ADDR/S_ACK/<read_address>/S_ACK/STOP
- Finally, read the data starting at the read_address previously issued:
  - START/D_ADDR+1/S_ACK/<readdata(0)>/M_ACK/<readdata(1)>/M_ACK/<readdata(2)>/M_ACK/.../.../<readdata(n-1)>/M_ACK/<readdata(n)>/ NACK/STOP

where:

readdata(0) is the data from CX25874/5 register <read_address>

readdata(1) is the data from CX25874/5 register <read_address>+1

readdata(2) is the data from CX25874/5 register <read_address>+2

As long as the CX25874/5 detects an acknowledge from the serial master (M_ACK) after providing the readdata, it will expect the read transaction to continue.

When no acknowledge is received, the encoder will end the read operation. Using this approach, consecutive register reads can be provided with less software overhead.

As long as the CX25874/5 detects an acknowledge from the serial master (M_ACK) after providing the read data, it will expect the read transaction to continue.

When no acknowledge is received, the encoder will end the read operation. Using this approach, consecutive register reads can be provided with less software overhead.

To read just one register location, every programming step remains the same up to the point where the read data transaction occurs.

In this case, the master should simply substitute a STOP in place of the M_ACK. The final step of the transaction will therefore be:

- START/D_ADDR + 1/S_ACK/<readdata>/NACK/STOP

Table 2-3 contains the bit map for all of the encoder's read-only registers. Table 2-4 contains the data details. As mentioned previously, to enable full register readback, the EN_REG_RD bit must be set to 1.

Table 2-3. Bit Map for Read-Only Registers

Register Address	7	6	5	4	3	2	1	0
00	ID[2:0]			VERSION[4:0]				
02	MONSTAT_A	MONSTAT_B	MONSTAT_C	CCSTAT_E	CCSTAT_O	FIELD_CNT[2:0]		
04	Reserved	SECAM	PLL_RESET_OUT	PLL_LOCK	FIFO_OVER	FIFO_UNDER	PAL	Reserved
06	MONSTAT_A	MONSTAT_B	MONSTAT_C	MONSTAT_D	FIELD_CNT[3:0]			

Table 2-4. Data Details for All Read-Only Registers

Bit Names	Data Definition
ID[2:0]	Indicates the part number of the Conexant VGA Encoder. The following ID[2:0] is returned.When the Conexant VGA Encoder present is: 000 Bt868 (Buteo, 1st generation encoder, no Macrovision) 001 Bt869 (Buteo, 1st generation encoder, with Macrovision) 010 CX25870 (Accipiter, 2ndgeneration encoder, no Macrovision) 011 CX25871 (Accipiter, 2nd generation encoder, with Macrovision) 100 CX25872 (Aquila Lite, 3rd generation encoder, no Macrovision) 101 CX25873 (Aquila Lite, 3rd generation encoder, with Macrovision) 110 CX25874 (Aquila, 3rd generation encoder, no Macrovision) 111 CX25875 (Aquila, 3rd generation encoder, with Macrovision)
VERSION[4:0]	Version number; for Revision A of the CX25874/875, these bits are all 00000. Revision B is denoted by 00001 of the CX25874/875. Device marking on package is “CX25874/5-12P.” Revision C is denoted by 00010 of the CX25874/875. Device marking on package is “CX25874/5-13P.” Revision D is denoted by 00011 of the CX25874/875. Device marking on package is “CX25874/5-14P.”
MONSTAT_A	Monitor connection status for DACA output, 1 denotes monitor connected to DACA.
MONSTAT_B	Monitor connection status for DACB output, 1 denotes monitor connected to DACB.
MONSTAT_C	Monitor connection status for DACC output, 1 denotes monitor connected to DACC.
MONSTAT_D	Monitor connection status for DACD output, 1 denotes monitor connected to DACD.
CCSTAT_E	High if closed-caption data has been written for the even field; it is low immediately after the clock run-in on the extended service line for the even field.
CCSTAT_O	High if closed-caption data has been written for the odd field; it is low immediately after the clock run-in on the closed caption line for the odd field.
FIELD_CNT[3:0]	Field number, where 0000 indicates the first field, 1111 indicates the 15th field. An extra bit was added to accommodate the SECAM standard.
SECAM	Indicates status of SECAM mode. If the encoder is outputting SECAM, this bit will be set to 1.
PLL_RESET_OUT	PLL reset state.
PLL_LOCK	High when PLL is locked. Will be low if PLL loses lock.
FIFO_OVER	Set to one if FIFO overflows. Reset on read.
FIFO_UNDER	Set to one if FIFO underflows. Reset on read.
PAL	Indicates status of PAL mode. If the encoder is outputting PAL or SECAM, this bit will be set to 1. If the encoder is transmitting NTSC, this bit is set to 0.

2.4 Writing Registers

Following a start condition, writing 0x88 as the device ID initiates write access to the CX25874/875 registers when the ALTADDR pin is low. Alternative device ID 0x8A initiates write access when the ALTADDR pin is high. If the data is written sequentially in subaddress order, only the first subaddress needs to be written; the internal address counter will automatically *increment by two* after each write to the next register.

When writing an entirely new, complete register set to the CX25874/875, make sure to skip register 0xB8. This is the autoconfiguration register, and writing any value to it after having loaded values into other registers will replace desired data with unwanted data in register 38 and register indices 0x76–0xB4.

For read/write register programming details, see Table 2-5. The table is sorted in alphabetical order by bit/register name.

Table 2-5. Programming Details for All Read/Write Registers *(1 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
625LINE	Bit 2–A2	0 = 525-line format (NTSC-M, NTSC-J, PAL-M), 480p HDTV 1 = 625-line format (PAL-BDGHI, PAL-N, PAL-Nc, SECAM, 625p HDTV
ADPT_FF	Bit 7–34	0 = Disable adaptive flicker filter. (DEFAULT) 1 = Enable adaptive flicker filter.
AUTO_CHK	Bit 7–32	It is recommended that this bit only be used while generating NTSC/PAL/SECAM outputs. 0 = Normal operation. (DEFAULT) 1 = The status of the monitor connections will be automatically checked once per frame during the VBI. This bit should not be set for HDTV output modes.
BLANKI	Bit 5–D6	0 = Active low BLANK* pin. (DEFAULT) 1 = Active high BLANK* pin.
BLNK_IGNORE	Bit 4–6C	0 = Use BLANK* pin to indicate the active pixel region in CCIR 656 mode. (DEFAULT) 1 = Use registers H_BLANKI and V_BLANKI to determine the active pixel region in CCIR 656 mode.
BLUEFLD	Bit 4–D6	0 = Normal operation. (DEFAULT) 1 = Generate standard-definition blue field. The encoder does not require any digital input signals (CLKI, P[11]-P[0], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
BPB_SYNC_DIS	Bit 3–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Blue/P_B output or bilevel sync on VGA Blue output. (DEFAULT) 1 = Disables trilevel sync on HDTV Blue/P_B output or bilevel sync on VGA Blue output. This bit will have to be set manually for EIA-770.3 compliance.
BST_AMP[7:0]	Bits [7:0]–A6	Color burst amplitude factor. Each bit adjustment represents 1.25 mV of burst amplitude. This register has no effect on the SECAM DR and DB color burst amplitudes.
BY_PLL	Bit 6–A0	0 = Use on chip PLL (DEFAULT) 1 = Bypass PLL (encoder clock is crystal frequency).

Table 2-5. Programming Details for All Read/Write Registers *(2 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
BY_YCCR	Bit 6–D8	0 = Luma cross color reduction filter on. 1 = Bypass luma cross color reduction filter. Optimal standard-definition quality most often realized with this setting. (DEFAULT)
C_ALTFF[1:0]	Bits [4:3]–34	Chroma alternate flicker filter selection. This bit will only have an effect when ADPT_FF is set. C_ALTFF should always be programmed to a value greater than or equal to F_SELC. 00 = 5 line (DEFAULT) 01 = 2 line 10 = 3 line 11 = 4 line
C_THRESH[2:0]	Bits [5:3]–36	Controls the sensitivity or limit of turning on the alternate flicker filter for chroma in adaptive mode. (DEFAULT = 000)
CATTENUATE[2:0]	Bits [2:0]–CC	Chroma Attenuation. Used for saturation control. 000 = 1.0 gain No Attenuation (DEFAULT) 001 = 15/16 gain 010 = 7/8 gain 011 = 3/4 gain 100 = 1/2 gain 101 = 1/4 gain 110 = 1/8 gain 111 = 0 gain (Force Chroma to 0)
CC_ADD[11:0]	Bits [3:0]–D4 and Bits [7:0]–D2	Closed-captioning DTO increment.
CCF1B1[7:0]	Bits [7:0]–C0	This is the first byte of closed-caption information for the odd field, line 21 for NTSC or line 22 for PAL. Data is encoded LSb first.
CCF1B2[7:0]	Bits [7:0]–C2	This is the second byte of closed-caption information for the odd field, line 21 for NTSC or line 22 for PAL. Data is encoded LSb first.
CCF2B1[7:0]	Bits [7:0]–BC	This is the first byte of closed-caption information for the even field, line 284 for NTSC or line 335 for PAL. Data is encoded LSb first.
CCF2B2[7:0]	Bits [7:0]–BE	This is the second byte of closed-caption information for the even field, line 284 for NTSC or line 335 for PAL. Data is encoded LSb first.
CCORING[2:0]	Bits [5:3]–CC	Chroma Coring. Values below the CCORING[2:0] limit are automatically clamped to a saturation value of 0. 000 = Bypass (DEFAULT) 001 = 1/128 of range (± 1/256 of range) 010 = 1/64 of range (± 1/128 of range) 011 = 1/32 of range (± 1/64 of range) 100 = 1/16 of range (± 1/32 of range) 101 = 1/8 of range (± 1/16 of range) 110 = 1/4 of range (± 1/8 of range) 111 = Reserved

Table 2-5. Programming Details for All Read/Write Registers *(3 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
CCR_START[9] CCR_START[8] CCR_START[7:0]	Bit 7 of D6, Bit 4 of D4, and Bits [7:0] of D0	Closed-captioning clock run-in start in clock cycles from leading edge of HSYNC*. Refer to the closed-captioning (CC) section for more details.
CCSEL[3:0]	Bits [3:0]–5E	Line position of Closed Captioning (CC) Content. Controls which line Closed Captioning (CC) data is encoded. Each line enable is independent. 0001 = Closed Captioning (CC) on line 19 (525-line) and line 21 (625-line) 0010 = Closed Captioning (CC) on line 20 (525-line) and line 22 (625-line) 0100 = Closed Captioning (CC) on line 21 (525-line) and line 23 (625-line) (DEFAULT) 1000 = Closed Captioning (CC) on line 22 (525-line) and line 24 (625-line)
CHECK_STAT	Bit 6–BA	Writing a 1 to this bit checks the status of the monitor connections at the DAC output. This is also automatically performed on any reset condition, including a software reset. This bit is self-clearing.
CHROMA_BW	Bit 7–D8	0 = Normal digital chroma bandwidth. See the figure entitled Digital Chrominance Standard Bandwidth Filter (DEFAULT). 1 = Wide digital chroma bandwidth. See the figure entitled Digital Chrominance Wide Bandwith Filter.
CLPF[1:0]	Bits [7:6]–96	Chroma Post-Flicker Filter/Scaler Horizontal Low-Pass Filter: 00 = Bypass (DEFAULT) 01 = Reserved 10 = Chroma Horizontal LPF2 setting 11 = Chroma Horizontal LPF3 setting

Table 2-5. Programming Details for All Read/Write Registers *(4 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
CONFIG[5:0]	Bits [6:4] and Bits [2:0]–B8	The combination of CONFIG[5:3] and CONFIG[2:0] determines the autoconfiguration mode entered by the CX25874/875 immediately after register 0xB8 is written. Check Appendix C for a list of all register values by autoconfiguration mode. Additional details for each autoconfiguration mode are found in Appendix C as well. Review Section 3.7.2.9 for illustrations of the 640x480, 800x600, and 1024x768 autoconfiguration modes and how they can be used for TV out size control in NTSC or PAL. Review Section 3.7.2.9 for illustrations of the 640x480, 800x600, and 1024x768 autoconfiguration modes.

CONFIG [5:0]	Input Format	Active Resolution	Output	Output Ratio	Mode
000000	= RGB	640x480	NTSC	Overscan = Lower	Mode 0
000001	= RGB	640x480	PAL-BDGHI	Overscan = Standard	Mode 1
000010	= RGB	800x600	NTSC	Overscan = Alternate	Mode 2
000011	= RGB	800x600	PAL-BDGHI	Overscan = Lower	Mode 3
000100	= YCrCb	640x480	NTSC	Overscan = Lower	Mode 4
000101	= YCrCb	640x480	PAL-BDGHI	Overscan = Standard	Mode 5
000110	= YCrCb	800x600	NTSC	Overscan = Alternate	Mode 6
000111	= YCrCb	800x600	PAL-BDGHI	Overscan = Lower	Mode 7
001000	= RGB	640x400	NTSC	Overscan = Standard	Mode 8
001001	= RGB	640x400	PAL-BDGHI	Overscan = Standard	Mode 9
001010	= RGB	1024x768	NTSC	Overscan = Standard	Mode 10
001011	= RGB	1024x768	PAL-BDGHI	Overscan = Standard	Mode 11
001100	= RGB	320x240	NTSC	Pix Double Set = Standard	Mode 12
001101	= RGB	320x240	PAL-BDGHI	Pix Double Set = Standard	Mode 13
001110	= YCrCb	1024x768	NTSC	Overscan = Higher	Mode 14
001111	= YCrCb	1024x768	PAL-BDGHI	Overscan = Higher	Mode 15
010000	= RGB	640X480	NTSC	Overscan = Standard	Mode 16
010001	= RGB	640x480	PAL-BDGHI	Overscan = Lower	Mode 17
010010	= RGB	800x600	NTSC	Overscan = Lower	Mode 18
010011	= RGB	800x600	PAL-BDGHI	Overscan = Standard	Mode 19
010100	= RGB	640X480	PAL-60 (China)	Overscan = Lower	Mode 20
010101	= YCrCb	640x480	PAL-BDGHI	Overscan = Lower	Mode 21
010110	= YCrCb	800x600	NTSC	Overscan = Lower	Mode 22
010111	= YCrCb	800x600	PAL-BDGHI	Overscan = Standard	Mode 23
011000	= RGB	720x400	NTSC	9-dot font for DOS Overscan =Standard	Mode 24
011001	= RGB	720x400	PAL-BDGHI	9-dot font for DOS Overscan =Standard	Mode 25
011010	= RGB	1024x768	NTSC	Overscan = Lower	Mode 26
011011	= RGB	800X600	PAL-60 (China)	Overscan = Lower	Mode 27
011100	= YCrCb	720x480	NTSC	Interlaced Input, Slave Interface Overscan = 0% DIV2 set. EN_XCLK set. CCIR601 timing.	Mode 28

Table 2-5. Programming Details for All Read/Write Registers *(5 of 18)*

<table>
<tr><th>Bit/Register Names</th><th>Bit Location</th><th>Bit/Register Definition</th></tr>
<tr><td>CONFIG[5:0] (cont'd)</td><td>Bits [6:4] and Bits [2:0]–B8</td><td>The combination of CONFIG[5:3] and CONFIG[2:0] determines the autoconfiguration mode entered by the CX25874/875 immediately after register 0xB8 is written. Check Appendix C for a list of all register values and timing parameters for each autoconfiguration mode. Additional details for each autoconfiguration mode are found in Appendix C as well. Review Section 3.7.2.9 for illustrations of the 640x480, 800x600, and 1024x768 autoconfiguration modes and how they can be used for TV out size control in NTSC or PAL.
Review the programmable video adjustment controls-size subsection for illustrations of the 640x480, 800x600, and 1024x768 autoconfiguration modes.
<table>
<tr><th>CONFIG [5:0]</th><th>Input Format</th><th>Active Resolution</th><th>Output</th><th>Output Ratio</th><th>Mode</th></tr>
<tr><td>011101</td><td>= YCrCb</td><td>720x576</td><td>PAL-BDGHI</td><td>Interlaced Input, Slave Interface Overscan = 0% DIV2 set. EN_XCLK set. CCIR601 timing.</td><td>Mode 29</td></tr>
<tr><td>011110</td><td>= YCrCb</td><td>1024x768</td><td>NTSC</td><td>Overscan = Lower</td><td>Mode 30</td></tr>
<tr><td>011111</td><td>= RGB</td><td>720x576</td><td>PAL-BDGHI</td><td>Overscan = ~ 0% Noninterlaced Input for DVD</td><td>Mode 31</td></tr>
<tr><td>100000</td><td>= RGB</td><td>640x480</td><td>NTSC</td><td>Overscan = Higher</td><td>Mode 32</td></tr>
<tr><td>100001</td><td>= RGB</td><td>640x480</td><td>PAL-BDGHI</td><td>Overscan = Higher</td><td>Mode 33</td></tr>
<tr><td>100010</td><td>= RGB</td><td>800x600</td><td>NTSC</td><td>Overscan = Higher</td><td>Mode 34</td></tr>
<tr><td>100011</td><td>= RGB</td><td>800x600</td><td>PAL-BDGHI</td><td>Overscan = Higher</td><td>Mode 35</td></tr>
<tr><td>100100</td><td>= YCrCb</td><td>640x480</td><td>NTSC</td><td>Overscan = Higher</td><td>Mode 36</td></tr>
<tr><td>100101</td><td>= YCrCb</td><td>640x480</td><td>PAL-BDGHI</td><td>Overscan = Higher</td><td>Mode 37</td></tr>
<tr><td>100110</td><td>= YCrCb</td><td>800x600</td><td>NTSC</td><td>Overscan = Higher</td><td>Mode 38</td></tr>
<tr><td>100111</td><td>= YCrCb</td><td>800x600</td><td>PAL-BDGHI</td><td>Overscan = Higher</td><td>Mode 39</td></tr>
<tr><td>101000</td><td>= RGB</td><td>800x600</td><td>NTSC</td><td>Overscan = Standard</td><td>Mode 40</td></tr>
<tr><td>101001</td><td>= RGB</td><td>320x200</td><td>PAL-BDGHI</td><td>Pix Double Set Overscan = Standard</td><td>Mode 41</td></tr>
<tr><td>101010</td><td>= RGB</td><td>1024x768</td><td>NTSC</td><td>Overscan = Higher</td><td>Mode 42</td></tr>
<tr><td>101011</td><td>= RGB</td><td>1024x768</td><td>PAL-BDGHI</td><td>Overscan = Higher</td><td>Mode 43</td></tr>
<tr><td>101100</td><td>= RGB</td><td>720x480</td><td>NTSC</td><td>Noninterlaced Input for DVD Overscan = ~ 0%</td><td>Mode 44</td></tr>
<tr><td>101101</td><td>= RGB</td><td>320x200</td><td>NTSC</td><td>Pix Double Set Overscan = Standard</td><td>Mode 45</td></tr>
<tr><td>101110</td><td>= RGB</td><td>640x480</td><td>PAL-M (Brazil)</td><td>Overscan = Standard</td><td>Mode 46</td></tr>
<tr><td>101111</td><td>= RGB</td><td>640x480</td><td>PAL-Nc (Argentina)</td><td>Overscan = Standard</td><td>Mode 47</td></tr>
</table></td></tr>
<tr><td>CSC_SEL</td><td>Bit 0–32</td><td>0 = Standard color space conversion for RGB to Y (R-Y) (B-Y) based on Y =0 .299R +0 .587G +0 .114 B (DEFAULT)
1 = HDTV color space conversion for RGB to Y (R-Y) (B-Y) based on Y = 0.2126R + 0.7152G + 0.0722B</td></tr>
</table>

Table 2-5. Programming Details for All Read/Write Registers *(6 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
CVBSD_INV	Bit 2–D8	0 = Normal operation. (DEFAULT) 1 = Invert CVBS_DLY output.
DACDISA	Bit 0–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACA output. Current is set to 0 mA; output will go to 0 V.
DACDISB	Bit 1–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACB output. Current is set to 0 mA; output will go to 0 V.
DACDISC	Bit 2–BA	0 = Normal operation. (DEFAULT) 1 = Disables DACC output. Current is set to 0 mA; output will go to 0 V.
DACDISD	Bit 3–BA	0 = Normal Operation. (DEFAULT) 1 = Disables DACD output. Current is set to 0 mA; output will go to 0 V.
DACOFF	Bit 4–BA	0 = Normal operation. (DEFAULT) 1 = Disables DAC output current and internal voltage reference for all DACs. This will limit power consumption to just the internal digital circuitry. DACs cannot be detected while DACs are off.
DATDLY	Bit 7–74	0 = No delay in falling edge pixel data. (DEFAULT) 1 = Delays the falling edge pixel data by 1 full clock period. This bit is used to correct a multiplexed input data sequence that delivers a pixel on a falling edge and the following rising edge (rather than a rising edge and the following falling edge, as expected).
DATDLY_RE	Bit 2–32	0 = No delay in rising edge pixel data. (DEFAULT) 1 = Delays the rising edge pixel data by 1 full clock period. This bit is used together with DATSWP to correct a multiplexed input data sequence that delivers a pixel on a falling edge and the following rising edge with the falling edge and rising edge data swapped.
DATSWP	Bit 6–74	0 = VGA Encoder expects an order of rising edge data/falling edge data coming from the graphics controller (DEFAULT). 1 = Swaps the falling edge pixel data with the rising edge pixel data at the input of the pixel port.
DB_LIMITN[10:8] DB_LIMITN[7:0]	Bits [5:3]–54 and Bits [7:0]–52	Lower bound limit for DB frequency deviation in SECAM. Review SECAM Output Section.
DB_LIMITP[10:8] DB_LIMITP[7:0]	Bits [2:0]–54 and Bits [7:0]–50	Upper bound limit for DB frequency deviation in SECAM. Review SECAM Output Section.
DCHROMA	Bit 1–C4	0 = Normal operation. (DEFAULT) 1 = Disable the chrominance portion of video output. Composite and S-Video outputs appear as gray scale.
DIS_CLKO	Bit 1–30	0 = Enable CLKO output. (DEFAULT) 1 = Three-state CLKO output. This will disable the CLKO output when not needed, i.e., an external clock is used (Slave Interface). Disabling CLKO is also effective in reducing the current draw in SLEEP mode.
DIS_FFILT	Bit 6–C8	0 = Enables Standard Flicker Filter. (DEFAULT) 1 = Disables Standard Flicker Filter.

Table 2-5. Programming Details for All Read/Write Registers *(7 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
DIS_GMSHC	Bit 6–CC	0 = Enables Chroma Pseudo Gamma Removal. (DEFAULT) 1 = Disables Chroma Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMSHY	Bit 6–CA	0 = Enables Luma Pseudo Gamma Removal. (DEFAULT) 1 = Disables Luma Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMUSHC	Bit 7–CC	0 = Enables Chroma Anti-Pseudo Gamma Removal. (DEFAULT) 1 = Disables Chroma Anti-Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_GMUSHY	Bit 7–CA	0 = Enables Luma Anti-Pseudo Gamma Removal. (DEFAULT) 1 = Disables Luma Anti-Pseudo Gamma Removal. Optimal standard-definition quality most often realized with this setting. It is important to set this bit manually.
DIS_PLL	Bit 2–30	0 = PLL enable. (DEFAULT) 1 = PLL disable. In nonsleep mode, if an external clock is being used and the PLL is not needed, this bit will disable the PLL function. ***GENERAL NOTE:*** Some of the special modes are not available when the PLL is disabled.
DIS_SCRST	Bit 4–A2	0 = Normal operation. The subcarrier phase is reset to 0 at the beginning of each color field sequence. (DEFAULT) 1 = Disables subcarrier reset event at beginning of field sequence.
DIS_YLPF	Bit 7–C8	0 = Enable Luma Initial Horizontal Low-Pass filter. (DEFAULT) 1 = Disable Luma Initial Horizontal Low-Pass filter.
DIV2	Bit 6–D4 and Bit 4–38	0 = Normal operation. (DEFAULT) 1 = Divides input pixel rate by two (for any interlaced timing input). Useful for DVD playback resolutions. The DIV2 bit in register D4 was kept for Bt868/869 and CX25870/871 compatibility purposes. The DIV2 bit in register 38 is autoconfigurable. These bit values always mirror each other. Changing the state of one DIV2 register field automatically updates the other DIV2 register field.
DIV2_LATCH	Bit 0–3A	This bit only has an effect when DIV2 = 1. 0 = Data is clocked at rising edge of CLKI. (DEFAULT) 1 = Data is clocked at rising and falling edges of CLKI.
DR_LIMITN[10:8] DR_LIMITN[7:0]	Bits [5:3]–4E and Bits [7:0]–4C	Lower bound limit for DR frequency deviation in SECAM. Review SECAM Output Section.
DR_LIMITP[10:8] DR_LIMITP[7:0]	Bits [2:0]–4E and Bits [7:0]–4A	Upper bound limit for DR frequency deviation in SECAM. Review SECAM Output Section.
E656	Bit 6–D6	0 = Input pixel format defined by IN_MODE[3:0] register. (DEFAULT) 1 = CCIR 656 input on P[7:0] port, or P[11:4] port.
EACTIVE	Bit 2–6C	0 = Black burst. (DEFAULT) 1 = Enable normal video.

Table 2-5. Programming Details for All Read/Write Registers *(8 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
ECBAR	Bit 2–C4	0 = Normal operation. (DEFAULT) 1 = Enable standard-definition color bars. The encoder does not require any digital input signals (CLKI, P[11]-P[0], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
ECCF1(ECC)	Bit 4–C4	0 = Disables closed-caption encoding on field 1. (DEFAULT) 1 = Enables closed-caption encoding on field 1.
ECCF2(EXDS)	Bit 5–C4	0 = Disables closed-caption encoding on field 2. (DEFAULT) 1 = Enables closed-caption encoding on field 2.
ECCGATE	Bit 3–C4	0 = Normal closed-caption encoding. (DEFAULT) 1 = Enables closed-caption encoding constraints. After encoding, future encoding is disabled until a complete pair of new data bytes is received. This prevents encoding of redundant or incomplete data.
ECLIP	Bit 6–A2	0 = Normal operation. (DEFAULT) 1 = Enable clipping; DAC values less than 31 hex are made 31 by the encoder.
EN_BLANKO	Bit 7–C6	Interface bit: Works in conjunction with EN_DOT, EN_OUT, and SLAVE. Controls direction of BLANK* signal. 0 = Enables BLANK* as an input. 1 = Enables BLANK* pin as an output, or no BLANK* signal is utilized in the system interface. (DEFAULT)
EN_DOT	Bit 6–C6	Interface bit: Works in conjunction with EN_BLANKO, EN_OUT, and SLAVE. Controls blanking method. 0 = Encoder uses its internal counters to determine the active-versus-blanked regions of input data. (DEFAULT) 1 = Encoder uses the BLANK* signal being received to determine where active video starts (rising edge by default) and where blanking region starts (falling edge by default).
EN_OUT	Bit 0–C4	Interface bit: Works in conjunction with EN_BLANKO, EN_DOT, and SLAVE. Turns timing outputs on or off. 0 = Three-state (CLKO, HSYNC*, VSYNC*, BLANK* and FIELD) timing outputs. 1 = Allows CLKO and other outputs to be enabled, depending upon EN_BLANKO register bit and the SLAVE bit. (DEFAULT)
EN_REG_RD	Bit 6–6C	0 = Use ESTATUS[1:0] register to select readback status registers. Enable Bt869-like Legacy read-back method. (DEFAULT) 1 = Enable Standard serial register readback of all registers.
EN_SCART	Bit 3–6C	Enables SCART video output for Europe. OUT_MODE[1:0] field must be set to 11 (VGA Mode) and HDTV_EN bit must be set to 0. 0 = Enables VGA mode. DACs will output analog RGB with standard bilevel (-40 IRE) analog syncs (DEFAULT). 1 = Enables SCART output mode. DAC will transmit SCART compatible RGB outputs and a composite video output, which includes an analog sync.
EN_XCLK	Bit 7–A0	0 = Encoder generates pixel clock based on its mode settings and transmits this frequency via the CLKO pin for master and pseudo-master interfaces. (DEFAULT) 1 = Use CLKI pin as pixel clock source. This bit must be set for slave interface.

Table 2-5. Programming Details for All Read/Write Registers *(9 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
ESTATUS[1:0]	Bits [7:6]–C4	Bt868/869 Legacy serial readback status bit selection. Used in conjunction with EN_REG_RD, CHECK_STAT, AUTO_CHK, and MONSTAT_x bits. Review the table entitled ESTATUS Readback Bit Map.
EWSSF1	Bit 6–60	0 = Disable field 1 WSS data. (DEFAULT) 1 = Enable field 1 WSS data.
EWSSF2	Bit 7–60	0 = Disable field 2 WSS data. (DEFAULT) 1 = Enable field 2 WSS data (only applicable to 525 line standard-definition and 1080i high-definition outputs only).
F_SELC[2:0]	Bits [5:3]–C8	Chroma Standard Flicker Filter: 000 = 5-Line (DEFAULT): most aggressive setting 001 = 2-Line: least aggressive setting 010 = 3-Line 011 = 4-Line 100 = Alternate 5-Line 101 = Alternate 5-Line 110 = Alternate 5-Line 111 = Alternate 5-Line
F_SELY[2:0]	Bits [2:0]–C8	Luma Standard Flicker Filter: 000 = 5-Line (DEFAULT): most aggressive setting 001 = 2-Line: least aggressive setting 010 = 3-Line 011 = 4-Line 100 = Alternate 5-Line 101 = Alternate 5-Line 110 = Alternate 5-Line 111 = Alternate 5-Line
FFCBAR	Bit 5–6C	0 = Normal operation. (DEFAULT) 1 = Enable high-definition or standard-definition flicker filtered color bars. The encoder does not require any digital input signals (CLKI, P[11]-P[0], HSYNC*, VSYNC*, BLANK*) to generate SDTV color bars. If the encoder is receiving a proper power supply and ground it will be able to transmit this pattern from memory.
FFRTN	Bit 7–36	Alternate flicker filter detect and select. This bit is effective only when ADPT_FF = 1. 0 = Once the adaptive algorithm selects the alternate filter, use that filter's coefficients for the rest of the samples for that line. For example, the sequence could be STD/STD/ALT/ALT/ALT; (DEFAULT) 1 = Once the adaptive algorithm selects the alternate filter, use the filter's coefficients for that sample only. For example, the sequence with FFRTN=1 could be STD/STD/ALT/STD/STD.
FIELD_ID	Bit 3–D8	0 = Suppress the SECAM field synchronization signal. (DEFAULT) 1 = Enable the SECAM field synchronization signal (bottle-neck pulses).
FIELDI	Bit 5–C6	0 = Logical 1 from the FIELD pin indicates an even field is being output. (DEFAULT) 1 = Logical 1 from the FIELD pin indicates an odd field is being output.

Table 2-5. Programming Details for All Read/Write Registers *(10 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
FILFSCONV[5:0]	Bits [5:0]–58	Adjust SECAM high-frequency pre-emphasis filter according to the clock frequency. Review the SECAM Output section for the correct equations.
FIL4286INCR[7:0]	Bits [7:0]–56	Adds a phase offset to the UV digital components. Review the SECAM Output section for the correct equations.
FLD_MODE[1:0]	Bits [1:0]–6C	CX25874/875 uses this bit to interpret HSYNC* and VSYNC* edges and field detection in slave mode. 00 = A leading edge of VSYNC* that occurs within ±1/4 of HCLKI from the leading edge of HSYNC* indicates the beginning of odd field. A leading edge of VSYNC* that occurs within ±1/4 of HCLKI from the center of the line indicates the beginning of even field. 01 = A leading edge of VSYNC* occurs during HSYNC* active indicates the beginning of odd field. A leading edge of VSYNC* occurs during HSYNC* inactive indicates the beginning of even field. 10 = A leading edge of VSYNC* coincides with the leading edge of HSYNC* indicates the beginning of odd field. A leading edge of VSYNC* does not coincide with the leading edge of HSYNC* indicated the beginning of even field. (DEFAULT) 11 = Reserved.
FM	Bit 7–A2	This bit must be enabled for a valid SECAM video output. 0 = QAM color encoding (NTSC/PAL). (DEFAULT) 1 = FM color encoding (SECAM).
GY_SYNC_DIS	Bit 4–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Green/Y output or bilevel sync on VGA G output. (DEFAULT) 1 = Disables trilevel sync on HDTV Green/Y output or bilevel sync on VGA G output.
H_ACTIVE[10:8] H_ACTIVE[7:0]	Bits [6:4]–86 and Bits [7:0]–78	Number of active input and output pixels.
H_BLANKI[9] H_BLANKI[8] H_BLANKI[7:0]	Bit 0–38, Bit 3–8E, and Bits [7:0]–8C	Number of CLKI clock cycles between the digital HSYNC* leading edge and first active pixel.
H_BLANKO[9:8] H_BLANKO[7:0]	Bits [7:6]–9A and Bits [7:0]–80	Number of CLKO clock cycles between leading edge of analog horizontal sync and active video.
H_CLKI[10:8] H_CLKI[7:0]	Bits [2:0]–8E and Bits [7:0]–8A	Number of CLKI clock cycles between consecutive leading edges of the digital HSYNC* signal.
H_CLKO[11:8] H_CLKO[7:0]	Bits [3:0]–86 and Bits [7:0]–76	Number of CLKO clock cycles per analog line.
H_FRACT[7:0]	Bits [7:0]–88	Fractional number of input clocks per line. No effect if 00.
HALF_CLKO	Bit 3–3A	0 = Normal operation. (DEFAULT) 1 = CLKO (clock output) frequency divided by 2 while being transmitted.
HBURST_BEGIN[8] HBURST_BEGIN [7:0]	Bit 2–38 and Bits [7:0]–7C	This register contains the number of CLKO clock cycles between the analog horizontal sync falling edge and the 50% point of the first colorburst cycle.

Table 2-5. Programming Details for All Read/Write Registers *(11 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
HBURST_END[8] HBURST_END[7:0]	Bit 3–38 and Bits [7:0]–7E	This register contains the number of CLKO clock cycles minus 128 between the analog horizontal sync falling edge and the 50% point of the last colorburst cycle. Make sure to subtract 128 CLKO clock cycles from the calculated 50% point of the last colorburst cycle value and load into this register.
HD_SYNC_EDGE	Bit 2–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1 and RASTER_SEL is nonzero. 0 = Trilevel sync edges transition time is equal to 4 input clocks. (DEFAULT) 1 = Trilevel sync edges transition time is equal to 2 input clocks.
HDTV_EN	Bit 7–2E	Enable HDTV output mode, OUT_MODE[1:0] register bits must be set to 11 (VGA mode) and EN_SCART must = 0. 0 = Enables VGA mode. DACs will output analog RGB with standard bilevel (-40 IRE) analog syncs. See Section 1.3.49 for details. (DEFAULT) 1 = Enables HDTV output mode. DACs will output HDTV compatible RGB or component video (Y/ P_R/ P_B) outputs. Trilevel syncs and vertical synchronizing/broad pulses will be inserted automatically if RASTER_SEL[1:0] = nonzero. ***GENERAL NOTE:*** The EN_SCART bit must be 0 for HDTV Output Mode to be functional.
HSYNC_WIDTH [7:0]	Bits [7:0]–7A	Analog horizontal sync width in number of CLKO clock cycles.
HSYNCI	Bit 3–C6	0 = Configures the encoder to send/receive an active low HSYNC* digital signal (DEFAULT) 1 = Configures the encoder to send/receive an active high HSYNC* digital signal.
HSYNOFFSET[9:8] HSYNOFFSET[7:0]	Bits [7:6]–70 and Bits [7:0]–6E	A 2s-complement number. The values range from –512 pixels to +511 pixels. This register manipulates the falling edge position of the digital HSYNC* output from the CX25874/875. The default value is 0 and denotes the standard position of the HSYNC* leading edge. This register is only effective in master interface. (DEFAULT = 0x00)
HSYNWIDTH[5:0]	Bits [5:0]–70	Controls the duration/width of the digital HSYNC output pulse. Value will be hexadecimal and its units are in terms of pixels. A value of 0 is a disallowed condition. The acceptable range is 0x02 pixels to 0x3F pixels (=63 decimal). The default value is 0x02. Never set to 0. This register is only effective in master interface. (DEFAULT = 0x02)
HUE_ADJ[7:0]	Bits [7:0]–5C	This register controls the color hue. It does this by adjusting the color subcarrier phase during the video active region. Increasing this value by 1 unit has the effect of increasing the phase by (360/256) = 1.406 degrees. (DEFAULT = 0x00)

Table 2-5. Programming Details for All Read/Write Registers *(12 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
IN_MODE[3] and IN_MODE[2:0]	Bit 3–32 and Bits [2:0]–C6	This bit is used in conjunction with IN_MODE[2:0] to configure the encoder to receive a desired input pixel format. Format of input pixels when IN_MODE[3] = 0 (MSb of this 4-bit sequence): 0000 = 24-bit RGB multiplexed 0001 = 16-bit RGB multiplexed 0010 = 15-bit RGB multiplexed 0011 = Reserved 0100 = 24-bit YCrCb multiplexed 0101 = 16-bit YCrCb multiplexed 0110 = Alternate 16-bit YCrCb multiplexed 0111 = Reserved Format of input pixels when IN_MODE[3] = 1(MSb of this 4-bit sequence): 1000 = Alternate 24-bit RGB multiplexed 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Alternate 24-bit YCrCb multiplexed 1101 = Reserved 1110 = Reserved 1111 = Reserved See Table 1-2 for data/pin assignments for desired input pixel format.
LUMADLY[1:0]	Bits [1:0]–D6	Used to program the luminance delay in pixels for the CVBS_DLY and Y_DLY output modes. This binary number provides for a delay of up to three pixels in time. 00 = No delay (DEFAULT) 01 = 1 pixel 10 = 2 pixels 11 = 3 pixels
MCB[7:0]	Bits [7:0]–AA	Multiplication factor for Cb (or B-Y) component prior to subcarrier modulation.
MCOMPU[7:0]	Bits [7:0]–3E	Multiplication factor for component video U output. Value 0x80 (DEFAULT) represents 1.0 scale factor.
MCOMPV[7:0]	Bits [7:0]–40	Multiplication factor for component video V output. Value 0x80 (DEFAULT) represents 1.0 scale factor.
MCOMPY[7:0]	Bits [7:0]–3C	Multiplication factor for component video Y output. Value 0x80 (DEFAULT) represents 1.0. scale factor.
MCR[7:0]	Bits [7:0]–A8	Multiplication factor for Cr (or R-Y) component prior to subcarrier modulation.
MODE2X	Bit 7–D4	0 = Normal operation (DEFAULT). 1 = Divides selected input clock by two (allows for single edge rather than double-edge clock input for pixel latching) for noninterlaced type of data and timing inputs.
MSC[31:0]	Bits [7:0]–B4, B2, B0, AE	Subcarrier increment.

Table 2-5. Programming Details for All Read/Write Registers *(13 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
MSC_DB[31:0]	Bits [7:0]–48,–46, –44, –42	Subcarrier increment for Db component of SECAM. MSC_DB = int ((272/H_CLKO) * 2^{32} + 0.5)
MY[7:0]	Bits [7:0]–AC	Multiplication factor for Luma component. Controls adjustment of contrast.
NI_OUT	Bit 0–A2	0 = Interlaced analog video output. (DEFAULT) 1 = Noninterlaced analog video output. Odd (first) field is always transmitted.
OFFSET_RGB	Bit 1–32	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Standard RGB digital input. Range is 0 – 255 decimal. (DEFAULT) 1 = HDTV OFFSET RGB digital input. Range is 16 – 235 decimal.
OUT_MODE[1:0]	Bits [3:2]–D6	00 = Video[0] = Composite (CVBS), Video[1] = Luminance (Y), Video[2] = Chrominance (C), Video[3] = Luma_Delay (Y_DLY). Routing of Video [0] – [3] from DACs controlled with OUT_MUXx bit fields. (DEFAULT) 01 = Video[0–3] is CVBS_DLY/ Y/ C/ Y_DLY. Rarely used. 10 = Video[0–3] is V/ Y/ U/ Y_DLY. Consult the YCRCB 480i (YUV) Standard-Definition Component Video Outputs section for more programming detail. 11 = Video[0–3] is VGA (RGB/x), SCART (R/G/B/Composite), or HDTV output mode. Consult the SCART Output, VGA (RGB)-DAC Output, and HDTV Appendix E sections for more programming detail.
OUT_MUXA[1:0]	Bits [1:0]–CE	00 = Output Video[0] on DACA (DEFAULT = Composite [CVBS]) 01 = Output Video[1] on DACA 10 = Output Video[2] on DACA 11 = Output Video[3] on DACA
OUT_MUXB[1:0]	Bits [3:2]–CE	00 = Output Video[0] on DACB 01 = Output Video[1] on DACB (DEFAULT = Luminance (Y) 10 = Output Video[2] on DACB 11 = Output Video[3] on DACB
OUT_MUXC[1:0]	Bits [5:4]–CE	00 = Output Video[0] on DACC 01 = Output Video[1] on DACC 10 = Output Video[2] on DACC (DEFAULT = Chrominance) 11 = Output Video[3] on DACC
OUT_MUXD[1:0]	Bits [7:6]–CE	00 = Output Video[0] on DACD 01 = Output Video[1] on DACD 10 = Output Video[2] on DACD 11 = Output Video[3] on DACD (DEFAULT = Luma Delay [Y_DLY])
PAL_MD	Bit 5–A2	Video output switch bit after power-up. 0 = Disable phase alternation (NTSC and SECAM). (DEFAULT) 1 = Enable phase alternation (PAL).
PHASE_OFF[7:0]	Bits [7:0]–B6	Subcarrier phase offset. SCH Phase increased by 1.406 degrees per bit increment. This register is 2s complement in nature (DEFAULT = 00).

Table 2-5. Programming Details for All Read/Write Registers *(14 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
PIX_DOUBLE	Bit 6–38	Low resolution pixel doubling bit. 0 = Encoder accepts each pixel input individually and processes it. (DEFAULT) 1 = Encoder replicates/copies each input pixel received. This bit is automatically set for autoconfiguration modes #12, #13, #41, and #45.
PKFIL_SEL[1:0]	Bits [5:4]–D8	Text sharpening filter. Also referred to as the luma peaking filter selection (Refer to Section 1.3.39 and Figures 1-37 through 1-40 for details). 00 = Bypass (DEFAULT) 01 = Filter 1 (1 dB gain) 10 = Filter 2 (2 dB gain) 11 = Filter 3 (3.5 dB gain)
PLL_32CLK	Bit 5–38	Use this bit primarily to support the 1024 x 768 resolution and additional 800 x 600 overscan options. For more details, review the 3:2 Clocking Mode section. 0 = Use PLL 3x pixel clock output. (DEFAULT) 1 = Use PLL generated 2x pixel clock to run the encoder and output timing section. Use PLL generated 3x pixel clock to run the flicker filter. The 3x pixel clock will be output from the CLKO pin during either state of this bit.
PLL_FRACT[15:0]	Bits [7:0]–9E, –9C	Fractional portion of PLL multiplier.
PLL_INPUT	Bit 1–3A	0 = PLL uses the crystal or oscillator between XTALIN and XTALOUT pins to generate the CLKO programmed frequency. (DEFAULT) 1 = PLL uses {CLKI / 2} as the reference for the PLL.
PLL_INT[5:0]	Bits [5:0]–A0	Integer portion of PLL multiplier.
PLL_KEEP_ALIVE	Bit 4–30	0 = Normal operation. (DEFAULT) 1 = Keeps PLL enabled during the sleep mode. This bit is overwritten by DIS_PLL. If the PLL is used to provide a system clock, this bit keeps it functioning if the rest of the chip is slept through either the sleep pin or sleep bit. This bit has no affect if DIS_PLL is set.
PROG_SC	Bit 0–D8	SECAM subcarrier control bit. PROG_SC only has an effect when FM bit is set. 0 = SECAM subcarrier is generated on lines 23–310 and 336–623. (DEFAULT) 1 = SECAM subcarrier is generated on the active lines defined by V_BLANKO[7:0] and V_ACTIVEO[8:0].
RAND_EN	Bit 7–3A	0 = Disable DAC randomizer (DEFAULT) 1 = Enable DAC randomizer to change linearity and yield potentially better TV out quality
RASTER_SEL[1:0]	Bits [1:0]–2E	This bit is only effective when HDTV_EN = 1, and OUT_MODE[1:0] = 11 00 = Device does not generate trilevel sync automatically in HDTV output mode. Trilevel sync periods dictated by active HSYNC* input signal (as HIGHSYNC) and active VSYNC* input signal (as LOWSYNC). This selection must be used to support the 625p (576p) format. (DEFAULT) 01 = Trilevel sync, broad pulse, and timing generation for 480p format. 10 = Trilevel sync, broad pulse, and timing generation for 720p format. 11 = Trilevel sync, broad pulse, and timing generation for 1080i format.
REGFSCONV[5:0]	Bits [5:0]–58	Works in conjunction with FIL_4286INCR[7:0] to set gain on UV digital component. Review the SECAM output section for the correct equations.

Table 2-5. Programming Details for All Read/Write Registers *(15 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
Reserved	Various	Reserved for future software compatibility; should be set to 0 for normal operation.
RGB2YPRPB	Bit 6–2E	HDTV output switching bit. This bit is only effective when HDTV_EN = 1, OUT_MODE[1:0] = 11, RASTER_SEL[1:0] = nonzero, and IN_MODE[3:0] = a RGB input format. 0 = Digital RGB Input to HDTV RGB output. (DEFAULT) 1 = Digital RGB Input to HDTV YP_RP_B output.
RPR_SYNC_DIS	Bit 5–2E	This bit is only effective when OUT_MODE[1:0] = 11, HDTV_EN = 1, and RASTER_SEL is nonzero. 0 = Enables trilevel sync on HDTV Red/P_R output or bilevel sync on VGA R output. (DEFAULT) 1 = Disables trilevel sync on HDTV Red/P_R output or bilevel sync on VGA R output. This bit will have to be set manually for EIA-770.3 compliance.
SC_PATTERN	Bit 1–D8	SECAM phase sequence. SC_PATTERN only has an effect when FM bit is set. 0 = 0° 0° 180° 0° 0° 180° SECAM subcarrier phase sequence. (DEFAULT) 1 = 0° 0° 0° 180° 180° 180° SECAM subcarrier phase sequence.
SERIALTEST[7:0]	Bits [7:0]–28	Use this register for testing the write and read ability of the serial master. A consecutive write and read sequence will return the original value. (DEFAULT = 0x00).
SETUP	Bit 1–A2	0 = Setup off. The 7.5 IRE pedestal setup is disabled for active video lines (NTSC-J, PAL-B, PAL-D, PAL-G, PAL-H, PAL-I, PAL-Nc, and SECAM). 1 = Setup on. The 7.5 IRE pedestal setup is enabled for active video lines (NTSC-M, PAL-M, and PAL-N). (DEFAULT)
SLAVE	Bit 5–BA	Interface bit: Works in conjunction with EN_BLANKO, EN_DOT, and EN_OUT bits. Controls whether the interface will be timing Master or timing Slave. 0 = Configures encoder as the timing master. HSYNC* and VSYNC* will be transmitted as outputs when this bit or a combination of this bit and SLAVE pin is 0. 1 = Configures encoder as the timing slave (pseudo-master or slave interface). HSYNC* and VSYNC* will be received as inputs when this bit is 1. (DEFAULT)
SLEEP_EN	Bit 7–30	0 = Normal operation. (DEFAULT) 1 = Enables sleep state. Shuts down all internal clocks except the serial port interface clock. Disables all digital I/O pins except: SLEEP, ALTADDR, CLKI, CLKO, and XTALOUT. Disables the PLL. Turns off all DACs and VREF. SLEEP and RESET* pins are never disabled.
SRESET	Bit 7–BA	0 = Normal Operation. (DEFAULT) 1 = Setting this bit performs a software reset. All registers are reset to their default state, which is 640x480 in, NTSC out, autoconfiguration mode #0. This bit is automatically cleared.
SYNC_AMP[7:0]	Bits [7:0]–A4	Multiplication factor for controlling the analog sync amplitude. SYNC_AMP + 1 LSb (least significant bit) = +1.25 mV increase in the analog sync amplitude.
TIMING_RST	Bit 7–6C	0 = Normal Operation. (DEFAULT) 1 = Enable timing reset. Resets timing and pixel counters to 1 This bit is automatically cleared. The designer should wait a minimum of 1 ms, after the last register write before enabling TIMING_RST.

Table 2-5. Programming Details for All Read/Write Registers *(16 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
V_ACTIVEI[9:8] V_ACTIVEI[7:0]	Bits [3:2]–96 and Bits [7:0]–94	Number of active input lines.
V_ACTIVEO[8] V_ACTIVEO[7:0]	Bit 7–86 and Bits [7:0]–84	Number of active output lines/field.
V_BLANKI[7:0]	Bits [7:0]–92	Number of input lines between VSYNC* leading edge and first active line.
V_BLANKO[7:0]	Bits [7:0]–82	Line number of first active output line (number of blank lines + 1).
V_LINESI[10] V_LINESI[9:8] V_LINESI[7:0]	Bit 1–38, Bits [1:0]–96, Bits [7:0]–90	Number of vertical input lines. This register value must match the graphic controller's VTOTAL register for a new overscan ratio.
V_SCALE[13:8] V_SCALE[7:0]	Bits [5:0]–9A and Bits [7:0]–98	Vertical scaling coefficient. VSR = V_ACTIVEI / (ALO * [1 – VOC]) V_SCALE[13:0] = (int) ((VSR – 1) * 2^{12})
VBLANKDLY	Bit 4–8E	0 = Normal operation. (DEFAULT) 1 = The effective vertical blanking value in the second field is V_BLANKI+1. Commonly used in CCIR601 input. No effect if 0.
VSYNC_DUR	Bit 3–A2	0 = Generates 2.5-line VSYNC analog output (found in equalization and serration pulse region). Common for most PAL and SECAM formats. 1 = Generates 3 line VSYNC analog output (found in equalization and serration pulse region). Common for all NTSC, PAL-N, PAL-M, and PAL-60 formats. (DEFAULT)
VSYNCI	Bit 4–C6	0 = CX25874/875 transmits or receives active digital low VSYNC*. (DEFAULT) 1 = CX25874/875 transmits or receives active digital high VSYNC*.
VSYNWIDTH[2:0]	Bits [2:0]–74	Controls the width of the VSYNC* output pulse. Denotes the number of lines the VSYNC* digital signal remains low on field transitions. Value will be hexadecimal and its units are in terms of lines. A value of 0 is a disallowed condition. The acceptable range is 1 line to (2^3 –1) lines. The default value is 1. Never set to 0. This register is only effective in master interface.
WSSDAT[20:1]	Bits [7:0]–64, –62, and Bits [3:0]–60	Wide screen signaling (WSS) data bits. Review WSS section for more details.
WSSINC[19:0]	Bits [3:0]–6A and Bits [7:0]–68,–66	WSS DTO increment bits. Review WSS section for more details.
XDSSEL[3:0]	Bits [7:4]–5E	Line position of Extended Data Services (XDS) Content. Controls which line contains Extended Data Services data. Each line enable is independent of the other. 0001 = Extended Data Services on line 282 (525-line) and line 333 (625-line). 0010 = Extended Data Services on line 283 (525-line) and line 334 (625-line). 0100 = Extended Data Services on line 284 (525-line) and line 335 (625-line). (DEFAULT) 1000 = Extended Data Services on line 285 (525-line) and line 336 (625-line).

Table 2-5. Programming Details for All Read/Write Registers *(17 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
XTL_BFO_DIS	Bit 5–30	On power-up, a 50% duty cycle buffered output will be transmitted at the frequency found between the XTALIN and XTALOUT ports from the XTL_BFO pin #3. 0 = Enable buffer crystal clock output. [DEFAULT] 1 = Disable buffer crystal clock output.
XTAL_PAD_DIS	Bit 6–30	0 = Normal operation. (DEFAULT) 1 = Disable XTALIN and XTALOUT crystal pin. Encoder must receive main clock through CLKI pin.
Y_ALTFF[1:0]	Bits [1:0]–34	Luma alternate flicker filter selection. This bit will only have an effect when ADPT_FF is set. Y_ALTFF should always be programmed to a value greater than or equal to F_SELY. 00 = 5 line (DEFAULT) 01 = 2 line 10 = 3 line 11 = 4 line
Y_OFF[7:0]	Bits [7:0]–5A	Brightness control. This is the luminance level offset. Expressed as a 2s complement number. (DEFAULT = 0x00) The luminance level offset is referenced from black, and can be adjusted from -22.31 IRE (below black) to +22.14 IRE (above black). Active video will be added to the offset level. Y_OFF is a 2s complement number, such that 0x00 = 0 IRE offset 0x7 is +22.14 IRE offset and 0x8 is –22.31 IRE offset. 1 lsb = 1.25 mV or 175 IRE of adjustment.
Y_THRESH[2:0]	Bits [2:0]–36	Controls the sensitivity or limit of turning on the alternate flicker filter for luma in adaptive flicker filter mode. (DEFAULT = 000)
YATTENUATE[2:0]	Bits [2:0]–CA	Works in conjunction with register MY for contrast control. This bit field adjusts Luma Attenuation in discrete steps. 000 = 1.0 gain (no attenuation) (DEFAULT) 001 = 15/16 gain 010 = 7/8 gain 011 = 3/4 gain 100 = 1/2 gain 101 = 1/4 gain 110 = 1/8 gain 111 = 0 gain (Force Luma to 0)
YC2YP	Bits 7–26	0 = Normal operation (DEFAULT) 1 = Converts YCrCb digital color space to YPrPb color space. This bit should only be set when outputting HDTV analog YP_RP_B based on a YCrCb input format.
YCORING[2:0]	Bits [5:3]–CA	Luma Coring. These bits control the black level coring limit. Values below the YCORING[2:0] limits that follow are automatically clamped to pure black by the encoder. 000 = Bypass (DEFAULT) 001 = 1/128 of range 010 = 1/64 of range 011 = 1/32 of range 100 = 1/16 of range 101 = 1/8 of range 110 = 1/4 of range 111 = Reserved

Table 2-5. Programming Details for All Read/Write Registers *(18 of 18)*

Bit/Register Names	Bit Location	Bit/Register Definition
YLPF[1:0]	Bits [5:4]–96	Luma Post-Flicker Filter/Scaler Horizontal Low-Pass Filter: 00 = Bypass (DEFAULT) 01 = Luma Horizontal LPF1 setting 10 = Luma Horizontal LPF2 setting 11 = Luma Horizontal LPF3 setting
YSELECT	Bit 6–36	This bit will only have an effect when ADPT_FF is set. 0 = Use the C_THRESH value to determine the threshold for turning on the alternate flicker filter setting for chrominance. (DEFAULT) 1 = Use the Y_THRESH value to determine the threshold for turning on the alternate flicker filter setting for chrominance. Both chroma and luma digital data is automatically processed with their alternate flicker filter settings when the Y_THRESH limit is exceeded.

3 PC Board Considerations

For optimum performance of the Conexant Encoder, proper CMOS layout techniques should be studied before PC board layout is begun.

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA (or VDD) and GND (or VSS) pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals, and layers 2 and 3 for ground and power, respectively.

3.1 Component Placement

Components should be placed as close as possible to the associated pin in order for traces to be connected point to point. The optimum layout places the CX25874/875 as close as possible to the power supply connector and the video output connector, as illustrated in Figure 3-1.

Some other PC board layout tips to follow are:

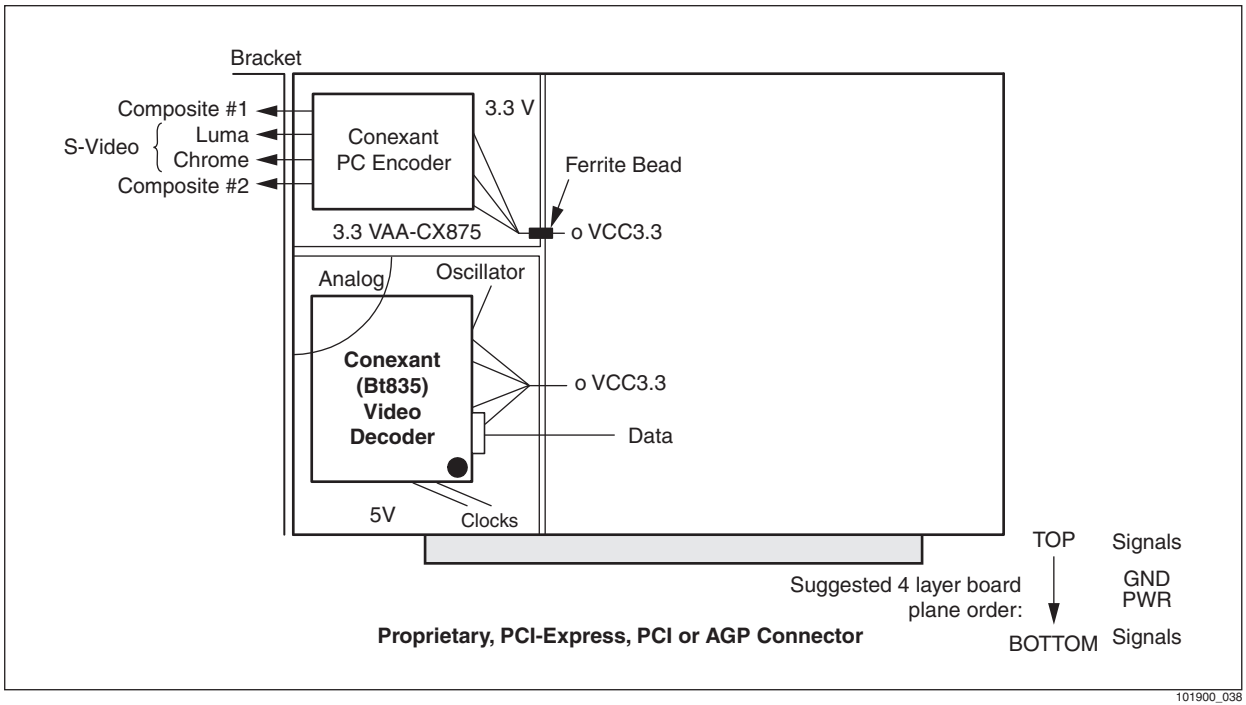
- Include a silk screen layer of labels in your layout artwork showing each component and its reference designation. Label numbered test nodes and the correct polarity of diodes and electrolytic capacitors.
- Leave adequate space around components so ESD transients only have minimally adverse effects on ICs.
- Make sure signals that need access for troubleshooting or analysis are easy to find and probe.
- Keep trace lengths as short as possible.
- Avoid redundant signal vias.
- Avoid indirect routing or S-routing. This adds to EMI and degrades signal quality.
- Include a 33 Ω series resistor on each digital input signal line exceeding 1 MHz in switching speed and possessing a 3.3 V signal switch. Use an 18 Ω resistor if peak-to-peak signal level is less than 2.0 V. FF DENC inputs meeting this criteria are P[11:0] and CLKI. The DENC output falling into this category is CLKO. Place series termination as close to the source (transmitting) device. A reduction in signal ringing and noise is the beneficial result of series termination.

3.2 Power and Ground Planes

For optimum performance, a common digital and analog ground plane and a common digital and analog power plane are recommended. The power plane should provide power to all CX25874/875 power pins, reference voltage (VREF) circuitry, PLL compensation (PLL COMP), and COMP decoupling.

The CX25874/875 power plane should be connected to the graphics system power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 3-1 and 3-2. This bead should be located within 3 inches of the encoder. The bead provides resistance to switching currents by acting as a resistor at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001. For a typical parts list of key passive components and a parts list of other typically used components, see Section 3.3. For recommended schematics and layout to use when designing the CX25874/5, see Section 3.4.

Figure 3-1. Power Plane Illustration

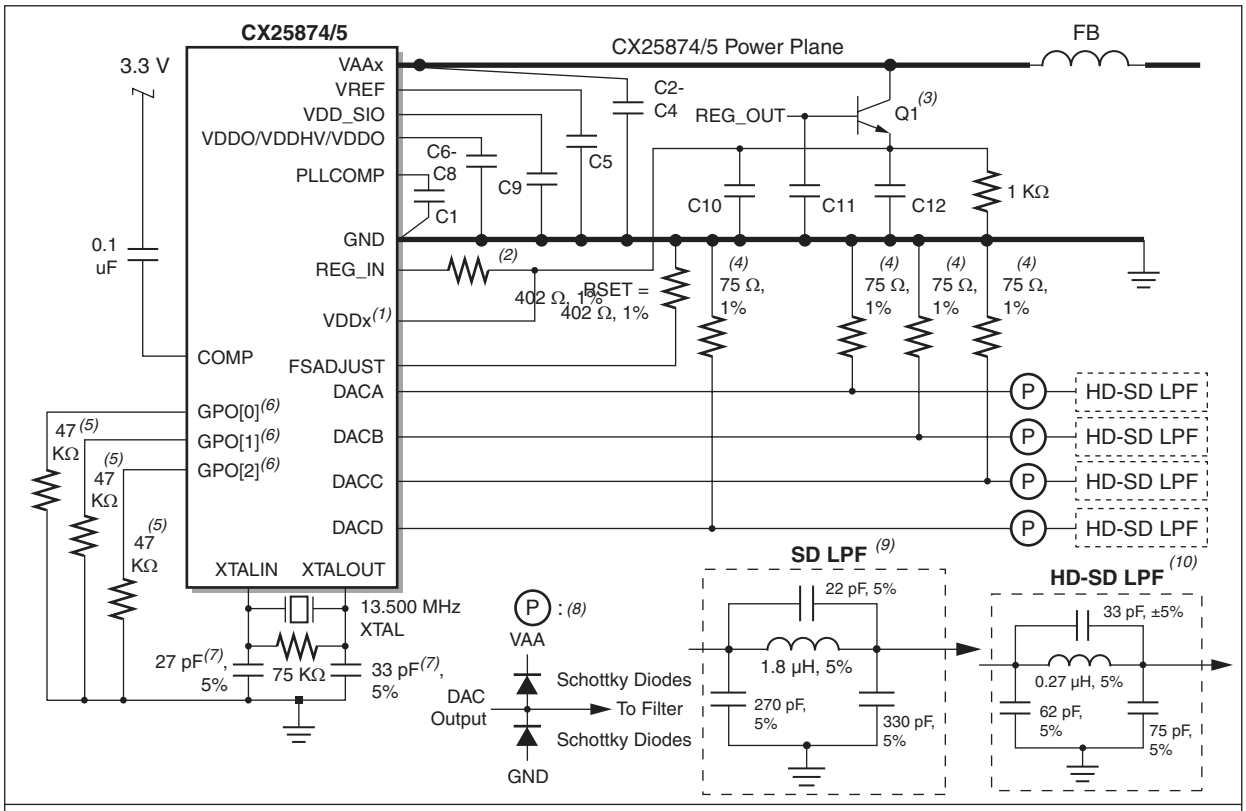


All ground pins of the Conexant encoder should connect to a common ground plane to provide a low-impedance return path for the supply currents. Wherever possible, each ground pin should be connected directly to the ground lead of the closest decoupling capacitor. Short and wide traces should be used to minimize the lead inductance.

3.3 Key Passive Components and Output Filters

Figure 3-2 illustrates the key passive components that should be integrated into all designs incorporating the CX25874/5 encoder. Please pay special attention to the *General Notes* and *Footnotes* in Figure 3-2. Table 3-1 contains parametric and ordering information for the BJT transistor, ferrite bead, capacitors, Shottky diode, resistors, crystal, and inductors illustrated in Figure 3-2. Table 3-2 provides a recommended parts list for other typically used components. Figure 3-3 exhibits the frequency response of the Standard-Definition (SD) low-pass filter. The passband of this filter will typically be DC to 8 MHz. Figure 3-4 exhibits the frequency response of the High-Definition/Standard-Definition (HD-SD) low-pass filter. The passband of this filter will typically be DC to 30 MHz.

Figure 3-2. Connection Diagram for Output Filters and Other Key Passive Components/SDTV and HDTV Out Only



GENERAL NOTES:

1. No RF Modulation has been included within any of the DAC outputs. Baseband video is always generated by the CX25874/5.
2. The HD-SD LPF imparts a passband of DC – 30 MHz whenever used.
3. The SD (Standard Definition) LPF imparts a passband of DC – 8 MHz whenever used.

FOOTNOTES:

(1) Both VDDO pins (#36 and #11) must also be tied to the low voltage power supply if a sub 3.3 V interface with the graphics controller (or data master) is required. See Figure 3-6 for an illustration.

(2) This resistor is not necessary for the CX25874/5-13P, -14P (Revisions C and D) encoders. CX25874/5-12P (Revision B) requires inclusion of this resistor. Revision D will return 00011 from the VERSION[4:0] field when register address 0x00 is read.

(3) Worst case power being dissipated by this BJT npn transistor in the active region (driving the encoder core) is 90 mW. This transistor should be rated for at least 200 mW in applications using the CX25874/5.

(4) The series termination resistors should be placed as close to the CX25874/5 as possible.

(5) Inclusion of these resistors allows for a direct substitution of CX25874/5 with the CX25872/3.

(6) If GPO[0-2] unused, connect to GND in manner shown.

(7) Depending on the parasitic capacitance of your PCB and loading expectations of your crystals, these capacitor values may change slightly. Generally, the 27 pF and 33 pF combination matches a 20 pF internal XTAL load.

(8) The input protection Schottky Diodes ((P)) should be placed as close to the CX25874/5 as possible.

(9) This low-pass filter network should be placed as close as possible to the RCA, S-Video, or other output connector to reduce EMI emissions. This network can replace the HD-SD LPF if a passband of DC-30 MHz is desired. This filter's frequency response is illustrated in Figure 3-3.

(10) This low-pass filter network should be placed as close as possible to the RCA, S-Video, or other output connector to reduce EMI emissions. This network can replace the SD-LPF if a passband of DC-30 MHz is desired. This filter's frequency response is illustrated in Figure 3-4.

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***Table 3-1. Recommended Parts List for Key Active and Passive Components in Figure 3-2** (1 of 2)*

Reference Part Number from Figure 3-2	Part Value	Required Tolerance	Dielectric	Pic Spec	Recommended Vendor(1)	Vendor Part Number(2)	PCB Footprint(3)
C1, C10	1.0 µF	+80%, –20%	Y5V	5404R51–002	Murata	GRM39Y5V105Z010	0603
C2–C4, C5, C9, C11–C12	0.1 µF	20%	X7R	5404R24-037	AVX	0603YC104MATMA	0603
	0.1 µF	10%	X7R	N/A	Anchor	CAP0.1UFSMT-0603	0603
C6–C8	0.01 µF	20%	—	—	—	—	SOT-23
P–Schottky Diode	BAT54S	—	—	5443R10-004	Philips	BAT54S	0603
	BAV99-DIO-SOT-23	—	—	—	Digi-Key	BAV99ZXCT-ND	0603
R1–R4	75 Ω	1%	—	5424R19-085	ROHM	MCR03FX75R0	0603
R5	1000 Ω	5%	—	5424R20-049	ROHM	MCR03JW102	0603
R6	75 kΩ	5%	—	5424R20-094	ROHM	MCR03JW753	0603
RSET	402 Ω	1%	—	5424R19-156	ROHM	MCR03FX4020	SMT3 (SOT23)
Q1	2N3904	5%	—	NO PICSPEC	ROHM	MMST3904	0603
—	—	—	—	—	Motorola	Q750MMBT3904	—
Capacitor from XTALIN to GND	27 pF	5%	NPO	5404R23-018	AVX	06035A270JATNA	0603
Capacitor from XTALOUT to GND	33 pF	5%	NPO	5404R23-019	AVX	06035A330JATNA	—
Capacitor in HD-SD low-pass filter (LPF)	33 pF	5%	NPO	5404R23-019	AVX	06035A330JATNA	0603
	33 pF	5%	NPO	N/A	Digi-Key	PCC330ACVCT-ND	0603
Capacitor #1 in HDSD LPF to GND	62 pF	5%	NPO	NO PICSPEC	ROHM	MCH185A620JK	0603
Capacitor #2 in HDSD LPF to GND	75 pF	5%	NPO	NO PICSPEC	ROHM	MCH185A750JK	0603
Inductor in series with DAC output	0.27 µH	10%	—	NO PICSPEC	Taiyo Yuden	LK2125R27K	2125_0805

***Table 3-1. Recommended Parts List for Key Active and Passive Components in Figure 3-2** (2 of 2)*

Reference Part Number from Figure 3-2	Part Value	Required Tolerance	Dielectric	Pic Spec	Recommended Vendor(1)	Vendor Part Number(2)	PCB Footprint(3)
FB; surface mount ferrite bead	Typical Impedance 56 Ω @ 25 MHz, 95 Ω @ 100 MHz, Rdc (MΩ)= 0.9, weight=0.30 g	N/A	N/A	NO PICSPEC	Fair-Rite	2743021447 (preferred)	16 mm width bead
	Typical Impedance <1 Ω @ 0 MHz, 23 Ω @ 25 MHz, 47 Ω @ 100 MHz, weight=0.30 g	N/A	N/A	NO PICSPEC	Fair-Rite	2743019447 (alternate)	16 mm width bead
Y1 – Fundamental operation, parallel resonant, 20 pF load	13.500 MHz XTAL	25 ppm total tolerance over 0–70 °C	—	NO PICSPEC	MMD	D20DA1-13.500 MHz	HC49/US SMD
U1	CX25874/5 Encoder	N/A	N/A	—	Conexant	CX25875	7 mm 64TQFP

GENERAL NOTE: Substitution of passives with similar characteristics will not degrade the encoder's performance.

FOOTNOTE:

(1) Recommended Vendor is only listed as a guide.

(2) Vendor part numbers are only listed as a guide. The part numbers have been used within Conexant reference design PCBs for the CX25874/5.

(3) The 0805 footprint may be used in place of the 0603 footprint where necessary.

Table 3-2. Recommended Parts List for Other Typically Used Components

Reference Part Number from Figure 3-2	Part Value	Required Tolerance	Dielectric	Pic Spec	Recommended Vendor(1)	Vendor Part Number(2)	PCB Footprint (3)
Decoupling capacitor	10 µF	+80%, –20%	Y5V		Taiyo Yuden	LMK316F106Z	1206
RN1, RN2, RN3	33 Ω RPACK	5%		NO PICSPEC	ROHM	MNR14EOABJ330	1632
Resistor for minimizing signal under/overshoot	33 Ω	5%		5424R20-013	ROHM	MCR03JW330	0603
Test Point	TPI						25 mil via
Resistor for enabling different stuffing options	0 Ω	5%		5424R20-146	ROHM	MCR03JW000	0603

GENERAL NOTE: Substitution of passives with similar characteristics will not degrade the encoder's performance.

FOOTNOTE:

(1) Recommended Vendor is only listed as a guide.

(2) Vendor part numbers are only listed as a guide. The part numbers have been used within Conexant reference design PCBs for the CX25874/5.

(3) The 0805 footprint may be used in place of the 0603 footprint where necessary.

Figure 3-3. SD Low-Pass Filter (LPF) Frequency Response

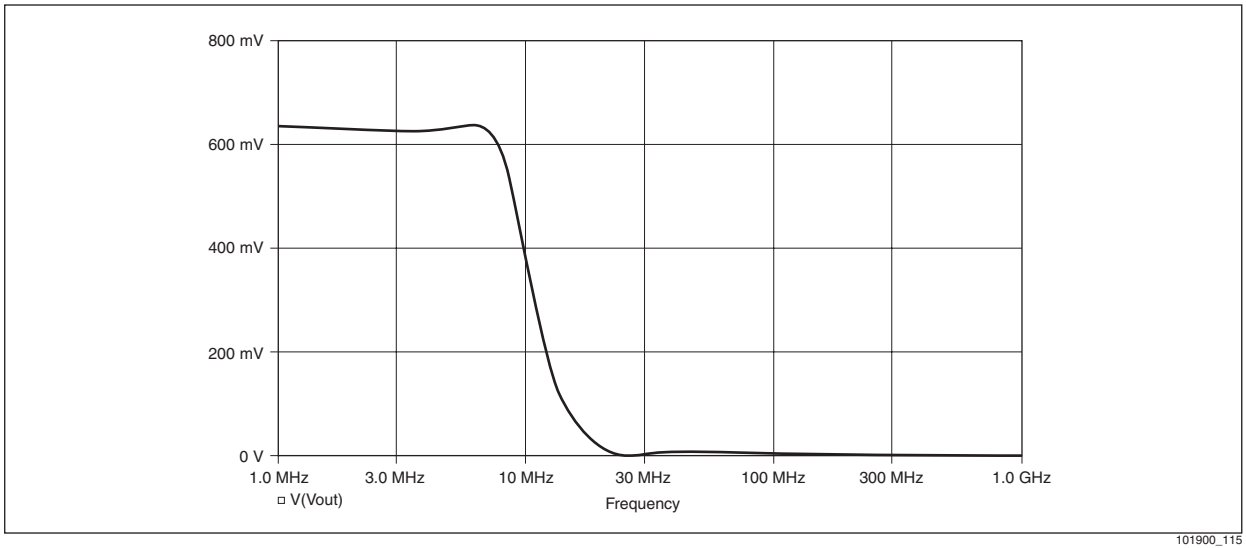
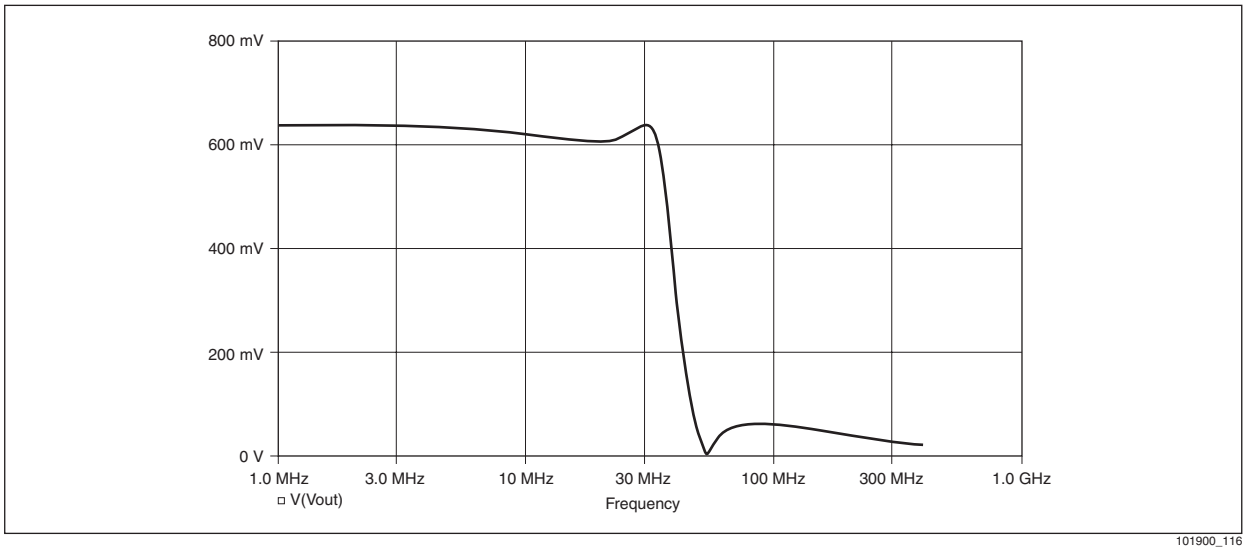


Figure 3-4. HD-SD Low-Pass Filter (LPF) Frequency Response



3.4 Recommended Schematics and Layout

3.4.1 Reference Schematics for Implementation of CX25874/5

For the CX25874/5 to operate at an optimal technical level, it is imperative to adopt the passive components, values, tolerances, and guidelines contained in the following figures.

Conexant has done extensive lab testing with these components, and found that they yield the best combination of performance and price.

The complete schematic diagram for a 3.3 V only design incorporating the CX25874/5 is illustrated in Figure 3-5.

The complete schematic diagram for a mixed 3.3 V and 1.5 V design incorporating the CX25874/5 is illustrated in Figure 3-6.

For a complete schematic diagram for a mixed 3.3V and alternate lower voltage (1.8 V or 1.1 V) design environment, request assistance from your local FAE. The finished schematic for the 3.3 V/1.8 V or 3.3 V/1.1 V case will look similar to Figure 3-6.

When CCIR656 syncless interface is used to connect this encoder to a master device, the HSYNC*, VSYNC*, BLANK* I/O signals serve no purpose. For this CCIR656 case only, tie each signal (HSYNC*, VSYNC*, BLANK*) through a 10 kΩ pullup resistor to the voltage level found on the VDDHV supply pin (pin #25).

Substitution of resistors, capacitors, inductors, and crystals with nonrecommended values or greater than recommended tolerances may degrade the video output quality of the CX25874/875 encoder.

Figure 3-5. CX25874/5 3.3 V Recommended Schematic for Connection with 3.3 V Master Device—Mixed HDTV and SDTV Outputs

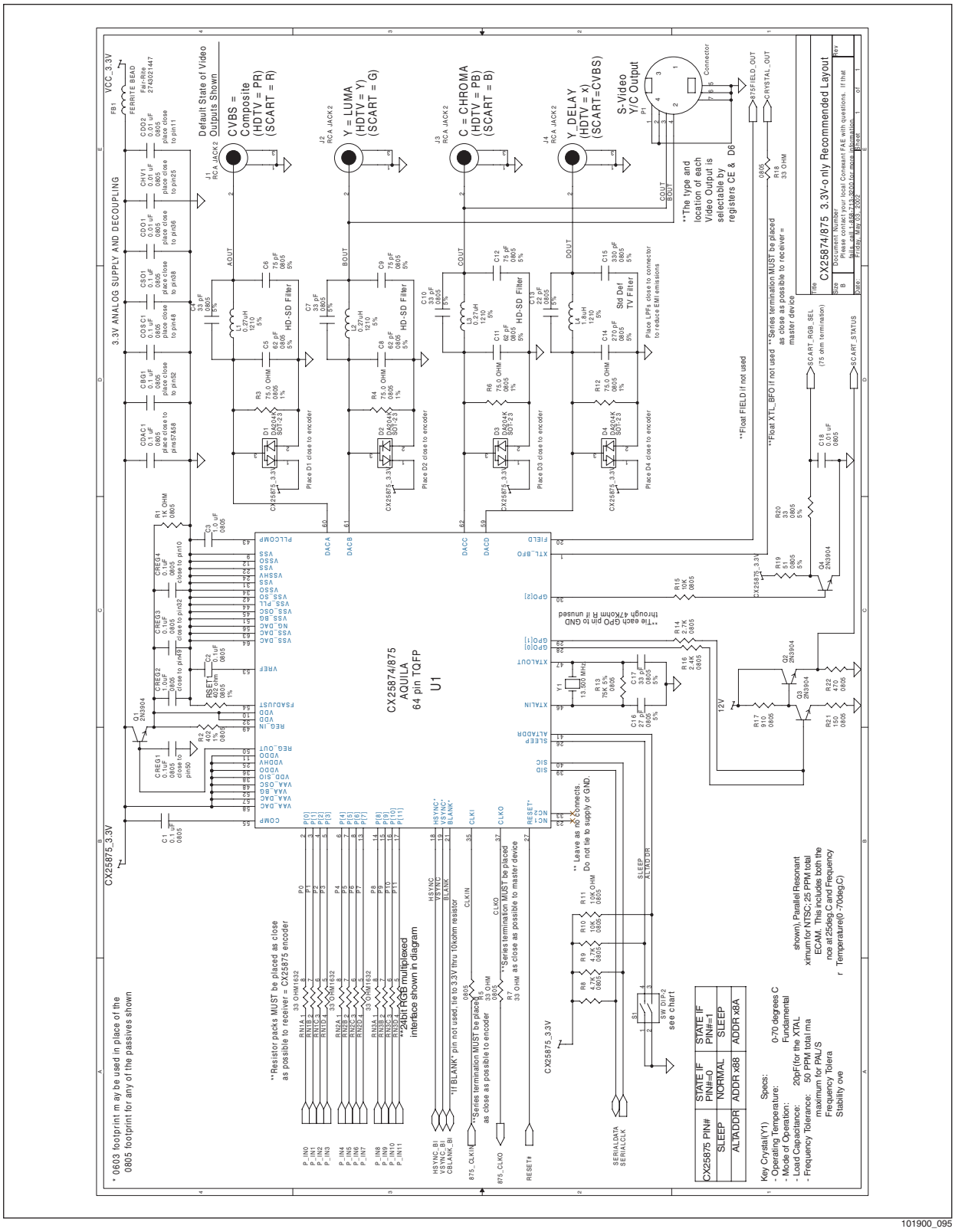
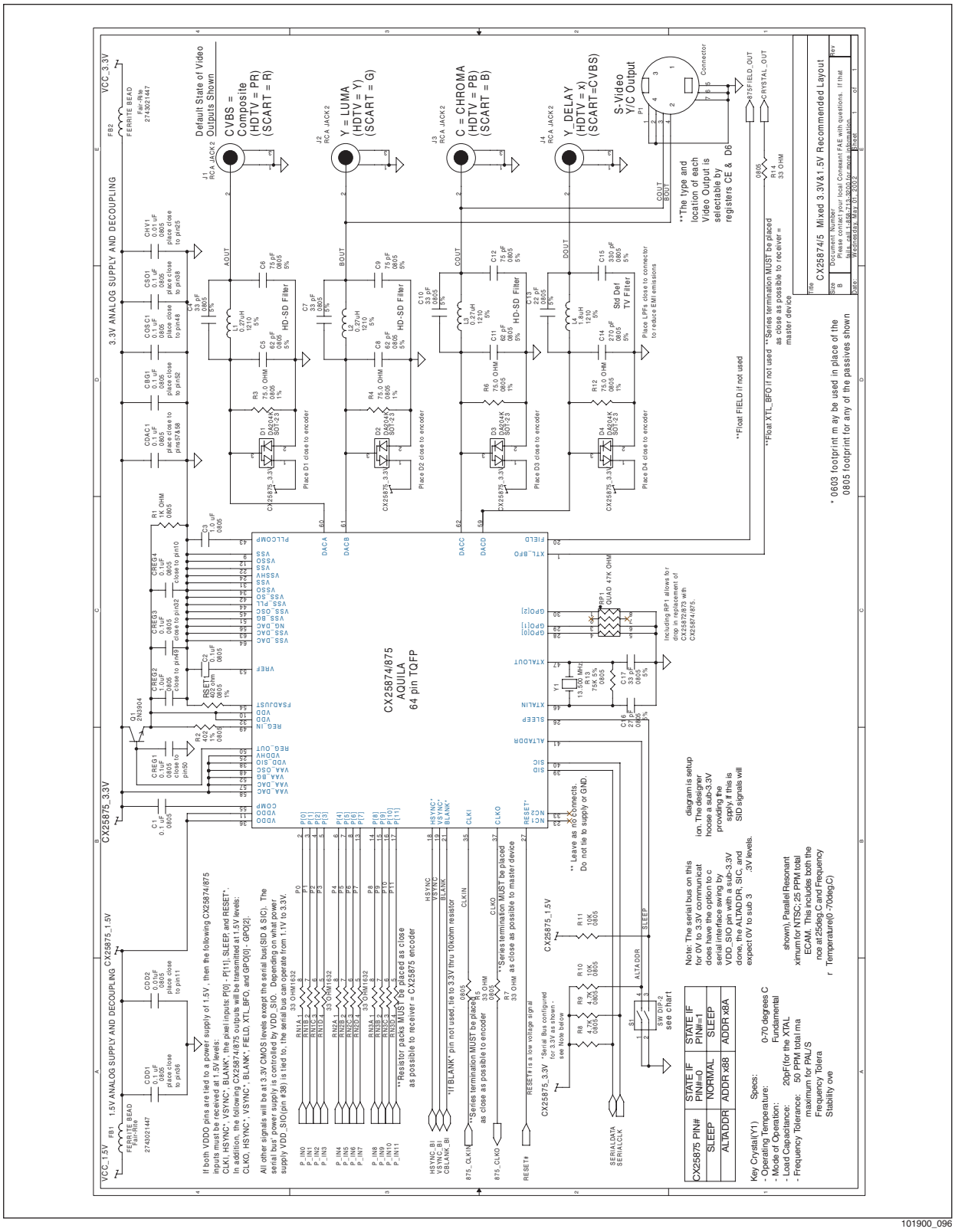


Figure 3-6. CX25874/5 3.3 V/1.5 V Recommended Schematic for Connection with 1.5 V Master Device—Mixed HDTV and SDTV Outputs



3.4.2 Reference PCB Layout for Implementation of CX25874/5

Conexant has successfully designed, tested, debugged, and fabricated numerous graphics and/or daughter cards that incorporate the CX25874/5. The following sample layout plots were extracted from the CX25874/5 reference design daughter card. This encoder takes in pixel data (P[0] - P[11] and control signals (HSYNC*, VSYNC*, RESET*, CLKI, CLKO, SIC, SID) through the two-row, 50-pin inline header. The encoder transmits its Composite, S-Video, or Component YC_RC_B outputs through an on-board, 9-pin miniDIN connector and associated breakout cable (not shown). Figures 3-7 through 3-12 are provided strictly for reference.

Figure 3-7. Top Silk Screen

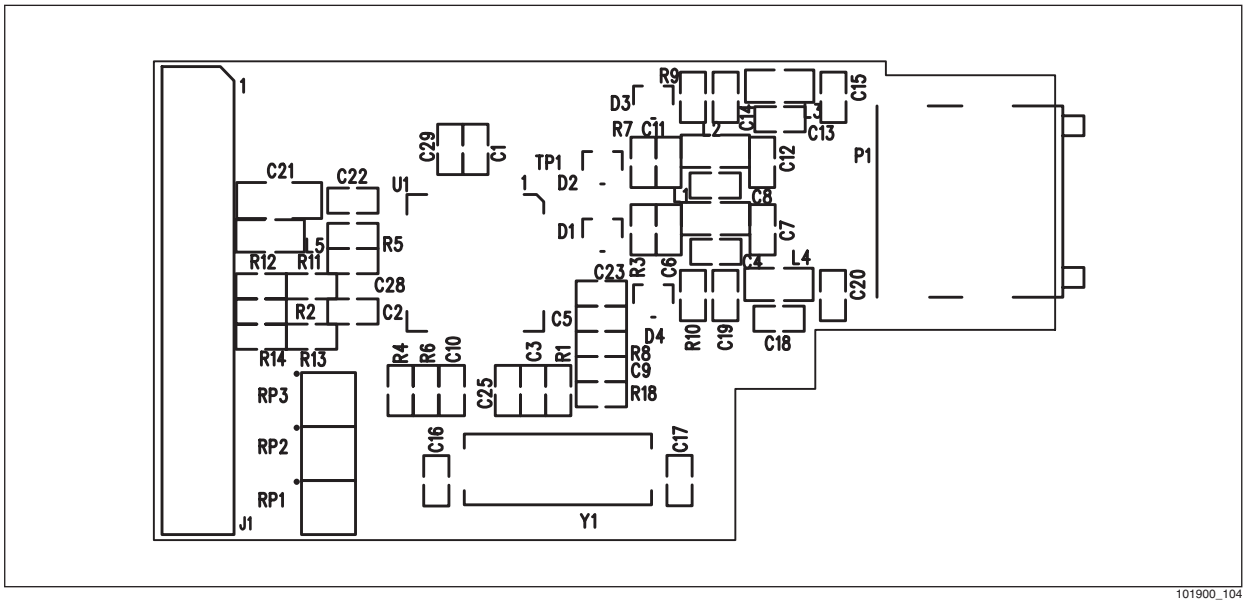


Figure 3-8. Top Circuit—Board Layer 1 (Component Side)

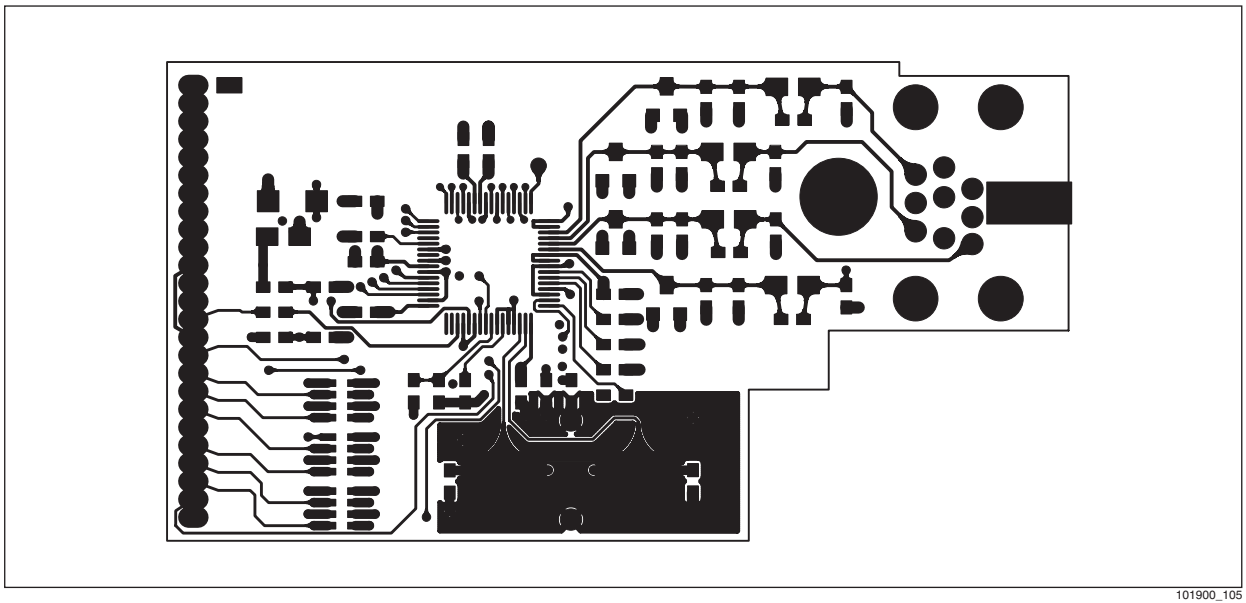


Figure 3-9. Ground Layer—Board Layer 2

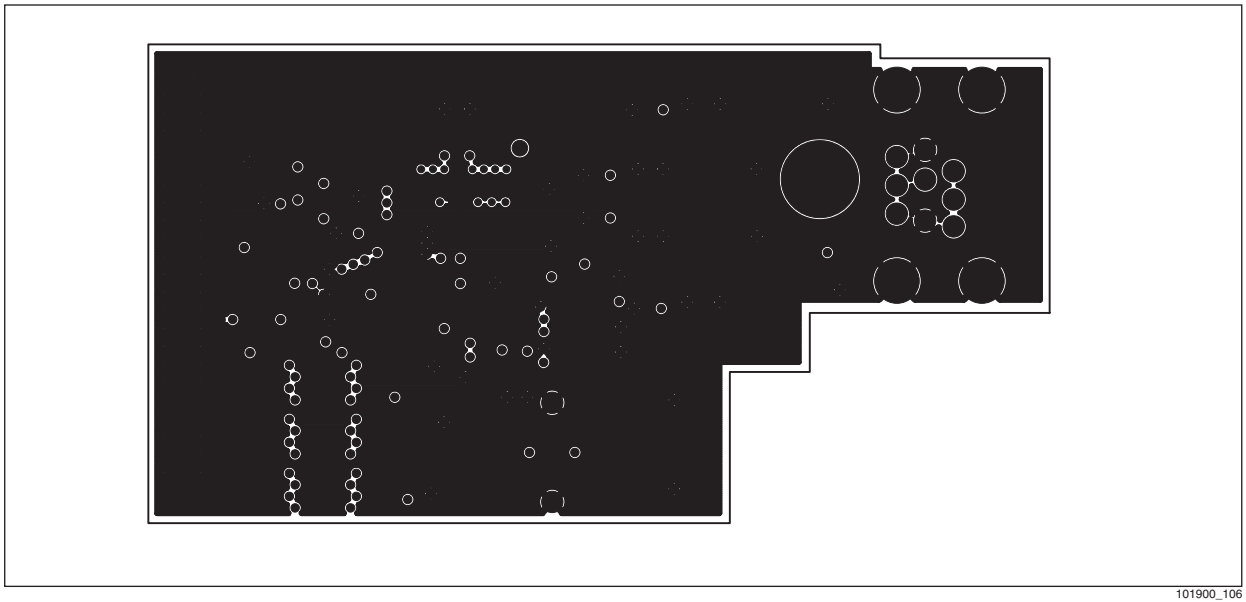


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Figure 3-10. Power Layer—Board Layer 3

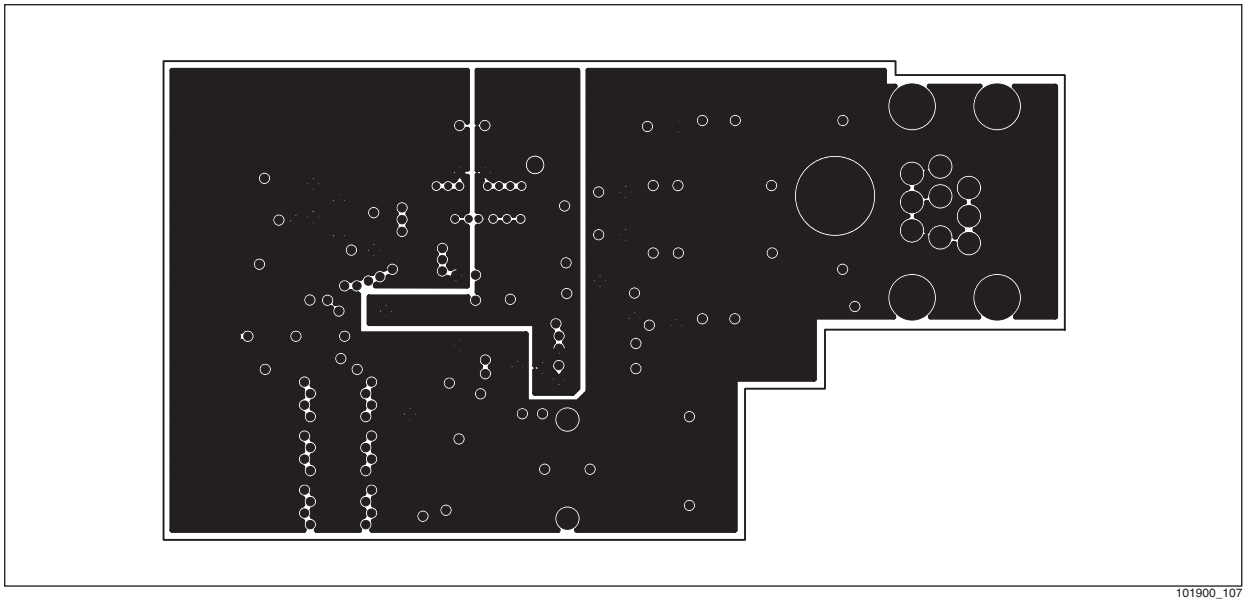

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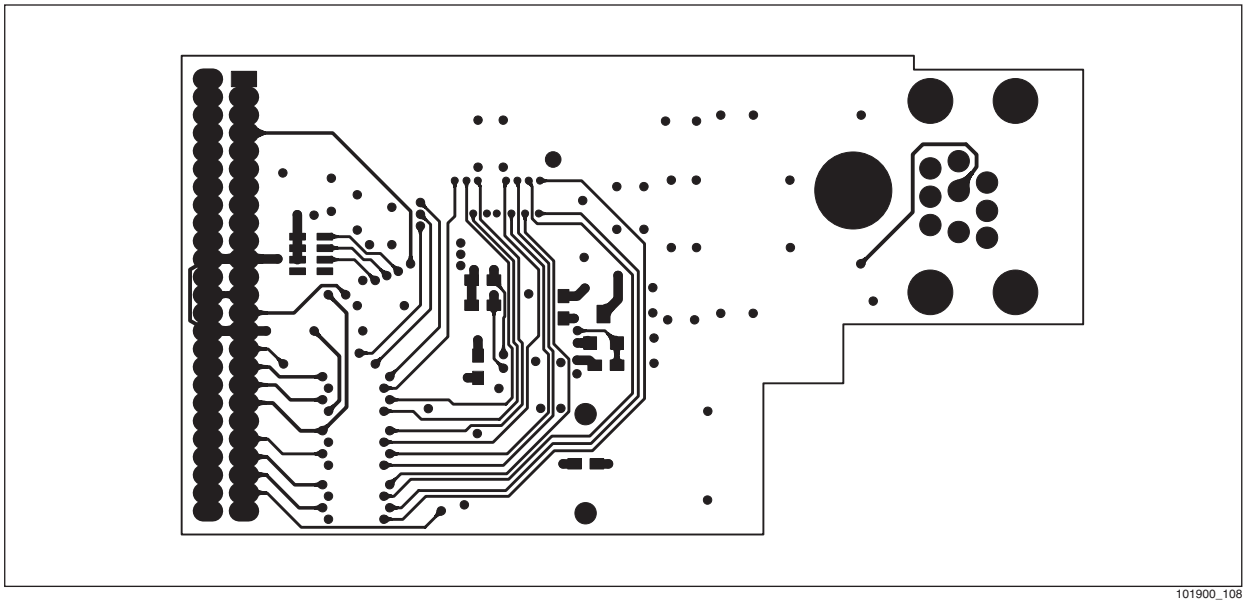
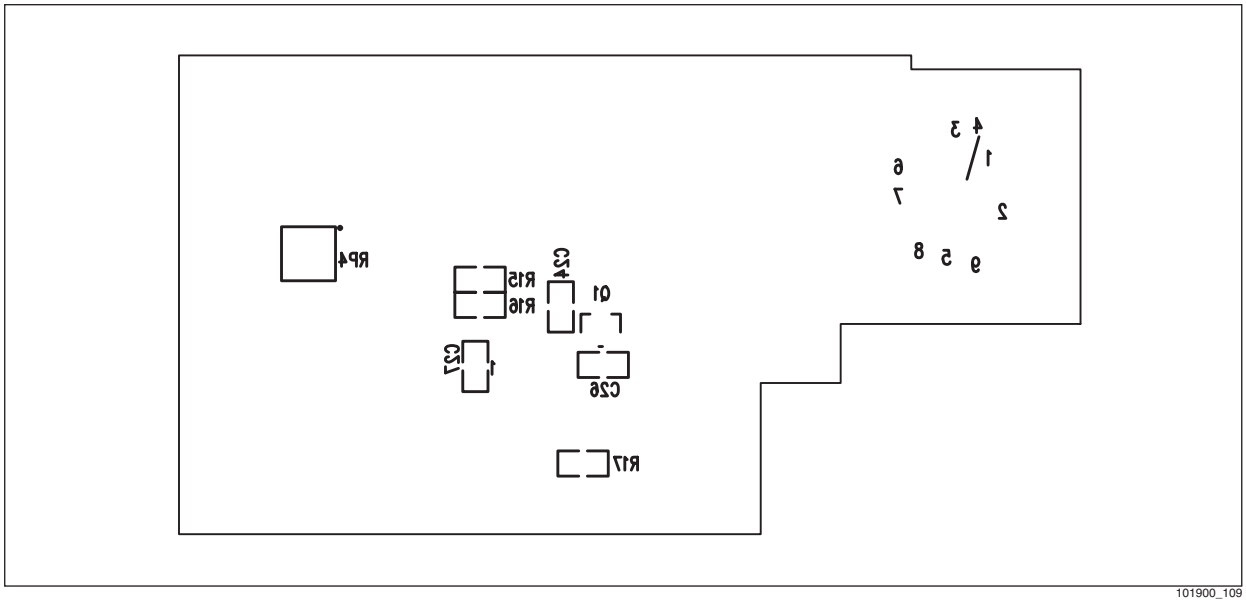
Figure 3-11. Bottom Circuit—Board Layer 4 (Solder Side)



101900_108

Figure 3-12. Bottom Silk Screen



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3.5 Decoupling

3.5.1 Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors can be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

3.5.2 Power Supply Decoupling

The best power supply performance is obtained with a 0.1 μF or 0.01 μF ceramic capacitor decoupling each analog power (VAA) pin and each digital power (VDD) pin. The capacitors should be placed as close as possible to the device VAA/VDD pins and GND pins and connected with short, wide traces.

The 0.1 μF and 0.01 μF capacitors are for high-frequency power supply noise rejection. Inclusion of a 1.0 nF and a 1.0 μF capacitor between the group of VAA/VDD pins and GND/VSS pins will improve power supply decoupling at intermediate frequencies as well.

When a linear regulator is used, the proper power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, or low-voltage interface is implemented, and the switching frequency is close to the raster scan frequency. About 5 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

3.5.3 COMP Decoupling

The COMP pin must be decoupled to the closest 3.3 V power supply, typically with a 0.1 μF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

For interfacing with a sub 3.3 V data master, the COMP pin must also be tied directly to the sub 3.3 V power supply. This is in addition to the decoupling capacitor connection explained above.

3.5.4 VREF Decoupling

A 0.1 μF ceramic capacitor should be used to decouple this input to GND.

3.5.5 PLL COMP Decoupling

A 1.0 μF ceramic capacitor should be used to decouple this pin to GND.

3.5.6 REG_OUT Decoupling

A 0.1 uF ceramic capacitor should be used to decouple this pin to GND. Place this capacitor as close to pin 50 as possible. This will minimize any ringing and noise from the PCB from reaching the core of the encoder.

3.5.7 REG_IN Decoupling

This pin is also called VDD1 (pin # 49). A 1.0 uF ceramic capacitor should be used to decouple this pin to GND. Place this capacitor as close to pin 49 as possible. This will minimize any ringing and noise from the PCB from reaching the core of the encoder.

The 402 Ω ± 1% resistor between pin 49 of the CX25874/5 and the emitter of the BJT-type transistor raises the core voltage by a few millivolts to the encoder.

A 1 kΩ load resistor should also be attached from the emitter of the BJT-type transistor to GND to better establish an emitted bias current.

3.6 Signal Interconnect

3.6.1 Digital Signal Interconnect

The digital inputs to the CX25874/875 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by fast transitioning clock edges, data edges (less than 3 ns), and overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary because feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time. Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing, overshoot, and undershoot can be reduced by damping each >1 MHz line with a series resistor. Values between 15 Ω to 56 Ω are recommended since ringing is mitigated and the RC time constant associated with each series resistor does not adversely affect the data transfer process.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90-degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

3.6.2 Analog Signal Interconnect

The CX25874/875 analog output traces should be located as close as possible to the output connectors and be of equal length to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; therefore digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the CX25874/875 to minimize reflections. Unused DAC analog outputs should be left floating.

3.7 Applications Information

3.7.1 Changes Required to Accommodate CX25874/875 in CX25870/1 Designs

3.7.1.1 Software

The CX25874/5 is software backward compatible with Conexant's first and second generation VGA Encoders, the Bt868/869 and CX25870/1. This means that all register indices for the Bt868/869 and CX25870/1 were carried forward to the exact same indices for the CX25874/5. For Conexant's third generation encoder, several new registers were added, but the actual addresses used were outside of the address range, 0x28 and 0x2E through 0xD6, reserved for the CX25870/1 legacy functionality. Some Reserved bits within the CX25870/1 did take on significance with the CX25874/5 where necessary to improve existing or turn on new features. For a relative register map, see Table 3-3.

Table 3-3. Relative Register Map for CX25874/5

Register Address(es)	Register Type	Access Type
0x00 to 0x06 (1)	Shared CX25874/5, CX25870/871, and Bt868/869 registers	Read Only
0x08 to 0x24	Not used. Reserved for future use.	N/A
0x26	CX25874/5-specific register	Read/Write
0x28	Shared CX25874/5 and CX25870/871 registers	Read/Write
0x2A to 0x2C	Not used. Reserved for future use.	N/A
0x2E to 0x6A	Shared CX25874/5 and CX25870/871 registers	Read/Write
0x6C to 0xD6	Shared CX25874/5, CX25870/871, and Bt868/869 registers	Read/Write
0xD8	Shared CX25874/5 and CX25870/871 registers	Read/Write

FOOTNOTE:
(1) Must be accessed through Legacy read procedure with ESTATUS[1:0] in Bt868/869.

Like the CX25870/1, this third generation Conexant encoder can be read from using the Standard serial method as well as the Legacy serial method. To use the Standard procedure, the master issues CX25874/5's device ID and subaddress in consecutive bytes, and the slave acknowledges with an acknowledge pulse after each transaction. Upon completion of these two steps, the slave transmits the final byte which contains the eight bits of data. The Bt868/869 cannot be read from in this manner and instead relies solely on the Legacy method. This process is explained step-by-step in the TV DAC Detection Procedures section of this specification.

Another difference in terms of software between the CX2587x encoders and the Bt868/869 is the power-up video output routing. After power-up or after a signal-driven reset has been received, the CX25874/5 transmits Video0 as Composite (CVBS) on DAC_A, Video1 = Luma (Y) on DAC_B, Video2 = Chroma (C) on DAC_C, and Video3 = Luma Delay (Y_DLY) on DAC_D. The Bt868/869 was different in this respect. On power-up, it sent out Video0 = Composite (CVBS) from

DAC_A, DAC_B, and DAC_C. Reprogramming register 0xCE correctly ensures proper video output routing no matter what is required for the connectors and video subsystem.

Another difference between the CX25874/5 and the two previous generation encoders is the default video output state. On power-up, the CX25874/5 will broadcast Video[0] = Composite – black burst from DAC_A, Video[1] = Luminance – black burst from DAC_B, Video[2] = Chrominance – black burst from DAC_C, and Video3 = Luma Delay (Y_DLY) – black burst from DAC_D. Basically, by default, the CX25874/5 outputs black burst NTSC on power-up. This allows the television to initially sync and prevents any white flashes from being visible as the encoder reaches an ambient condition. However, after reaching a normal operating state, the encoder's video outputs each continue to transmit black burst thus preventing any sort of picture from being visible when the DACs first become activated. To correct this, bit 2 of register 0x6C must be manually set. Bit 2 is the EACTIVE bit. For most standard-definition video output modes, except SCART, programming register 0x6C to 84 hex will allow normal NTSC or PAL video to appear.

As a result of the backwards software register compatibility of the CX25874/5 to the previous generation encoder pairs, code written for the CX25870/1 should run seamlessly on the CX25874/5. If for some reason, the television quality coming from the newest encoders does not exceed or at least match the television quality coming from the past generation encoders, then modifications to the existing source code may be necessary. The following list summarizes all the software changes that were made between the CX25874/5 generation and the previous Conexant VGA encoders (e.g., CX25870/1 and Bt868/869).

- ID[2:0] field changes for CX25872/3/4/5.

  The ID[2:0] field = 100 for Aquila Lite without Macrovision (CX25872), the ID[2:0] field = 101 for Aquila Lite with Macrovision (CX25873), the ID[2:0] field = 110 for Aquila without Macrovision (CX25874), and the ID[2:0] field = 111 for Aquila with Macrovision (CX25875). Conexant recommends polling for the ID[2:0] in either BIOS, the graphics driver, or both to determine what particular Conexant PC encoder is present.
- Integration of new, tested, and reliable TV detection algorithm and code for the CX25872/3 and CX25874/5 encoder products from Conexant.

  The detect algorithm for the CX25872/873 is different from the previous TV detection algorithms for the Bt868/869 and CX25870/1 which relied on a No-Operation loop of varying lengths of times.

  This length of time was different for the Bt868/869 and CX25870/1 which ended up causing less than 100 percent correct detection. Review the TV DAC Detection Procedures subsection for a description of this new algorithm and the C code to implement it within a driver.
- Black burst – Register 0x6C needs to be programmed to enable active video.

  Bit 2 of register 0x6C is the EACTIVE bit. For most standard-definition video output modes, except SCART, programming register 0x6C to 84 hex will allow normal NTSC, PAL, SECAM, or Component Y CR CB 480i video to appear after power-up.

- VERSION[4:0] field.

  VERSION[4:0] = 00001 for Rev. B, and VERSION[4:0] = 00010 for Rev. C of the CX25874/5. The VERSION field will be different for the CX25870/1 or the Bt868/869 used in production now. If the existing software does not care about the VERSION field, then this difference has no impact on the existing graphics driver.
- New autoconfiguration modes – #16, #20, #27, #31.

  The CX25874/5 now has the full complement of 48 autoconfiguration modes. Two new modes (#20 and #27) enable PAL-60 for support of the China market. Mode #31 is a mode intended for PAL DVD support with a progressive RGB input while mode #16 is another 640x480 NTSC overscan option. These autoconfiguration modes were disabled in the CX25870/871. This is strictly a software improvement for the CX25874/5 encoder pair.
- Autoconfiguration modes – #31 and #44 change the interface between the encoder and GPU. Autoconfiguration mode #31 (new in CX25874/5) and mode #44 (from CX25870/1 originally) now configure the CX25872/3 into the pseudo-master interface. All other autoconfiguration modes throw the encoder into master interface as was the case with the CX25870/1.
- CLKO is output on power-up and not three-stated.

  Register C4 contains the EN_OUT bit. This bit is set to 1 by default within CX25874/5 so the CLKO signal is output on power-up and not three-stated as before with the CX25870/1.
- Non-multiplexed YCrCb and RGB input data formats disallowed.

  The CX25874/5 does not contain any support for non-multiplexed input data formats due to lack of the upper pixel data bus (P[12] – P[23]) that existed with CX25870/1 and Bt868/869. Register 0xC6 does not allow for non-multiplexed input data formats to be programmed.
- Interface on power-up changes to pseudo-master.

  SLAVER, bit 5 of register 0xBA, now equals 1 by default in the CX25874/5 on power-up and after a pin based reset. The CX25874/5 will therefore expect to receive digital HSYNC* and VSYNC* from the master IC in pseudo-master interface and not transmit them as was the case with the CX25870/871 and Bt868/869.

Of course, to enable new features within the CX25872/3, such as General Purpose outputs (GPO[0]-GPO[2], Macrovision copy protection for progressive scan outputs, WSS high-definition support and others, some software changes and new register sets will be necessary. This usually equates to the release of a new driver and/or graphics BIOS for support of the CX25874/5.

3.7.1.2 Hardware

The CX25874 and CX25875 are pin-to-pin compatible with each other. However, since the CX25874/5 is housed in a plastic 64-pin TQFP package, it is not pin-to-pin compatible with the 80-pin Bt868/869 or CX25870/1 encoder pairs. The device is pin-to-pin compatible with its lower-end counterpart, the CX25872/3 with the exception of pins 28, 29, and 30. This group of pins are grounds within the CX25872/3 but comprise the three general-purpose outputs present on the CX25874/5. One final difference concerns pin 59. With the CX25872/3, this pin is a no connect. With the CX25874/5, pin 59 is labeled as DACD and can be used in the same manner as any of the other DACs.

It is possible to create a single PCB layout to accommodate either the CX25872/3 or the CX25874/5. To do this:

- Tie pin 28 to ground through a 47 kΩ resistor.
- Tie pin 29 to ground through a 47 kΩ resistor.
- Tie pin 30 to ground through a 47 kΩ resistor.
- Incorporate an appropriate low-pass filter network, set of protection diodes, and load resistor (75 Ω). Unstuff if CX25872/3 is used, or unstuff resistor from pin 59 if CX25874/5 is used.
- Attach pin 59 to its low-pass filter network through a 0Ω resistor. Unstuff the 0Ω resistor if CX25872/3 is used since this encoder lacks DACD.

To mitigate risk in transitioning from the CX25870/1 to the CX25874/5, the CX25874/5 [7 mm x 7 mm] square footprint fits inside the [14 mm x 14 mm] square footprint of the previous generation CX25870/1. There is approximately 3 mm on each side of the CX25874/5 chip for traces and vias to interconnect the CX25870/1 and CX25874/5 signals. In addition, if necessary, signals could be routed to the inside of the CX25874/5 and down to the solder side of the PCB to get the CX25874/5—unique signals beyond the CX25870/1 pad ring. This cannot be penetrated unless the signal is common with the CX25870/1.

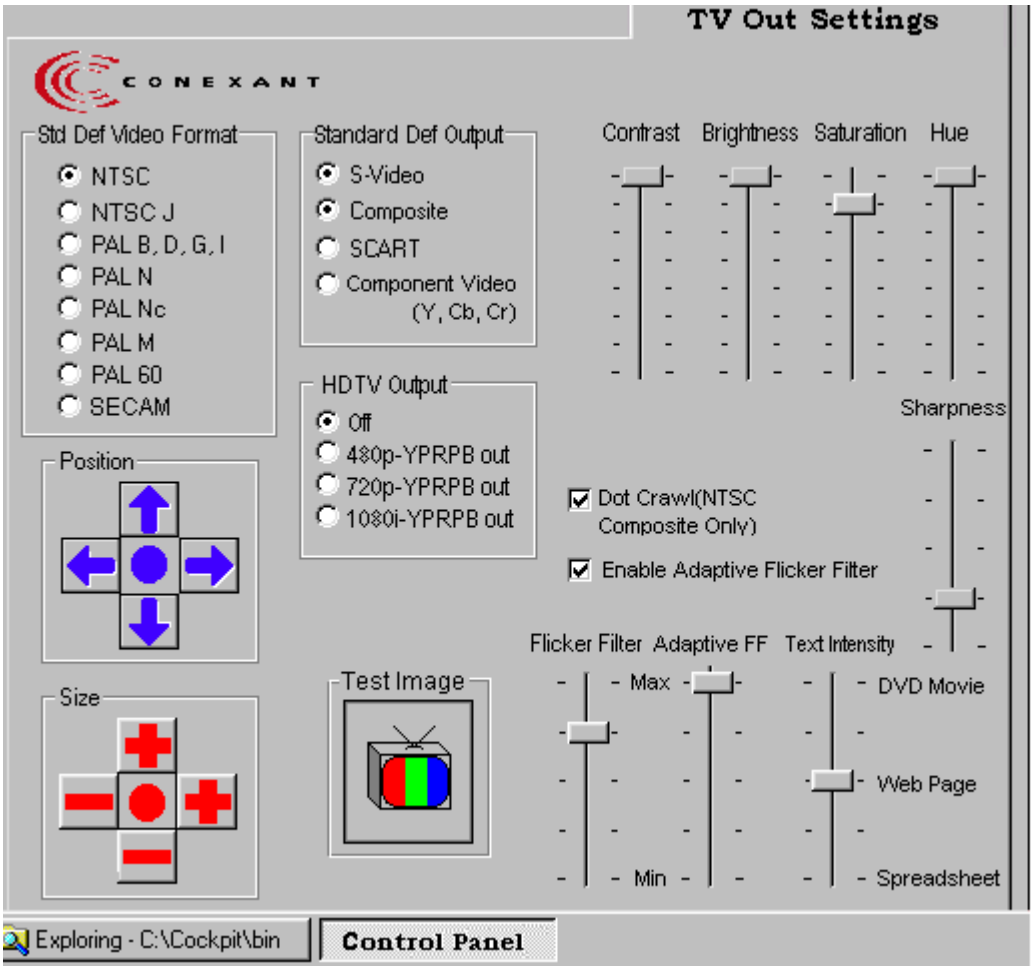
For further information on the part-within-part layout, contact your local Conexant field applications engineer.

3.7.2 Programmable Video Adjustment Controls

The quality of the TV out picture can be altered depending on the digital input content, the settings of various output video adjustment control registers, and the TV itself. The values of the CX25874/875's Y_OFF, MY, Y_ATTEN, MCB, MCR, C_ATTEN, and PHASE_OFF registers all definitely impact the perceived quality of the analog NTSC/PAL/SECAM video signal. As a result, for graphics cards that utilize the encoder, Conexant recommends the inclusion of a GUI for TV out. By designing this intelligent control panel, the end user can improve the TV image quality by adjusting the proper slider or other controls at his disposal. Behind these controls, intelligence must be embedded in the TV out source code and driver so the values of certain registers get adjusted depending on the status of the corresponding radio button, checkbox, slider, or pulldown menu.

An illustration of a sample GUI for TV out is shown in Figure 3-13.

Figure 3-13. Conexant Recommended TV Out GUI for CX25874/875



A set of optimal video-quality settings have been integrated into every TV out script shipped with the new CX875EVK evaluation kit. Conexant recommends new software drivers use these register values by default when enabling a new resolution and video format.

3.7.2.1 Contrast

Contrast is a video quality that refers to how far the whitest whites are from the blackest blacks in an analog video waveform. If the peak white is far away from the peak black, the image is said to have high contrast. With high contrast, the image is very pure like a black and white tile floor. If the two parameters are very close together, the image is said to have poor, or low, contrast. With low amounts of contrast, an image may be referred to as being washed-out. Instead of easily recognized black portions of the image versus white parts, the image with low contrast looks gray.

Register MY[7:0] in conjunction with register Y_ATTENUATE[2:0] controls adjustment of contrast. Y_ATTENUATE has eight possible values ranging from 1.0 gain (No attenuation) to 0 gain (Force Luminance to 0). Conexant recommends inclusion of an 8-level slider to control the Contrast level. Each single movement of the slider should reprogram this bit field to a different fractional value. Lab testing has shown that values from ¾ gain (Y_ATTENUATE=011) to 15/16 gain (i.e., 001) yield the crispest TV picture.

Register MY modifies the luminance multiplier allowing for a larger or smaller luminance range. For more drastic changes in the Contrast, change MY. For more subtle changes, shifting the Y_ATTENUATE field as the end user moves the slider should be sufficient.

Since the difference between contrast and brightness is usually understood by video professionals only, Conexant recommends the designer increment or decrement the YATTENUATE[2:0] field for either brightness or contrast adjustments.

3.7.2.2 Saturation

Saturation is the amount of color present. For example, a lightly saturated green looks olive-green to gray while a fully saturated green looks pine tree green. Saturation does not mean the brightness of a color, just how much pigment is used to make the color itself. The less pigment, the less saturated the color is, effectively adding white to the pure color.

The amount of Saturation is controlled by the bit field named CATTENUATE[2:0]. CATTENUATE has eight possible values ranging from 1.0 gain (No attenuation) to 0 gain (Force Chrominance to 0). Conexant recommends inclusion of an 8-level slider to control Saturation level. Each single movement of the slider should reprogram this bit field to a different fractional value. Lab testing has shown that values from ¾ gain (CATTENUATE=011) to 1.0 gain (i.e., 000) yield the crispest TV picture.

3.7.2.3 Brightness

Brightness is defined to be the intensity of the video level and refers to how much light is emitted from the display. The amount of Brightness is controlled by the register named Y_OFF[7:0].

Y_OFF[7:0] is a 2s complement number, such that a value of 0x00 is 0 IRE offset, a value of 0x7F is an increase of 22.14 IRE above black level. The active video will then be added to the offset level set by the Y_OFF value.

Since the difference between contrast and brightness is usually understood by video professionals only, Conexant recommends the designer increment or decrement the YATTENUATE[2:0] field for either brightness or contrast adjustments.

3.7.2.4 Hue

Hue refers to the wavelength of the color. That means that hue is the term used to represent the base color–red, green, magenta, yellow, and so forth. Hue is completely separate from the intensity or the saturation of the color. For example, a red hue could look brown at low saturation, fire-engine red at a higher level of saturation, or pink at a high brightness level. All three colors have the same hue however.

Occasionally, the end user may need to alter the hue. The method for adjusting this parameter with the CX25874/875 is to program a different value to the HUE_ADJ register. This method changes the hue in the composite and S-Video signals for NTSC, PAL, and SECAM waveforms according to the following equation:

*Desired Phase Offset (in degrees) = [360° / 256] * (HUE_ADJ)*

A slider labeled 'HUE' should be included in the GUI so minor alterations (±20°) in this parameter are possible. Major alterations(>20°) in the phase offset are not recommended since dramatic hue shifts will result in different colors than the original.

3.7.2.5 Sharpness

Occasionally, drastic phase shifts occur at the borders of dialog boxes within applications programs and with certain combinations of text and background colors. This is due to the primary and secondary colors being at opposite ends of the UV hue spectrum. The result of these phase differences is that the edges or text look blurry to the observer.

The CX25874/875 has a bit field available named PKFIL_SEL[1:0] to sharpen these edges so they look crisper on the television. Four choices are available, each of which enables a different type of peaking filter. The 0 dB (Bypass) filter is the defaulted level while gains of 1 dB, 2 dB, and 3.5 dB are also possible.

3.7.2.6 Dot Crawl

Dot crawl refers to a specific image artifact that is the result of the NTSC standard. When some computer generated text shows up on top of a video clip being shown, close viewing of the TV will show some pixels or jaggies rolling up or down the picture in the area of a dialog box's edges. Another term for this phenomenon is creepy-crawlies or the zipper effect.

Conexant has derived software code to minimize the dot crawl. This is not a register or bit within the CX25874/875 but rather a complicated software algorithm that modifies the 90-degree color subcarrier shift exhibited in four consecutive NTSC fields. To obtain this code, file a request with your local Conexant sales office. The algorithm/ function for dot crawl should be enabled with the NTSC Composite output only. It will have no effect for PAL or SECAM outputs.

3.7.2.7 Standard and Adaptive Flicker Filter

Flicker occurs when the refresh rate of the video is too low. In digital encoders, flicker can also occur when processing an image that contains many fine vertical divisions such as lines that are only 1 or 2 lines wide. When the encoder stores, combines (by vertically interpolating data), and converts two consecutive incoming frames into 1 output field, portions of the image containing just a few lines can be placed on different analog output lines. Since the position of the output line is not the same from field to field, it appears to flicker at the vertical refresh rate.

This annoying artifact can be eliminated by selecting an appropriate flicker filter setting, one that trades off vertical resolution and text clarity against flicker reduction. The flicker filter slider shown in Figure 3-14 modifies the F_SELY[2:0] and F_SELC[2:0] bit fields together anytime the end user changes the particular level. Internal testing has shown that certain application programs such as spreadsheets look best with more flicker filtering while others, such as games and DVD movies, look best with less. In addition, the active resolution also affects the amount of flicker filtering required. 640x480 and lower resolutions rarely require a maximum flicker filter setting, whereas the 1024x768 resolution often does.

With five standard flicker filter levels available, Conexant recommends programming the following bit values in according to the slider level in Table 3-4.

Table 3-4. Programming Bit Settings According to Slider Level

Flicker Filter Slider Level	F_SELY[2:0]	F_SELC[2:0]
Level 5 = Maximum	000 = 5 line. DIS_FFILT = 0.	011 = 4 line. DIS_FFILT = 0.
Level 4	011 = 4 line. DIS_FFILT = 0.	010 = 3 line. DIS_FFILT = 0.
Level 3	010 = 3 line. DIS_FFILT = 0.	001 = 2 line. DIS_FFILT = 0.
Level 2	001 = 2 line. DIS_FFILT = 0.	001 = 2 line. DIS_FFILT = 0.
Level 1 = Minimum	Do not care. DIS_FFILT = 1.	Do not care. DIS_FFILT = 1.

NOTE: The optimal performance for the Standard Flicker Filter is usually achieved by configuring F_SELC to 1 line less than the F_SELY setting.

The CX25874/875 also has an adaptive flicker filter (i.e., Adaptive FF). This feature is explained in Section 1.3.20. The recommended TV out Graphical User Interface allows the usage of the adaptive flicker filter only if the box to enable it is checked. Once this is done, the ADPT_FF bit should get set (=1). The optimal adaptive flicker filter bit settings are shown in Table 3-5.

Table 3-5. CX25874/875 Optimal Adaptive Flicker Filter Bit Settings by Active Resolution

	Adaptive Flicker Filter Registers and Bit Settings										
Adaptive Flicker Filter Slider Level	**Reg 0x34**	**Reg 0x36**	**ADPT FF**	**Y ALTFF**	**C ALTFF**	**Y THRESH**	**C THRESH**	**Y SELECT**	**FFRTN**	**BYYCR**	**CHROMA BW**
Level 1= Min = 640x480 and lower	9B	C0	On=Checked	4-line	4-line	000	000	On	On	1	0
Level 2 = 720x480, 720x576	9B	24	On=Checked	4-line	4-line	100	100	Off	Off	1	0
Level 3 = 800x600	80	92	On=Checked	5-line	5-line	010	010	Off	On	1	0
Level 4 = between 800x600 and 1024x768	80	64	On=Checked	5-line	5-line	100	100	On	Off	1	0
Level 5=Max=1024x768	80	F6	On=Checked	5-line	5-line	110	110	On	On	1	0

When the Adaptive Flicker Filter is on, the Standard Flicker Filter continues to work normally. Indeed, many of the lines and/or pixels will still be filtered at the more moderate standard flicker filter level. However, as the encoder analyzes and processes each pixel, it will periodically come across certain regions requiring a more aggressive filter setting. For these areas only, more forceful Adaptive Flicker Filter value is used. With the dynamic ability of the CX25874/875, the end user can enjoy an optimal TV out environment without having to manually adjust the amount of flicker filtering depending on his given application. The CX25874/875 provides this functionality so long as the Adaptive Flicker Filter slider and control boxes are included. When the adaptive element is turned on, an additional five flicker reduction settings can be applied by moving the control pad to another level.

Through testing, Conexant recommends the bit settings in Table 3-4 get reprogrammed according to the state of the Adaptive Flicker Filter slider.

Integrating both flicker filter sliders and the correct intelligence behind them makes the CX25874/875 ideal for Internet browsing, DVD movie watching, or game playing by overcoming many of the quality problems like image flicker, illegible text, and low-definition graphics that plague other TV encoders.

3.7.2.8 Screen Position

There are many TV manufacturers, and most models display the active picture in a slightly different position relative to the bezel of the television itself. To allow the end user the ability to position the TV picture directly in the middle of his screen, or any other reasonable location, Conexant recommends inclusion of several Position control buttons.

There should be four directional controls included; two for horizontal adjustment and two for vertical adjustment. For practical usage, the maximum adjustment amounts should be limited to 25 pixels horizontally and 10 lines vertically from the default position. Values greater than these cause a good portion of the active region to be hidden behind the bezel of the TV thus rendering this area useless.

From experience, Conexant recommends incrementing the graphics controller's HSYNC_START register by 5 pixels every time the LEFT(= '–') or RIGHT(= '+') button is clicked within the GUI. Every mouse click will also require reprogramming the CX25874/875's H_BLANKI register so the active data does not get chopped off on the opposite side.

Vertically, the software driver should add or subtract two lines from the prior vertical position every time the UP(= '+') or DOWN(= '–') button is clicked within the GUI. This means that the VSYNC_START register should be increased or decreased by two lines for every vertical click by the end user. The corresponding modification that needs to be made to the CX25874/875 is an add/subtract of two lines to the original value in its V_BLANKI register.

As an illustration, assume the end user clicked on the Right button once. Internally, this action would mean that the graphics controller's new HSYNC_START register value needs to be $\{HSYNC\_START_{default} - 5 \text{ pixels}\}$. As the timing master, this would force the controller to issue its HSYNC* digital signal's leading edge five pixel clock cycles earlier in time. The software engineer also must add five pixels to the controller's HSYNC_END register to maintain the original HSYNC* pulse duration (8–20 pixels is common). Finally, within the CX25874/875, the H_BLANKI[9:0] register must be increased by five pixels so the encoder can accommodate the five extra pixels of blanking to start each line and still display the original active portion of the line.

Now, assume the end user clicked on the Down button once. This action dictates that more blanking will exist before the active region is displayed. This operation requires decrementing the graphics controller's new VSYNC_START register value to $(VSYNC\_START_{default} - 5 \text{ lines})$. As the timing master, this would force the controller to issue its VSYNC* digital signal's leading edge five lines earlier in time than before. The software engineer must also subtract five lines to the controller's VSYNC_END register to maintain the same VSYNC* pulse duration (nominally two-to-six lines). Within the encoder, the V_BLANKI[7:0] register must be incremented by 5 lines so the encoder can accommodate the five more lines of blanking required to start the field and still display the original active area of the frame.

For an explanation of the Left and Up buttons, simply apply the opposite offsets to the values explained for the Right and Down operations. Remember that SYNC_START/END always works in the opposite direction of picture movement. If the Position control works correctly, the end user should see a gradual change to either the X and Y position of the active image after each corresponding mouse click.

3.7.2.9 Screen Size

This control pad is used by the end user to change the active X and Y dimensions of the TV out picture. This is done by modifying the amount of horizontal (X dimension) and vertical (Y dimension) overscan compensation. Ideally, there should be four directional controls included: two for horizontal adjustment and two for vertical adjustment. For practical usage, the maximum amounts of HOC and VOC should be limited to 25 percent (or five mouse clicks in any direction). The minimal amounts of HOC and VOC should be capped at 10 percent since percentages smaller than this often make the TV image so large that all edges are behind the bezel of the TV, rendering the outer regions of the Windows™ operating system desktop useless.

Based on testing, Conexant recommends changing the HOC percentage by ~ 3 percent from its previous value for each + or – horizontal mouse click within the GUI. The + symbol denotes a larger picture size in that direction (and a decrease in the amount of horizontal blanking or HOC percent) and a – sign corresponds to smaller picture size.

In addition, TV out software designers should vary the VOC percentage by ~ 3 percent from its previous value for each + or – vertical mouse click within the GUI. The + symbol denotes a larger picture size in that direction and a – sign corresponds to smaller picture size (and an increase in the amount of vertical blanking or VOC percent).

The overscan percentages horizontally and vertically are independent of each other. However, the TV out picture looks best when HOC and VOC are equal or within 2 percent of each other. Having realized this fact, Conexant has incorporated many autoconfiguration modes that have a minimal difference (i.e., Delta) between the HOC and VOC ratios.

The autoconfiguration modes for the CX25874/875 that pertain to the desktop resolutions are summarized in Figures 3-14 through 3-19.

Figure 3-14. CX25874/875 Autoconfiguration Modes for 640 x 480 RGB In, NTSC Out Desktop Resolutions

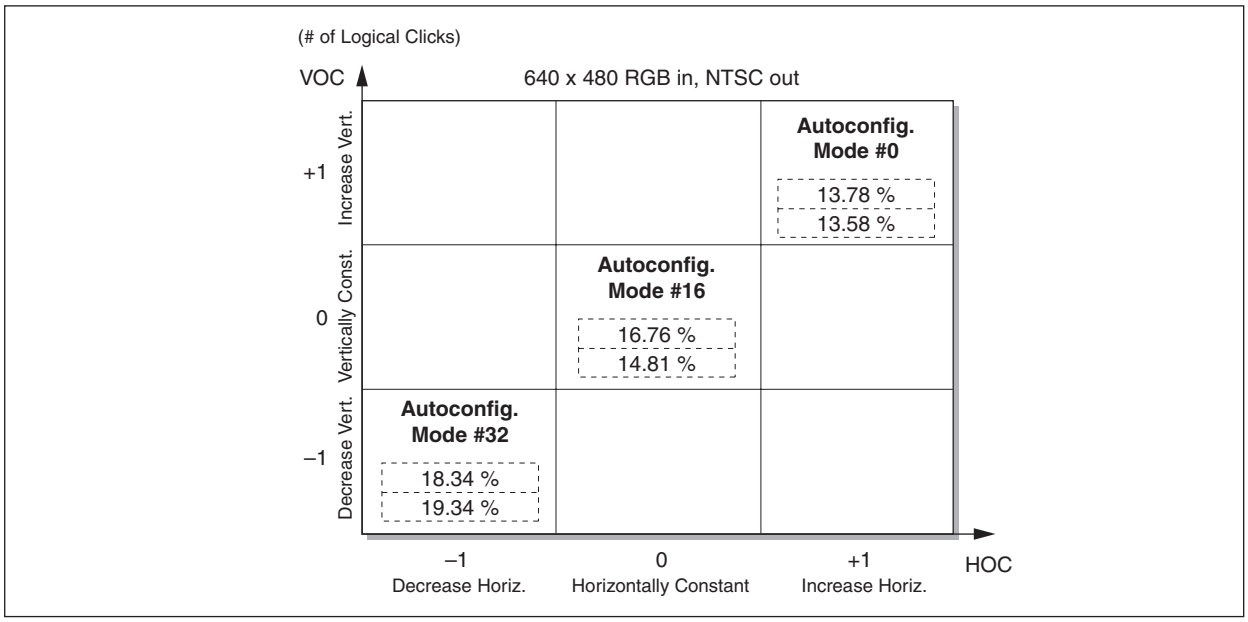


Figure 3-15. CX25874/875 Autoconfiguration Modes for 640 x 480 RGB In, PAL-BDGHI Out Desktop Resolutions

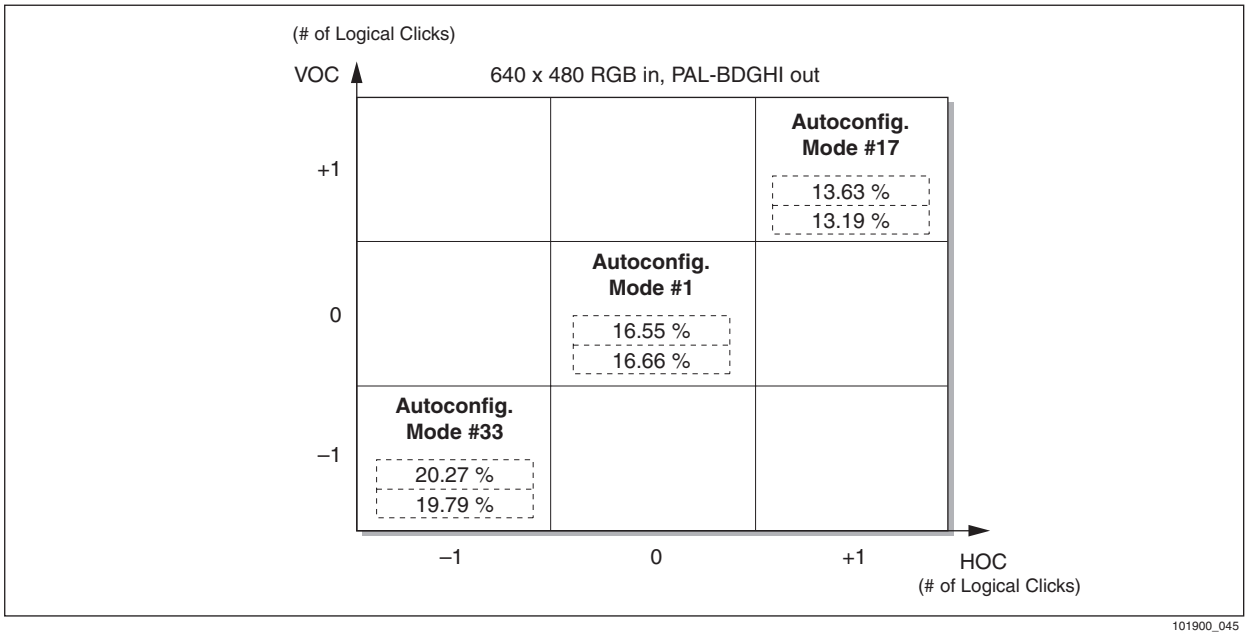


Figure 3-16. CX25874/875 Autoconfiguration Modes for 800 x 600 RGB In, NTSC Out Desktop Resolutions

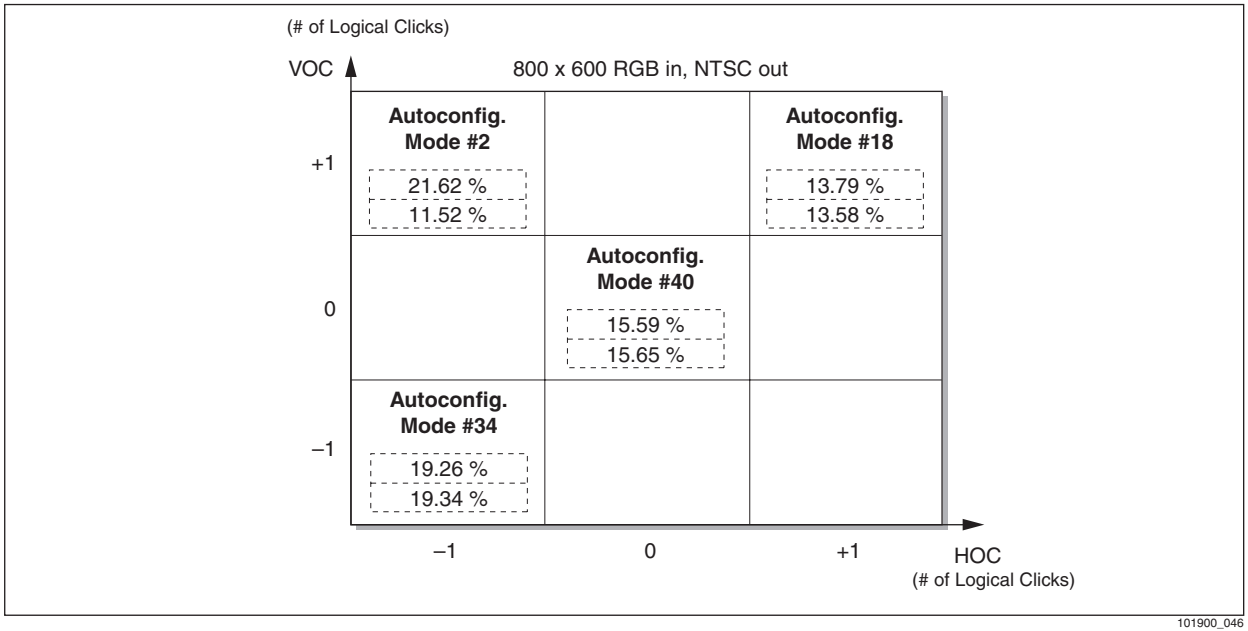


Figure 3-17. CX25874/875 Autoconfiguration Modes for 800 x 600 RGB In, PAL-BDGHI Out Desktop Resolutions

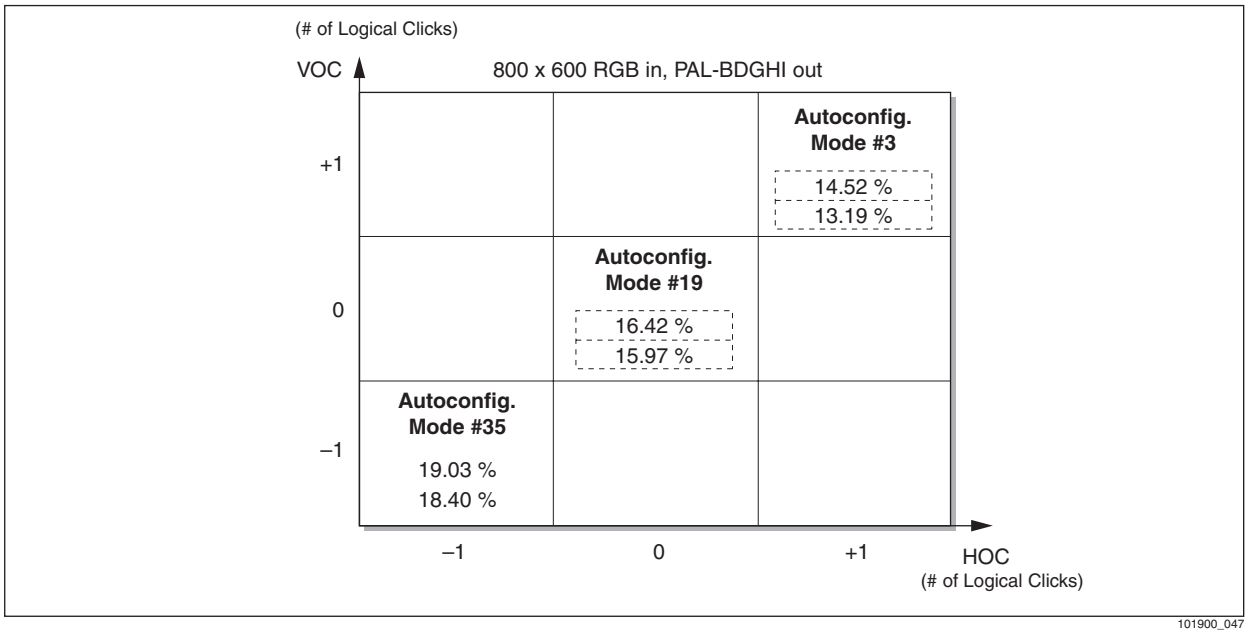


Figure 3-18. CX25874/875 Autoconfiguration Modes for 1024 x 768 RGB In, NTSC Out Desktop Resolutions

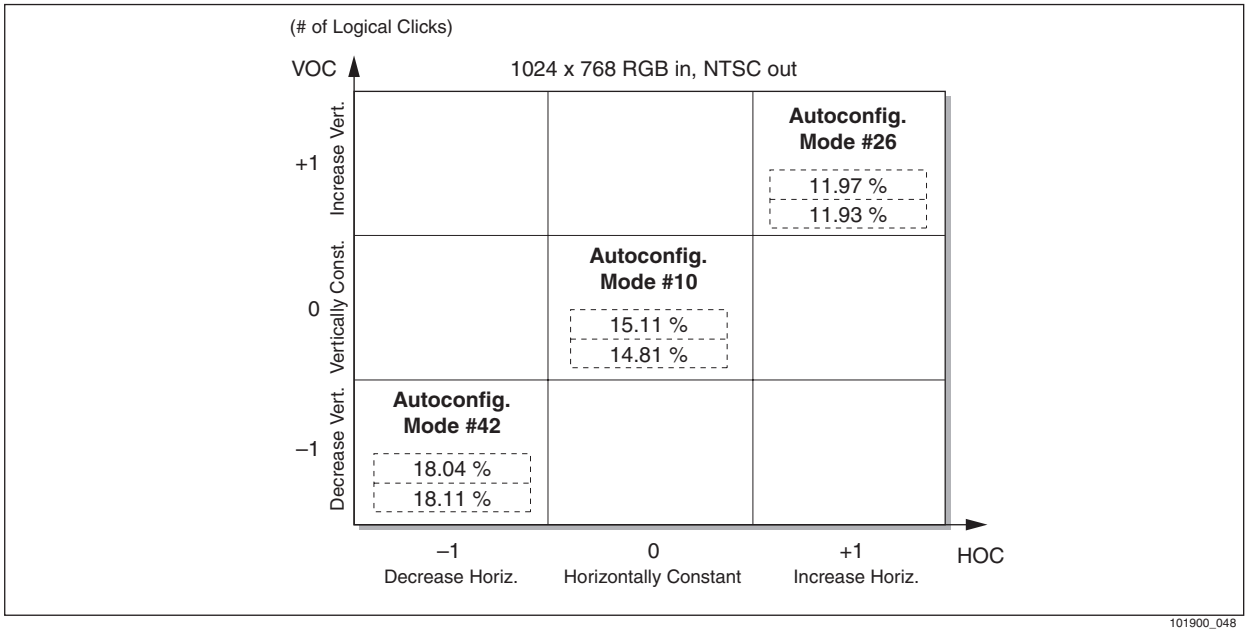
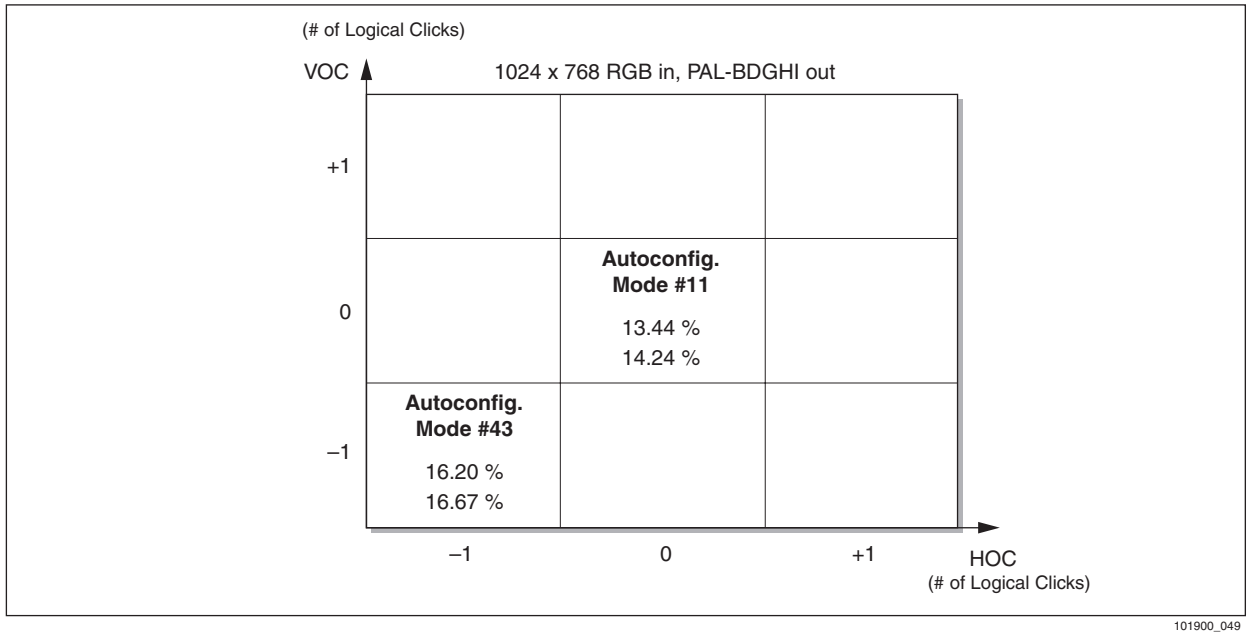


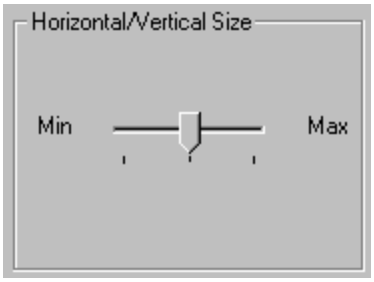
Figure 3-19. CX25874/875 Autoconfiguration Modes for 1024 x 768 RGB In, PAL-BDGHI Out Desktop Resolutions



Customers are urged to enable the autoconfiguration mode that is in the middle of each chart as the default size for each active resolution. To accomplish this, the encoder's CONFIG[5:0] bit field must be programmed to the desired mode. In addition, the graphics controller's HTOTAL register must be programmed to match the CX25874/875's H_CLKI[10:0] value, and VTOTAL register must be programmed to match the CX25874/875's V_LINESI[10:0] value. Other minor modifications may be necessary. The specific procedure to follow to enable different overscan ratios is explained in an application note titled *Supporting TV Out with Non-Standard Graphics Input Resolutions*. Request this document from your local Conexant Sales representative for help on the size video adjustment.

A simpler alternative to independent horizontal and vertical size buttons is to replace the directional control pad with a slider. This slider would only have three tick marks and would cycle through the different sizes available based on the autoconfiguration modes that exist for the specific desktop resolution and video output type. This concept is illustrated in Figure 3-20.

Figure 3-20. Direction-Less Size Control Pad



The slider would alter the horizontal and vertical size of the TV picture simultaneously by changing the overscan percentages by the same amount. Size control should only be effective for desktop resolutions such as 640x480, 800x600, and 1024x768. Nonstandard resolutions should choose a single size with a moderate amount of overscan compensation (HOC and VOC = 11 percent–16 percent) and not allow the end user to deviate from this choice by graying out the Size slider.

3.7.3 System Block Diagrams

The CX25874/875 can be designed into any system that requires analog standard-definition television outputs (NTSC/PAL/SECAM/SCART/Component YC_RC_B) or high-definition television outputs (YP_BP_R/HD RGB) based on a digital RGB or YCrCb set of inputs.

Figures 3-21 and 3-22 provide system block diagrams to illustrate several common applications which presently utilize the CX25874/875 encoder.

Figure 3-21. System Block Diagram for Desktop/Portable PC with TV Out

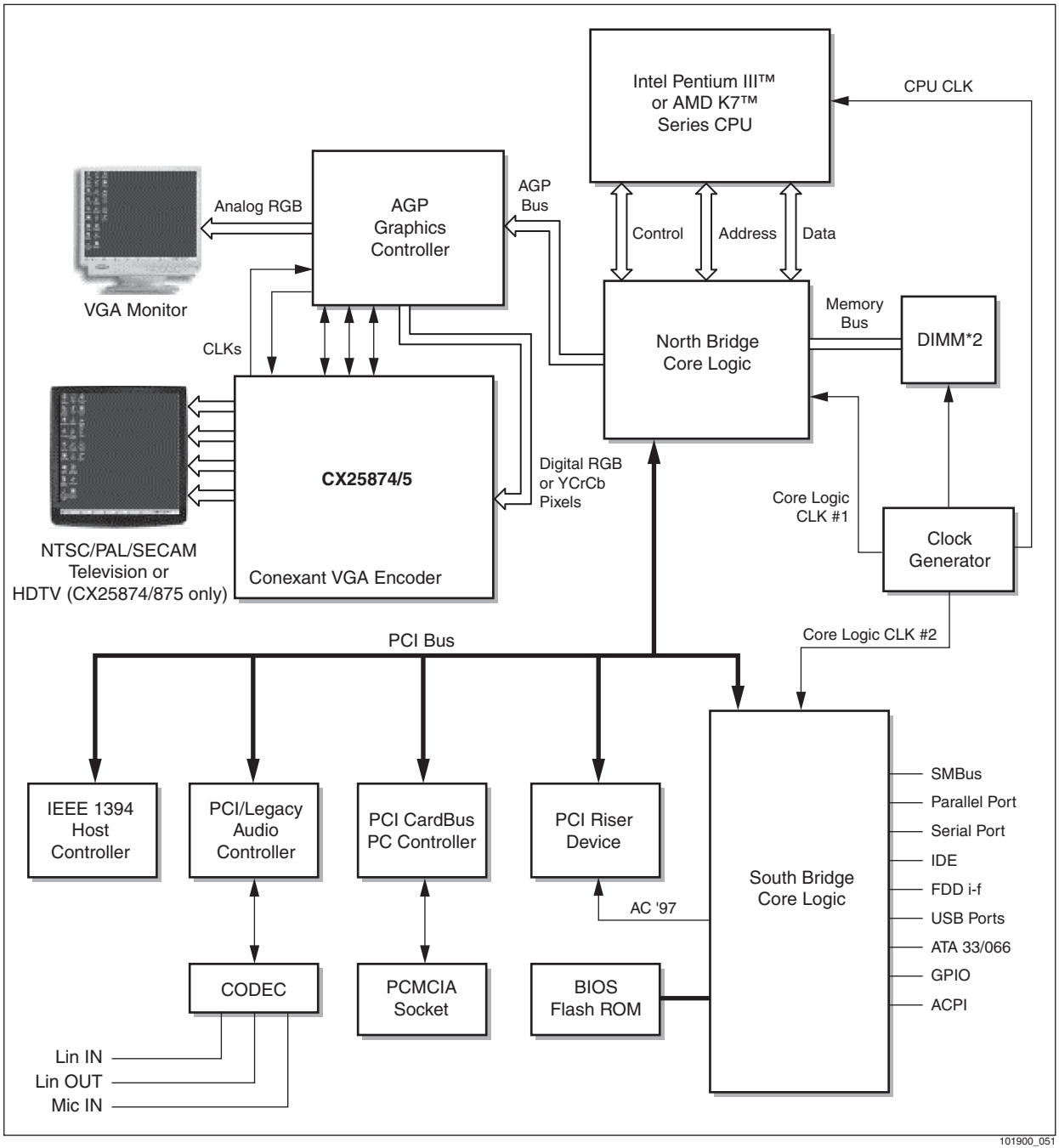
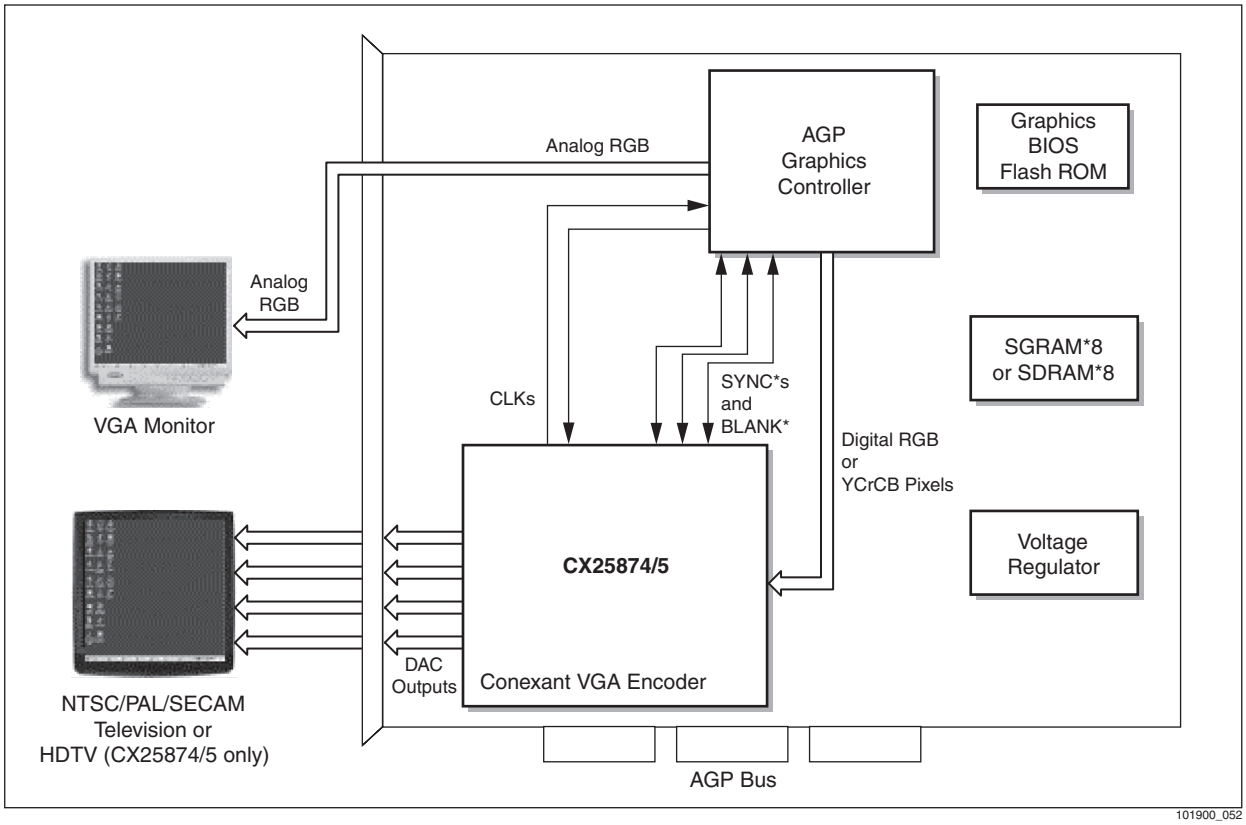


Figure 3-22. System Block Diagram for Graphics Card with TV Out



3.7.4 Electrostatic Discharge and Latchup Considerations

Correct electrostatic discharge (ESD) handling procedures are required to prevent device damage. Device damage can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided; they could delay VAA and VDD power to the device. Ferrite beads must be used only for power decoupling. Inductors cause a time-constant delay that induces latchup, and should not be substituted for a ferrite bead.

Latchup can be prevented by ensuring that all VAA and VDD pins are at the same potential and by forcing all AGND and VSS pins to be at the same potential. The VAA and VDD supply voltage must be applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

3.7.5 Clock and Subcarrier Stability

The color subcarrier frequency is derived directly from the XTALIN and XTALOUT ports when EN_XCLK=0 (master, pseudo-master interface). The color subcarrier frequency is derived directly from the main clock input, CLKI, when EN_XCLK=1 (slave interface). In either case any jitter or frequency deviation from 13.500 MHz (XTALIN and XTALOUT) or the CLKI (slave interface) rate will be transferred directly to the color subcarrier. Jitter within the valid clock cycle interval will result in hue noise on the color subcarrier on the order of 0.9–1.6 degrees per nanosecond. Random hue noise can result in degradation in the AM/PM noise ratio (typically around 40 dB for consumer media such as Videodiscs and VCRs). Periodic or coherent hue noise can result in differential phase error (which is limited to 10 degrees by FCC cable TV standards).

Any frequency deviation of CLKI from the transmitted clock (i.e., CLKO) will challenge the subcarrier tracking capability of the destination receiver. This may range from a few parts-per-million (ppm) for broadcast equipment, to 100 ppm for industrial equipment, to >100 ppm for consumer equipment. Greater subcarrier tracking range generally results in poorer subcarrier decoding dynamic range. So, receivers that tolerate jitter and wide subcarrier frequency deviation will introduce more noise in the decoded image. Crystal-based clock sources with a maximum total deviation of 50 ppm (NTSC) or 25 ppm (PAL, SECAM) across the temperature range of 0 °C to 70 °C produce the best results for consumer and industrial applications. In rare cases, temperature-compensated clock sources with tighter tolerances may be warranted for broadcast or more stringent PAL, component YC_RC_B, or HDTV applications.

Some applications call for maintaining correct Subcarrier-Horizontal (SC-H) phasing for correct color framing. This requires subcarrier coherence within specified tolerances over a four-field interval for 525-line systems or 8 fields for 625-line systems. Any clock interruption (even during vertical blanking interval) which results in mis-registration of the CLKI input or nonstandard pixel counts per line, can result in SC-H excursions outside the NTSC limit of ±40 degrees (reference EIA RS170A) or the PAL limit of ±20 degrees (reference EBU D23-1984).

In slave interface, any deviation exceeding the 50 ppm (NTSC) or 25 ppm (PAL, SECAM) limits of the number clock cycles between HSYNC* falling edges may result in an unintentional switch to Master Mode.

A list of recommended crystals and crystal vendors is contained in Appendix B. Do not substitute another 13.500 MHz crystal for one of those found in Appendix B unless the crystal delivers the following performance criteria:

- Mode of Operation: Fundamental
- Load Capacitance: 20 pF (for a crystal circuit using 27 pF and 33 pF capacitors)
- Temperature Range: 0 °C – 70 °C
- Frequency Tolerance: 25 ppM total recommended; includes both the tolerance at 25 °C and stability over 0 °C – 70 °C
- Miscellaneous: Crystal must operate in parallel resonance and not in series resonance

Additional testing is often necessary to determine the routing capacitance of the crystal holder from pin to pin. If these items are not known, the designer should try crystals with higher or lower load capacitances (e.g., 16 pF, 18 pF, 22 pF) or adjust the capacitors to GND from XTALIN and XTALOUT by 3 pF–7 pF each to fine tune the oscillating frequency. To reiterate, 13.5000 MHz must be generated with a maximum tolerance of ±338 Hz to generate high-quality standard-definition or HDTV video.

3.7.6 Radio Frequency Modulator Issues and Filtering

The CX25874/875 internal upsampling filter alleviates external filtering requirements by moving significant sampling alias components above 19 MHz and reducing the sinx/x aperture loss up to the filter's passband cutoff of 5.75 MHz. While typical chrominance subcarrier decoders can handle the CX25874/875 output signals without analog filtering, the higher frequency alias products pose some EMI concerns and may create troublesome images when introduced to a radio frequency (RF) modulator. When the video is presented to an RF modulator, it should be free of energy in the region of the aural subcarrier (4.5 MHz for NTSC, 5.5–6.5 MHz for PAL). Hence some additional frequency traps may be necessary when the video signal contains fundamental or harmonic energy (as from unfiltered character generators) in that region. Where better frequency response flatness is required, some peaking in the analog filter is appropriate to compensate for residual digital filter losses with sufficient margin to tolerate 10 percent reactive components.

A three-pole elliptical standard-definition (SD) low-pass filter (one inductor, three capacitors) with a 6.75 MHz passband can provide at least 45 dB attenuation (including sinx/x loss) of frequency components above 20 MHz and provide some flexibility for mild peaking or special traps. An inductor value with a self-resonant frequency above 80 MHz is chosen so that its intrinsic capacitance contributes less than 10 percent of the total effective circuit value. The inductor itself may induce 1 percent (0.1 dB) loss. Any additional ferrites introduced for EMI control should have less than 5 Ω impedance below 5 MHz to minimize additional losses. Any capacitors to ground from the output pins are compensating for the parasitic capacitance of the chip plus any protection diodes and lumped circuit traces (about 22 pF + 5 pF/diode). Some filter peaking can be accomplished by splitting the 75 Ω source impedance across the reactive PI filter network. However, this will also introduce some chrominance-luminance delay distortion in the range of 10–20 ns for a maximum of 0.5 dB boost at the subcarrier frequency.

The filter network feeding an RF modulator may include the aforementioned trap, which could take two forms depending on the depth of attenuation and type of resonator device employed. Contact your local Conexant field applications engineer for an illustration of the trap circuit.

The trap circuitry can interact with the low-pass filter, compromising frequency response flatness. A simple PNP buffer can preserve the benefits of an oversampling encoder when simultaneous Composite Video Baseband Signals (CVBS) are required for driving external cables. In addition, an active video buffer, serves to isolate the RF modulator signal amplitude from anomalies in the external termination. This buffer can be implemented with a transistor array or video amplifier IC which provides a gain of two (before series termination), capable of driving 740 µA into the 75 Ω destination, and is biased within its input/output compliance range. When simultaneous Y/C (S-video) outputs are not required, a second CVBS signal can be created (with a 600 mV sync to tip offset) by tying these pins together with a single termination resistor (typically 75 Ω) and driving the low-pass filter circuit.

The RF modulator typically has a high input impedance (about 1 k Ω ±30 percent) and loose tolerance. Consequently, the amplitude variation at the modulator input will be greater, especially when the trap is properly terminated at the modulator input for maximum effect. Some modulators, video or aural fidelity, degrade dramatically when overdriven, so the value of the effective termination (nominally 37.5 Ω) may

need to be adjusted downward to maintain sufficient linearity (or depth of modulation margin) in the RF signal.

A two-section trap (with associated inductor) may be warranted to achieve better than 20 dB attenuation when stereo, SAP, or AM aural carriers are generated, or when >40 dB audio dynamic range is desired. Some impedance isolation (e.g., buffer) may be required before the trap to obtain the flattest frequency response.

3.8 CX25874/5 Evaluation Kits

Several reference design kits are available to demonstrate this encoder's features, to evaluate Conexant's encoder technology and TV out quality, and to facilitate implementation of the CX25874 or CX25875 into a customer's graphics subsystem.

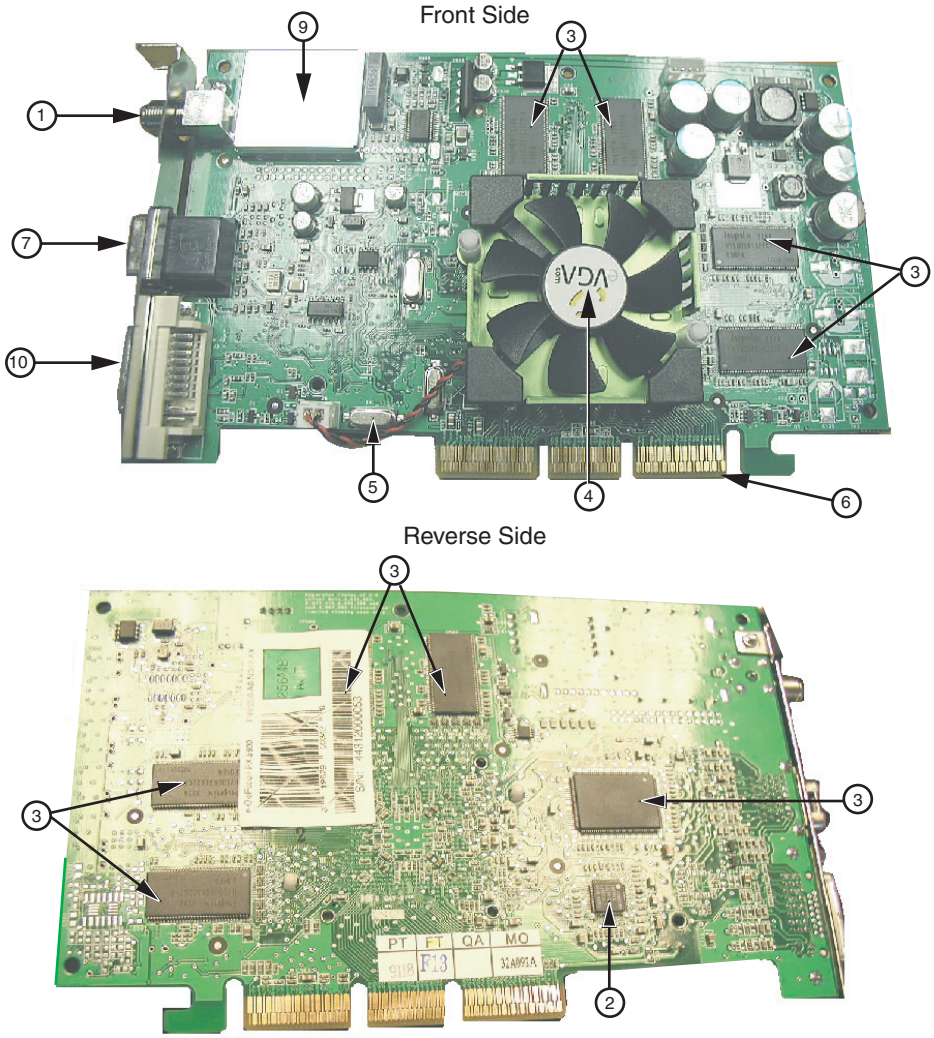
The first and most feature-rich kit is called the CX875EVK. The CX875EVK is an evaluation platform consisting of a single piece of hardware: the eVGA-manufactured and NVidia-designed GeForce FX 5600 GPU-based AGP graphics card, coupled with drivers from NVidia and encoder software from Conexant. The CX25875 encoder, mounted on the AGP card, is initialized and programmed through the NVidia software drivers and fine-tuned by using a Windows XP-compatible software application called Aquila Cockpit. The graphics card is designed to work with any present-day personal computer which runs on the Microsoft Windows XP operating system. The target personal computer should contain an Intel Pentium III™, IV™, or AMD Athlon®, Duron®, or other microprocessor. The GeForce FX 5600 GPU and CX25875 encoder exchange 24-bit RGB data, syncs, and clocks in pseudo-master interface using a 16-signal wide parallel bus called DVO.

The CX875EVK (ordering # CX04-D460) is specifically designed for video systems requiring the generation of high-quality flicker-free Composite, Y/C (S-Video), and Component Y PRPB (HDTV) signals from various RGB digital streams. The CX875EVK is used as a SDTV out demonstration tool for 640x480, 800x600, and 1024x768 desktop and 720x480, and 720x576 DVD active resolutions. This card is among the industry's first to provide HDTV out for 720x480 (480p), 1280x720 (720p), and 1920x1080 (1080i) active resolutions. Other resolutions are also possible in HDTV through NVidia's ingenious HDTV pan and overscan features. This EVK is also used as a basic development tool for display of nonstandard resolutions and different overscan compensation ratios. Custom register set generation, for the CX25875, based on a set of desired input conditions, is also possible with the CX875EVK through Aquila Cockpit.

Conexant's encoder software will not be shipped within this kit. This must be downloaded from the CX25875 http://www7.conexant.com/cx875 Secured web site after obtaining the site username and password. Graphics drivers for the NVidia GeForce FX 5600 are required as well, but are also not included. Visit the NVidia driver download website for this software.

Figure 3-23 shows the location of various components on the graphics card that comprises the CX875EVK kit.

Figure 3-23. GeForce FX 5600 CX875EVK Hardware: Front and Reverse Sides



1. Cable TV input: Attach the coaxial cable connector from either your cable system or your antenna directly to the input. Not needed for TV Out.
2. Conexant CX25875-14 TV Out encoder: CX25874 cannot be used as a substitute as of the print date of this manual (5/04) due to NVidia driver incompatibilities.
3. 256 MB DDRAM memory: 128-bit DDR Memory Interferrence used; 4 billion Msamples per second, 8.0 GB/s memory bandwidth.
4. NVidia GeForce FX5600 GPU with AGPx: See Section 2 for a summary of key graphics card and GPU features. GPU under cooling fan.
5. HC49/U surface mount crystal for CX25875: 13.500 MHz, fundamental mode of operation, 20 pF load preferred with parallel resonance, 25 PPM total tolerance at room and over temperature range 0 °C to 70 °C required.
6. Accelerated Graphics Port Interface: Must be plugged into an open AGP slot within the Windows-based personal computer loaded with Microsoft Windows XP. Power and ground are received from this bus.
7. VIVO Video Breakout Box: Plug the Video Breakout male cable included with the CX875EVK kit into this connector. This connector supports Composite Video Out (yellow connector), S-Video (black 5-pin connector, or HDTV YPRPB (Green, Red, and Blue, respectively). This connector also suports the VGA R/G/B analog output through the 15-pin VGA connector. CX875EVK delivers Single-Display VGA, Single-Display TV Out, or both simultaneously through Clone mode or Dual-Display mode.
8. DAC output filter circuits: Each filter contains 3 capacitors and 1 inductor to create a 30 MHz passband, satisfactory for both standard definition TV outputs such as NTSC/PAL/SECAM and high-definition TV outputs. These filters are embedded in the VIVO Video Breakout Box.
9. TV Tuner: Demodulates and tunes incoming broadcast TV input for display and capture.
10. 28-pin DVI-I connector: When connected to a DVI-compliant Flat Panel monitor, up to 1600 x 1200 resoltuion digital video out or VGA is possible. Plugging DVI-I to 15-pin VGA adapter into this forces CX875EVK to output secondary VGA R/G/B analog output.

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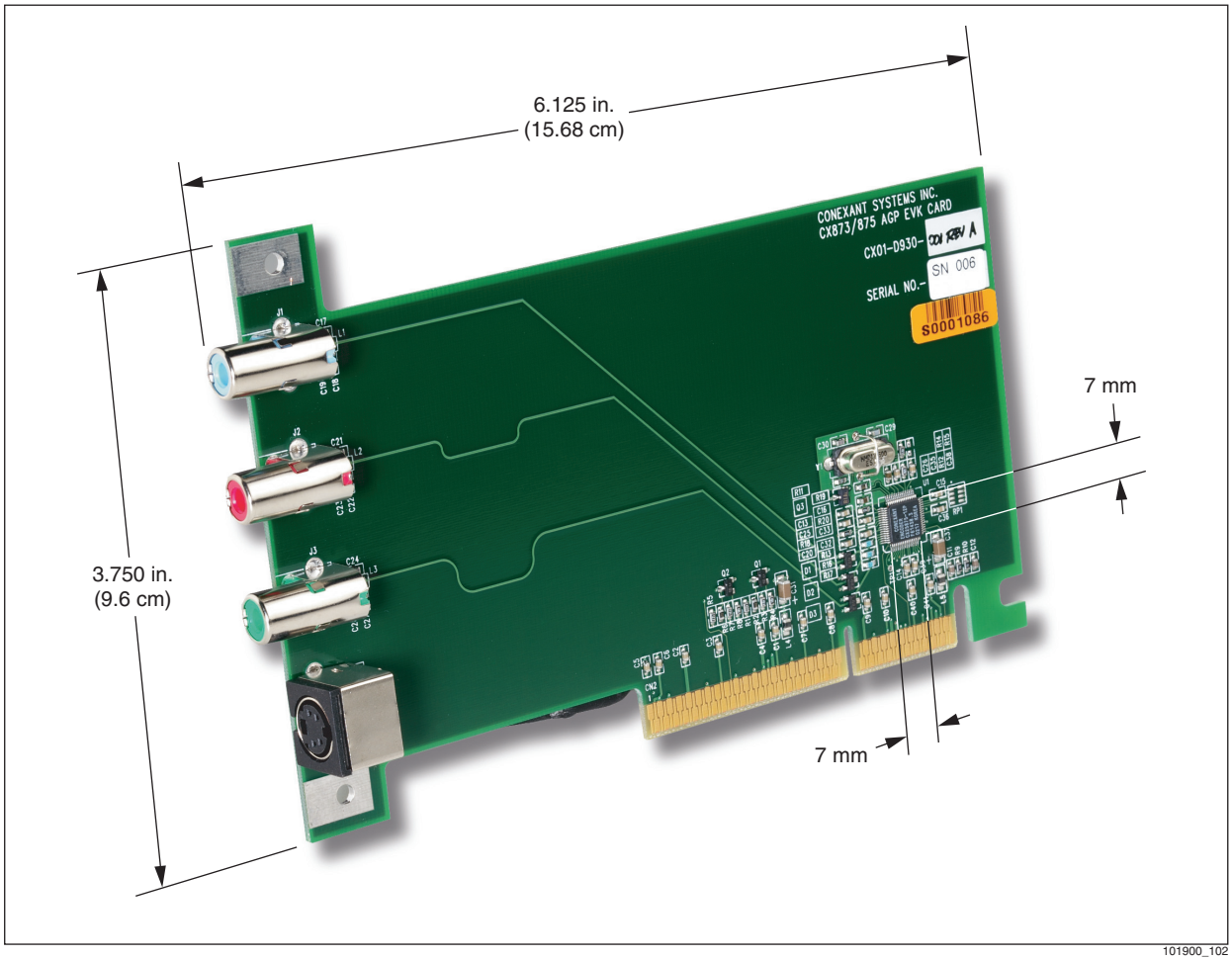
The second kit available is the CX875AGP EVK. This evaluation kit is an AGP plug-in card providing TV out capability for the NVidia nForce and nForce2 IGP core logic + GPU Devices. This combination type of master device is almost always mounted directly on a desktop or notebook computer's motherboard. The card itself contains only the required hardware for the TV out function and cannot generate TV out or even power up without a motherboard and AGP slot powered by the nForce series chipset.

The CX875AGP EVK hardware offers support for S-Video and Composite video. The hardware is controlled by a set of drivers written by NVidia. A recent set of nForce/nForce2 drivers should be already installed on PCs containing an nForce2 device. When drivers are not included within the PC, they must be downloaded and installed from the NVidia website directly.

Figure 3-24 shows the location of various components on the CX875AGP card that comprises the CX875AGP EVK kit.

Figure 3-24. CX875AGP Card

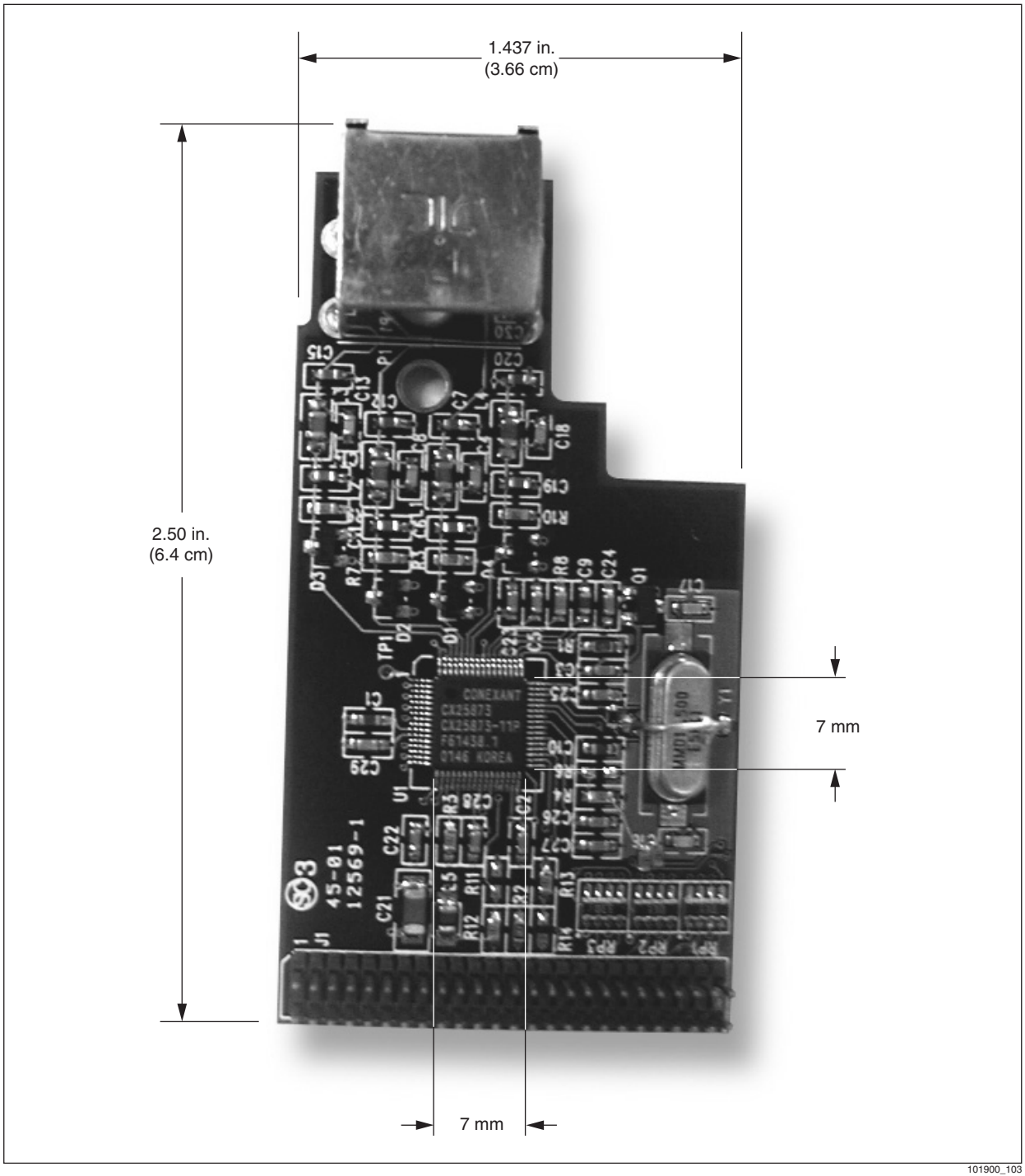


The third kit, named the CX875DCGF2EVK, is a two-card platform that mates together through a unique 50-pin, two-row header. Like all EVKs for the CX25875, this is an evaluation platform intended to demonstrate features and performance of the Conexant CX25874/5 VGA to TV encoder. The kit consists of two hardware cards: the NVidia GeForce2 AGP card, and the compact Conexant TV out module. The

CX25875 encoder, mounted on the TV out module, is programmed using this aforementioned Windows XP-compatible software application called Aquila Cockpit. The CX25875 daughter card is designed to work within certain NVidia graphics cards containing the GeForce2 graphics controller and a dedicated 50-pin, two-row connector.

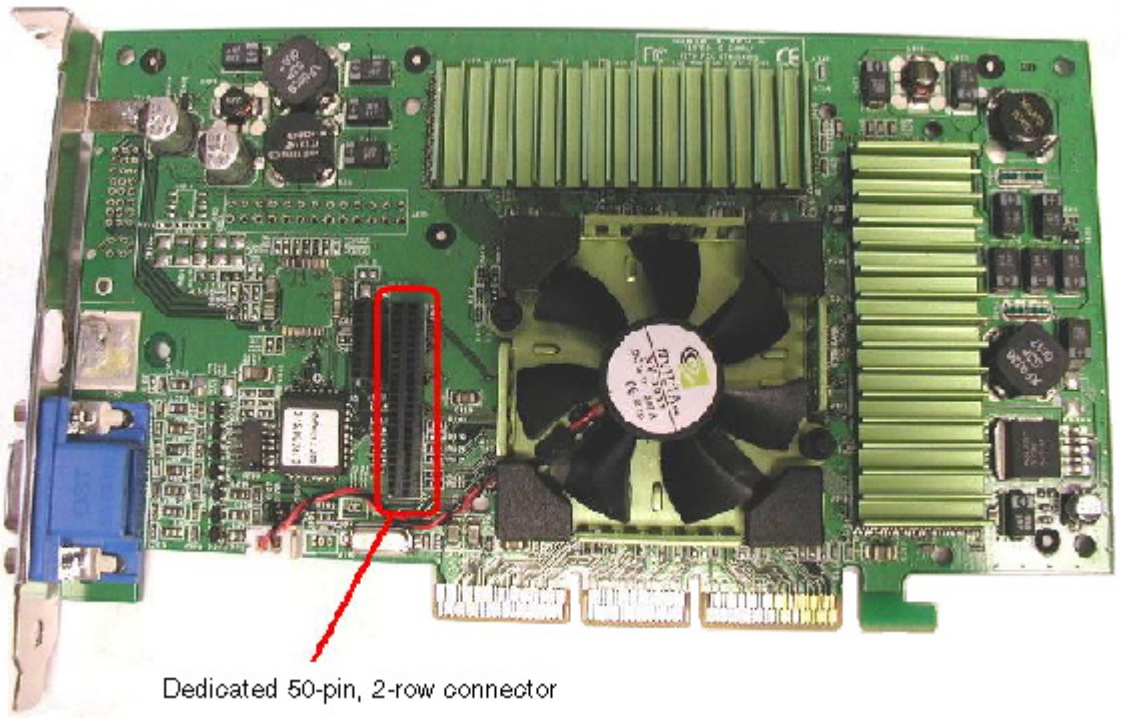
This platform's daughter card (DC) is shown in Figure 3-25.

Figure 3-25. CX25875 Daughter Card/ TV Out Module



This platform's GeForce2 MX based graphics card is shown in Figure 3-26. The two cards will be shipped within the kit connected to each other but they can be detached and used separately as necessary.

Figure 3-26. CX875DCGF2EVK's GeForce2 MX-Based Graphics Card

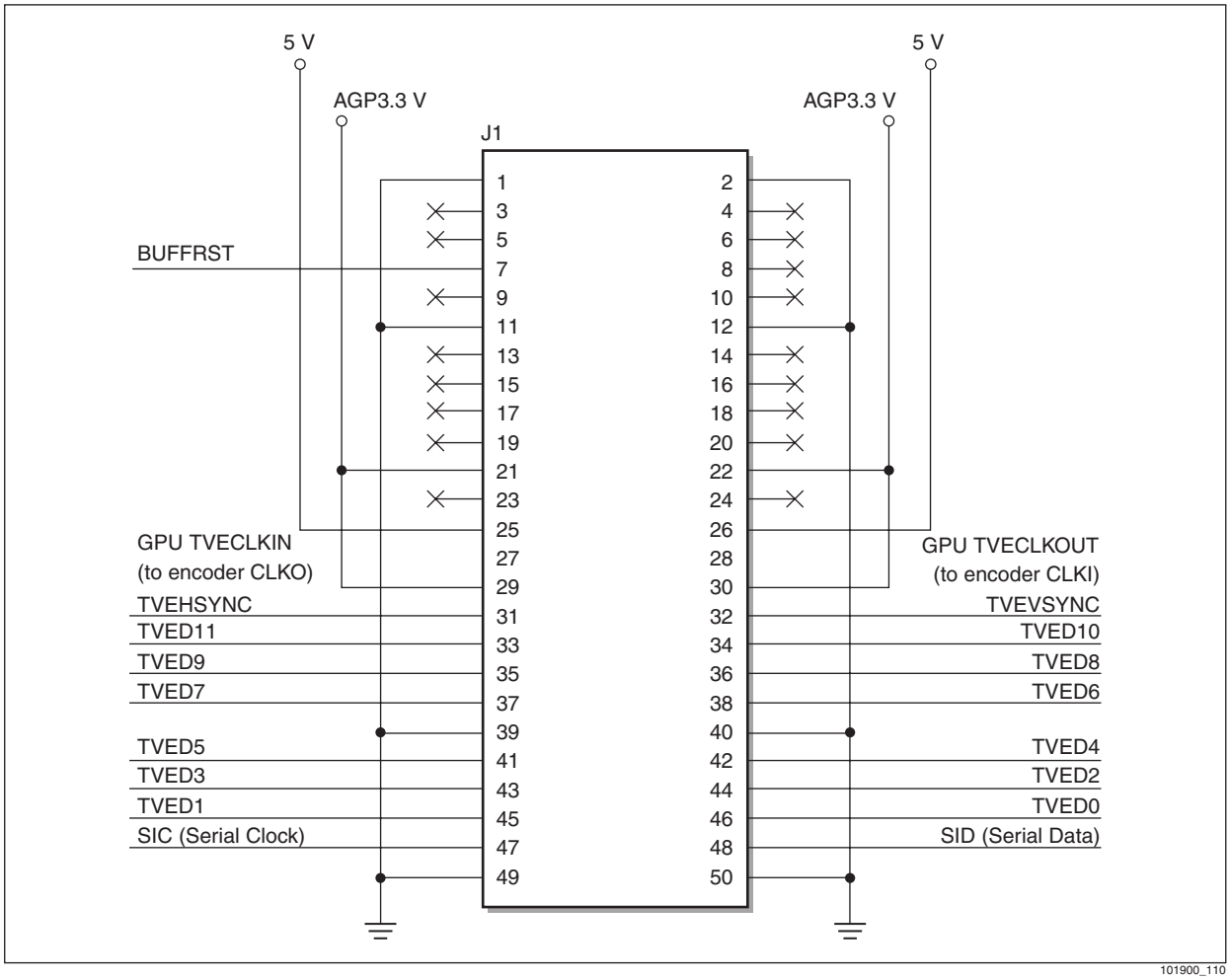


Since no other GPU vendors now produce graphics cards with this proprietary 2-row connector, after initial evaluation, this kit will have residual benefit in prototype development by detaching the daughter card and thus the encoder altogether and blue-wiring the pixel and control signals over to a new platform.

This blue-wire operation should only be done if a re-layout of a graphics card to accommodate the CX25874/5 encoder itself is not possible or it is too time consuming to do so. Initial prototyping with the TV out module and another GPU can be done by attaching each required encoder signal to the master device's input or output by soldering a wire from the appropriate pin on the header to a suitable point on the card containing the master device.

To facilitate this implementation, a connection diagram for the header mounted on the CX25874/5 daughter card/TV out module is shown in Figure 3-27. The header again is a 50-pin, dual-row, 0.05 cm x 0.05 cm male type.

Figure 3-27. Connection Diagram for the Dual-Row 50-pin Header on TV Module / Daughter Card Connection Diagram for the Dual-Row 50-pin Header on Daughter Card/TV Module



Each evaluation kit connects the encoder to a different master device. Thus, the format and type of interface the encoder uses to transmit and receive digital data and control signals varies from kit to kit. Interface possibilities include the AGP bus for connection to a core logic IC with an integrated graphics core, a local parallel data bus for connection to a graphics controller using point-to-point signal traces, a male header, a transposer board, a set of blue-wires, or even a ribbon cable. Different evaluation kits also provide different types of television outputs. Standard NTSC and PAL will always be possible through Composite and S-Video outputs. Higher featured kits will also make SECAM, PAL-60, PAL-Nc (Argentina), PAL-M (Brazil), Component Y CR CB (YUV 480i), HDTV YPRPB, and/or VGA RGB outputs available as well either through command-prompt based scripts files or the graphics drivers themselves. All necessary documents including an installation/instruction manual, pertinent software files, scripts (to enable optimal TV out quality), test images, video clips, schematics, and bill of materials are enclosed within each kit's encoder software .exe file downloaded from a the CX25875 secured HTTPs: website so setup and installation time is minimized.

All EVK kits will contain a customer letter describing the kit and an installation manual on how and where to download the correct graphics adapter drivers. Conexant ships adapters and cables with various kits to enable those video outputs that require three or four signals such as Component Y CR CB (YUV 480i), HDTV YPRPB, and SCART.

Ordering numbers and prices for each CX25874/5 Evaluation Kit can be obtained by calling your local Conexant Systems sales office or speaking with a field applications engineer.

Additional encoder evaluation kits and hardware are often under development with different interfaces to other master devices. Although there is no generic method yet to connect this encoder to the GPUs that often drive it, most Conexant evaluation kits expose all necessary digital interface signals for customization. Companies interested in designing with the CX25874/5 are urged to contact their local Conexant Systems sales office for technical assistance with their particular video subsystem. Reference designs created by Conexant are not intended to be manufactured by those using it and are strictly for evaluation purposes only. Expectations are that after schematic and layout reviews, some modifications will need to be done to each customer design. Additional software code and a revised driver for the master IC would also need to be developed to generate TV out directly from the CX25874/5 encoder.

3.9 Serial Interface

3.9.1 Data Transfer on the Serial Interface Bus

Figure 3-28 illustrates the relationship between SID (Serial Interface Data) and SIC (Serial Interface Clock) to be used when programming the internal registers via the Serial Interface bus. If the bus is not being used, both SID and SIC lines must be left high.

Every byte put onto the SID line should be 8 bits long (MSb first), followed by an acknowledge bit, which is generated by the receiving device. Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the slave device address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SID line low during the ninth clock pulse, then accept the data in subsequent bytes (auto-incrementing the subaddress) until another stop condition is detected.

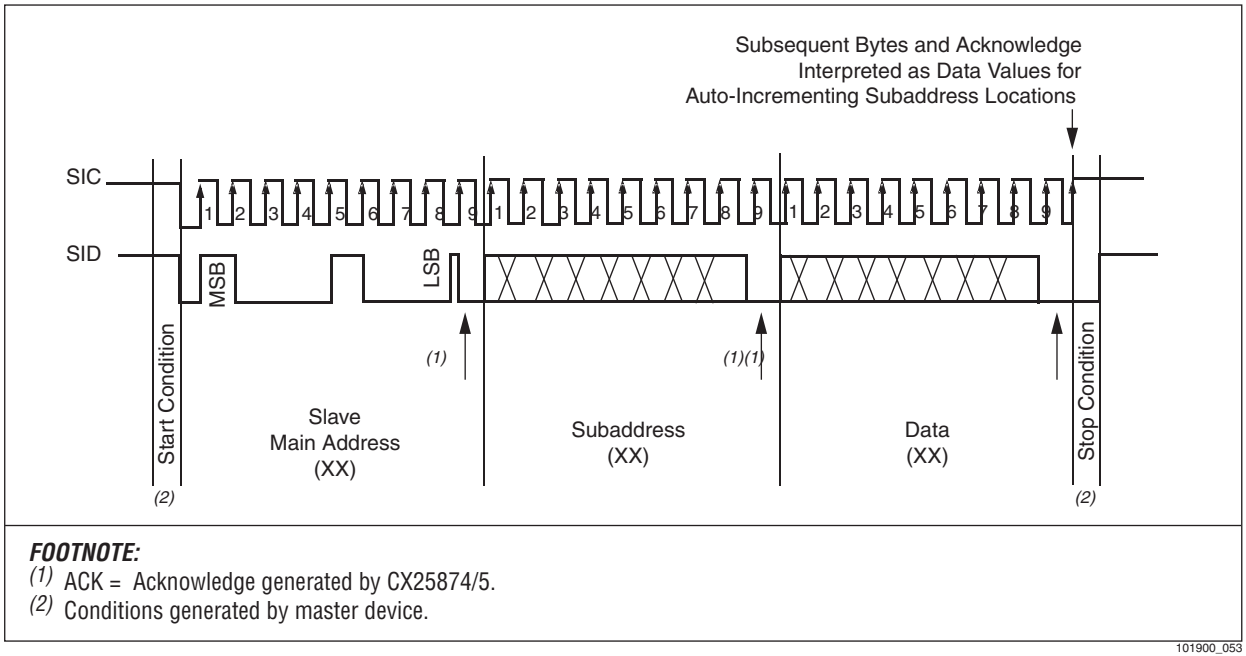
The eighth bit of the address byte is the read/write bit (high = read from addressed device; low = write to the addressed device). Data bytes are always acknowledged during the ninth clock pulse by the addressed device.

NOTE: During the acknowledge period, the transmitting device must leave the SID line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the CX25874/875 will remain in the state defined by the last complete data byte transmitted and any master acknowledge subsequent to reading the chip ID (subaddress 0x89 if ALTADDR pin is 0) is ignored.

The maximum serial interface speed for the CX25874/875 is 400 kHz.

Figure 3-28. Serial Programming Diagram for SIC and SID Signals



FOOTNOTE:
(1) ACK = Acknowledge generated by CX25874/5.
(2) Conditions generated by master device.

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4 Parametric Information

4.1 DC Electrical Parameters

DC electrical parameters are defined in Tables 4-1 through 4-3.

Table 4-1. DC Recommended Operating Condition

Parameter	Symbol	Min	Typical	Max[2]	Units
Power Supply	VAA_BG, VAA_DAC, VDDHV, VAA_OSC,	3.15	3.30	3.45	V
VDD Core Supply	VDD	1.24	1.3	1.36	V
Serial Input Supply (CX25874/875's serial bus always operates from 3.3 V to 1.1 V)	VDD_SIO	3.15	3.30	3.45	V
Low-Voltage Supply (for interface to 2.5 V master)[1]	VDDO, VDD_SIO	2.38	2.5	2.63	V
Low-Voltage Supply (for interface to 1.8 V master)[1]	VDDO, VDD_SIO	1.71	1.80	1.89	V
Low-Voltage Supply (for interface to 1.5 V master)[1]	VDDO, VDD_SIO	1.425	1.50	1.575	V
Low-Voltage Supply (for interface to 1.3 V master)[1]	VDDO, VDD_SIO	1.235	1.30	1.365	V
Low-Voltage Supply (for interface to 1.1 V master)[1]	VDDO, VDD_SIO	1.045	1.10	1.155	V
Voltage Supply (for interface to 3.3 V master)	VDDO, VDD_SIO	3.15	3.30	3.45	V
Ambient Operating Temperature	T_A	0	—	70	°C
Total DAC Terminated Load	R_{TERM}	37.1	37.5	37.9	Ω
Nominal RSET (series resistor FSADJUST pin to GND)	R_{SET}	398	402	406	Ω

FOOTNOTE:

(1) Any low-voltage interface from 1.1 V to 3.3 V can be accommodated by supplying the VDDO and VDD_SIO pins with the corresponding lower voltage supply ± 5%.

(2) Stresses above those listed in this column can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 4-2. DC Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max[2]	Units
Voltage on Any Signal Pin [1]	—	GND – 0.5		VDDx + 0.5[3]	V
Analog Output Short Circuit Duration to Any Power Supply or Common Ground	I_{SC}	—	—	Unlimited	Sec
Storage Temperature	T_S	–65	—	+150	°C
Junction Temperature	T_J	—	—	+125	°C
Peak Reflow Temperature	T_{VSOL}	—	—	220	°C
Thermal Resistance of Package	θ_{JA}	—	69	—	°C/W

FOOTNOTE:

[1] This device employs high-impedance CMOS circuitry on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.

[2] Stresses above those listed in this column can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

[3] VDDx refers to VAA_DAC, VDDO, VDD_SIO, VDDHV, VAA_OSC, VDD, VAA_BG.

Table 4-3. DC Characteristics for CX25874/875

Parameter	Symbol	Min	Typical	Max	Units
Video D/A Converter Resolution	—	10	10	10	Bits
Output Current-DAC Code 1023 (Iout full scale)	—	—	34.13	—	mA
Output Voltage-DAC Code 1023	—	—	1.28	—	V
Video Level Error (nominal resistors)	—	—	—	5	%
Output Capacitance (of DAC output)	—	—	22	—	pF
Input High Voltage @ 3.3 V (normal operation)	VIH	2.4	—	VDDO + 0.5	V
Input High Voltage @ 2.5 V (low-voltage pins)	VIH	1.75	—	VDDO + 0.5	V
Input High Voltage @ 1.5 V (low-voltage pins only)	VIH	1.05	—	VDDO + 0.5	V
Input High Voltage @ 1.1 V (low-voltage pins only)	VIH	0.77	—	VDDO + 0.5	V
Input Low Voltage @ 3.3 V (normal operation)	VIL	GND – 0.5	—	0.8	V
Input Low Voltage @ 2.5 V (low-voltage pins only)	VIL	GND – 0.5	—	0.6	V
Input Low Voltage @ 1.5 V (low-voltage pins only)	VIL	GND – 0.5	—	0.45	V
Input Low Voltage @ 1.1 V (low-voltage pins only)	VIL	GND – 0.5	—	0.33	V
Input High Current (Vin = 2.4 V)	IIH	—	—	1	µA
Input Low Current (Vin = 0.4 V)	IIL	—	—	–1	µA
Input Capacitance (f =1 MHz, Vin = 2.4 V)	CIN	—	7	—	pF
Input High Voltage (SIC, SID)	VIH	0.7 * VDD	—	VDD_SIO + 0.5	V
Input Low Voltage (SIC, SID)	VIL	GND – 0.5	—	0.3 * VDD_SIO	V
Output High Voltage @ 3.3 V (IOH = –400 µA)	VOH	2.4	—	VDDO	V
Output Low Voltage 3.3 V (IOL = 3.2 mA)	VOL	GND	—	0.4	V
Output High Voltage @ 1.1 V (IOH = –400 µA)	VOH	VDDO – 0.2	—	VDDO	V
Input Low Voltage @ 1.1 V (IOL = 3.2 mA)	VOL	GND	—	GND + 0.2	V
Three-State Current	IOZ	—	—	50	µA
Output Capacitance	CDOUT	—	10	—	pF

GENERAL NOTE: The above parameters are guaranteed over the full temperature range (0 °C to 70 °C), temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 3.3 V.

4.2 AC Electrical Parameters

AC electrical parameters are defined in Table 4-4.

The AC characteristics for the CX25874/5 were derived under the following normal test conditions. DAC output load ≤ 75 pF. HSYNC*, VSYNC*, BLANK*, and FIELD output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 3.3 V.

Table 4-4. AC Characteristics for CX25874/875 *(1 of 4)*

Parameter			Symbol	Min	Typical	Max	Units
	EIA/TIA 250C Ref	CCIR 567					
Hue Accuracy (1)	—	—	—	—	–0.8	—	deg p–p
Chroma Amplitude Accuracy (1)	—	—	—	—	–0.6	—	% p–p
Chroma AM Noise (all fields)	1 MHz Red Field	—	—	—	–61.2	—	dB rms
Chroma PM Noise (all fields)	1 MHz Red Field	—	—	—	–60.9	—	dB rms
Differential Gain	6.2.2.1	C3.4.1.3	—	—	0.4	—	% p–p
Differential Phase	6.2.2.2	C3.4.1.4	—	—	1.1	—	deg p–p
RMS SNR (unweighted 100 IRE Y ramp tilt correct)	6.3.1	—	—	—	–52.04	—	dB rms
Peak Periodic SNR @ 3.58 MHz	6.3.2	—	—	—	–75.2	—	dB p–p
100 IRE Multiburst	6.1.1	—	—	—	100.5	—	IRE
Multiburst @ 0.50 MHz	—	—	—	—	–0.05	—	dB
Multiburst @ 1.0 MHz	—	—	—	—	–0.11	—	dB
Multiburst @ 2.00 MHz	—	—	—	—	–0.20	—	dB
Multiburst @ 3.00 MHz	—	—	—	—	–0.31	—	dB
Multiburst @ 4.0 MHz	—	—	—	—	–0.46	—	dB
Multiburst @ 5.75 MHz	—	—	—	—	–1.54	—	dB
Chroma/Luma Gain Ineq	6.1.2.2	C3.5.3.1	—	—	96.8	—	%
Chroma/Luma Delay Ineq	6.1.2	C3.5.3.2	—	—	–1.01	—	ns
Short Time Distortion 100 IRE/ PIXEL (rising edge)	6.1.6	—	—	—	0.5	—	%
Short Time Distortion 100 IRE/ PIXEL (falling edge)	6.1.6	—	—	—	0.5	—	%
Luminance Nonlinearity	6.2.1	—	—	—	1.1	—	% p–p
Chroma/Luma Intermod	6.2.3	—	—	—	0.25	—	%
Chroma Nonlinear Gain	6.2.4.1	—	—	—	–3.3	—	%
Chroma Nonlinear Phase	6.2.4.2	—	—	—	0.4	—	deg

Table 4-4. AC Characteristics for CX25874/875 *(2 of 4)*

Parameter			Symbol	Min	Typical	Max	Units
	EIA/TIA 250C Ref	**CCIR 567**					
PSRR (Power Supply Ripple Rejection Ratio) of DAC output (full scale)	—	—	—	—	30[2]	—	dB
Pixel/Control Setup Time	—	—	1	3	—	—	ns
Pixel/Control Hold Time	—	—	2	0	—	—	ns
Control Output Delay Time [3]	—	—	3	—	—	10.0	ns
Control Output Hold Time [3]	—	—	4	2	—		ns
CLKI/O Frequency (standard mode)	—	—	—	—	—	80.0	MHz
CLKI/O Pulse Width Low Duty Cycle [4]	—	—	—	40	50	60	%
CLKI/O Pulse Width High Duty Cycle [4]	—	—	—	40	50	60	%
CLKO to CLKI Delay	—	—	7	—	—	0.8	CLKO cycles
Parameter			**Symbol**	**Min**	**Typical**	**Max**	**Units**
HDTV Output Timing Characteristics: 1080i (see Figure 4-9)							
Low-Sync Width			α	—	610	—	ns
Start of Line to End of Active Video			β	—	28.409	—	µs
High-Sync Width			χ	—	600.2	—	ns
Rising Edge of Sync to Start of Broad Pulse			δ	—	1.792	—	µs
Start of Line to Start of Active Video			ε	—	2.642	—	µs
Sync Rise Time			ϕ	—	47.5	—	ns
Total Line Time			—	—	29.229	—	µs
Active Line Time			—	—	25.728	—	µs

Table 4-4. AC Characteristics for CX25874/875 *(3 of 4)*

Parameter	Symbol	Min	Typical	Max	Units
HDTV Output Timing Characteristics: 720p (see Figure 4-10)					
Low-Sync Width	a	—	561	—	ns
Start of Line to End of Active Video	b	—	20.72	—	µs
High-Sync Width	c	—	560	—	ns
Rising Edge of Sync to Start of Broad Pulse	d	—	3.575	—	µs
Rising Edge of Sync to Start of Active Video	e	—	3.54	—	µs
Sync Rise Time	—	—	48.1	—	ns
Total Line Time	—	—	22.24	—	µs
Active Line Time	—	—	17.227	—	µs
HDTV Output Timing Characteristics: 576p (625p) see Figures 4-13 and 4-14)					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**
Pulse Width Between Consecutive Equalization-type Pulses	a	29.55	29.65	29.75	µs
Total Line Time	b	—	32.000	—	µs
Analog Sync Width	c	2.25	2.35	2.45	µs
Active Line Time	d	—	26.666	—	µs
Sync Fall Time(1)	α	95	100	105	ns
Start of Line to End of Active Video	β	—	31.917	—	µs
Start of Line to Start of Active Video	χ	—	5.25	—	µs
End of Active Video to Next Sync/start of Next Line	δ	0.60	0.75	0.90	µs
Bilevel Serration-type Pulse Period During VBI(2)	W	—	5H	—	µs
Bilevel Vertical Synchronizing Pulse Period During VBI(2)	X	—	5H	—	µs
Bilevel Serration-Type Pulse Duration During VBI Following Equalization-Type Pulses(3)	Y	—	39H	—	µs
Total VBI Time(4)	Z	—	1.568	—	ms
HDTV Output Timing Characteristics: 480p (see Figures 4-11 and 4-12)					
Pulse Width Between Consecutive Equalization-type Pulses	a	—	29.256	—	µs
Total Line Time	b	—	31.806	—	µs
Analog Sync Width	c	—	2.320	—	µs
Active Line Time	d	—	26.602	—	µs
Sync Fall Time(5)	α	—	70.0	—	ns
Start of Line to End of Active Video	β	—	31.210	—	µs

Table 4-4. AC Characteristics for CX25874/875 *(4 of 4)*

Parameter	Symbol	Min	Typical	Max	Units
Start of Line to Start of Active Video	χ	—	4.682	—	µs
End of Active Video to Next Sync/start of Next Line	δ	—	0.600	—	µs
Bilevel Serration-type Pulse Period During VBI[6]	W	—	190.1	—	µs
Bilevel Equalization-Type Pulse Period During VBI[6]	X	—	190.1	—	µs
Bilevel Serration-Type Pulse Duration During VBI Following Equalization-Type Pulses[7]	Y	—	952	—	µs
Total VBI Time[8]	Z	—	1.336	—	ms

GENERAL NOTE:

1. Guaranteed by characterization; NTSC output (except for HDTV output modes), no vertical or horizontal scaling. Flicker Filter and other internal low-pass filters bypassed, and contrast, brightness, saturation levels set to full scale.

FOOTNOTE:

(1) 100/7.5/100/7.5 Color bars normalized to burst.
(2) PSSR is measured with a 0.1 µF capacitor between the COMP and VAA_DAC pin; with a 0.1 µF capacitor connected between the VREF pin and AGND. The DAC output is set to full scale and a double-terminated 75 Ω (=37.5 Ω) load is used. PSRR is defined as 20 x log (ripple voltage at DAC output;/ripple voltage at VAA_DAC input). Limits from worst-case simulation only.
(3) Control pins are defined as: BLANK*, HSYNC*, VSYNC*, FIELD, CLKO, CLKI, RESET*.
(4) Guaranteed by design.
(5) Analog sync fall time measured from 90% of blank level to 10% of negative sync level.
(6) Equivalent to 6 analog 480p lines.
(7) Equivalent to 30 analog 480p lines.
(8) Equivalent to 42 analog 480p lines.

4.3 Power Consumption Results

Table 4-5 contains the power consumption numbers of the CX25874/5 under different operating conditions.

Table 4-5. CX25874/5 Operating Current, Operating Voltage, and Power-Related Results under Different Testing Conditions

Normal Operation = DACA, DACB, DACC, DACD ON)	Freq (MHz)	Iaa (ma)	Analog Power @3.3V	Core_I	Core Power	Idd (ma)	Digital Power @3.3 V	Tot al Power (W) @3.3 V
640x480 NTSC (mode0)	28.194469	168.5	0.556	9.8	0.0123	7.52	0.0372	0.5932
1024x768 NTSC (mode10)	68.724041	170.8	0.564	22.46	0.0283	11.67	0.0668	0.6305
HDTV (720p)	74.25	170	0.561	23.24	0.0293	12.15	0.0694	0.6304
HDTV (1080i)	74.25	170	0.561	25.27	0.0318	12.09	0.0717	0.6327
Sleep: SLEEP_EN bit = 1	**Freq (MHz)**	**Iaa (ma)**	**Analog Power @3.3 V**	**Core_I**	**Core Power**	**Idd (ma)**	**Digital Power @3.3 V**	**Tot al Power (W) @3.3 V**
640x480 NTSC (mode0)	28.194469	36.2	0.119	0	0.0000	4.13	0.0136	0.1331
1024x768 NTSC (mode10)	68.724041	94.6	0.312	0	0.0000	4.05	0.0134	0.3255
HDTV (720p)	74.25	0	0.000	0	0.0000	12.15	0.0401	0.0401
HDTV (1080i)	74.25	0	0.000	0	0.0000	12.09	0.0399	0.0399
Software Standby DACA, DACB, DACC, DACD OFF due to DACOFF bit = 1	**Freq (MHz)**	**Iaa (ma)**	**Analog Power @3.3 V**	**Core_I**	**Core Power**	**Idd (ma)**	**Digital Power @3.3 V**	**Tot al Power (W) @3.3 V**
640x480 NTSC (mode0)	28.194469	37.5	0.124	6.78	0.0085	7.52	0.0334	0.1571
1024x768 NTSC (mode10)	68.724041	42.2	0.139	20.96	0.0264	11.67	0.0649	0.2042
HDTV (720p)	74.25	0	0.000	23.24	0.0293	4.05	0.0426	0.0426
HDTV (1080i)	74.25	0	0.000	25.27	0.0318	4.05	0.0452	0.0452

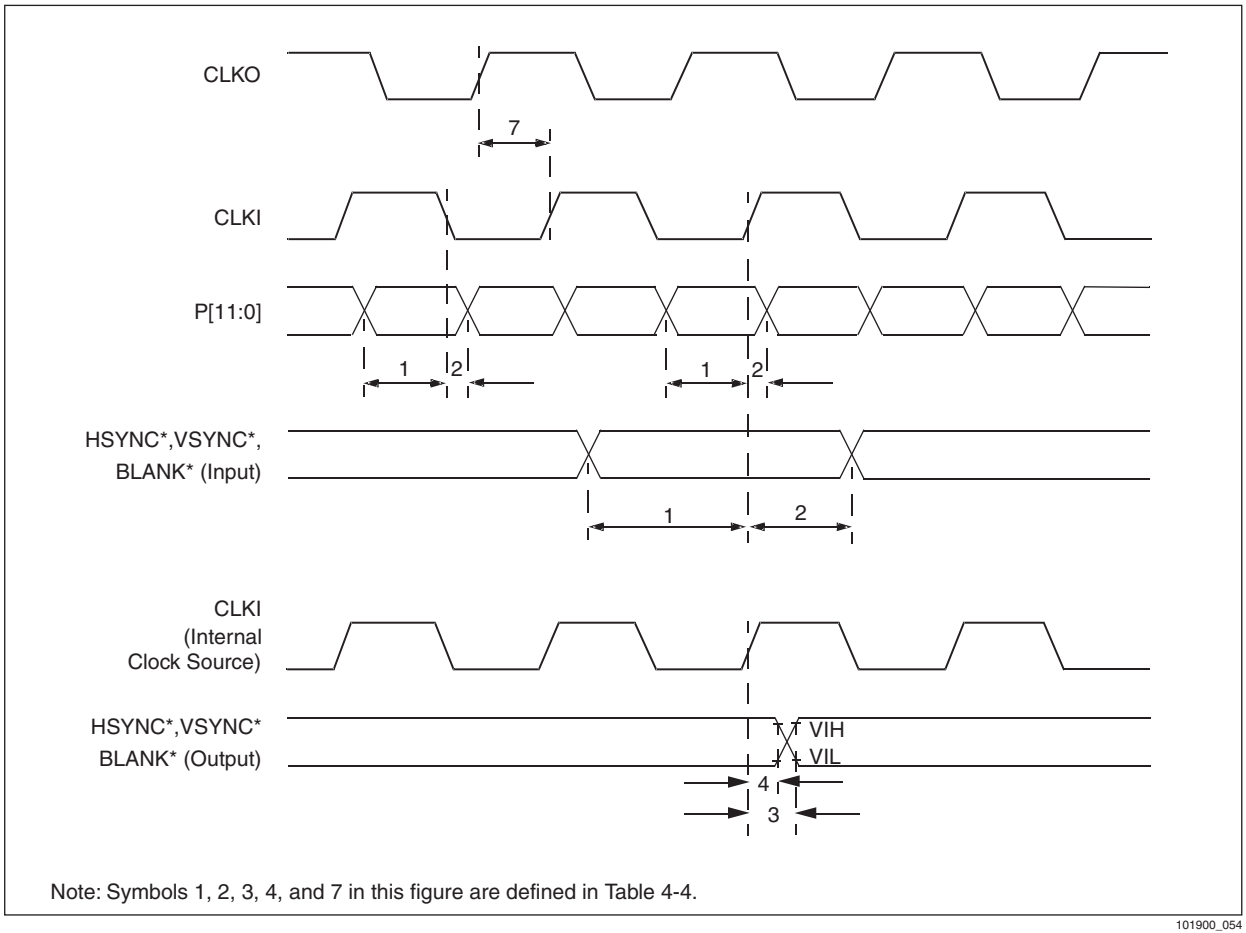
GENERAL NOTE:

1. Results obtained in this table tied all analog supply pins of CX25874/5 to 3.3 V.
2. Results obtained in this table tied all digital supply pins of CX25874/5 to 3.3 V.
3. CX25874/5 used 3.3 V peak-to-peak I/O levels to obtain these results.
4. CX25874/5 core voltage was 1.26 V.

4.4 Timing Diagrams

Figures 4-1 through 4-12 provide timing details and diagrams for important CX25874/5 digital input/output signals and analog video outputs.

Figure 4-1. Timing Details for All Interfaces



Note: Symbols 1, 2, 3, 4, and 7 in this figure are defined in Table 4-4.

101900_054

Figure 4-2. Master Interface Timing Relationship/Noninterlaced RGB/YCrCb Input

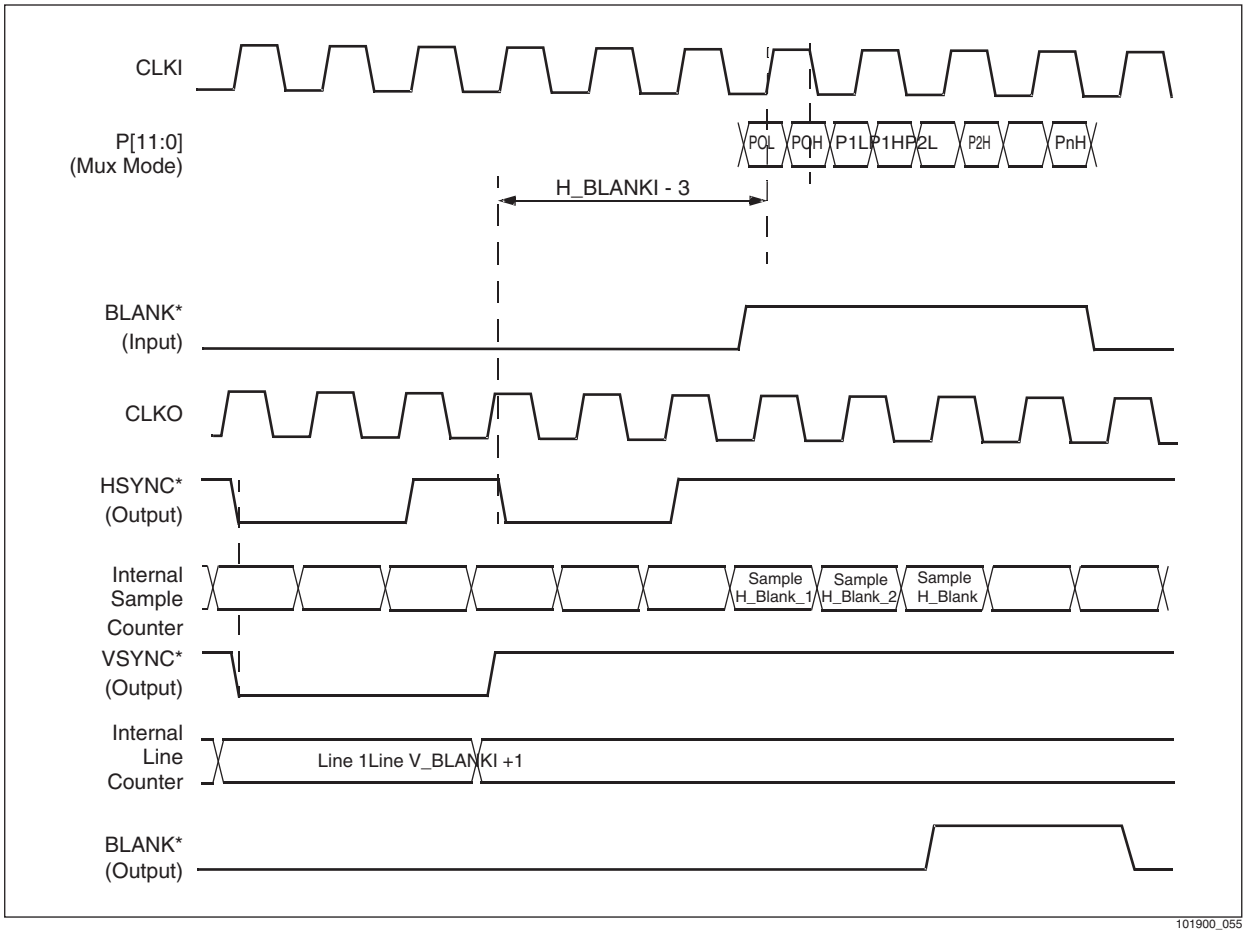


Figure 4-3. Pseudo-Master Interface Timing Relationship—Active Line/Noninterlaced RGB Input

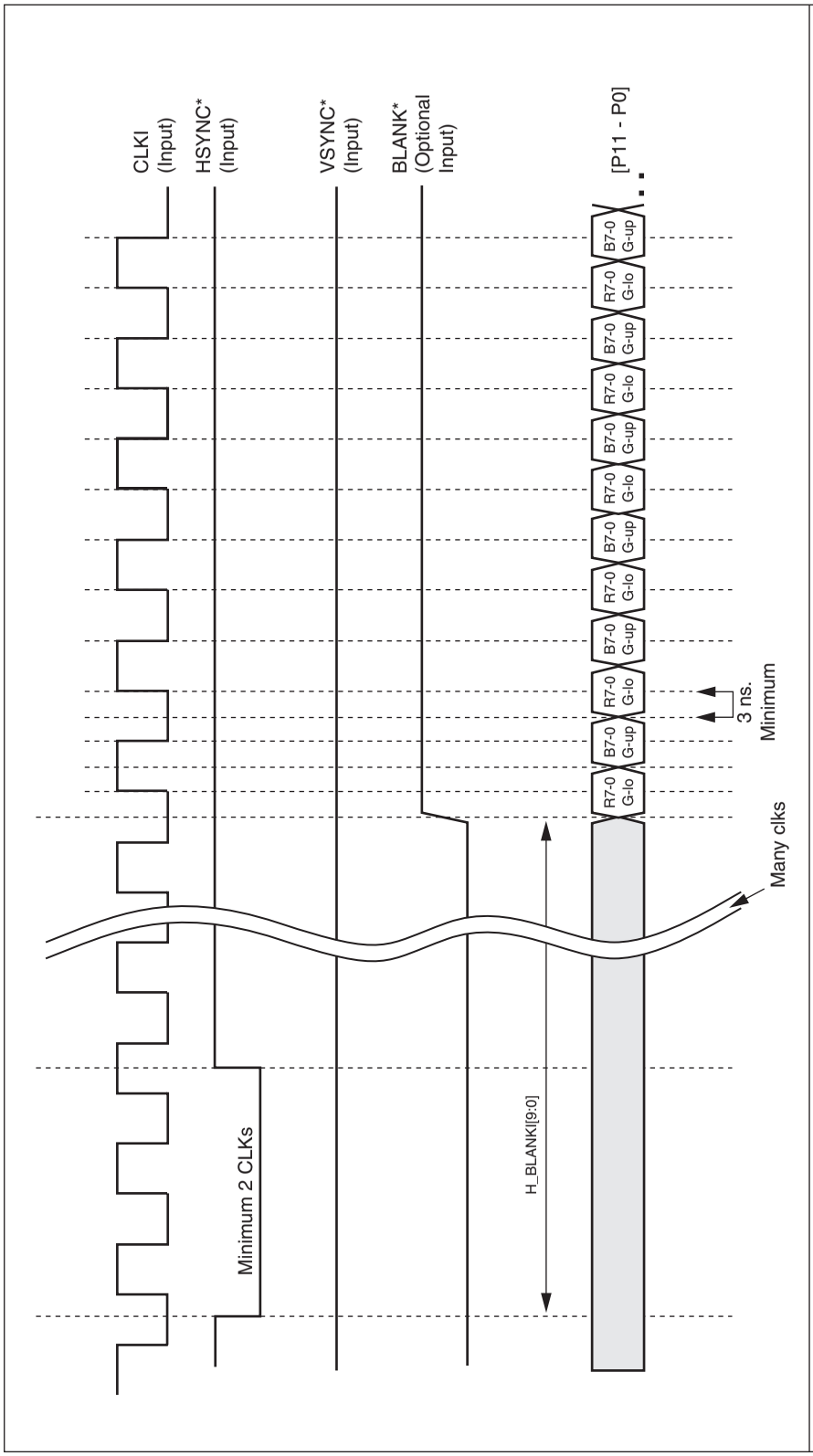
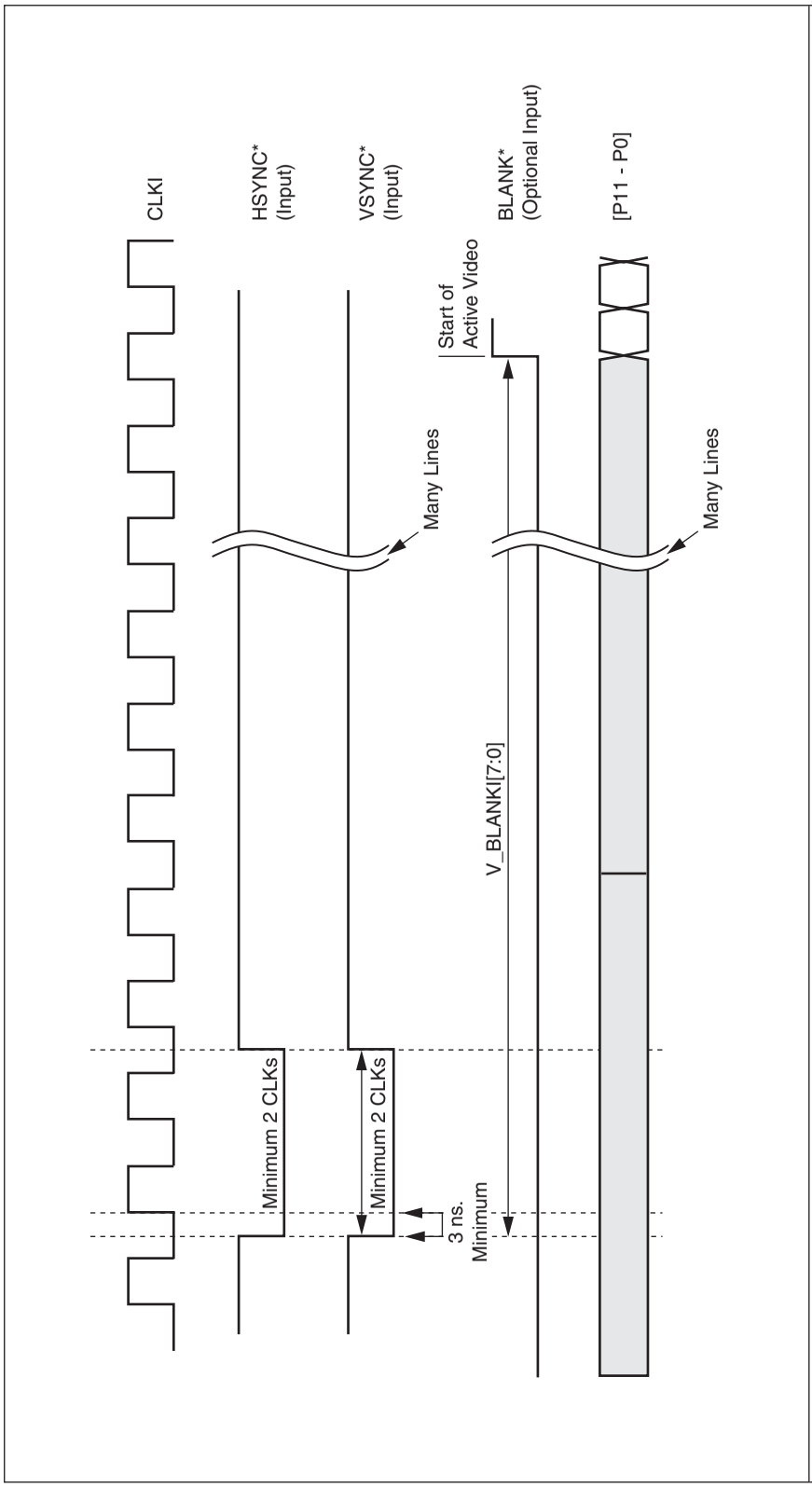


Figure 4-4. Pseudo-Master Timing Relationship Blank Line/Noninterlaced RGB/YCrCb Input



GENERAL NOTE:

1. For noninterlaced data transmission, to start each frame, the leading edge of HSYNC* and the leading edge of VSYNC* must be coincident (within 1 CLKI clock cycle). The location of these signals' respective trailing edges is not important relative to each other.
2. The duration of the HSYNC* pulse **MUST** be at least 2 complete CLKI cycles. The duration of the VSYNC* pulse **MUST** be a minimum of 2 CLKI cycles as well. It is acceptable for the HSYNC* to remain low for longer than 2 CLKI cycles but the signal's rising edge must be received by the CX25874/875 at least 1 pixel before the next HSYNC* falling edge which denotes the start of the next line. Likewise, VSYNC* can stay low for much longer than 2 CLKI cycles but the signal's rising edge must be received by the CX874/875 at least 1 complete line before the next VSYNC* falling edge which denotes the start of the next frame.
3. If a BLANK* signal is not used as part of the physical interface to a graphics controller, then the CX25874/875's H_BLANK[9:0] and V_BLANKI[7:0] registers must be programmed with values equivalent to the correct amount of horizontal pixel blanking and vertical line blanking from the master.

Figure 4-5. Slave Interface Timing Relationship/Noninterlaced RGB/YCrCb Input

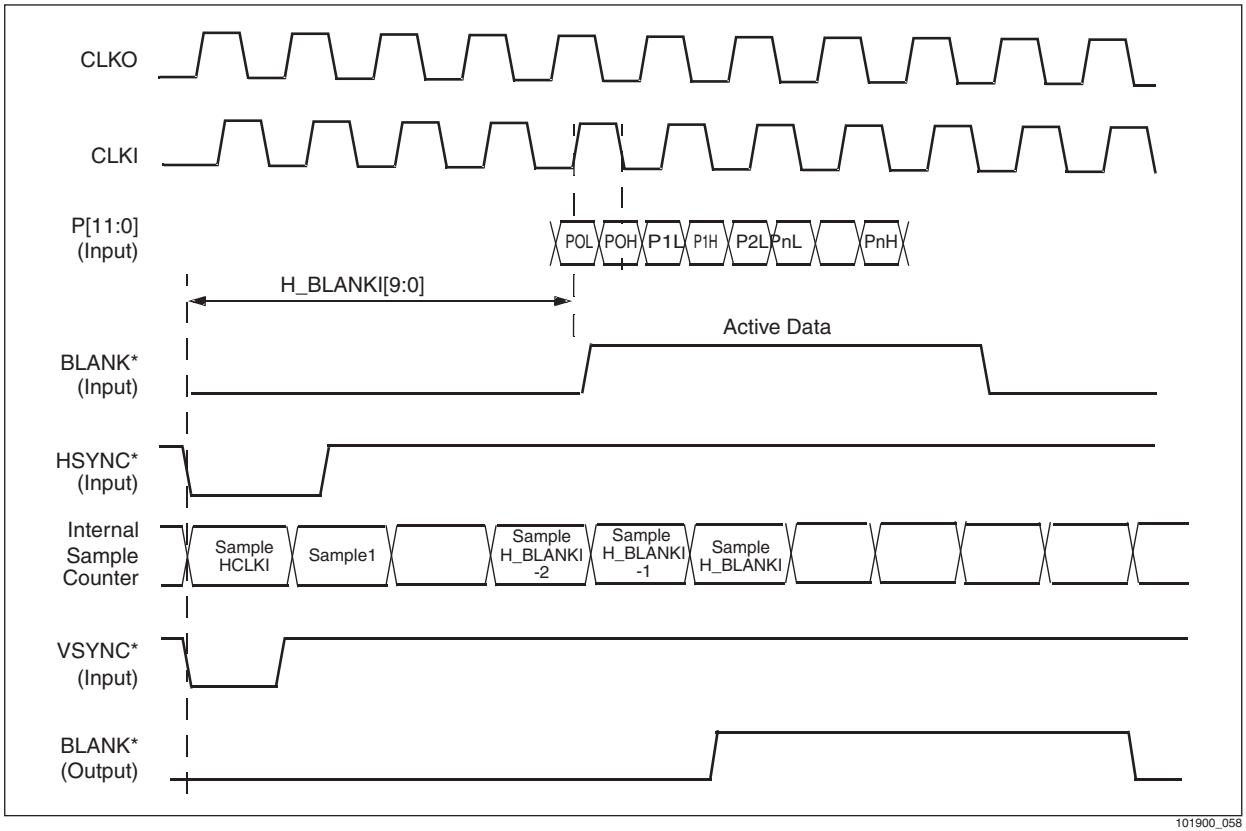
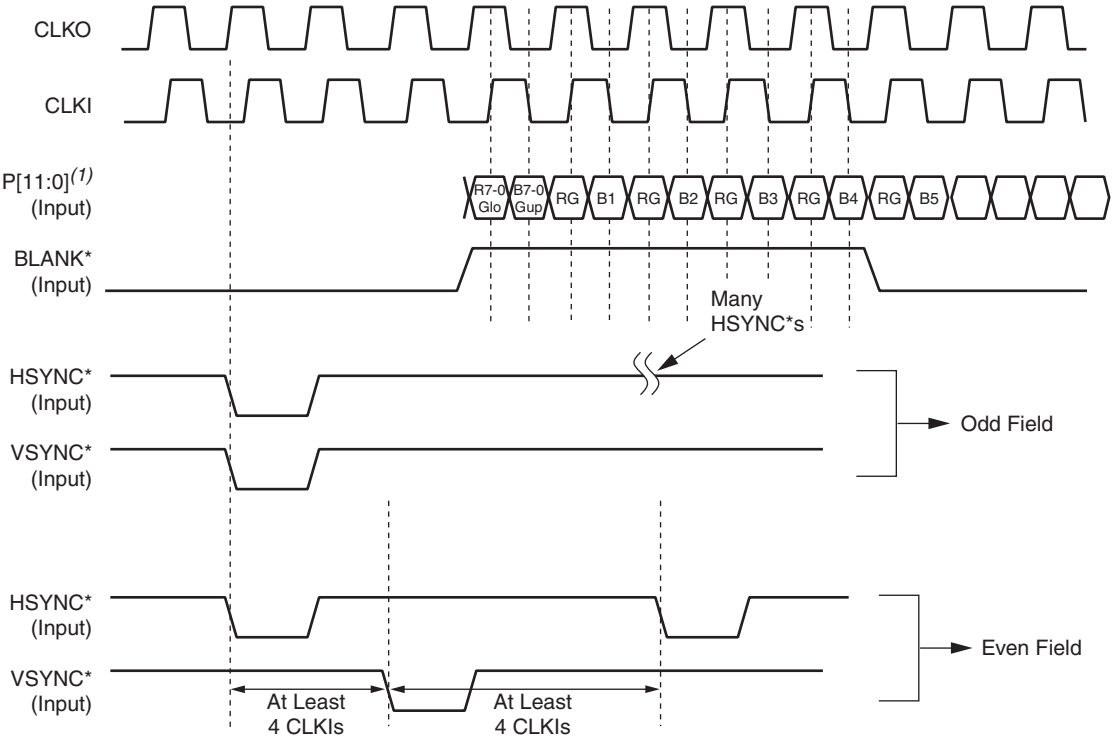


Figure 4-6. Slave Interface Timing Relationship/Interlaced Multiplexed RGB Input (FLD_MODE = 10—Default)



GENERAL NOTE:

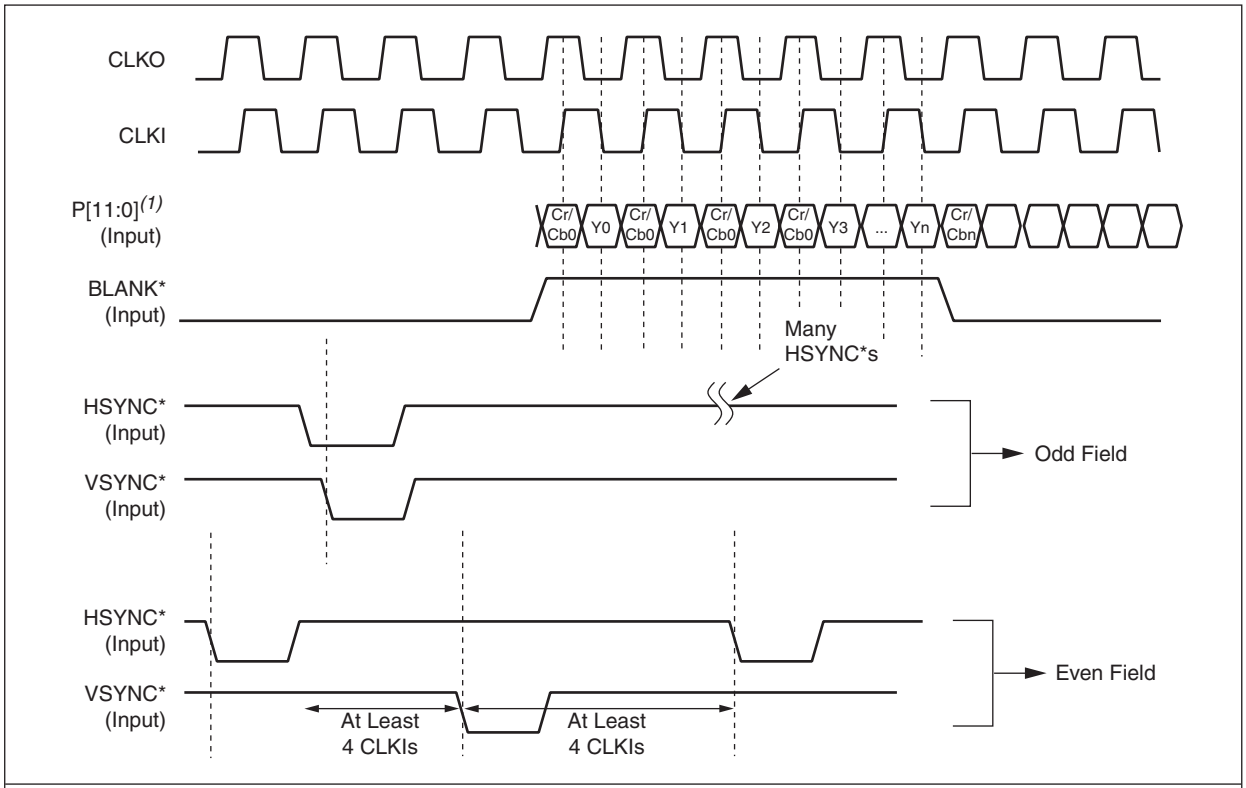
1. The CX25874/5's DIV2 bit must be set.
2. FLD_MODE[1:0] defined in Table 2-5.

FOOTNOTE:

(1) IN_MODE[3:0] = 0000, shown in the figure. IN_MODE[3:0] = 0010, 0001, and 1000, adheres to the same timing, but pixel data will be latched differently.

101900_059

Figure 4-7. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 01)



GENERAL NOTE:

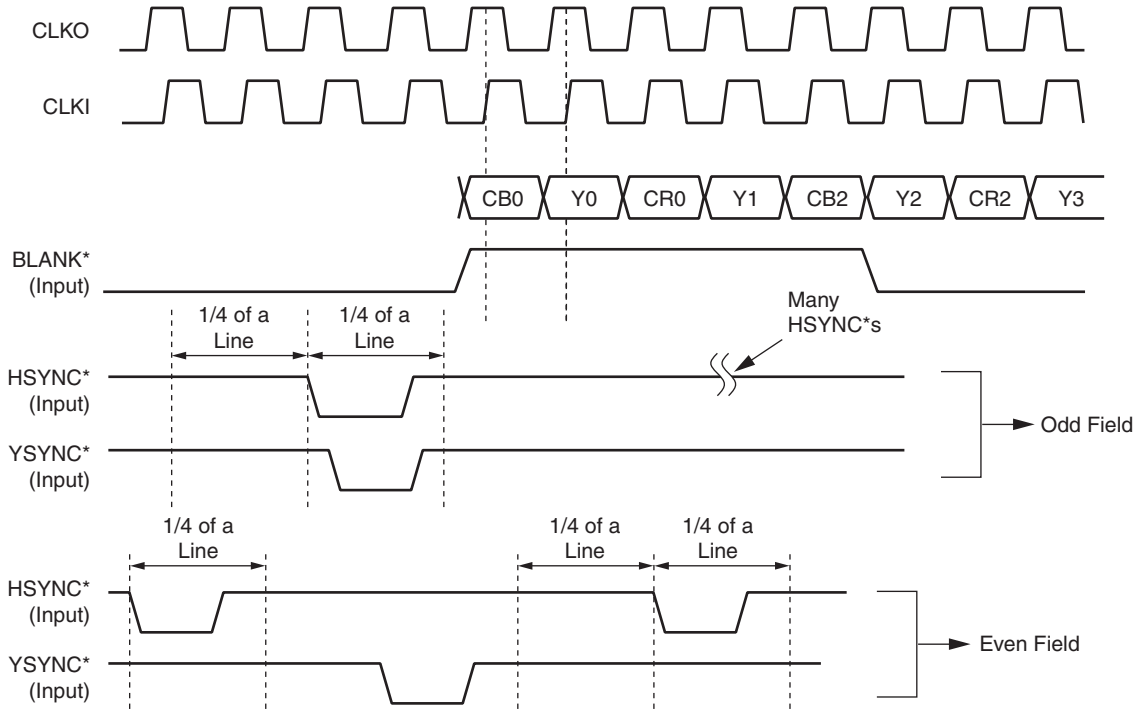
1. The CX25874/5's DIV2 bit must be set.
2. FLD_MODE[1:0] defined in Table 2-5.

FOOTNOTE:

(1) IN_MODE[3:0] = 0101 and IN_MODE[3:0] = 0110, shown in the figure. IN_MODE[3:0] = 1100 and 0100, adheres to the same timing, but pixel data will be latched differently.

101900_060

Figure 4-8. Slave Interface Timing Relationship/Interlaced Multiplexed YCrCb Input (FLD_MODE = 00)



GENERAL NOTE:

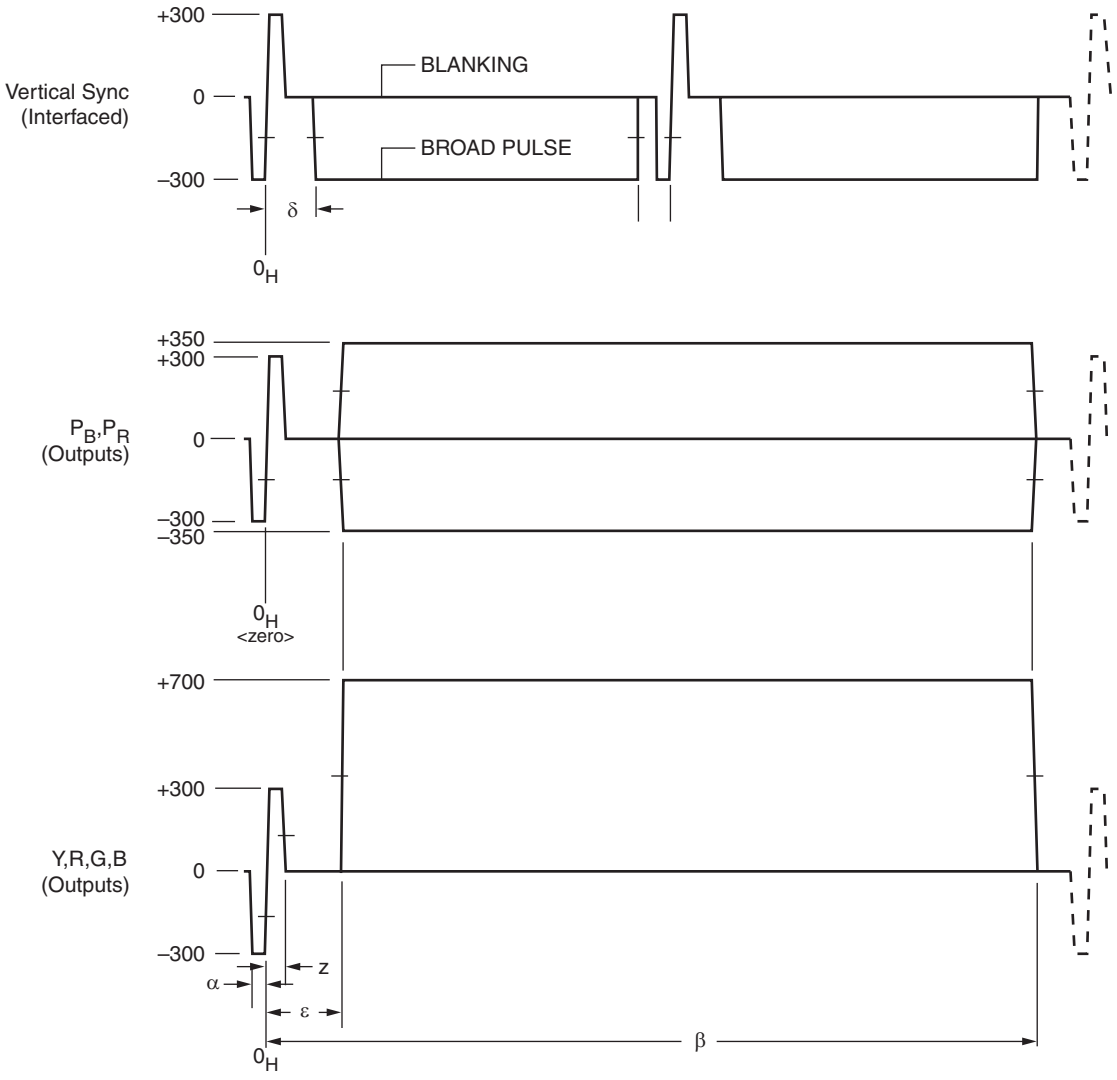
1. The CX25874/5's DIV2 bit must be set.
2. FLD_MODE[1:0] defined in Table 2-5.

FOOTNOTE:

(1) IN_MODE[3:0] = 0101 and IN_MODE[3:0] = 0110, shown in the figure. IN_MODE[3:0] = 1100 and 0100 adheres to the same timing, but pixel data will be latched differently.

101900_061

Figure 4-9. HDTV Output Horizontal Timing Details: 1080i

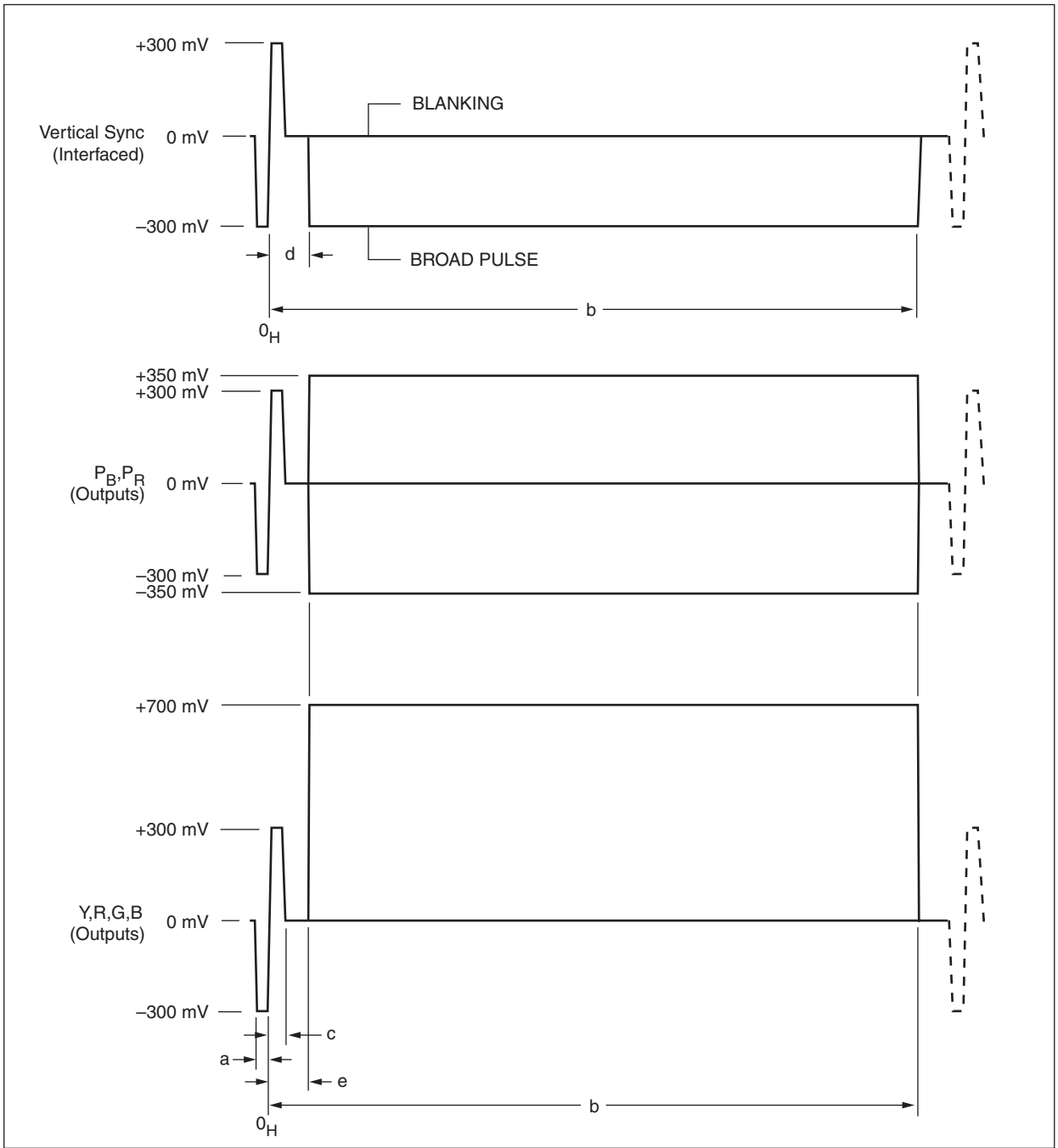


GENERAL NOTE:

1. Values for α, β, χ, δ, ε, and σ are given in Table 4-4.
2. Sync rise time (σ) is not shown here.
3. Amplitudes are expressed in mV.

101900_082

Figure 4-10. HDTV Output Horizontal Timing Details: 720p

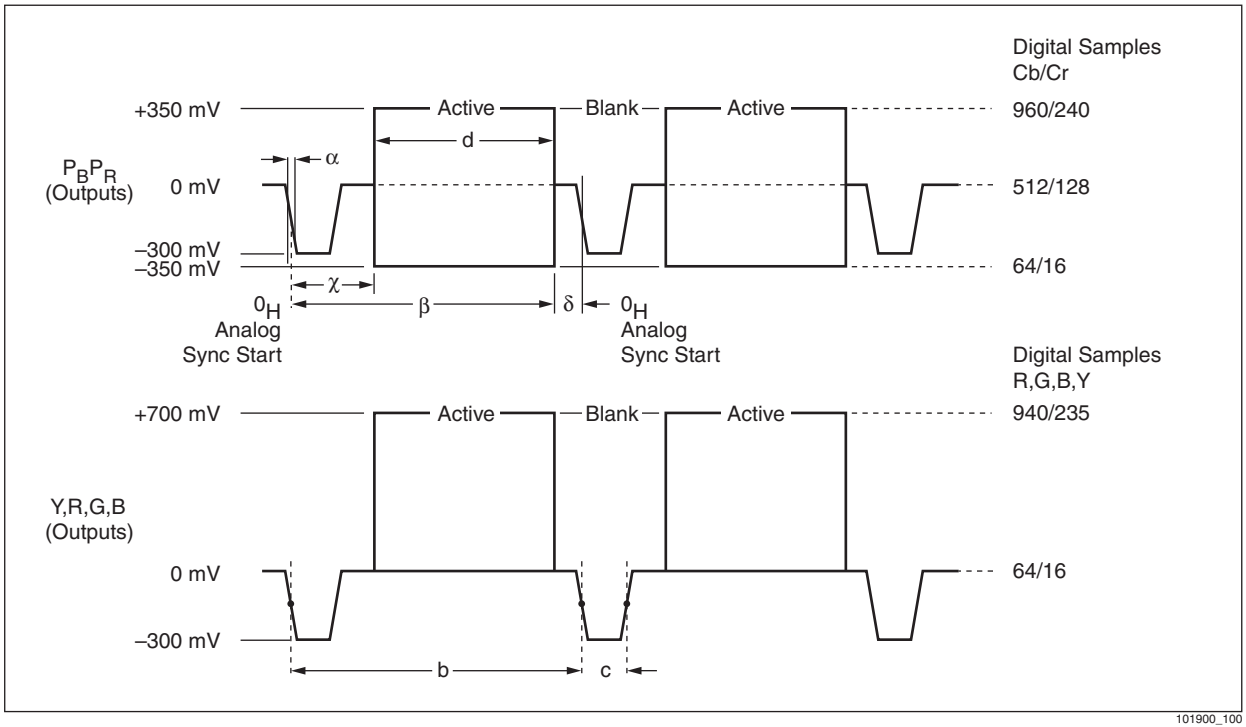


GENERAL NOTE:

1. Values for a, b, c, d, and e are given in Table 4-4.
2. Sync rise time is not shown here.
3. Amplitudes are expressed in mV.

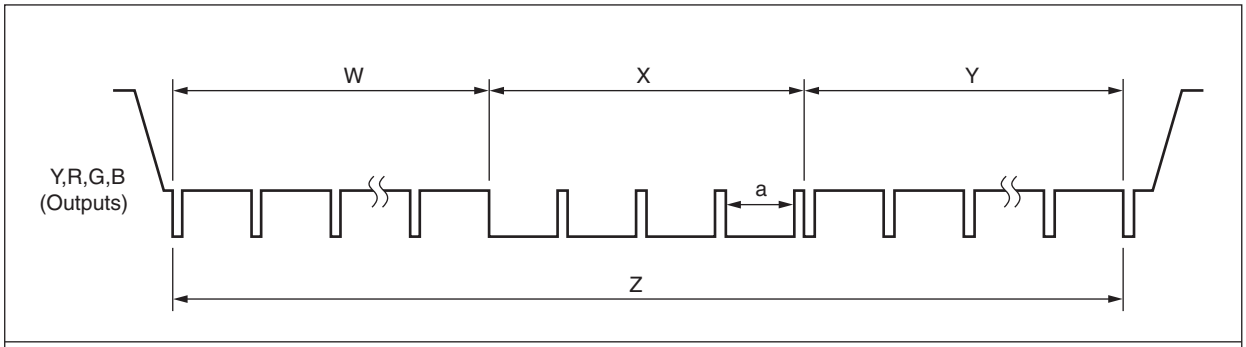
101900_083

Figure 4-11. HDTV Output Horizontal Timing Details: 480p



101900_100

Figure 4-12. HDTV Output Vertical Timing Details: 480p



GENERAL NOTE: Values for a, b, c, d, α, β, χ, δ, W, X, Y, and Z are given in Table 4-4.

101900_101

Figure 4-13. HDTV Output Horizontal Timing Details: 576p (625p)

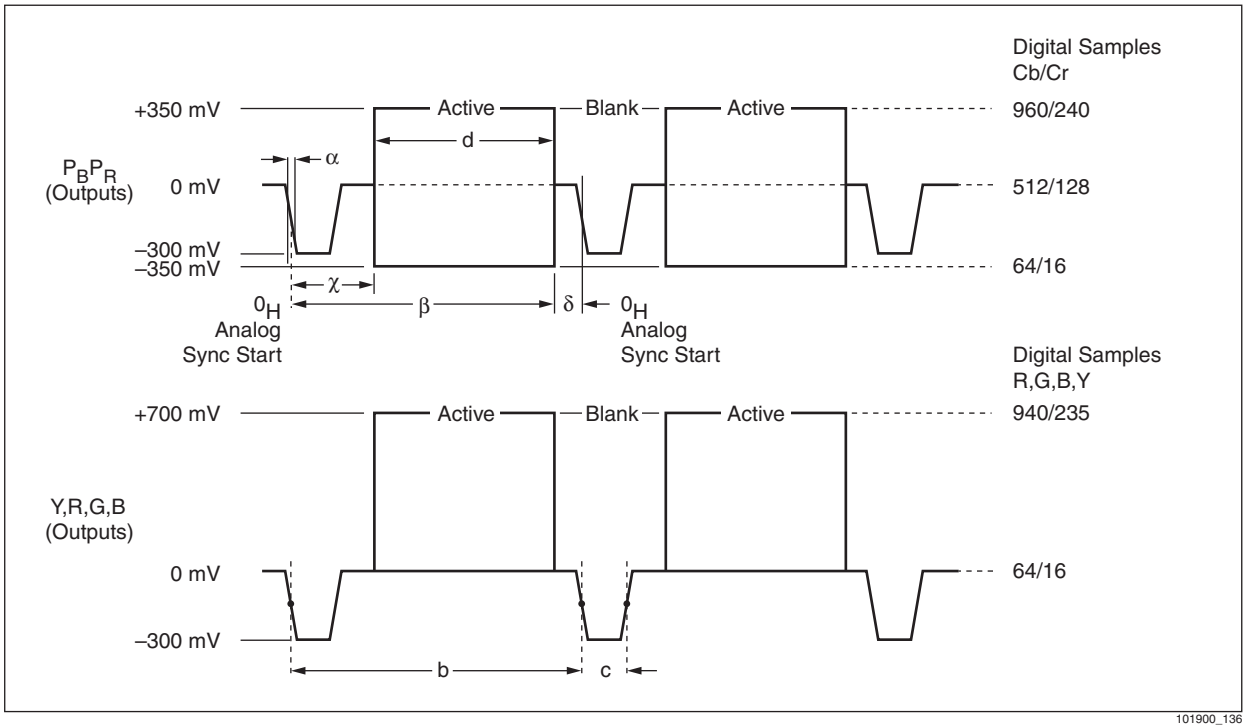
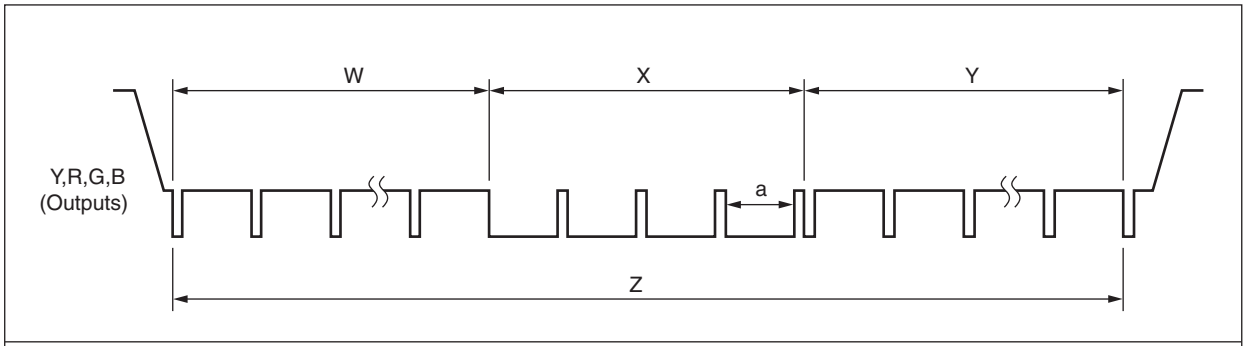


Figure 4-14. HDTV Output Vertical Timing Details: (576p (625p)



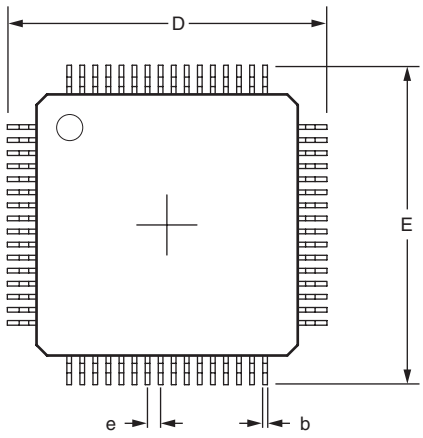
GENERAL NOTE: Values for a, b, c, d, α, β, χ, δ, W, X, Y, and Z are given in Table 4-2.

4.5 Mechanical Specifications

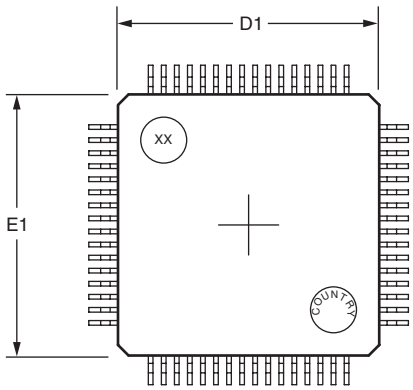
Figure 4-15 illustrates mechanical specifications for the CX25874and CX25875. The CX25874/5 is a 64-pin TQFP package.

Figure 4-15. 64-Pin TQFP Package Diagram

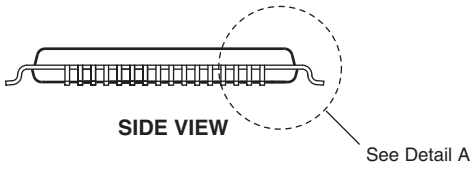
REVISIONS		
REV	DESCRIPTION	APPD/DATE
A	INITIAL RELEASE	M. WORREL 8/01/01
B	REMOVED EXPOSED PAD	M. WORREL 11/26/01



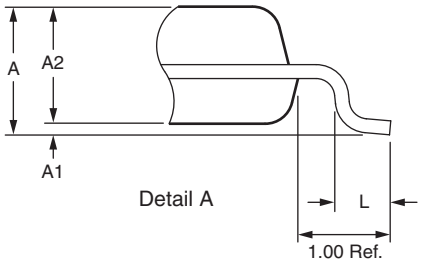
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Dim.	JEDEC Variation All Dimensions are in Millimeters ABD		
	Min.	Nom.	Max.
A	----	----	1.20
A1	0.05	----	0.15
A2	0.95	1.00	1.05
D		9.00 BSC.	
D1		7.00 BSC.	
E		9.00 BSC.	
E1		7.00 BSC.	
L	0.45	0.60	0.75
N		64	
e		0.4 mm	
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
ccc	----	----	0.08
ddd	----	----	0.07

BSC Tolerances on

Decimal	Angular
X.X ± 0.1 mm	± 1°
X.XX ± 0.05 mm	
X.XXX ± 0.025 mm	

GENERAL NOTE: BSC is defined to be this package's basic dimensions. BSC is a numerical value that represents the parameter's exact theoretical size, profile, or orientation, or a datum target.

101900_114

A

Scaling and I/O Timing Register Calculations Appendix

The calculated values are used to program the registers controlling the total active pixels and lines in the input frame and the output field, as well as the vertical scaling register and the clock PLL registers. These calculations assume pixel resolution for synchronizing the graphics controller, master interface operation unless otherwise stated, and require the following input values:

MFP—Minimum Front Porch Blanking in the Input in Clocks = max

(12, Controller_Minimum_Front_Porch_Blanking_Clocks);

MBP—Minimum Back Porch Blanking in the Input in Clocks = max

(4, Controller_Minimum_Back_Porch_Blanking_Clocks);

VOC—desired Vertical Overscan Compensation (e.g., 0.15)

HOC—desired Horizontal Overscan Compensation (e.g., 0.15)

V_ACTIVEI—Active Lines per Input Frame (e.g., 480 or 600 or 768)

H_ACTIVE—Active Pixels per Input Line (e.g., 640 or 800 or 1024)

ALO—Target Active Lines per Output Field (See Table A-3)

TLO—Total Lines per Output Field (See Table A-3)

ATO—Active Time per Output Line (See Table A-3)

TTO—Total Time per Output Line (See Table A-3)

Tables A-1 and A-2 contain details of the supported video output formats. Table A-3 details the constant software values depending on the video output. Figures A-1 through A-8 illustrate allowable overscan compensation pairs for the most common desktop active resolutions. Tables A-4 through A-27 list the most common overscan values for the 640 x 480, 800 x 600, and 1024 x 768 active resolutions that enable dual display on both the VGA monitor and TV.

Table A-1. Target Video Parameters for All Supported Standard-Definition TV Output Formats

Parameter Description	NTSC-M	NTSC-J	PAL-M	PAL-60	PAL-B,D,G,H,I	PAL-N	PAL-Nc	SECAM
HSYNC Width (μs)	4.7	4.7	4.7	4.7	4.7	4.7	4.7	4.7
HSYNC and VSYNC Height (V)	0.286	0.286	0.287	0.3	0.3	0.2857	0.3	0.3
HSYNC Rise/Fall Time (10% to 90%) (ns)	150	150	150	150	200(1)	200	200	200
Burst or Subcarrier Start (μs)	5.3	5.3	5.8	5.3	5.6	5.6	5.6	5.6
Burst Width (μs)	2.514 (9 cycles)	2.514 (9 cycles)	2.52 (9 cycles)	2.25 (10 cycles)	2.25 (10 cycles)	2.25 (10 cycles)	2.51 (9 cycles)	N/A
Subcarrier Frequency(2) (Hz)	3579545	3579545	3,575,611.49	4433618.75	4433618.75	4433618.75	3582056.25	for=4406250 fob=4250000
Burst or Subcarrier Height (V)	0.2857	0.2857	0.306	0.3	0.3	0.3	0.3	0.161
Phase Alternation	NO	NO	YES	YES	YES	YES	YES	NO
Number of Lines per Frame	525	525	525	525	625	625	625	625
Line Frequency (Hz)	15734.264	15734.264	15734.264	15734.264	15625	15625	15625	15625
Field Frequency (Hz)	59.94	59.94	59.94	59.94	50	50	50	50
Setup	YES	NO	YES	NO	NO	YES	NO	NO
First Active Line	22(3)	22(3)	22(3)	22(3)	23(4)	23(4)	23(4)	23(4)
Last Active Line	262(3)	262(3)	262(3)	262(3)	309(4)	309(4)	309(4)	309(4)
HSYNC to Blank End (μs)	9.2[9.037] (5)	9.2	9.2	9.2	10.5[9.778] (5)	9.2	10.5	10.5
Blank Begin to HSYNC (μs)	1.5[1.185] (5)	1.5	1.5	1.5	1.5[0.889] (5)	1.5	1.5	1.5
Black to 100% White (V)	0.661	0.714	0.661	0.7	0.7	0.661	0.7	0.7
Number of Lines each for Vertical Serration, Equalization	3	3	3	3	2.5	3	2.5	2.5

FOOTNOTE:

(1) Value for PAL-I is 250 ns.

(2) When programming the subcarrier increment, use relationship of F_{sc} to F_h as given in ITU-R BT.470 instead of F_{sc} to F_{CLK}.

(3) Using NTSC line numbering convention from ITU-R BT.470.

(4) Using PAL line numbering convention from ITU-R BT.470.

(5) ITU-R BT.601 blanking values given in square brackets [].

Table A-2. Key Parameters for All Supported Standard-Definition Video Output Formats

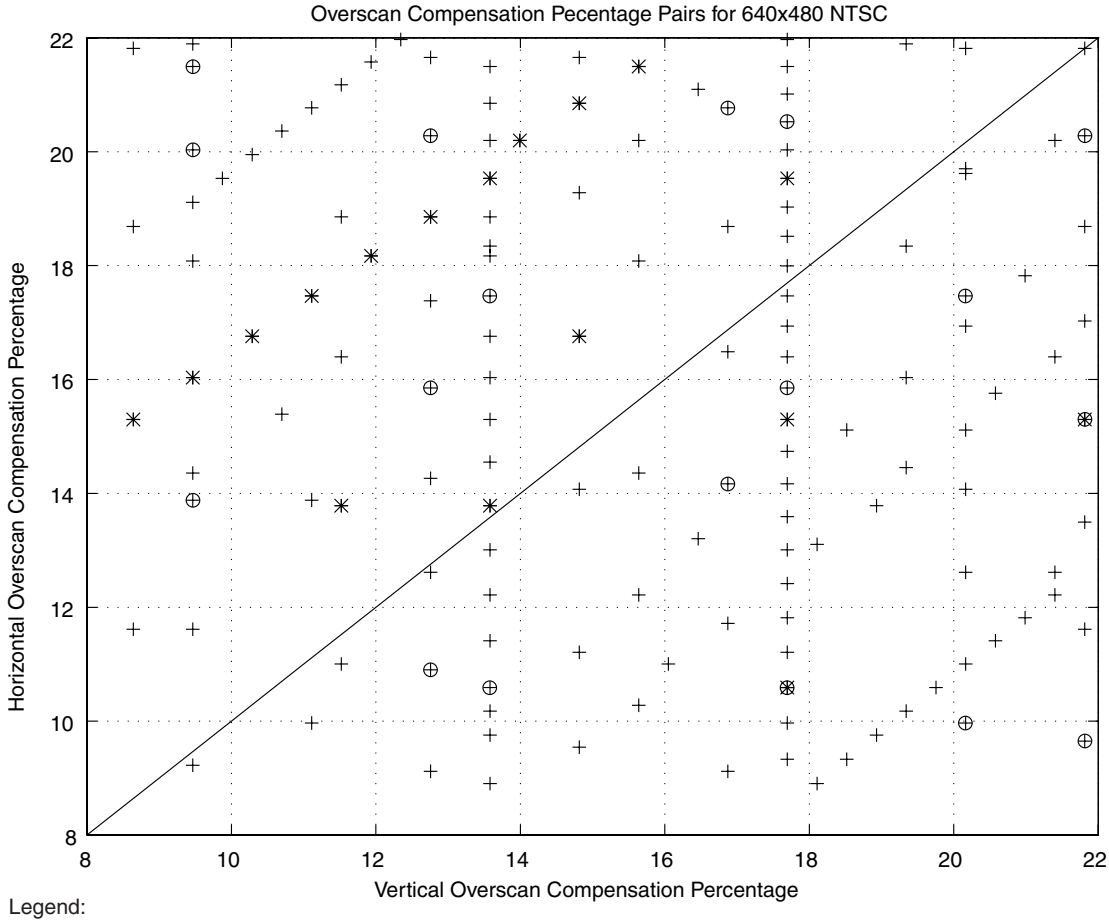
Mode	NTSC	NTSC-60Hz	PAL-BDGHI	PAL-N	PAL-Nc	PAL-M	PAL-60
FSC (Hz)	3,579,545	3,579,545	4,433,618.75	4,433,618.75	3,582,056.25	3,575,611.49	4,433,619.49
Burst Start	5.3 µs	5.3 µs	5.60 µs	5.60 µs	5.60 µs	5.80 µs	5.60 µs
Burst End	7.82 µs	7.82 µs	7.85 µs	7.85 µs	8.11 µs	8.32 µs	7.85 µs
HSYNC Width(1)	4.70 µs	4.70 µs	4.70 µs	4.70 µs	4.70 µs	4.70 µs	4.70 µs
HSYNC Frequency(1)	63.555 µs	64 µs	64 µs	64 µs	64 µs	63.555 µs	64 µs
Active Begin	9.40 µs	9.40 µs	10.5 µs	9.40 µs	10.5 µs	9.40 µs	10.5 µs
Image Center	35.667 µs	35.667 µs	36.407 µs	35.667 µs	36.407 µs	35.667 µs	36.407 µs
Blank Begin to HSYNC(1)	1.50 µs	1.50 µs	1.50 µs	1.50 µs	1.50 µs	1.50 µs	1.50 µs

FOOTNOTE:
(1) HSYNC in this table refers to the analog horizontal synchronization pulse that starts every scan line.

Table A-3. Constant Values Dependent on Encoding Mode

Modes	Interlaced		NonInterlaced	
	PAL	NTSC	PAL	NTSC
ALO	288	243	288	243
TLO	312.5	262.5	312	262
ATO	52.0 µs	52.65556 µs	52.0 µs	52.65556 µs
TTO	64.0 µs	63.55556 µs	64.0 µs	63.55556 µs

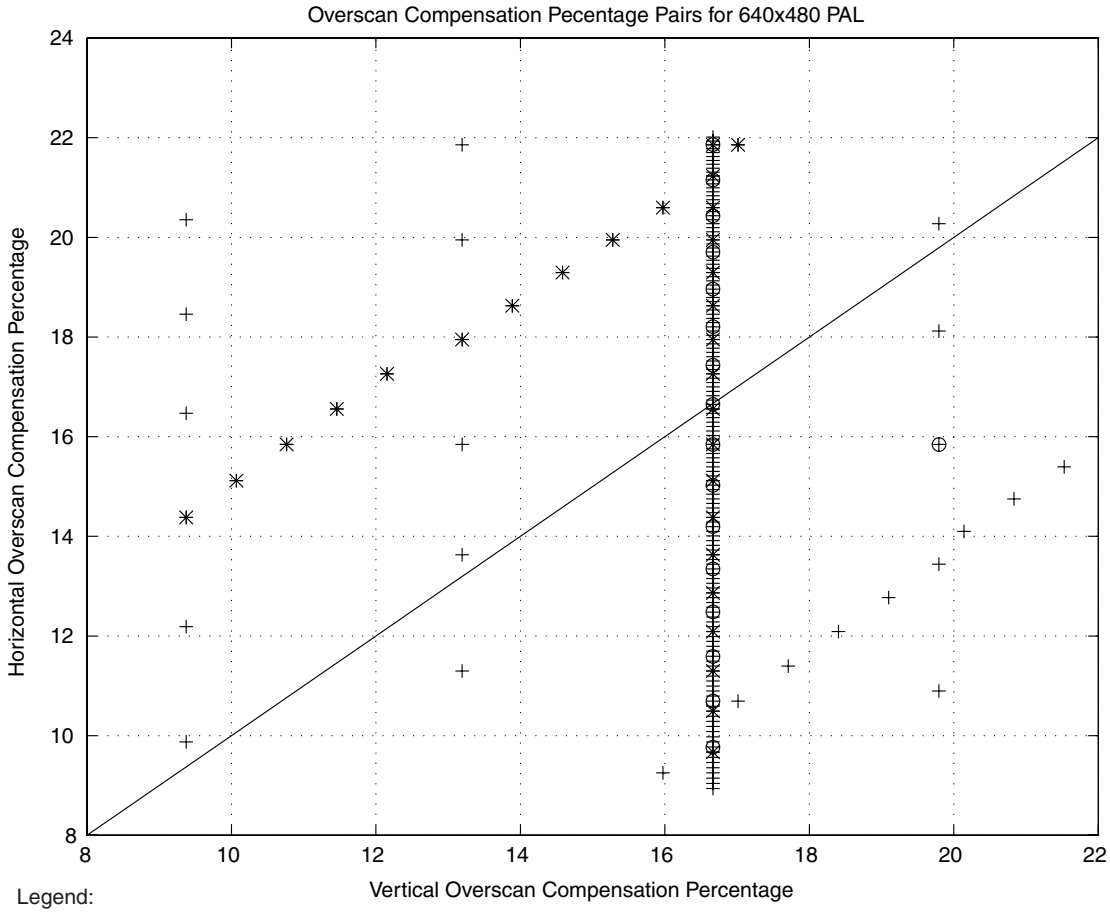
Figure A-1. Allowable Overscan Compensation Ratios for Dual Display, 640x480 Input, NTSC Output with 20 Clock HBlank Period



GENERAL NOTE: Use this chart for PAL-M and PAL-60 allowable overscan ratios.

101900_065

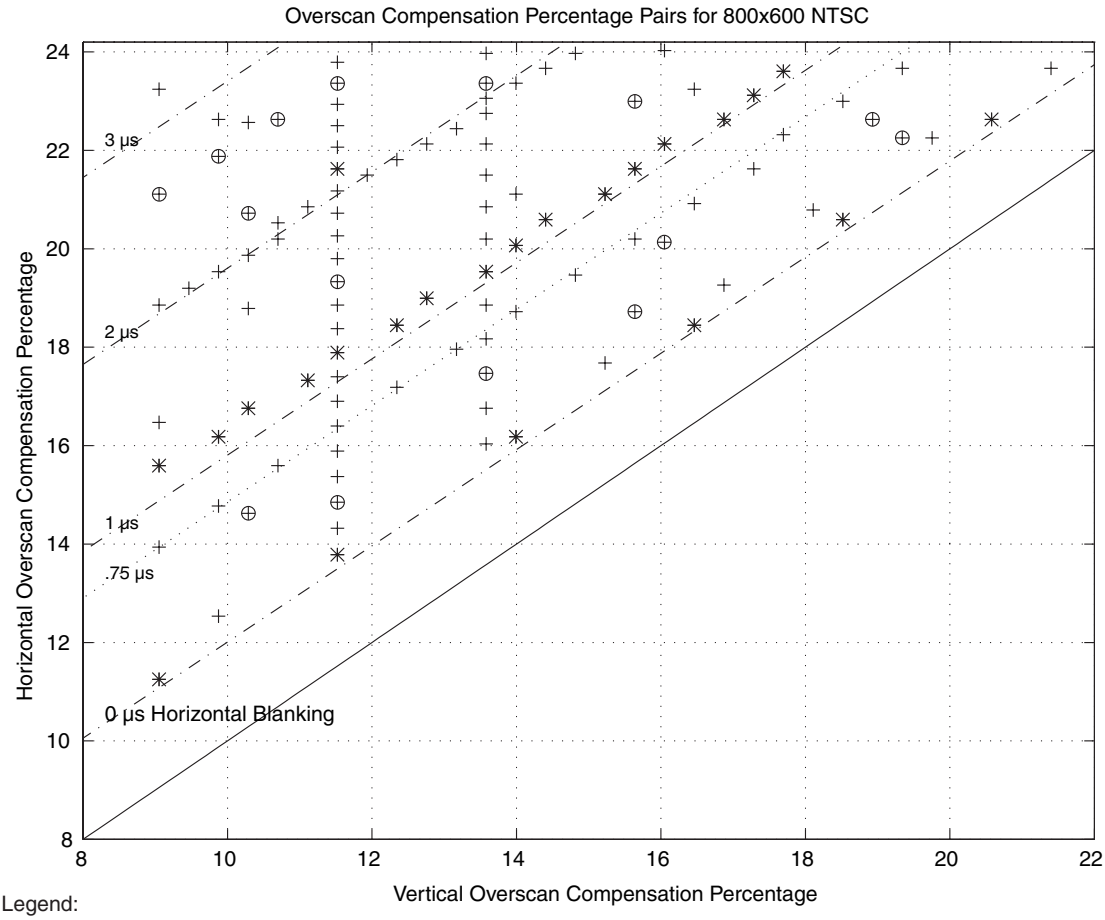
Figure A-2. Allowable Overscan Compensation Ratios for Dual Display, 640x480 Input, PAL-BDGHI Output with 20 Clock HBlank Period



GENERAL NOTE: Use this chart for SECAM allowable overscan compensation ratios.

101900_066

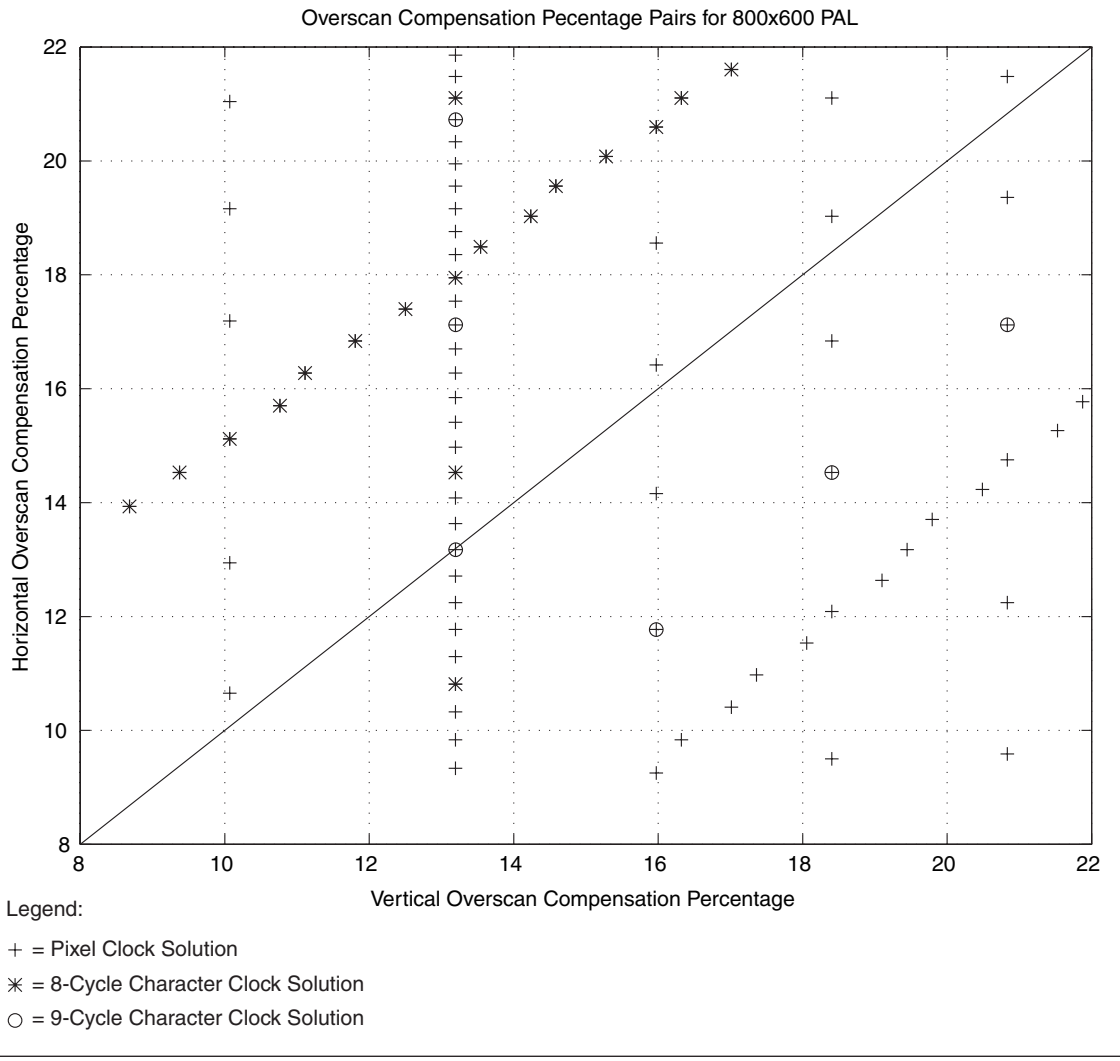
Figure A-3. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input, NTSC Output



GENERAL NOTE: Use this chart for PAL-M and PAL-60 allowable overscan ratios.

101900_067

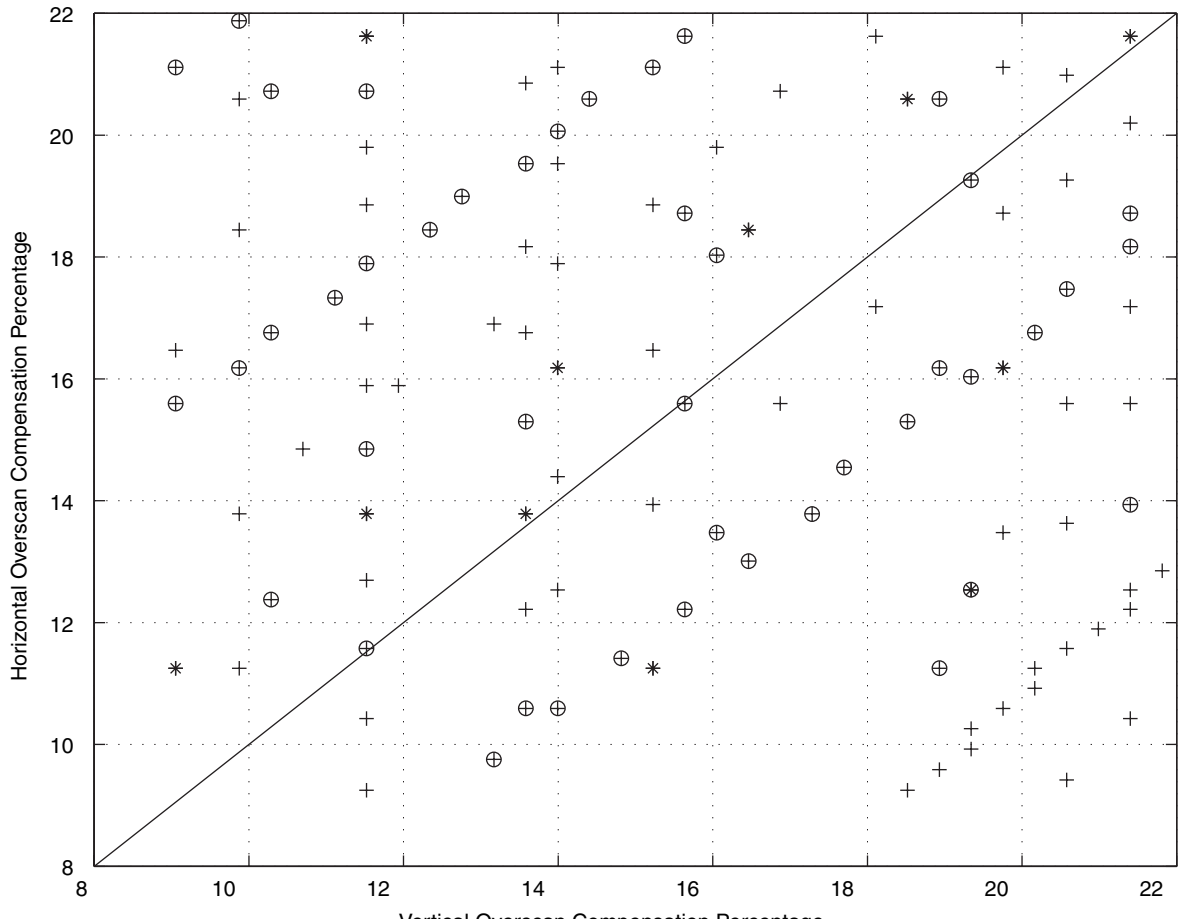
Figure A-4. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input, PAL–BDGHI Output, Standard Clocking Mode



GENERAL NOTE: Use this chart for SECAM allowable overscan compensation ratios.

101900_068

Figure A-5. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input, NTSC Output in 3:2 Clocking Mode

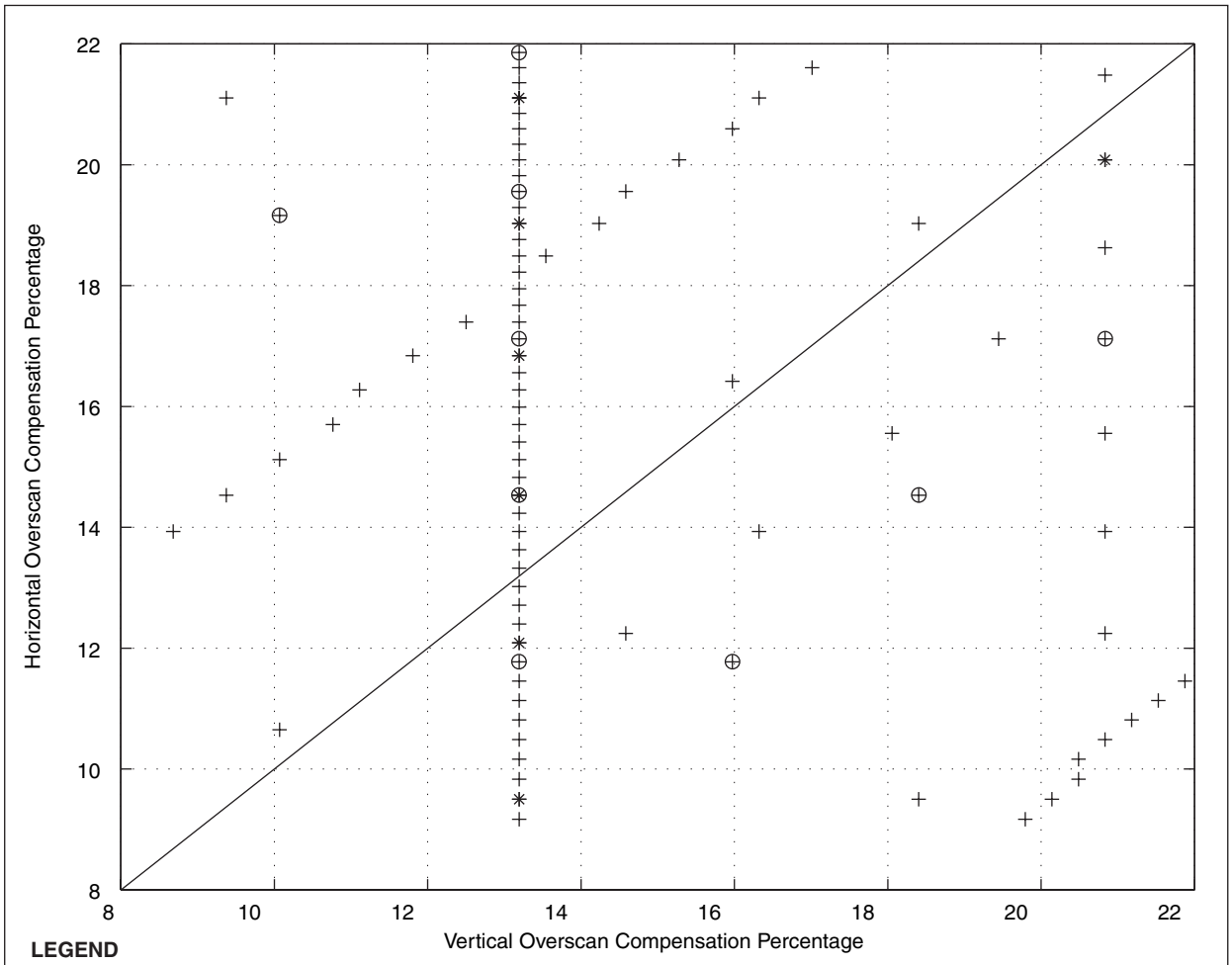


GENERAL NOTE:

1. All overscan solutions on this chart can be enabled by a data master that requires no more than 4 µs of HBlank time per line.
2. Use this chart for PAL-M and PAL-60 allowable overscan ratios.

101900_069

Figure A-6. Allowable Overscan Compensation Ratios for Dual Display, 800x600 Input, PAL-BDGHI Output in 3:2 Clocking Mode

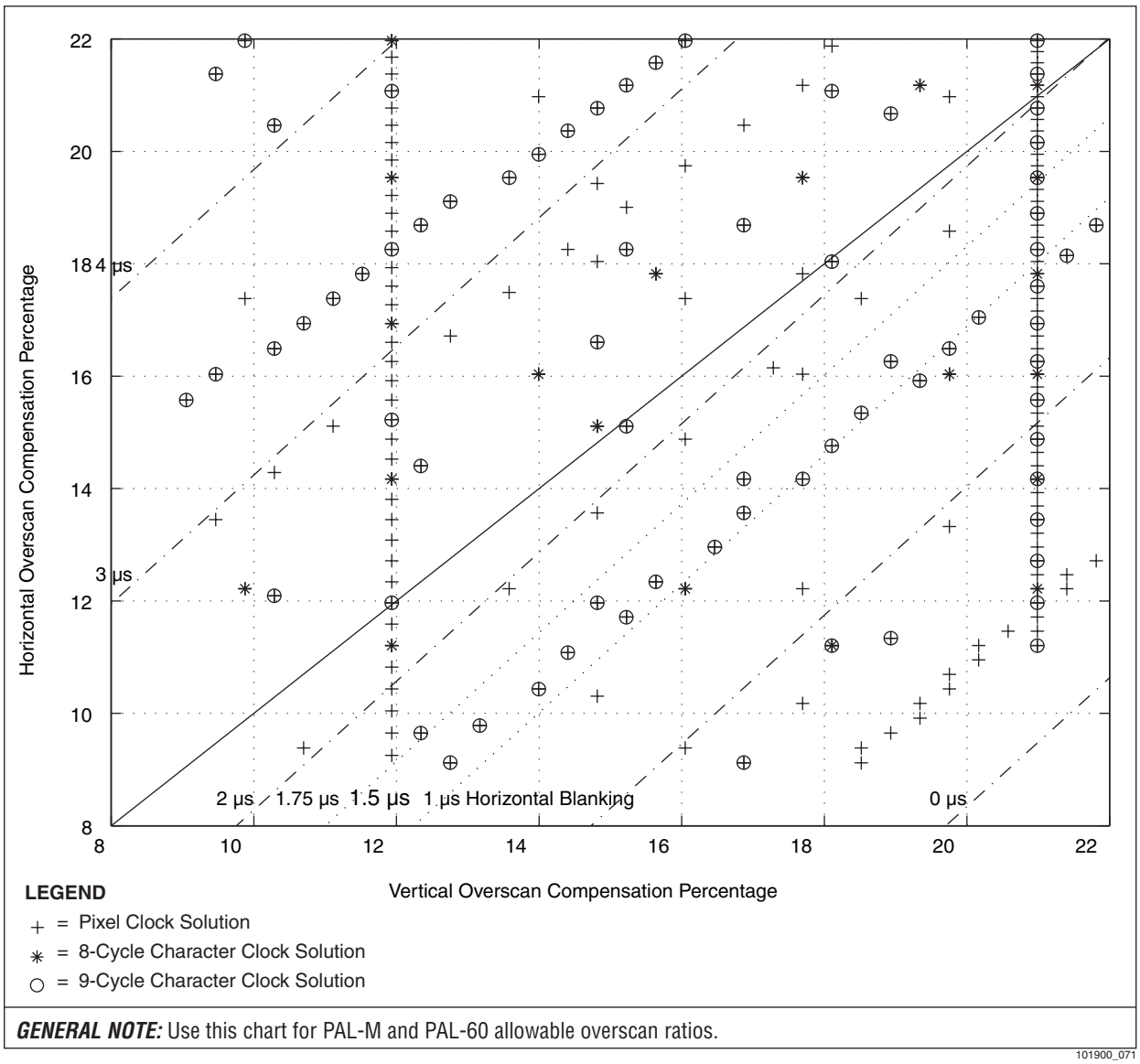


GENERAL NOTE:

1. All overscan solutions on this chart can be enabled by a data master that requires no more than 8 µs of HBlank time per line.
2. Use this chart for SECAM allowable overscan compensation ratios.

101900_070

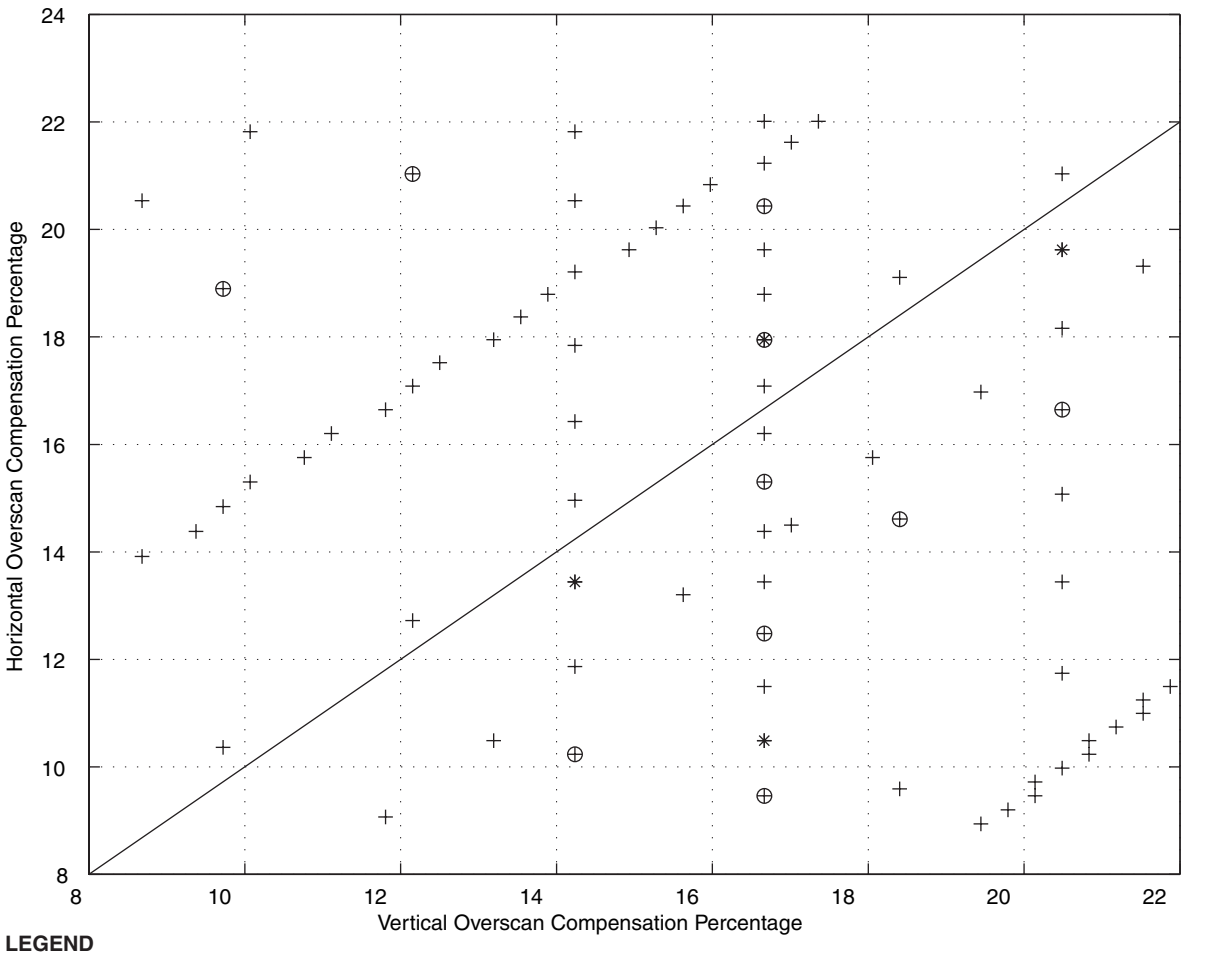
Figure A-7. Allowable Overscan Compensation Ratios for Dual Display, 1024x768 Input, NTSC Output



GENERAL NOTE: Use this chart for PAL-M and PAL-60 allowable overscan ratios.

101900_071

Figure A-8. Allowable Overscan Compensation Ratios for Dual Display, 1024x768 Input, PAL-BDGHI Output



GENERAL NOTE:

1. All overscan solutions on this chart can be enabled by a data master that requires no more than 3 µs of HBlank time per line.
2. Use this chart for SECAM allowable overscan compensation ratios.

101900_072

Table A-4. Overscan Values, 640 x 480 NTSC, Pixel-Based Controller, 1-Pixel Resolution, 2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
780	665	190	988	21.81	21.81	0.00
780	595	212	884	12.61	12.76	–0.14
784	600	210	896	13.79	13.58	0.21
780	630	200	936	17.47	17.70	–0.23
790	630	200	948	18.51	17.70	0.82
770	645	196	946	18.34	19.34	–1.00
770	585	216	858	9.97	11.11	–1.14
770	660	191	968	20.20	21.40	–1.20
770	615	205	902	14.36	15.64	–1.28
770	630	200	924	16.40	17.70	–1.30
770	600	210	880	12.22	13.58	–1.36
798	650	194	988	21.81	20.16	1.65
798	600	210	912	15.30	13.58	1.72
798	625	202	950	18.69	16.87	1.81
800	630	200	960	19.53	17.70	1.84
800	609	207	928	16.76	14.81	1.94
798	575	220	874	11.62	9.47	2.15
800	588	215	896	13.79	11.52	2.26
760	630	200	912	15.30	17.70	–2.40
756	650	194	936	17.47	20.16	–2.69
756	625	202	900	14.17	16.87	–2.70
810	630	200	972	20.53	17.70	2.83
756	600	210	864	10.59	13.58	–2.99

Table A-5. Overscan Values, 640 x 480 NTSC, Character Clock-Based Controller, 8-Pixel Resolution, 2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
784	600	210	896	13.79	13.58	0.21
800	630	200	960	19.53	17.70	1.84
800	609	207	928	16.76	14.81	1.94
800	588	215	896	13.79	11.52	2.26
760	630	200	912	15.30	17.70	–2.40
840	615	205	984	21.50	15.64	5.86
840	600	210	960	19.53	13.58	5.95
840	610	207	976	20.85	14.81	6.04
840	595	212	952	18.86	12.76	6.10
840	605	209	968	20.20	13.99	6.21
840	590	214	944	18.17	11.93	6.23
840	585	216	936	17.47	11.11	6.36
840	580	218	928	16.76	10.29	6.47
720	665	190	912	15.30	21.81	–6.51
840	575	220	920	16.03	9.47	6.57
840	570	222	912	15.30	8.64	6.66
720	630	200	864	10.59	17.70	–7.10

Table A-6. Overscan Values, 640 x 480 NTSC, Character Clock-Based Controller, 9-Pixel Resolution, 2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
756	650	194	936	17.47	20.16	–2.69
756	625	202	900	14.17	16.87	–2.70
810	630	200	972	20.53	17.70	2.83
756	600	210	864	10.59	13.58	–2.99
810	595	212	918	15.85	12.76	3.09
720	665	190	912	15.30	21.81	–6.51
720	630	200	864	10.59	17.70	–7.10
882	575	220	966	20.03	9.47	10.57
900	574	220	984	21.50	9.47	12.03

Table A-7. Overscan Values, 640 x 480 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, 2.5 µs HBlank *(1 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
946	625	240	946	16.73	16.67	0.07
944	625	240	944	16.56	16.67	–0.11
948	625	240	948	16.91	16.67	0.24
942	625	240	942	16.38	16.67	–0.29
950	625	240	950	17.09	16.67	0.42
950	600	250	912	13.63	13.19	0.44
940	625	240	940	16.20	16.67	–0.46
950	650	231	988	20.27	19.79	0.48
950	575	261	874	9.88	9.38	0.50
952	625	240	952	17.26	16.67	0.59
938	625	240	938	16.02	16.67	–0.64
954	625	240	954	17.43	16.67	0.77
936	625	240	936	15.84	16.67	–0.82
956	625	240	956	17.61	16.67	0.94
934	625	240	934	15.66	16.67	–1.00
958	625	240	958	17.78	16.67	1.11
932	625	240	932	15.48	16.67	–1.18
960	625	240	960	17.95	16.67	1.28
930	625	240	930	15.30	16.67	–1.36
962	625	240	962	18.12	16.67	1.45
928	625	240	928	15.12	16.67	–1.55
964	625	240	964	18.29	16.67	1.62
926	625	240	926	14.94	16.67	–1.73
966	625	240	966	18.46	16.67	1.79
924	625	240	924	14.75	16.67	–1.91
968	625	240	968	18.63	16.67	1.96
922	625	240	922	14.57	16.67	–2.10
970	625	240	970	18.79	16.67	2.13
920	625	240	920	14.38	16.67	–2.29
972	625	240	972	18.96	16.67	2.30

Table A-7. Overscan Values, 640 x 480 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, 2.5 µs HBlank *(2 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
974	625	240	974	19.13	16.67	2.46
918	625	240	918	14.19	16.67	–2.47
976	625	240	976	19.29	16.67	2.63
916	625	240	916	14.01	16.67	–2.66
978	625	240	978	19.46	16.67	2.79
914	625	240	914	13.82	16.67	–2.85
980	625	240	980	19.62	16.67	2.96

Table A-8. Overscan Values, 640 x 480 PAL-BDGHI, Character Clock-Based Controller, 8-Pixel Resolution, 2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
944	625	240	944	16.56	16.67	–0.11
952	625	240	952	17.26	16.67	0.59
936	625	240	936	15.84	16.67	–0.82
960	625	240	960	17.95	16.67	1.28
928	625	240	928	15.12	16.67	–1.55
968	625	240	968	18.63	16.67	1.96
920	625	240	920	14.38	16.67	–2.29
976	625	240	976	19.29	16.67	2.63
912	625	240	912	13.63	16.67	–3.04
984	625	240	984	19.95	16.67	3.28
904	625	240	904	12.87	16.67	–3.80
992	625	240	992	20.60	16.67	3.93
1000	625	240	1000	21.23	16.67	4.56
896	625	240	896	12.09	16.67	–4.58
1000	620	242	992	20.60	15.97	4.62
1000	615	244	984	19.95	15.28	4.67
1000	610	246	976	19.29	14.58	4.71
1000	605	248	968	18.63	13.89	4.74
1000	600	250	960	17.95	13.19	4.75
1000	630	239	1008	21.86	17.01	4.84
1000	575	261	920	14.38	9.38	5.01
1000	580	259	928	15.12	10.07	5.05
1000	585	257	936	15.84	10.76	5.08
1000	590	255	944	16.56	11.46	5.10
1000	595	253	952	17.26	12.15	5.11
1008	625	240	1008	21.86	16.67	5.19
888	625	240	888	11.30	16.67	–5.37
880	625	240	880	10.49	16.67	–6.18
872	625	240	872	9.67	16.67	–7.00

Table A-9. Overscan Values, 640 x 480 PAL-BDGHI, Character Clock-Based Controller, 9-Pixel Resolution, 2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
954	625	240	954	17.43	16.67	0.77
936	625	240	936	15.84	16.67	–0.82
972	625	240	972	18.96	16.67	2.30
918	625	240	918	14.19	16.67	–2.47
990	625	240	990	20.44	16.67	3.77
900	650	231	936	15.84	19.79	–3.95
900	625	240	900	12.48	16.67	–4.19
1008	625	240	1008	21.86	16.67	5.19
882	625	240	882	10.69	16.67	–5.97

Table A-10. Overscan Values, 800 x 600 NTSC, Pixel-Based Controller, 1-Pixel Resolution *(1 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
800	777	203	1184	18.45	16.46	1.98
800	819	193	1248	22.63	20.58	2.05
800	798	198	1216	20.59	18.52	2.07
800	756	209	1152	16.18	13.99	2.19
800	714	221	1088	11.25	9.05	2.20
800	735	215	1120	13.79	11.52	2.26
810	805	196	1242	22.25	19.34	2.91
810	770	205	1188	18.72	15.64	3.08
812	750	210	1160	16.76	13.58	3.18
810	735	215	1134	14.85	11.52	3.33
820	735	215	1148	15.89	11.52	4.37
826	750	210	1180	18.17	13.58	4.59
830	735	215	1162	16.90	11.52	5.38
840	780	202	1248	22.63	16.87	5.76
840	785	201	1256	23.12	17.28	5.84
840	765	206	1224	21.11	15.23	5.88
840	790	200	1264	23.61	17.70	5.91
840	750	210	1200	19.53	13.58	5.95
840	770	205	1232	21.62	15.64	5.99
840	755	209	1208	20.07	13.99	6.07
840	775	204	1240	22.13	16.05	6.08
840	740	213	1184	18.45	12.35	6.10
840	760	208	1216	20.59	14.40	6.19
840	730	216	1168	17.33	11.11	6.22
840	745	212	1192	18.99	12.76	6.24
840	720	219	1152	16.18	9.88	6.30
840	735	215	1176	17.89	11.52	6.37
840	725	218	1160	16.76	10.29	6.47
840	715	221	1144	15.59	9.05	6.54
850	777	203	1258	23.24	16.46	6.78

Table A-10. Overscan Values, 800 x 600 NTSC, Pixel-Based Controller, 1-Pixel Resolution *(2 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
850	756	209	1224	21.11	13.99	7.12
854	750	210	1220	20.85	13.58	7.27
850	735	215	1190	18.86	11.52	7.33
850	714	221	1156	16.47	9.05	7.42
860	735	215	1204	19.80	11.52	8.28
868	750	210	1240	22.13	13.58	8.55
870	735	215	1218	20.72	11.52	9.20
882	750	210	1260	23.36	13.58	9.78
880	735	215	1232	21.62	11.52	10.10
882	725	218	1218	20.72	10.29	10.43
890	735	215	1246	22.50	11.52	10.98
900	735	215	1260	23.36	11.52	11.84
900	728	217	1248	22.63	10.70	11.93
900	721	219	1236	21.88	9.88	12.00
900	714	221	1224	21.11	9.05	12.06
910	720	219	1248	22.63	9.88	12.75

Table A-11. Overscan Values, 800 x 600 NTSC, Character Clock-Based Controller, 8-Pixel Resolution, 0–1.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
800	777	203	1184	18.45	16.46	1.98
800	819	193	1248	22.63	20.58	2.05
800	798	198	1216	20.59	18.52	2.07
800	756	209	1152	16.18	13.99	2.19
800	714	221	1088	11.25	9.05	2.20
800	735	215	1120	13.79	11.52	2.26
840	780	202	1248	22.63	16.87	5.76
840	785	201	1256	23.12	17.28	5.84
840	765	206	1224	21.11	15.23	5.88
840	790	200	1264	23.61	17.70	5.91
840	750	210	1200	19.53	13.58	5.95
840	770	205	1232	21.62	15.64	5.99
840	755	209	1208	20.07	13.99	6.07
840	775	204	1240	22.13	16.05	6.08
840	740	213	1184	18.45	12.35	6.10
840	760	208	1216	20.59	14.40	6.19
840	730	216	1168	17.33	11.11	6.22
840	745	212	1192	18.99	12.76	6.24
840	720	219	1152	16.18	9.88	6.30
840	735	215	1176	17.89	11.52	6.37
840	725	218	1160	16.76	10.29	6.47
840	715	221	1144	15.59	9.05	6.54
880	735	215	1232	21.62	11.52	10.10

Table A-12. Overscan Values, 800 x 600 NTSC, Character Clock-Based Controller, 9-Pixel Resolution, 0–3.0 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
810	805	196	1242	22.25	19.34	2.91
810	770	205	1188	18.72	15.64	3.08
810	735	215	1134	14.85	11.52	3.33
882	750	210	1260	23.36	13.58	9.78
882	725	218	1218	20.72	10.29	10.43
900	735	215	1260	23.36	11.52	11.84
900	728	217	1248	22.63	10.70	11.93
900	721	219	1236	21.88	9.88	12.00
900	714	221	1224	21.11	9.05	12.06

Table A-13. Overscan Values 800 x 600 NTSC, Pixel-Based Controller, 1-Pixel Resolution, 3:2 Clocking Mode *(1 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1170	770	205	1144	15.59	15.64	–0.04
1170	735	215	1092	11.57	11.52	0.05
1170	805	196	1196	19.26	19.34	–0.08
1176	750	210	1120	13.79	13.58	0.21
1176	825	191	1232	21.62	21.40	0.22
1190	765	206	1156	16.47	15.23	1.24
1150	819	193	1196	19.26	20.58	–1.31
1190	810	195	1224	21.11	19.75	1.36
1190	720	219	1088	11.25	9.88	1.37
1150	756	209	1104	12.54	13.99	–1.46
1200	777	203	1184	18.45	16.46	1.98
1200	798	198	1216	20.59	18.52	2.07
1200	756	209	1152	16.18	13.99	2.19
1200	714	221	1088	11.25	9.05	2.20
1200	735	215	1120	13.79	11.52	2.26
1140	735	215	1064	9.25	11.52	–2.27
1134	775	204	1116	13.48	16.05	–2.57
1134	825	191	1188	18.72	21.40	–2.68
1134	800	197	1152	16.18	18.93	–2.75
1134	750	210	1080	10.59	13.58	–2.99
1218	750	210	1160	16.76	13.58	3.18
1120	810	195	1152	16.18	19.75	–3.57
1120	765	206	1088	11.25	15.23	–3.98
1230	735	215	1148	15.89	11.52	4.37
1100	819	193	1144	15.59	20.58	–4.98
1250	756	209	1200	19.53	13.99	5.54
1092	825	191	1144	15.59	21.40	–5.81
1260	765	206	1224	21.11	15.23	5.88
1260	750	210	1200	19.53	13.58	5.95
1260	770	205	1232	21.62	15.64	5.99

Table A-13. Overscan Values 800 x 600 NTSC, Pixel-Based Controller, 1-Pixel Resolution, 3:2 Clocking Mode *(2 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1260	755	209	1208	20.07	13.99	6.07
1260	740	213	1184	18.45	12.35	6.10
1260	760	208	1216	20.59	14.40	6.19
1260	730	216	1168	17.33	11.11	6.22
1260	745	212	1192	18.99	12.76	6.24
1260	720	219	1152	16.18	9.88	6.30
1260	735	215	1176	17.89	11.52	6.37
1260	725	218	1160	16.76	10.29	6.47
1260	715	221	1144	15.59	9.05	6.54
1080	805	196	1104	12.54	19.34	–6.81
1290	735	215	1204	19.80	11.52	8.28
1050	828	191	1104	12.54	21.40	–8.86
1050	816	194	1088	11.25	20.16	–8.92
1050	831	190	1108	12.85	21.81	–8.96
1050	819	193	1092	11.57	20.58	–9.00
1050	807	196	1076	10.26	19.34	–9.08
1050	822	192	1096	11.90	20.99	–9.09
1050	810	195	1080	10.59	19.75	–9.16
1050	825	191	1100	12.22	21.40	–9.18
1050	813	194	1084	10.92	20.16	–9.24
1050	798	198	1064	9.25	18.52	–9.27
1050	801	197	1068	9.59	18.93	–9.34
1050	804	196	1072	9.92	19.34	–9.42
1320	735	215	1232	21.62	11.52	10.10
1330	720	219	1216	20.59	9.88	10.72
1350	721	219	1236	21.88	9.88	12.00
1350	714	221	1224	21.11	9.05	12.06

Table A-14. Overscan Values 800 x 600 NTSC, Character Clocked-Based Controller, 8-Pixel Resolution, 3:2 Clocking Mode

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1176	750	210	1120	13.79	13.58	0.21
1176	825	191	1232	21.62	21.40	0.22
1200	777	203	1184	18.45	16.46	1.98
1200	798	198	1216	20.59	18.52	2.07
1200	756	209	1152	16.18	13.99	2.19
1200	714	221	1088	11.25	9.05	2.20
1200	735	215	1120	13.79	11.52	2.26
1120	810	195	1152	16.18	19.75	–3.57
1120	765	206	1088	11.25	15.23	–3.98
1080	805	196	1104	12.54	19.34	–6.81
1320	735	215	1232	21.62	11.52	10.10

Table A-15. Overscan Values 800 x 600 NTSC, Character Clocked-Based Controller, 9-Pixel Resolution, 3:2 Clocking Mode

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1170	770	205	1144	15.59	15.64	–0.04
1170	735	215	1092	11.57	11.52	0.05
1170	805	196	1196	19.26	19.34	–0.08
1134	775	204	1116	13.48	16.05	–2.57
1134	825	191	1188	18.72	21.40	–2.68
1134	800	197	1152	16.18	18.93	–2.75
1134	750	210	1080	10.59	13.58	–2.99
1260	765	206	1224	21.11	15.23	5.88
1260	750	210	1200	19.53	13.58	5.95
1260	770	205	1232	21.62	15.64	5.99
1260	755	209	1208	20.07	13.99	6.07
1260	740	213	1184	18.45	12.35	6.10
1260	760	208	1216	20.59	14.40	6.19
1260	730	216	1168	17.33	11.11	6.22
1260	745	212	1192	18.99	12.76	6.24
1260	720	219	1152	16.18	9.88	6.30
1260	735	215	1176	17.89	11.52	6.37
1260	725	218	1160	16.76	10.29	6.47
1260	715	221	1144	15.59	9.05	6.54
1080	805	196	1104	12.54	19.34	–6.81
1350	721	219	1236	21.88	9.88	12.00
1350	714	221	1224	21.11	9.05	12.06

Table A-16. Overscan Values, 800 x 600 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, >2.5 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
950	750	250	1140	13.63	13.19	0.44
950	775	242	1178	16.42	15.97	0.44
940	750	250	1128	12.71	13.19	–0.48
950	725	259	1102	10.65	10.07	0.58
950	800	235	1216	19.03	18.40	0.63
950	825	228	1254	21.48	20.83	0.65
960	750	250	1152	14.53	13.19	1.34
930	750	250	1116	11.77	13.19	–1.42
970	750	250	1164	15.41	13.19	2.22
920	750	250	1104	10.81	13.19	–2.38
980	750	250	1176	16.27	13.19	3.08
910	750	250	1092	9.83	13.19	–3.36
900	825	228	1188	17.12	20.83	–3.71
900	800	235	1152	14.53	18.40	–3.87
990	750	250	1188	17.12	13.19	3.93
900	775	242	1116	11.77	15.97	–4.20
1000	785	239	1256	21.61	17.01	4.59
1000	775	242	1240	20.60	15.97	4.62
1000	750	250	1200	17.95	13.19	4.75
1000	780	241	1248	21.10	16.32	4.79
1000	760	247	1216	19.03	14.24	4.79
1000	770	244	1232	20.08	15.28	4.80
1000	745	252	1192	17.40	12.50	4.90
1000	730	257	1168	15.70	10.76	4.94
1000	755	249	1208	18.49	13.54	4.95
1000	765	246	1224	19.56	14.58	4.97

Table A-17. Overscan Values, 800 x 600 PAL-BDGHI, Character Clock-Based Controller, 8-Pixel Resolution

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
960	750	250	1152	14.53	13.19	1.34
920	750	250	1104	10.81	13.19	–2.38
1000	785	239	1256	21.61	17.01	4.59
1000	775	242	1240	20.60	15.97	4.62
1000	750	250	1200	17.95	13.19	4.75
1000	780	241	1248	21.10	16.32	4.79
1000	760	247	1216	19.03	14.24	4.79
1000	770	244	1232	20.08	15.28	4.80
1000	745	252	1192	17.40	12.50	4.90
1000	730	257	1168	15.70	10.76	4.94
1000	755	249	1208	18.49	13.54	4.95
1000	765	246	1224	19.56	14.58	4.97
1000	740	254	1184	16.84	11.81	5.03
1000	725	259	1160	15.12	10.07	5.05
1000	720	261	1152	14.53	9.38	5.15
1000	735	256	1176	16.27	11.11	5.16
1000	715	263	1144	13.93	8.68	5.25
1040	750	250	1248	21.10	13.19	7.91

Table A-18. Overscan Values, 800 x 600 PAL-BDGHI, Character Clock-Based Controller, 9-Pixel Resolution

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Resolution
900	825	228	1188	17.12	20.83	–3.71
900	800	235	1152	14.53	18.40	–3.87
990	750	250	1188	17.12	13.19	3.93
900	775	242	1116	11.77	15.97	–4.20

Table A-19. Overscan Values 800 x 600 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, 3:2 Clocking Mode *(1 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1420	750	250	1136	13.33	13.19	0.13
1410	750	250	1128	12.71	13.19	–0.48
1430	750	250	1144	13.93	13.19	0.74
1400	825	228	1232	20.08	20.83	–0.75
1400	750	250	1120	12.09	13.19	–1.11
1440	750	250	1152	14.53	13.19	1.34
1390	750	250	1112	11.46	13.19	–1.74
1450	750	250	1160	15.12	13.19	1.92
1380	750	250	1104	10.81	13.19	–2.38
1460	750	250	1168	15.70	13.19	2.51
1370	750	250	1096	10.16	13.19	–3.03
1470	750	250	1176	16.27	13.19	3.08
1480	750	250	1184	16.84	13.19	3.65
1360	750	250	1088	9.50	13.19	–3.69
1350	825	228	1188	17.12	20.83	–3.71
1350	800	235	1152	14.53	18.40	–3.87
1350	775	242	1116	11.77	15.97	–4.20
1490	750	250	1192	17.40	13.19	4.20
1500	785	239	1256	21.61	17.01	4.59
1500	775	242	1240	20.60	15.97	4.62
1500	750	250	1200	17.95	13.19	4.75
1500	780	241	1248	21.10	16.32	4.79
1500	760	247	1216	19.03	14.24	4.79
1500	770	244	1232	20.08	15.28	4.80
1500	745	252	1192	17.40	12.50	4.90
1500	730	257	1168	15.70	10.76	4.94
1500	755	249	1208	18.49	13.54	4.95
1500	765	246	1224	19.56	14.58	4.97
1500	740	254	1184	16.84	11.81	5.03

Table A-19. Overscan Values 800 x 600 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, 3:2 Clocking Mode *(2 of 2)*

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1500	725	259	1160	15.12	10.07	5.05
1500	720	261	1152	14.53	9.38	5.15
1500	735	256	1176	16.27	11.11	5.16
1500	715	263	1144	13.93	8.68	5.25
1510	750	250	1208	18.49	13.19	5.30
1520	750	250	1216	19.03	13.19	5.83
1530	750	250	1224	19.56	13.19	6.36
1540	750	250	1232	20.08	13.19	6.89
1300	825	228	1144	13.93	20.83	–6.90
1550	750	250	1240	20.60	13.19	7.40
1560	750	250	1248	21.10	13.19	7.91
1570	750	250	1256	21.61	13.19	8.41
1250	822	229	1096	10.16	20.49	–10.32
1250	825	228	1100	10.49	20.83	–10.34
1250	828	227	1104	10.81	21.18	–10.37
1250	831	226	1108	11.14	21.53	–10.39
1250	834	225	1112	11.46	21.88	–10.42
1250	813	231	1084	9.17	19.79	–10.62
1250	816	230	1088	9.50	20.14	–10.64
1250	819	229	1092	9.83	20.49	–10.65

Table A-20. Overscan Values 800 x 600 PAL-BDGHI, Character Clock-Based Controller, 8-Pixel Resolution, 3:2 Clocking Mode

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1400	825	228	1232	20.08	20.83	–0.75
1400	750	250	1120	12.09	13.19	–1.11
1440	750	250	1152	14.53	13.19	1.34
1480	750	250	1184	16.84	13.19	3.65
1360	750	250	1088	9.50	13.19	–3.69
1520	750	250	1216	19.03	13.19	5.83
1560	750	250	1248	21.10	13.19	7.91

Table A-21. Overscan Values 800 x 600 PAL-BDGHI, Character Clock-Based Controller, 9-Pixel Resolution, 3:2 Clocking Mode

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1440	750	250	1152	14.53	13.19	1.34
1350	825	228	1188	17.12	20.83	–3.71
1350	800	235	1152	14.53	18.40	–3.87
1350	775	242	1116	11.77	15.97	–4.20
1530	750	250	1224	19.56	13.19	6.36

Table A-22. Overscan Values 1024 x 768 NTSC, Pixel-Based Controller, 1-Pixel Resolution, >1.50 µs Hblank *(1 of 2)*

Graphics Controller		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1170	945	214	1404	11.97	11.93	0.03
1170	1015	199	1508	18.04	18.11	–0.07
1170	980	206	1456	15.11	15.23	–0.11
1176	1050	192	1568	21.18	20.99	0.19
1170	1050	192	1560	20.77	20.99	–0.22
1176	975	207	1456	15.11	14.81	0.3
1182	1050	192	1576	21.58	20.99	0.59
1164	1050	192	1552	20.36	20.99	–0.63
1160	945	214	1392	11.21	11.93	–0.73
1180	945	214	1416	12.71	11.93	0.78
1188	1050	192	1584	21.97	20.99	0.98
1158	1050	192	1544	19.95	20.99	–1.04
1190	1035	195	1564	20.97	19.75	1.22
1190	990	204	1496	17.38	16.05	1.33
1152	1050	192	1536	19.53	20.99	–1.45
1150	945	214	1380	10.44	11.93	–1.5
1190	945	214	1428	13.45	11.93	1.51
1150	1008	200	1472	16.03	17.7	–1.66
1200	1029	196	1568	21.18	19.34	1.83
1200	1008	200	1536	19.53	17.7	1.84
1146	1050	192	1528	19.11	20.99	–1.88
1200	966	209	1472	16.03	13.99	2.04
1200	987	205	1504	17.82	15.64	2.18
1200	945	214	1440	14.17	11.93	2.23
1140	945	214	1368	9.65	11.93	–2.28
1140	1050	192	1520	18.69	20.99	–2.3
1200	924	219	1408	12.22	9.88	2.34
1134	1025	197	1476	16.26	18.93	–2.67
1134	950	213	1368	9.65	12.35	–2.69
1134	1000	202	1440	14.17	16.87	–2.7

Table A-22. Overscan Values 1024 x 768 NTSC, Pixel-Based Controller, 1-Pixel Resolution, >1.50 μs Hblank *(2 of 2)*

Graphics Controller		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1134	1050	192	1512	18.26	20.99	–2.73
1134	975	207	1404	11.97	14.81	–2.85
1210	945	214	1452	14.88	11.93	2.94
1218	975	207	1508	18.04	14.81	3.22
1220	945	214	1464	15.58	11.93	3.64
1230	945	214	1476	16.26	11.93	4.33
1240	945	214	1488	16.94	11.93	5
1250	945	214	1500	17.6	11.93	5.67
1260	990	204	1584	21.97	16.05	5.92
1260	985	205	1576	21.58	15.64	5.94
1260	980	206	1568	21.18	15.23	5.95
1260	960	210	1536	19.53	13.58	5.95
1260	975	207	1560	20.77	14.81	5.96
1260	965	209	1544	19.95	13.99	5.96
1260	970	208	1552	20.36	14.4	5.96
1260	925	218	1480	16.49	10.29	6.2
1260	930	217	1488	16.94	10.7	6.24
1260	935	216	1496	17.38	11.11	6.27
1260	940	215	1504	17.82	11.52	6.3
1260	945	214	1512	18.26	11.93	6.32
1260	950	213	1520	18.69	12.35	6.34
1260	955	212	1528	19.11	12.76	6.35
1260	915	221	1464	15.58	9.05	6.52
1260	920	220	1472	16.03	9.47	6.57
1270	945	214	1524	18.9	11.93	6.97

Table A-23. Overscan Values 1024 x 768 NTSC, Character Clock-Based Controller, 8-Pixel Resolution, >1.50 µs HBlank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1176	1050	192	1568	21.18	20.99	0.19
1176	975	207	1456	15.11	14.81	0.30
1160	945	214	1392	11.21	11.93	–0.73
1152	1050	192	1536	19.53	20.99	–1.45
1200	1029	196	1568	21.18	19.34	1.83
1200	1008	200	1536	19.53	17.70	1.84
1200	966	209	1472	16.03	13.99	2.04
1200	987	205	1504	17.82	15.64	2.18
1200	945	214	1440	14.17	11.93	2.23
1200	924	219	1408	12.22	9.88	2.34
1240	945	214	1488	16.94	11.93	5.00
1280	945	214	1536	19.53	11.93	7.60
1320	945	214	1584	21.97	11.93	10.04
1176	1050	192	1568	21.18	20.99	0.19
1176	975	207	1456	15.11	14.81	0.30
1160	945	214	1392	11.21	11.93	–0.73
1152	1050	192	1536	19.53	20.99	–1.45
1200	1029	196	1568	21.18	19.34	1.83
1200	1008	200	1536	19.53	17.70	1.84
1200	966	209	1472	16.03	13.99	2.04
1200	987	205	1504	17.82	15.64	2.18
1200	945	214	1440	14.17	11.93	2.23
1200	924	219	1408	12.22	9.88	2.34
1128	1050	192	1504	17.82	20.99	–3.17
1240	945	214	1488	16.94	11.93	5.00
1280	945	214	1536	19.53	11.93	7.60

Table A-24. Overscan Values 1024 x 768 NTSC, Character Clock-Based Controller, 9-Pixel Resolution

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1170	945	214	1404	11.97	11.93	0.03
1170	1015	199	1508	18.04	18.11	–0.07
1170	980	206	1456	15.11	15.23	–0.11
1170	1050	192	1560	20.77	20.99	–0.22
1188	1050	192	1584	21.97	20.99	0.98
1152	1050	192	1536	19.53	20.99	–1.45
1134	1025	197	1476	16.26	18.93	–2.67
1134	950	213	1368	9.65	12.35	–2.69
1134	1000	202	1440	14.17	16.87	–2.70
1134	1050	192	1512	18.26	20.99	–2.73
1134	975	207	1404	11.97	14.81	–2.85
1260	990	204	1584	21.97	16.05	5.92
1260	985	205	1576	21.58	15.64	5.94
1260	980	206	1568	21.18	15.23	5.95
1260	960	210	1536	19.53	13.58	5.95
1260	975	207	1560	20.77	14.81	5.96
1260	965	209	1544	19.95	13.99	5.96
1260	970	208	1552	20.36	14.40	5.96
1260	925	218	1480	16.49	10.29	6.20
1260	930	217	1488	16.94	10.70	6.24
1260	935	216	1496	17.38	11.11	6.27
1260	940	215	1504	17.82	11.52	6.30
1260	945	214	1512	18.26	11.93	6.32
1260	950	213	1520	18.69	12.35	6.34
1260	955	212	1528	19.11	12.76	6.35
1260	915	221	1464	15.58	9.05	6.52
1260	920	220	1472	16.03	9.47	6.57

Table A-25. Overscan Values 1024 x 768 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, >3 μs Hblank *(1 of 2)*

Graphics Controller		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1410	1000	240	1504	16.2	16.67	–0.46
1400	975	247	1456	13.44	14.24	–0.8
1400	1050	229	1568	19.62	20.49	–0.86
1440	1000	240	1536	17.95	16.67	1.28
1450	975	247	1508	16.43	14.24	2.19
1380	1000	240	1472	14.38	16.67	–2.29
1470	1000	240	1568	19.62	16.67	2.96
1350	1025	235	1476	14.61	18.4	–3.79
1350	1050	229	1512	16.65	20.49	–3.84
1350	975	247	1404	10.23	14.24	–4
1350	1000	240	1440	12.48	16.67	–4.19
1500	1000	240	1600	21.23	16.67	4.56
1500	1005	239	1608	21.62	17.01	4.61
1500	1010	238	1616	22.01	17.36	4.65
1500	980	245	1568	19.62	14.93	4.69
1500	985	244	1576	20.03	15.28	4.75
1500	960	250	1536	17.95	13.19	4.75
1500	990	243	1584	20.44	15.62	4.81
1500	965	249	1544	18.37	13.54	4.83
1500	945	254	1512	16.65	11.81	4.84
1500	995	242	1592	20.83	15.97	4.86
1500	970	248	1552	18.79	13.89	4.91
1500	950	253	1520	17.09	12.15	4.93
1500	975	247	1560	19.21	14.24	4.97
1500	935	257	1496	15.75	10.76	4.99
1500	920	261	1472	14.38	9.38	5.01
1500	955	252	1528	17.52	12.5	5.02
1500	940	256	1504	16.2	11.11	5.09
1500	925	260	1480	14.84	9.72	5.12
1500	930	259	1488	15.3	10.07	5.23

Table A-25. Overscan Values 1024 x 768 PAL-BDGHI, Pixel-Based Controller, 1-Pixel Resolution, >3 μs Hblank *(2 of 2)*

Graphics Controller		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1500	915	263	1464	13.91	8.68	5.23
1320	1000	240	1408	10.49	16.67	–6.18
1300	1050	229	1456	13.44	20.49	–7.05
1550	975	247	1612	21.82	14.24	7.58
1250	1065	226	1420	11.25	21.53	–10.2
1250	1056	228	1408	10.49	20.83	–10.3
1250	1068	225	1424	11.5	21.88	–10.3
1250	1047	230	1396	9.72	20.14	–10.4
1250	1059	227	1412	10.74	21.18	–10.4
1250	1038	232	1384	8.94	19.44	–10.5
1250	1050	229	1400	9.98	20.49	–10.5
1250	1062	226	1416	11	21.53	–10.5
1250	1041	231	1388	9.2	19.79	–10.5
1250	1053	228	1404	10.23	20.83	–10.6
1250	1044	230	1392	9.46	20.14	-–0.6

Table A-26. 1024 x 768 PAL-BDGHI, Character Clock-Based Controller, 8-Pixel Resolution, >4 μs Hblank

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1400	975	247	1456	13.44	14.24	–0.8
1400	1050	229	1568	19.62	20.49	–0.86
1440	1000	240	1536	17.95	16.67	1.28
1320	1000	240	1408	10.49	16.67	–6.18

Table A-27. Overscan Values 1024 x 768 PAL-BDGHI, Character Clock-Based Controller, 9-Pixel Resolution

Controller Pixels		Encoder Pixels		Overscan (Percent)		
Total		Active	Total			
H_CLKI	V_LINESI	V_ACTIVEO	H_CLKO	Horizontal	Vertical	Delta
1440	1000	240	1536	17.95	16.67	1.28
1350	1025	235	1476	14.61	18.4	–3.79
1350	1050	229	1512	16.65	20.49	–3.84
1350	975	247	1404	10.23	14.24	–4
1350	1000	240	1440	12.48	16.67	–4.19

B

Approved Crystal Vendors Appendix

Conexant conducted a series of internal tests and used the results to generate this list of approved crystal vendors for the CX25874/5. Manufacturers not appearing in this list may be acceptable, but verification testing on the target PCB with samples is recommended prior to production.

Standard Crystal (El Monte, CA)

Phone Number: (626) 443-2121

FAX Number: (626) 443-9049

E-mail:stdxtl@pacbell.net

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:AAL13M500000GXE20A

Half Height/50 ppm:AAK13M500000GXE20A

Full Height/25 ppm:Did Not Qualify

MMD Components (Irvine, CA)

Phone Number: (949) 753-5888

FAX Number: (949) 753-5889

E-mail:info@mmdcomp.com

Internet:www.mmdcomp.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50ppm Total Tolerance:A20BA1-13.500 MHz

Half Height/50 ppm:B20BA1-13.500 MHz

Full Height/25 ppm:MMC-135-13.500 MHz (not tested)

Half Height/25 ppm:MMC-136-13.500 MHz (not tested)

General Electronics Devices (San Marcos, CA)

Phone Number: (760) 591-4170

FAX Number: (760) 591-4164

E-mail:gedlm@4dcomm.com

Internet:www.gedlm.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:PKHC49-13.500-.020-.005

Half Height/50 ppm:PKHC49/-13.500-.020-.005

Full Height/25 ppm:PKHC49/-13.500-.020-.0025-15R

Half Height/25 ppm:PKHC49/-13.500-.020-.0025

Fox Electronics (Fort Myers, FL)

Phone Number: (941) 693-0099

FAX Number: (941) 693-1554

E-mail:sales@foxonline.com

Internet:www.foxonline.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:HC49U-13.500 /50/0/70/20 pF

Half Height/50 ppm:HC49S-13.500/50/0/70/20 pF

Full Height/25 ppm:HC49U-13.500 /25/0/70/20 pF

Half Height/25 ppm:HC49S-13.500 /25/0/70/20 pF (not tested)

Bomar Crystal Co. (Middlesex, NJ)

Phone Number: (732) 356-7787

FAX Number: (732) 356-7362

E-mail:sales@bomarcrystal.com

Internet:www.bomarcrystal.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:BRC1C14F-13.50000 or

BC1DDA120-13.50000

Half Height/50 ppm:ACR-49S012025-13.50000 or

BC14DDA120-13.50000

Full Height/25 ppm:BRCIH14F-13.50000 or

BC1AAA120-13.50000

Half Height/25 ppm:BC14AAA120-13.50000 (not tested)

ILSI America (Reno, NV)

Phone Number: (775) 851-8880x103 / (888)355-4574

FAX Number: (775) 851-8882

E-mail:e-mail@ilsiamerica.com

Internet:www.ilsiamerica.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:HC49U-25/25-13.500-20

Half Height/50 ppm:HC49US-FB1F20-13.500

Full Height/25 ppm:Did Not Qualify

Cardinal Components (Wayne, NJ)

Phone Number: (973) 785-1333

FAX Number: (973) 785-0053

E-mail:cardinal@cardinalxtal.com

Internet:www.cardinalxtal.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:C49-A4BRC7-50-13.5D20

Half Height/50 ppm:CLP-A4BRC7-70-13.5D20

Full Height/25 ppm:C49-A4B6C4-25-13.5D20

Half Height/25 ppm:CLP-A4B6C4-25-13.5D20

Raltron Electronics Corp. (Miami, FL)

Phone Number: (305) 593-6033

FAX Number: (305) 594-3973

E-mail:Sales@raltron.com

Internet:www.raltron.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:A-13.500-20-RS1

Half Height/50 ppm:AS-13.500-20-RS1

Full Height/25 ppm:A-13.500-20-RS1

Half Height/25ppm:AS-13.500-20-SMD-NV

Valpey-Fisher (Hopkinton, MA)

Phone Number: (508) 435-6831

FAX Number: (508) 435-5289

Internet:www.valpeyfisher.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:M490013.500020RSVM

Half Height/50 ppm:M49K013.50002099VM

Full Height/25 ppm:M490013.50002099VM

Corning Frequency Control (Mount Holly Springs, PA)

Phone Number: (717) 486-3411

FAX Number: (717) 486-5920

E-mail:sales@ofc.come

Internet:www.corningfrequency.com

Part Numbers for 13.500 MHz, Fundamental, 20 pF Load Crystal with an HC49U Type of Package:

Full Height/50 ppm Total Tolerance:TQ RSD 13.5FH50

Half Height/50 ppm:TQ RSD 13.5LP50

Full Height/25 ppm:TQ RSD 13.5FH25

Half Height/25 ppm:TQ RSD 13.5LP25 (not tested)

C

Autoconfiguration Mode Register Values and Details Appendix

This encoder contains 48 autoconfiguration modes. Tables C-1 through C-9 contain all register values that change when the autoconfiguration register 0xB8 is written. These tables also contain pertinent video parameters for each mode.

Table C-1. CX25874/875 Register Values for Autoconfiguration Modes 0–4 *(1 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
Autoconfig Register (index 0xB8) Hexadecimal Value	00	01	02	03	04
Purpose of mode	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	640x480	640x480	800x600	800x600	640x480
Overscan Ratio	Lower	Standard	Alternate	Lower	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.79	16.56	21.62	14.53	13.79
Vertical Overscan Ratio/ Percentage (VOC)	13.58	16.67	11.52	13.19	13.58
Overscan Percentages Delta (HOC - VOC)	0.21	–0.11	10.10	1.34	0.21
H_CLKI = HTOTAL	784	944	880	960	784
VLINES_I = VTOTAL	600	625	735	750	600
H_BLANKI = Horizontal Blanking Region	126	266	66	140	126
V_BLANKI = Vertical Blanking Region	75	90	86	95	75
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	28195793	29500008	38769241	36000000	28195793
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character

Table C-1. CX25874/875 Register Values for Autoconfiguration Modes 0–4 *(2 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	00	00
0x76	00	60	A0	00	00
0x78	80	80	20	20	80
0x7A	84	8A	B6	AA	84
0x7C	96	A6	CE	CA	96
0x7E	60	68	B4	9A	60
0x80	7D	C1	55	0D	7D
0x82	22	2E	20	29	22
0x84	D4	F2	D8	FC	D4
0x86	27	27	39	39	27
0x88	00	00	00	00	00
0x8A	10	B0	70	C0	10
0x8C	7E	0A	42	8C	7E
0x8E	03	0B	03	03	03
0x90	58	71	DF	EE	58
0x92	4B	5A	56	5F	4B
0x94	E0	E0	58	58	E0
0x96	36	36	3A	3A	36
0x98	92	00	CD	66	92
0x9A	54	50	9C	96	54
0x9C	0E	72	14	00	0E
0x9E	88	1C	3B	00	88
0xA0	0C	0D	11	10	0C
0xA2	0A	24	0A	24	0A
0xA4	E5	F0	E5	F0	E5
0xA6	76	58	74	57	76
0xA8	79	81	77	80	C0
0xAA	44	49	43	48	89
0xAC	85	8C	85	8C	9A
0xAE	00	0C	BA	18	00

Table C-1. CX25874/875 Register Values for Autoconfiguration Modes 0–4 *(3 of 3)*

Autoconfiguration Mode #	0	1	2	3	4
0xB0	00	8C	E8	28	00
0xB2	80	79	A2	87	80
0xB4	20	26	17	1F	20

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-2. CX25874/875 Register Values for Autoconfiguration Modes 5–10 *(1 of 2)*

Autoconfiguration Mode #	5	6	7	8	9	10
Autoconfig Register (index 0xB8) Hexadecimal Value	05	06	07	10	11	12
Purpose of Mode	Desktop	Desktop	Desktop	Boot-Up Screen	Boot-Up Screen	Desktop
Type of Digital Input	YCrCb	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	640x480	800x600	800x600	640x400	640x400	1024x768
Overscan Ratio	Standard	Alternate	Lower	Standard	Standard	Standard
Horizontal Overscan Ratio/ Percentage (HOC)	16.56	21.62	14.53	17.47	15.12	15.11
Vertical Overscan Ratio/ Percentage (VOC)	16.67	11.52	13.19	17.70	13.19	14.81
Overscan Percentages Delta (HOC - VOC)	–0.11	10.10	1.34	–0.23	1.93	0.30
H_CLKI = HTOTAL	944	880	960	936	1160	1176
VLINES_I = VTOTAL	625	735	750	525	500	975
H_BLANKI = Horizontal Blanking Region	266	66	140	259	363	133
V_BLANKI = Vertical Blanking Region	90	86	95	76	64	130
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	29500008	38769241	36000000	29454552	28999992	68727276
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	00	00	20
0x76	60	A0	00	50	40	60
0x78	80	20	20	80	80	00
0x7A	8A	B6	AA	8A	88	D8
0x7C	A6	CE	CA	9C	A2	F2
0x7E	68	B4	9A	6A	64	EE
0x80	C1	55	0D	A9	AF	71
0x82	2E	20	29	27	29	24
0x84	F2	D8	FC	CA	FC	D0
0x86	27	39	39	27	27	4B
0x88	00	00	00	00	00	00

Table C-2. CX25874/875 Register Values for Autoconfiguration Modes 5–10 *(2 of 2)*

Autoconfiguration Mode #	5	6	7	8	9	10
0x8A	B0	70	C0	A8	88	98
0x8C	0A	42	8C	03	6B	85
0x8E	0B	03	03	0B	0C	04
0x90	71	DF	EE	0D	F4	CF
0x92	5A	56	5F	4C	40	82
0x94	E0	58	58	90	90	00
0x96	36	3A	3A	36	35	3F
0x98	00	CD	66	00	9A	6E
0x9A	50	9C	96	50	49	AB
0x9C	72	14	00	46	8E	A3
0x9E	1C	3B	00	17	E3	8B
0xA0	0D	11	10	0D	0C	1E
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	58	74	57	75	58	74
0xA8	CE	BE	CB	79	82	77
0xAA	92	87	90	44	49	43
0xAC	A4	9A	A4	85	8C	85
0xAE	0C	BA	18	C7	E9	00
0xB0	8C	E8	28	71	5D	00
0xB2	79	A2	87	1C	23	00
0xB4	26	17	1F	1F	27	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-3. CX25874/875 Register Values for Autoconfiguration Modes 11–15 *(1 of 2)*

Autoconfiguration Mode #	11	12	13	14	15
Autoconfig Register (index 0xB8) Hexadecimal Value	13	14	15	16	17
Purpose of Mode	Desktop	Game	Game	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	YCrCb	YCrCb
Active Resolution	1024x768	320x240, Pix_Double Set	320x240, Pix_Double Set	1024x768	1024x768
Overscan Ratio	Standard	Standard	Standard	Higher	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	13.44	13.79	15.84	15.11	13.44
Vertical Overscan Ratio/ Percentage (VOC)	14.24	13.58	19.79	14.81	14.24
Overscan Percentages Delta (HOC - VOC)	–0.80	0.21	–3.95	0.30	–0.80
H_CLKI = HTOTAL	1400	1568	1800	1176	1400
VLINES_I = VTOTAL	975	300	325	975	975
H_BLANKI = Horizontal Blanking Region	329	349	385	133	329
V_BLANKI = Vertical Blanking Region	131	37	50	130	131
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI
Frequency of CLK (Hz)	68249989	14097896	14625000	68727276	68249989
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character	Pixel or Character
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	40	40	20	20
0x76	60	00	50	60	60
0x78	00	80	80	00	00
0x7A	D6	84	8A	D8	D6
0x7C	FE	96	A4	F2	FE
0x7E	E6	60	66	EE	E6
0x80	87	7D	B7	71	87
0x82	2B	22	32	24	2B
0x84	F8	D5	EA	D0	F8
0x86	4B	27	27	4B	4B
0x88	00	00	00	00	00
0x8A	78	20	08	98	78

Table C-3. CX25874/875 Register Values for Autoconfiguration Modes 11–15 *(2 of 2)*

Autoconfiguration Mode #	11	12	13	14	15
0x8C	49	5D	81	85	49
0x8E	0D	1E	1F	04	0D
0x90	CF	2C	45	CF	CF
0x92	83	25	32	82	83
0x94	00	F0	F0	00	00
0x96	3F	31	31	3F	3F
0x98	EC	49	A4	6E	EC
0x9A	A1	42	40	AB	A1
0x9C	55	0E	00	A3	55
0x9E	55	88	00	8B	55
0xA0	1E	0C	0D	1E	1E
0xA2	24	0A	24	0A	24
0xA4	F0	E5	F0	E5	F0
0xA6	56	76	58	74	56
0xA8	7F	79	81	BD	C9
0xAA	47	44	49	87	8F
0xAC	8C	85	8C	9A	A4
0xAE	57	00	32	00	57
0xB0	F8	00	BB	00	F8
0xB2	F1	80	CD	00	F1
0xB4	18	20	26	14	18

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-4. CX25874/875 Register Values for Autoconfiguration Modes 16–21 *(1 of 2)*

Autoconfiguration Mode #	16	17	18	19	20	21
Autoconfig Register (index 0xB8) Hexadecimal Value	20	21	22	23	24	25
Purpose of Mode	Desktop	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	640x480	640x480	800x600	800x600	640x480	640x480
Overscan Ratio	Standard	Lower	Lower	Standard	Lower	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	16.76	13.63	13.78	16.42	13.78	13.63
Vertical Overscan Ratio/ Percentage (VOC)	14.81	13.19	13.58	15.97	13.58	13.19
Overscan Percentages Delta (HOC - VOC)	1.95	0.44	0.21	0.45	0.20	0.44
H_CLKI = HTOTAL	800	950	1176	950	784	950
VLINES_I = VTOTAL	609	600	750	775	600	600
H_BLANKI = Horizontal Blanking Region	140	271	329	131	126	271
V_BLANKI = Vertical Blanking Region	81	76	94	109	75	76
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	PAL-60	PAL-BDGHI
Frequency of CLK (Hz)	29202793	28500011	52867138	36812508	28195793	28500011
Type of Clock	Pixel Only	Pixel Only	Pixel or Character	Pixel Only	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	20	00	00	00
0x76	40	20	C0	34	00	20
0x78	80	80	20	20	80	80
0x7A	8A	86	A6	AE	84	86
0x7C	9A	A0	BA	CE	9E	A0
0x7E	68	60	98	A0	5E	60
0x80	A1	9D	D9	2B	7D	9D
0x82	24	29	22	2D	22	29
0x84	D1	FC	D4	F4	D4	FC
0x86	27	27	38	39	27	27
0x88	00	00	00	00	00	00
0x8A	20	B6	98	B6	10	B6

Table C-4. CX25874/875 Register Values for Autoconfiguration Modes 16–21 *(2 of 2)*

Autoconfiguration Mode #	16	17	18	19	20	21
0x8C	8C	0F	49	83	7E	0F
0x8E	03	0B	0C	03	03	0B
0x90	61	58	EE	07	58	58
0x92	51	4C	5E	6D	4B	4C
0x94	E0	E0	58	58	E0	E0
0x96	06	36	3A	3B	06	36
0x98	1F	B8	B7	AE	92	B8
0x9A	55	4E	5D	97	54	4E
0x9C	A1	AB	1B	72	0E	AB
0x9E	FA	AA	7F	5C	88	AA
0xA0	0C	0C	17	10	0C	0C
0xA2	0A	24	0A	24	20	24
0xA4	E5	F0	E5	F0	F0	F0
0xA6	75	58	74	57	58	58
0xA8	79	82	78	80	82	CE
0xAA	44	49	43	48	49	93
0xAC	85	8C	85	8C	8C	A4
0xAE	7C	2C	00	01	7C	2C
0xB0	1A	25	00	04	23	25
0xB2	61	D3	00	D5	41	D3
0xB4	1F	27	1A	1E	28	27

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-5. CX25874/875 Register Values for Autoconfiguration Modes 22–26 *(1 of 2)*

Autoconfiguration Mode #	22	23	24	25	26
Autoconfig Register (index 0xB8) Hexadecimal Value	26	27	30	31	32
Purpose of Mode	Desktop	Desktop	Boot-Up Screen	Boot-Up Screen	Desktop
Type of Digital Input	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	800x600	800x600	720x400	720x400	1024x768
Overscan Ratio	Lower	Standard	Standard	Standard	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.79	16.42	17.47	15.12	11.97
Vertical Overscan Ratio/ Percentage (VOC)	13.58	15.97	17.70	13.19	11.93
Overscan Percentages Delta (HOC - VOC)	0.21	0.45	–0.23	1.93	0.04
H_CLKI = HTOTAL	1176	950	1053	1305	1170
VLINES_I = VTOTAL	750	775	525	500	945
H_BLANKI = Horizontal Blanking Region	329	131	291	411	127
V_BLANKI = Vertical Blanking Region	94	109	76	64	115
Type of Video Output	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	52867138	36812508	33136345	32625000	66272724
Type of Clock	Pixel or Character	Pixel Only	Pixel or 9-Character only	Pixel or 9-Character only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	00	00	00	20
0x76	C0	34	3A	28	F8
0x78	20	20	D0	D0	00
0x7A	A6	AE	9C	9A	D0
0x7C	BA	CE	B0	B6	EA
0x7E	98	A0	88	80	E0
0x80	D9	2B	DD	E3	37
0x82	22	2D	27	29	21
0x84	D4	F4	CA	FC	D7
0x86	38	39	28	28	4A
0x88	00	00	00	00	00
0x8A	98	B6	1D	19	92

Table C-5. CX25874/875 Register Values for Autoconfiguration Modes 22–26 *(2 of 2)*

Autoconfiguration Mode #	22	23	24	25	26
0x8C	49	83	23	9B	7F
0x8E	0C	03	0C	0D	04
0x90	EE	07	0D	F4	B1
0x92	5E	6D	4C	40	73
0x94	58	58	90	90	00
0x96	3A	3B	36	35	3F
0x98	B7	AE	00	9A	9A
0x9A	5D	97	50	49	A9
0x9C	1B	72	2E	00	5D
0x9E	7F	5C	BA	80	74
0xA0	17	10	0E	0E	1D
0xA2	0A	24	0A	24	0A
0xA4	E5	F0	E5	F0	E5
0xA6	74	57	75	57	74
0xA8	BF	CB	78	80	77
0xAA	88	90	43	48	43
0xAC	9A	A4	85	8C	85
0xAE	00	01	95	97	2F
0xB0	00	04	81	1A	A1
0xB2	00	D5	A7	CA	BD
0xB4	1A	1E	1B	22	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-6. CX25874/875 Register Values for Autoconfiguration Modes 27–30 *(1 of 2)*

Autoconfiguration Mode #	27	28[5]	29[5]	30
Autoconfig Register (index 0xB8) Hexadecimal Value	33	34	35	36
Purpose of Mode	Desktop	DVD/CCIR601 Input, Slave Interface EN_XCLK bit = 1	DVD/CCIR601 Input, Slave Interface EN_XCLK bit = 1	Desktop
Type of Digital Input	RGB	YCrCb	YCrCb	YCrCb
Active Resolution	800 x 600	720x480	720x576	1024x768
Overscan Ratio	Lower	None (DVD Playback)	None (DVD Playback)	Lower
Horizontal Overscan Ratio/ Percentage (HOC)	13.78	0.00	0.00	11.97
Vertical Overscan Ratio/ Percentage (VOC)	13.58	0.00	0.00	11.93
Overscan Percentages Delta (HOC - VOC)	0.20	0.00	0.00	0.04
H_CLKI = HTOTAL	1176	858	864	1170
VLINES_I = VTOTAL	750	262	312	945
H_BLANKI = Horizontal Blanking Region	329	10	10	127
V_BLANKI = Vertical Blanking Region	94	19	22	115
Type of Video Output	PAL-60	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	52867138	27000000	27000000	66272724
Type of Clock	Pixel or Character	Pixel or Character	Pixel or Character	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	20	10	10	20
0x76	C0	B4	C0	F8
0x78	20	D0	D0	00
0x7A	A6	7E	7E	D0
0x7C	C6	90	98	EA
0x7E	94	58	54	E0
0x80	D9	03	15	37
0x82	22	14	17	21
0x84	D4	F0	20	D7
0x86	38	26	A6	4A
0x88	00	15	FA	00

Table C-6. CX25874/875 Register Values for Autoconfiguration Modes 27–30 *(2 of 2)*

Autoconfiguration Mode #	27	28[5]	29[5]	30
0x8A	98	5A	60	92
0x8C	49	0A	0A	7F
0x8E	0C	13	13	04
0x90	EE	06	38	B1
0x92	5E	13	16	73
0x94	58	F0	20	00
0x96	0A	31	35	3F
0x98	B7	00	00	9A
0x9A	5D	40	40	A9
0x9C	1B	00	00	5D
0x9E	7F	00	00	74
0xA0	17	8C	8C	1D
0xA2	20	0A	24	0A
0xA4	F0	E5	F0	E5
0xA6	57	76	59	74
0xA8	80	C1	CF	BD
0xAA	48	89	93	87
0xAC	8C	9A	A4	9A
0xAE	63	1F	CB	2F
0xB0	1C	7C	8A	A1
0xB2	34	F0	09	BD
0xB4	20	21	2A	14

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-7. CX25874/875 Register Values for Autoconfiguration Modes 31–36 *(1 of 2)*

Autoconfiguration Mode #	31	32	33	34	35	36
Autoconfig Register (index 0xB8) Hexadecimal Value	37	40	41	42	43	44
Purpose of Mode	DVD/ noninterlaced input	Desktop	Desktop	Desktop	Desktop	Desktop
Type of Digital Input	RGB	RGB	RGB	RGB	RGB	YCrCb
Active Resolution	720 x 576	640x480	640x480	800x600	800x600	640x480
Overscan Ratio	Very Low (DVD Playback)	Higher	Higher	Higher	Higher	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	–0.01	18.34	20.27	19.26	19.03	18.34
Vertical Overscan Ratio/ Percentage (VOC)	0.00	19.34	19.79	19.34	18.40	19.34
Overscan Percentages Delta (HOC - VOC)	–0.01	–1.00	0.48	–0.08	0.63	–1.00
H_CLKI = HTOTAL	886	770	950	1170	950	770
VLINES_I = VTOTAL	625	645	650	805	800	645
H_BLANKI = Horizontal Blanking Region	145	113	271	323	131	113
V_BLANKI = Vertical Blanking Region	42	100	104	125	122	100
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	27687503	29769241	30875015	56454552	37999992	29769241
Type of Clock	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	00	00	20	00	00
0x76	EC	64	B8	58	80	64
0x78	D0	80	80	20	20	80
0x7A	82	8C	92	B0	B2	8C
0x7C	9C	9E	AC	C8	D4	9E
0x7E	5A	6E	72	AC	AA	6E
0x80	2F	B5	F3	2D	57	B5
0x82	16	2A	33	2A	31	2A
0x84	22	C5	E9	C5	EC	C5

Table C-7. CX25874/875 Register Values for Autoconfiguration Modes 31–36 *(2 of 2)*

Autoconfiguration Mode #	31	32	33	34	35	36
0x86	A6	27	27	39	39	27
0x88	00	00	00	00	00	00
0x8A	76	02	B6	92	B6	02
0x8C	91	71	0F	43	83	71
0x8E	03	03	0B	0C	03	03
0x90	71	85	8A	25	20	85
0x92	2A	64	68	7D	7A	64
0x94	40	E0	E0	58	58	E0
0x96	0A	36	36	3B	3B	36
0x98	00	50	48	11	F6	50
0x9A	50	57	51	A1	98	57
0x9C	39	14	E4	46	8E	14
0x9E	4E	3B	B8	17	E3	3B
0xA0	0C	0D	0D	19	10	0D
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	59	75	58	74	57	75
0xA8	82	79	81	77	7F	C0
0xAA	49	44	48	43	48	89
0xAC	8C	85	8C	85	8C	9A
0xAE	57	F2	3D	21	E1	F2
0xB0	53	40	E7	0B	5B	40
0xB2	FE	C8	C2	59	DE	C8
0xB4	28	1E	24	18	1D	1E

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-8. CX25874/875 Register Values for Autoconfiguration Modes 37–42 *(1 of 2)*

Autoconfiguration Mode #	37	38	39	40	41	42
Autoconfig Register (index 0xB8) Hexadecimal Value	45	46	47	50	51	52
Purpose of Mode	Desktop	Desktop	Desktop	Desktop	Game	Desktop
Type of Digital Input	YCrCb	YCrCb	YCrCb	RGB	RGB	RGB
Active Resolution	640x480	800x600	800x600	800x600	320x200, Pix_Double Set	1024x768
Overscan Ratio	Higher	Higher	Higher	Standard	Standard	Higher
Horizontal Overscan Ratio/ Percentage (HOC)	20.27	19.26	19.03	15.59	21.86	18.04
Vertical Overscan Ratio/ Percentage (VOC)	19.79	19.34	18.40	15.64	30.90	18.11
Overscan Percentages Delta (HOC - VOC)	0.48	–0.08	0.63	–0.05	–9.04	–0.07
H_CLKI = HTOTAL	950	1170	950	1170	2000	1170
VLINES_I = VTOTAL	650	805	800	770	315	1015
H_BLANKI = Horizontal Blanking Region	271	323	131	323	453	127
V_BLANKI = Vertical Blanking Region	104	125	122	105	65	150
Type of Video Output	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC	PAL-BDGHI	NTSC
Frequency of CLK (Hz)	30875015	56454552	37999992	54000000	31500000	71181793
Type of Clock	Pixel Only	Pixel Only	Pixel Only	Pixel Only	Pixel or Character	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	00	20	00	20	40	20
0x76	B8	58	80	F0	E0	C8
0x78	80	20	20	20	80	00
0x7A	92	B0	B2	AA	94	E0
0x7C	AC	C8	D4	BE	B0	FC
0x7E	72	AC	AA	9E	78	FA
0x80	F3	2D	57	F3	09	AB
0x82	33	2A	31	25	42	28
0x84	E9	C5	EC	CE	CA	C8
0x86	27	39	39	38	27	4B

Table C-8. CX25874/875 Register Values for Autoconfiguration Modes 37–42 *(2 of 2)*

Autoconfiguration Mode #	37	38	39	40	41	42
0x88	00	00	00	00	00	00
0x8A	B6	92	B6	92	D0	92
0x8C	0F	43	83	43	C5	7F
0x8E	0B	0C	03	0C	1F	04
0x90	8A	25	20	02	3B	F7
0x92	68	7D	7A	69	41	96
0x94	E0	58	58	58	C8	00
0x96	36	3B	3B	3B	31	3F
0x98	48	11	F6	EF	21	DE
0x9A	51	A1	98	5E	80	AD
0x9C	E4	46	8E	00	00	E8
0x9E	B8	17	E3	00	00	A2
0xA0	0D	19	10	18	0E	1F
0xA2	24	0A	24	0A	24	0A
0xA4	F0	E5	F0	E5	F0	E5
0xA6	58	74	57	74	58	74
0xA8	CD	BE	CB	78	81	77
0xAA	92	87	90	43	48	43
0xAC	A4	9A	A4	85	8C	85
0xAE	3D	21	E1	17	D3	C2
0xB0	E7	0B	5B	5D	2D	72
0xB2	C2	59	DE	74	08	4F
0xB4	24	18	1D	19	24	13

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

Table C-9. CX25874/875 Register Values for Autoconfiguration Modes 43–47 *(1 of 2)*

Autoconfiguration Mode #	43	44[1]	45	46	47
Autoconfig Register (index 0xB8) Hexadecimal Value	53	54	55	56	57
Purpose of Mode	Desktop	DVD/ noninterlaced input	Game	Desktop for Brazil	Desktop for Argentina
Type of Digital Input	RGB	RGB	RGB	RGB	RGB
Active Resolution	1024x768	720x480	320x200, Pixel_Double Set	640x480	640x480
Overscan Ratio	Higher	Very Low (DVD Playback)	Standard	Standard	Standard
Horizontal Overscan Ratio/ Percentage (HOC)	16.20	1.24	20.20	13.79	16.56
Vertical Overscan Ratio/ Percentage (VOC)	16.67	1.23	21.40	13.58	16.67
Overscan Percentages Delta (HOC - VOC)	–0.47	0.01	–1.20	0.21	–0.11
H_CLKI = HTOTAL	1410	880	1848	784	944
VLINES_I = VTOTAL	1000	525	275	600	625
H_BLANKI = Horizontal Blanking Region	337	140	429	126	266
V_BLANKI = Vertical Blanking Region	147	36	43	75	90
Type of Video Output	PAL-BDGHI	NTSC	NTSC	PAL-M (Brazil)	PAL-Nc (Argentina)
Frequency of CLK (Hz)	70499989	27692310	30461552	28195793	29500008
Type of Clock	Pixel Only	Pixel or Character	Pixel or Character	Pixel Only	Pixel Only
Register Address	**Register Value**	**Register Value**	**Register Value**	**Register Value**	**Register Value**
0x38	24	00	40	00	00
0x76	C0	E0	90	00	60
0x78	00	D0	80	80	80
0x7A	DC	82	90	84	8A
0x7C	08	92	A2	A4	A6
0x7E	F0	5C	72	6A	70
0x80	BF	1B	CD	7D	C1
0x82	2F	13	2B	22	2E
0x84	F1	F2	C2	D4	F2
0x86	4B	26	27	27	27

Table C-9. CX25874/875 Register Values for Autoconfiguration Modes 43–47 *(2 of 2)*

Autoconfiguration Mode #	43	44[1]	45	46	47
0x88	00	00	00	00	00
0x8A	82	70	38	10	B0
0x8C	51	8C	AD	7E	0A
0x8E	0D	03	1F	03	0B
0x90	E8	0D	13	58	71
0x92	93	24	2B	4B	5A
0x94	00	E0	C8	E0	E0
0x96	3F	36	31	36	36
0x98	33	00	C3	92	00
0x9A	A3	50	40	54	50
0x9C	55	C5	D9	0E	72
0x9E	55	4E	89	88	1C
0xA0	1F	0C	0D	0C	0D
0xA2	24	0A	0A	2A	24
0xA4	F0	E5	E5	F0	F0
0xA6	56	76	75	57	57
0xA8	7E	79	78	80	80
0xAA	47	44	44	48	48
0xAC	8C	85	85	8C	8C
0xAE	9B	D1	33	6E	1E
0xB0	29	45	28	DB	C0
0xB2	26	17	15	76	15
0xB4	18	21	1E	20	1F

GENERAL NOTE:

1. RGB digital input denotes that the CX25874/875 will be configured to receive the RGB default pixel input mode after an autoconfiguration command which is 24-bit, RGB-multiplexed (i.e., IN_MODE[3:0] = 0000). If the desired RGB pixel input mode is NOT 24-bit RGB-multiplexed, the CX25874/875's IN_MODE[3:0] bits must be programmed to the desired RGB pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
2. YCrCb digital input denotes that the CX25874/875 will be configured to receive YCrCb pixel data after an autoconfiguration command. The CX25874/875's IN_MODE[3:0] bits must be programmed to the desired YCrCb pixel input mode immediately before initiating a write to the CONFIG[5:0] bits.
3. CX25874/875 registers not listed in this table (including IN_MODE[3:0]) do not get reprogrammed as a result of an autoconfiguration command.
4. Character or Pixel signifies that this overscan ratio is acceptable for 8-clock per character graphics controllers or pixel-clock controllers.
5. The CX25874/5 will be the clock master immediately after any autoconfiguration mode EXCEPT modes 28 and 29, which will set the device to clock slave (EN_XCLK = 1). Modes 31 and 44 will force pseudo-master interface.
6. These autoconfiguration values assume a 13.500 MHz crystal resides between the XTALIN and XTALOUT pins.

FOOTNOTE:

(1) Mode 44 would ideally have 858 clocks per line. However, since 858 is not a multiple of 8, then 880 clocks per line was utilized instead.

D

Closed Caption Pseudo Code Appendix

```
/* Filename: CC_87x_Function.C */

//Causes CX2587x encoder to encode 2 bytes of data on every Odd
Field=Field 1

#include stdio.h

#include conio.h

<#include other necessary header files>


char   CCdatabyte1, CCdatabyte2;// Define global variables


//Any graphics controller/MPEG2 Decoder is assumed to be the I2C
master for this design

//Controller/Data Master sends the CX2587x the digital CC bytes
necessary for encoding into the Composite Video signal or Luma
signal for S-Video output

//H_CLKO[11:0] value should exist in hex format. This register
equals bits3-0 of register 0x86 and bits 7-0 of register 0x76


87x_CCEncoding_onField1(int CCdatabyte1, int CCdatabyte2, int
H_CLKO)

{

int CBITS, CC_PIPE1, CC_ADD_HEX, CCR_START_HEX, CCSEL, ReadBit;

int ReadBitArray[8] = {0};//initializes all element of ReadBitArray
to 0

float CC_ADD;

float CCR_START;


CBITS = 17;

CC_PIPE1=60;

CCSEL = 4;//CCSEL[3:0] = 0100 so CC data is encoded on line 21

    //for 525-line systems and line 23 for 625-line systems


//Initialization Section

Write ECCGATE to 1;   //this is bit 3 of register C4 for the CX2587x

//no further closed caption encoding will be performed

//until CCF1B1 & CCF1B2 registers are again written;
```

```
//null will be transmitted on appropriate CC line in this case
Write ECCF1 to 1;//this is bit 4 of register C4 for the CX2587x
//Enables CC encoding on Field 1
Write ECCF2 to 0;//this is bit 5 of register C4 for the CX2587x
//Disables CC encoding for Field 2

if (625LINE == 0)  //"625LINE" = bit 2 of register 0xA2

      {// 525-line format=NTSC is being transmitted
      //by CX2587x. This assumes PAL-M = another 525 line format is
      not allowed

[equation] CC_ADD  = ($pow(2, CBITS+5)/1716)*1716.0/H_CLKO;
//equation to determine CC_ADD register for NTSC
CC_ADD_hex = DEC_TO_HEX_CONVERSION(float CC_ADD);
//assumes DEC_TO_HEX_CONVERSION fxn this should already exist
somewhere in customer's code

Write CC_ADD(CC_ADD_hex);//CC_ADD[11:0] register is
//comprised of bits[3:0] of
//register 0xD4 and bits[7:0] of
//CX2587x register 0xD2

[equation] CCR_START = H_CLKO*10.003*27/1716 + CC_PIPE1;
//eqn to determine CCR_START register for NTSC
                CCR_START_hex = DEC_TO_HEX_CONVERSION(float
CCR_START);
   //assumes DEC_TO_HEX_CONVERSION fxn this should already exist
   somewhere in customer's code

Write CCR_START(CCR_START_hex);
      //CCR_START[8:0] register is
      //comprised of bit[4] of register
      //0xD4 and bits[7:0] of CX2587x
      //register 0xD0
}
else
{
// 625-line format = PAL is being transmitted by CX2587x
//this assumes PAL-M with its' 525 line format is not allowed
```

```
[equation] CC_ADD  = ($pow(2, CBITS+5)/1716)*1728.0/H_CLKO;
      //eqn to determine CC_ADD register for PAL

CC_ADD_hex = DEC_TO_HEX_CONVERSION(float CC_ADD);
      //assumes DEC_TO_HEX_CONVERSION fxn this should already
      exist somewhere in customer's code
Write CC_ADD(CC_ADD_hex);//CC_ADD[11:0] register is
      //comprised of bits[3:0] of
      //register 0xD4 and bits[7:0] of //CX2587x register 0xD2

[equation] CCR_START = H_CLKO*10.003*27/1728  + CC_PIPE1;
      //eqn to determine CCR_START register for PAL
CCR_START_hex = DEC_TO_HEX_CONVERSION(float CCR_START);
      //assumes DEC_TO_HEX_CONVERSION fxn already exists somewhere
      in customer's code

Write CCR_START(CCR_START_hex);
      //CCR_START[8:0] register is
      //comprised of bit[4] of register
      //0xD4 and bits[7:0] of CX2587x
      //register 0xD0
}

//Previous Initialization Code only needs to be performed once by
I2C compatible master

//Closed Caption Encoding Operation
ReadBitArray[] = CX875ReadbackFxn(ESTATUS = 01);
//CCSTAT_O will be ReadBitArray[3] after this function executes
Or
ReadBit = ReadCCSTAT_O();
      //CX2587x has full readback ability of all bits.
      //No longer is it necessary to use legacy Bt869 method of
      reading //back status bits

if (ReadBitArray[3] == 0)
      //alternative IF statement could be 'if (ReadBit == 0)'
{
      //Closed Caption bytes for Field 1 = Odd Field have already
      been //encoded and CCSTAT_O has been cleared
Write CCF1B1(CCdatabyte1);//assumes CCdatabyte1 is in hex format //
already. Encode new CC data.
```

```
Write CCF1B2(Ccdatabyte2);//assumes CCdatabyte2 is in hex format //
already.  Encode new CC data.

      //data is not latched until second of the 2 byte data
      sequence is written

      //this prevents writing of partial data sequence

      //for this reason, data must be written in order of Byte 1
      and then Byte 2


      //CCSTAT_O will be automatically be set by the CX2587x until
      CC bytes for odd

      //field = Field 1 have been encoded

}

else

//CCSTAT_O = 1 because CC data has already been written for Field
1=ODD field & has not yet been encoded onto analog video output
signal for the odd field

//CCSTAT_O will be reset immediately after the clock run-in online
284 for NTSC //and line 335 for PAL

return 0;//CCSTAT_0 = 1 so CC bytes were not encoded on this pass
through the 87x_CCEncoding_onField1 procedure


return 0;

}

//*************************************************

Bt869ReadbackFxn(int ESTATUS)

//Unlike the Bt868/869 Conexant VGA encoder, the CX2587x series
does have //registers than can be directly read-back. As a result,
this //Bt869ReadbackFxn should only be used IF the software
engineer seeks to use //the legacy method of readback found in the
Bt868/869.

{

int ReadMONSTAT_CCArray[8] = {0};  //entire array now holds 0


Write ESTATUS; //ESTATUS[1:0]= {bits 7(MSb) and 6 of register 0xC4}
ESTATUS[1:0]= 01 from function call.

      //00 and 10 possible for ESTATUS as well

      //yielding different readback information


Graphics controller issues 0x89 or 0x8B for the CX2587x's device
address;

//no subaddress required here since the CX2587x

//only has 1 read register to check with the legacy method

//This step has the effect of reading a single byte //of data from
the CX2587x
```

```
        //Table 2-2 Readback bit map says that MONSTAT_A,B,C bits =
        bits 7-5
        //while Bit 4 = CCSTAT_E, bit 3 = CCSTAT_O,
        // bits 2-0 = FIELD[2:0]
// This ensures the least significant bit of the device write
portion of the transaction is '1' which indicates to the encoder
that it must send a byte of data on the serial transaction. Do not
write a subaddress to the CX2587x(this is not necessary since the
CX2587x only appears to have 1 read register with the legacy
method) and then read the "next" byte after the ACK.

Controller_Transmits_I2C_STOP; //Serial Master must issue a STOP
command to
        //finish the Read transaction.  An ACK is not necessary
        before closing the transaction because the CX2587x just
        ignores the ACK anyway
return(ReadMONSTAT_CCArray[]);
}
```

E

HDTV Output Mode Appendix

NOTE: Conexant is pursuing multiple patents surrounding this function.

E.1 Introduction

A HDTV system can display images that are better than existing standard-definition TV formats such as NTSC, PAL, and SECAM. HDTV pictures are more true-to-life because the resolution of the TV image is much higher, and the colors are more accurate.

Many HDTVs are being equipped with a HD Input port that accepts analog Component YP_BP_R or analog RGB or both.

Recognizing this fact, Conexant has included an HDTV Output Mode within the CX25874/5 which generates the analog Component YP_BP_R or analog RGB outputs necessary for driving an HDTV's HD Input port(s).

While in HDTV mode, the device will output either analog RGB or analog YP_BP_R signals and automatically insert trilevel synchronization pulses (when necessary) and vertical synchronizing broad pulses. The output waveforms and requirements related to the input timing and data on the input side of the CX25874/5 are explained in this section and in the listed SMPTE standards governing the HDTV resolutions.

E.2 Allowable Interfaces for HDTV Output Mode

The interface that the CX25874/5 must use in HD Output Mode is either type of video timing slave interface. In this configuration, the HSYNC* and VSYNC* signals must be received as inputs while the BLANK* signal's usage is optional. The encoder cannot transmit the timing signals that initiate the start of a line or the start of a frame in this mode at all. The CX25874/5 can provide a reference clock output—CLKO, or not transmit it, as needed. The EN_OUT bit will control whether or not a CLKO signal is active.

The BLANK* signal will not be required for the HDTV Output Mode interface if the graphics controller outputs the digital codes for the analog blanking level. For analog RGB component video outputs, the digital code for blanking is 00 hex for digital R, G, and B. For offset analog RGB component video outputs, the digital code for blanking is 10 hex for the digital R, G, and B pixel inputs. Finally, for analog Component YP_BP_R video outputs, the digital code for blanking is 10 hex for digital Y and 80 hex for digital Pr and Pb.

If the graphics controller does not possess the ability to output specific digital codes, then a BLANK* signal is a necessary part of this interface.

The allowable interfaces for HDTV Output Mode are illustrated in Figures E-1 and E-2.

Figure E-1. CX25874/875's Pseudo-Master Interface with a Graphics Controller as the Timing Master

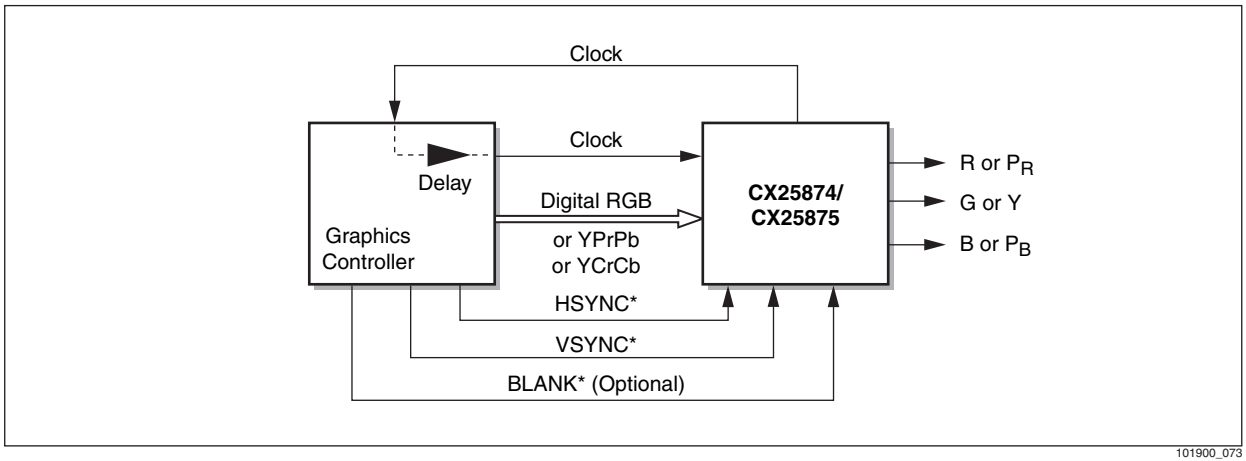
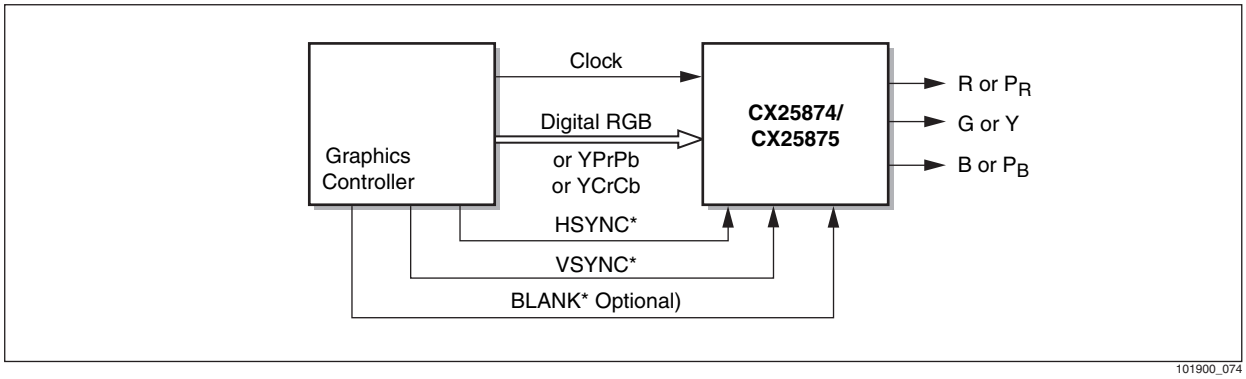


Figure E-2. CX25874/875's Slave Interface with a Graphics Controller as the Timing Master



E.2.1 Interface Bit Functionality in HDTV Output Mode

When the CX25874/5 is transmitting High-Definition Outputs, several interface bits behave differently than their operation while broadcasting standard-definition television. These bits and their technical functionality are summarized in the following list:

- The BLANK* pin must be an input regardless of the slave or pseudo-master interface. If the blank function is not enabled with the BLANK* pin, then the BLANK* pin (#21) should be tied high permanently.
- The EN_BLANKO bit has no effect because the BLANK* signal MUST be an input. The same rule holds for VGA(R/G/B) – DAC Output operation.
- The EN_DOT bit has no effect. This bit is related to the standard flicker filter.
- The FLD_MODE[1:0] bit field has no effect. For 1080i or any other HD-related interlaced input, VSYNC*'s leading edge must be received within ±5 clock cycles of the middle of the total line length. For 1080i, this means the VSYNC* leading edge must be received on any clock period between the (2200 / 2) ± 5 clocks = 1095th and 1106th clock pulse.
- The polarity reversing bits (HSYNCI, VSYNCI, and BLANKI) perform the same operations as they do with standard-definition outputs.

E.3 Interface Timing Between the HDTV Source Device (Master) and CX25874/CX25875 (Timing Slave)

While in HDTV Output Mode, the CX25874/5 encoder should receive interface signals from the MPEG2 decoder or display processor. The interface signals that should be shared between the two devices are the HSYNC*, VSYNC*, BLANK*, CLKI, and Pixel Data lines (P[11:0]). The BLANK* signal is optional. This signal is only necessary if the data master cannot transmit the digital codes representing the BLANK levels to the CX25874/5. To reiterate, the codes for the digital blanking levels of the R, G, B inputs are equal to 00 hex. The digital codes for blanking change to 10 hex for the R, G, and B pixel inputs if conversion to offset analog RGB component video outputs is desired. Finally, the values for digital Y must be 10 hex and for Pr and Pb, digital samples have to equal 80 hex for the BLANK period for Component Video Out (YPBPR). CLKO will only be necessary if Pseudo-Master is used as the chosen interface.

To switch the CX25874/5 encoder into HDTV Output mode, the serial master must program both the OUT_MODE[1:0] bits to 11(DAC Mode) and set the HDTV_EN bit to 1 (bit 7 of the HDTV Register). Immediately after these bits have been set and writes to all other registers listed in Table E-1 or Table E-2 (choose the correct Table and column based on the input format and ATSC resolution), the encoder will be set up to properly generate a set of HDTV Outputs.

The process of enabling HDTV is not complete however. The final step required to generate the desired HDTV resolution is to configure the master device to transmit the progressive or interlaced timing (HSYNC* and VSYNC*), clock (CLKI), and data signals ([P11-P0]) required by the encoder and in accordance with the video parameters listed in Table E-1 or Table E-2. The signals received by the encoder should match the timing diagrams found at the back of this Appendix.

Table E-1. Video Parameters for 480p, 576p, 720p Progressive HDTV Output Formats

Purpose of Mode	HDTV 480p	HDTV 483p: (Japan 525p) 60 Hz Progressive	HDTV 576p: 625p 60 Hz Progressive	HDTV 720p
Type of Digital Input	RGB	RGB	RGB	RGB
Active Resolution	720x480	720x483	720x576	1280x720
Overscan Ratio	None	None	None	None
Horizontal Overscan Ratio/Percentage (HOC)	0.00	0.00	0.00	0.00
Vertical Overscan Ration Percentage (VOC)	0.00	0.00	0.00	0.00
Overscan Percentages Delta (HOC-VOC)	0.00	0.00	0.00	0.00
H_CLKI = HTOTAL	858	858	864	1650
VLINES_I = VTOTAL	525	525	625	750
H_BLANKI = Horizontal Blanking Region	122	122	132	260
V_BLANKI = Vertical Blanking Region	36	36	45	25
Type of Digital Input	Noninterlaced	Noninterlaced	Noninterlaced	Noninterlaced
Frequency of CLK (Hz)	27000000	27000000	27000000	74250000
Type of Video Output	HDTV Y PR PB	HDTV Y PR PB	HDTV Y PR PB	HDTV Y PR PB
TV Out Screen Size	Full Screen	Full Screen	Full Screen	Full Screen
Type of Clock	Pixel Only	Pixel Only	Pixel Only	Pixel Only
Source of Mode	North American/ non-Japan consumer HDTV	HDTV 480p but GPU Master issues 3 more active lines	ITU_R.BT.1358 Euro HDTV	North American/ non-Japan consumer HDTV

Table E-2. Video Parameters for 1035i, 1080i Interlaced HDTV Output Formats

Purpose of Mode	Japan HDTV 1035i	HDTV 1080i
Type of Digital Input	RGB	RGB
Active Resolution	1920x1035i	1920x1080i
Overscan Ratio	None	None
Horizontal Overscan Ratio/Percentage (HOC)	0.00	0.00
Vertical Overscan Ration Percentage (VOC)	0.00	0.00
Overscan Percentages Delta (HOC-VOC)	0.00	0.00
H_CLKI = HTOTAL	22.00	22.00
VLINES_I = VTOTAL	1125i	1125i
H_BLANKI = Horizontal Blanking Region	consult specification	192
V_BLANKI = Vertical Blanking Region	consult specification	20 (field 1) 20.5 (field 2)
Type of Digital Input	Noninterlaced	Noninterlaced
Frequency of CLK (Hz)	74250000	74250000
Type of Video Output	HDTV Y PR PB	HDTV Y PR PB
TV Out Screen Size	Full Screen	Full Screen
Type of Clock	Pixel Only	Pixel Only
Source of Mode	1080i but GPU Master issues 45 fewer active lines	North American/non-Japan consumer HDTV

Table E-3. CX25874/5 Register Settings for Alternate 24-bit RGB Multiplexed In—HDTV YP_BP_R Out and HDTV RGB Out *(1 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i / 1035i	720p	625p	480p	
	CX25874/5 Register Values				
0xD6	0C	0C	0C	0C	OUT_MODE [1:0] field set to 11=DAC Mode to turn on HDTV outputs. Video[0-3] is HDTV Output Mode. HDTV_EN bit must be set as well. Video[0] = HD R or PR, Video[1] = HD G or Y, Video[2] = HD B or PB
0x2E	C3	C2	C5	C5	HDTV_EN set. RGB2YPRPB set. RASTER_SEL[1:0] field adjusted for each ATSC resolution. HD_SYNC_EDGE set for 480p and 625p resolutions only. For RGB out, RGB2YPRPB bit must be 0 so this register will be 83 / 82 / or 85. For EIA770.3 compliance, disable the trilevel sync on both the P_R and P_B outputs by setting the RPR_SYNC_DIS (bit 5) and BPB_SYNC_DIS (bit 3) bits. Program this register to 0xED for this case.
0x32	01	01	00	00	CSC_SEL bit set for hi-frequency ATSC resolutions only.
0x3C	80	80	80	80	MCOMPY stays the same for 480p/720p/1080i in, Y/PR/PB out. or RGB out.
0x3E	45	45	48	48	MCOMPU must be changed for 480p and 720p/1080i in, Y/PR/PB out. MCOMPU must be changed to 80hex for 480p/720p/1080i in, RGB out.
0x40	51	51	5B	5B	MCOMPV must be changed for 480p and 720p/1080i in, Y/PR/PB out. MCOMPV must be changed to 80hex for 480p/720p/1080i in, RGB out.
0xC4	01	01	01	01	State of EN_OUT varies according to interface used with master device. Hex value of 01 for this register corresponds to Pseudo-Master without a BLANK* interface.
0xC6	80	80	80	80	State of EN_BLANKO and EN_DOT varies according to interface used with master device. Hex value of 80 for this register corresponds to Pseudo-Master without a BLANK* interface. IN_MODE[2:0] = 000 - defines input format as 24-bit RGB multiplexed.
0xCE	24	24	24	24	Adjust this register as necessary to route Y/PR/PB out from the CX25874/5's 4 DACs OUT_MUXD[1:0]= 00 =Video[0] = PR = R {Disabled from DACDISD=1} OUT_MUXC[1:0]= 10 =Video[2] = PB = B OUT_MUXB[1:0]= 01 =Video[1] = Y = G OUT_MUXA[1:0]= 00 =Video[0] = PR = R
0xA0	21	21*	0C	0C	PLL_INT[5:0] = 21 for 720p @ 74.25 MHz *PLL_INT[5:0] = 20 for 720p @ 74.16 MHz For slave interface, set the MSb of this register (EN_XCLK) to 1.

Table E-3. CX25874/5 Register Settings for Alternate 24-bit RGB Multiplexed In—HDTV YP_BP_R Out and HDTV RGB Out *(2 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i / 1035i	720p	625p	480p	
	CX25874/5 Register Values				
0x9E	00	00**	00	00	PLL_FRACT[15:8] = 00 for 720p @ 74.25 MHz **PLL_FRACT[15:8] = F5 for 720p @ 74.16 MHz
0x9C	00	00**	00	00	PLL_FRACT[7:0] = 00 for 720p @ 74.25 MHz **PLL_FRACT[7:0] = C3 for 720p @ 74.16 MHz
0xA2	xx	xx	04	00	xx = Don't Care For 625p, the 625LINE bit must = 1 For 480p, the 625LINE bit must = 0
0xBA	28	28	28	28	SLAVE set. Interface is slave timing (pseudo-master or slave) HSYNC*/VSYNC* sent to CX25874/5. DACD disabled. PR/Y/PB transmitted from DACA/DACB/DACC
WAIT state = 75 ms.	Yes	Yes	Yes	Yes	Ready encoder for timing reset operation. 75 ms = many factors of safety.
0x6C	C6	C6	C6	C6	Set TIMING_RESET bit. Cleared automatically.

GENERAL NOTE:

1. (*) = If graphics controller is character based with 8 pixel clocks/character, PLL_INT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
2. (**) = If graphics controller is character based with 8 pixel clocks/character, PLL_FRACT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
3. The primacy difference between 625p and 480p HDTV modes is in register 0xA2. For 625p, the 625LINE bit = 1, and for 480p, the 625LINE bit = 0.

The difference between 1080i and 1035i is that the 1035i has these additional blank lines: 21–40, 558–560, 584–602, 1121–1123.

Table E-4. CX25874/5 Register Settings for 24-bit YPrPb (or YCrCb) Multiplexed In—HDTV YP_BP_R Out *(1 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i 1035i	720p	625p	480p	
	CX25874/5 Register Values				
0xD6	0C	0C	0C	0C	OUT_MODE [1:0] field set to 11=DAC Mode to turn on HDTV Outputs. Video[0-3] is HDTV Output Mode. HDTV_EN bit must be set as well. Video[0] = HD PR, Video[1] = HD Y, Video[2] = HD PB
0x2E	AB***	AA***	AD***	AD***	HDTV_EN set. RGB2YPRPB off. RASTER_SEL[1:0] field adjusted for each ATSC resolution. HD_SYNC_EDGE set for 480p and 625p resolutions only. For EIA770.3 compliance, the trilevel sync has been disabled on both the PR and PB outputs by setting the RPR_SYNC_DIS (bit 5) and BPB_SYNC_DIS (bit 3) bits. Program this register to 0xED for this case.
0x32	08	08	08	08	IN_MODE[3] = 1 = input format is Alternate 24-bit YPrPb multiplexed. YCrCb digital input formats can also be supported with a register manipulation. Contact Conexant for more details.
0x3C	80	80	80	80	MCOMPY stays the same for 480p/720p/1080i in, Y/PR/PB out.
0x3E	80	80	80	80	MCOMPU stays the same for 480p/720p/1080i in, Y/PR/PB out.
0x40	80	80	80	80	MCOMPV stays the same for 480p/720p/1080i in, Y/PR/PB out.
0xC4	01	01	01	01	State of EN_OUT varies according to interface used with master device. Hex value of 01 for this register corresponds to Pseudo-Master without a BLANK* interface.
0xC6	84	84	84	84	State of EN_BLANKO and EN_DOT varies according to interface used with master device. Hex value of 80 for this register corresponds to Pseudo-Master without a BLANK* interface. IN_MODE[2:0] = [1]100 - input format is Alternate 24bit YP_RP_B multiplexed
0xCE	24	24	24	24	Adjust this register as necessary to route Y PR PB out from the CX25874/5's 4 DACs OUT_MUXD[1:0]= 00 =Video[0] = PR {Disabled from DACDISD=1} OUT_MUXC[1:0]= 10 =Video[2] = PB OUT_MUXB[1:0]= 01 =Video[1] = Y OUT_MUXA[1:0]= 00 =Video[0] = PR
0xA0	21	21*	8C	8C	PLL_INT[5:0] = 21 for 720p @ 74.25 MHz *PLL_INT[5:0] = 20 for 720p @ 74.16 MHz
0x9E	00	00**	00	00	PLL_FRACT[15:8] = 00 for 720p @ 74.25 MHz **PLL_FRACT[15:8] = F5 for 720p @ 74.16 MHz
0x9C	00	00**	00	00	PLL_FRACT[7:0] = 00 for 720p @ 74.25 MHz **PLL_FRACT[7:0] = C3 for 720p @ 74.16 MHz

Table E-4. CX25874/5 Register Settings for 24-bit YPrPb (or YCrCb) Multiplexed In—HDTV YP_BP_R Out *(2 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i / 1035i	720p	625p	480p	
	CX25874/5 Register Values				
0xA2	xx	xx	04	00	xx = Don't Care For 625p, the 625LINE bit must = 1 For 480p, the 625LINE bit must = 0
0xBA	28	28	28	28	SLAVE set. Interface is slave timing (pseudo-master or slave) HSYNC* and VSYNC* sent to CX25874/5. DACD disabled. PR transmitted from DACA, Y transmitted from DACB, and PB transmitted from DACC
WAIT state = 75 ms	Yes	Yes	Yes	Yes	Ready encoder for timing reset operation. 75 ms = many factors of safety.
0x6C	C6	C6	C6	C6	Set TIMING_RESET bit. Cleared automatically.

GENERAL NOTE:

1. (*) = If graphics controller is character based with 8 pixel clocks/character, PLL_INT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
2. (**) = If graphics controller is character based with 8 pixel clocks/character, PLL_FRACT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
3. (***) = Conversion from YPrPb and YCrCb digital input to HDTV RGB Out not possible with CX25874/5.

The difference between 1080i and 1035i is that the 1035i has these additional blank lines: 21–40, 558–560, 584–602, 1121–1123.

In the default format, the HSYNC* signal is active low and must always be received as an input in HDTV Output Mode. Its function is to allow the graphics controller to tell the encoder when the start of a line occurs. Check the timing diagrams that appear later in this section for proper HSYNC* timing.

In the default format, the VSYNC* signal is active low and must always be received as an input in HDTV Output Mode. Its function is to allow the graphics controller to tell the encoder when the start of a frame occurs. Check the timing diagrams that appear later in this section for proper VSYNC* timing.

By default, the clock output signal will be transmitted via the CLKO port. Therefore, the CX25874/5 will be in Pseudo-Master interface. To switch into Slave interface, the user must reset the EN_OUT bit to turn off CLKO.

Table E-5 summarizes the default pseudo-master HDTV interface.

Table E-5. Default State of CX25874/5 Immediately After Switch into HDTV Output Mode

Input Signals			CLKO	State of the CX25874/5
BLANK*	HSYNC*	VSYNC*		State of Encoder in HDTV Output Mode
Optional	H	H	Active	Digital RGB—Analog HD RGB or Digital YPrPb—Analog HD YP_BP_R DAC Conversion
Optional	L	H	Active	Start of a New Line
Optional	L	L	Active	Start of a New Frame

The timing diagrams found at the end of this Appendix (Figures E-5 through E-9) must be replicated with actual timing by the MPEG2 Decoder or Display Processor for the encoder to provide correct HDTV analog RGB or analog YP_BP_R component video outputs.

E.4 Syncless HDTV Interface Using Digital Timing Codes

A very unique attribute of the CX25874/5 is that this device's encoder core, like the CX25891/2 combination DVI encoder, can be configured to use the SAV (Start of Active Video) and EAV (End of Active Video) CCIR656-compatible timing reference codes embedded in the pixel stream to determine the beginning and end of lines and frames. As a result, the control signals HSYNC*, VSYNC*, and BLANK* are not needed with this high-definition interface, and these pins are ignored during this type of operation because these timing events are contained in the timing reference codes. All other aspects of the timing interface continue to operate in accordance with the aforementioned SMPTE standards 274M, 293M, and 296M. The SAV and EAV codes replacing the HSYNC* and VSYNC* edge transitions and signals are the only differences here.

The designer should realize that to operate the syncless HDTV interface properly, the digital timing codes must be embedded in each of the digital color signals, i.e., in each of R,G, and B or Y, Pr, and Pb. This is necessary for proper operation in CX25874/5. For more guidelines and the recommended sequence of registers and values to write to the device, choose your desired HDTV format, and program the encoder register bank as listed in Table E-4. After the master device begins sending correct syncless code-based timing along with the correct pixel clock frequency and associated data signals (back of this section) and after the steps from Table E-4 are completed for the chosen HDTV mode, the CX25874/5 will generate proper Y PR PB HDTV Outputs.

Table E-6. CX25874/5 Register Settings for Syncless 24-Bit YPrPb (or YCrCb) Multiplexed In—HDTV YP_BP_R Out *(1 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i / 1035i	720p	625p (576p)	480p	
	CX25874/5 Register Values				
0xD6	4C	4C			E656 bit = 1. Encoder in syncless interface. OUT_MODE [1:0] field set to 11=DAC Mode to turn on HDTV Outputs. Video[0-3] is HDTV Output Mode. HDTV_EN bit must be set as well. Video[0] = HD PR, Video[1] = HD Y, Video[2] = HD PB
0x26	00*	00*			If YCrCb digital data is driven into CX25891/2 instead of YPrPb data, then program this register to 80 hex. This sets YC2YP bit.
0x2E	AB***	AA***			HDTV_EN set. RGB2YPRPB off. RASTER_SEL[1:0] field adjusted for each ATSC resolution. HD_SYNC_EDGE set for 480p and 625p resolutions only. The trilevel sync has been disabled on both the PR and PB outputs by setting the RPR_SYNC_DIS (bit 5) and BPB_SYNC_DIS (bit 3) bits. Trilevel sync only appears on Y output.
0x32	08	08			IN_MODE[3] = 1 = input format is Alternate 24-bit YPrPb multiplexed. YCrCb digital input formats can also be supported with a register manipulation. Review definition for IN_MODE bit field.
0x3C	80	80			MCOMPY stays the same for 480p/720p/1080i in, Y/PR/PB out.
0x3E	80	80			MCOMPU stays the same for 480p/720p/1080i in, Y/PR/PB out.
0x40	80	80			MCOMPV stays the same for 480p/720p/1080i in, Y/PR/PB out.
0xC4	01	01			State of EN_OUT varies according to interface used with master device. Hex value of 01 for this register corresponds to Pseudo-Master without a BLANK* interface.
0xC6	84	84			State of EN_BLANKO and EN_DOT varies according to interface used with master device. Hex value of 80 for this register corresponds to Pseudo-Master without a BLANK* interface. IN_MODE[2:0] = [1]100 - input format is Alternate 24-bit YP_RP_B multiplexed. Review definition for IN_MODE bit field.
0xCE	64	64			Adjust this register as necessary to route Y PR PB out from the CX25891/2's 4 DACs OUT_MUXD[1:0]= 01 =Video[0] = Y {Disabled from DACDISD=1} OUT_MUXC[1:0]= 10 =Video[2] = PB OUT_MUXB[1:0]= 01 =Video[1] = Y OUT_MUXA[1:0]= 00 =Video[0] = PR
0xA0	A1	A1*			EN_XCLK bit = 1 indicating encoder in pure slave interface. PLL_INT[5:0] = 21 for 720p @ 74.25 MHz *PLL_INT[5:0] = 20 for 720p @ 74.16 MHz
0x9E	00	00**			PLL_FRACT[15:8] = 00 for 720p @ 74.25 MHz **PLL_FRACT[15:8] = F5 for 720p @ 74.16 MHz

Table E-6. CX25874/5 Register Settings for Syncless 24-Bit YPrPb (or YCrCb) Multiplexed In—HDTV YP_BP_R Out *(2 of 2)*

CX25874/5 Register Address	ATSC Resolution				Explanation/Comments
	1080i / 1035i	720p	625p (576p)	480p	
	CX25874/5 Register Values				
0x9C	00	00**			PLL_FRACT[7:0] = 00 for 720p @ 74.25 MHz **PLL_FRACT[7:0] = C3 for 720p @ 74.16 MHz
0xA2	02	02			SETUP bit = 1. For 625p, the 625LINE bit must = 1 For 480p, the 625LINE bit must = 0
0xBA	28	28			SLAVE bit set. Interface is slave timing (pseudo-master or slave) HSYNC and VSYNC events sent to CX25874/5 as EAV and SAV codes. DACD disabled. PR transmitted from DACA, Y transmitted from DACB, and PB transmitted from DACC. DACD could be re-enabled as a second Luma (Y) output.
WAIT state = 75 ms	Yes	Yes			Ready encoder for timing reset operation. 75 ms = many factors of safety.
0x6C	C6	C6			Set TIMING_RESET bit. Cleared automatically.

GENERAL NOTE:

1. (*) = If graphics controller is character based with 8 pixel clocks/character, PLL_INT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
2. (**) = If graphics controller is character based with 8 pixel clocks/character, PLL_FRACT should be modified to generate a 74.16000 MHz CLKO and CLKI frequency.
3. (***) = Conversion from YPrPb and YCrCb digital input to HDTV RGB Out not possible with CX25874/5.
4. The difference between 1080i and 1035i is that the 1035i has these additional blank lines: 21–40, 558–560, 584–602, 1121–1123.

E.5 Automatic Trilevel Sync Generation

The CX25874/5 will automatically generate an analog synchronization pulse with three distinct voltage levels for every leading edge it receives at its HSYNC* input (so long as RASTER_SEL[1:0] = 10 or 11). This trilevel pulse will be comprised of a –300 mV LOWSYNC level, a +300 mV HIGHSYNC level, and a 0 mV BLANKING level offset by +350 mVDC because the CX25874/5 cannot output negative voltages. Figure 3, Analog and Digital Timing Relationships, of the SMPTE-274M specification, shows a very detailed diagram of the trilevel sync and start of a line in 1080i mode. Figure 11 of this same SMPTE standard illustrates the horizontal timing and trilevel sync in more detail.

For those formats which require trilevel syncs, such as 1080i and 720p, the timing for certain portions of the synchronization pulses differ slightly. For instance, the amount of time each pulse is at a voltage level of –300 mV (LOWSYNC) is not the same from one resolution (ATSC format) to another. For 1080i, the time for the LOWSYNC level each line is 44T(44 clock periods = 44*(1/74.25 MHz)= 592.5 ns For 720p, the same interval is 40T periods long which equates to 40 * (1/74.25 MHz)= 538.7 ns.

In 480p resolution, in accordance with the SMPTE-293M specification, the CX25874/5 outputs only bilevel analog synchronization pulses.

As Figure 3, Analog and Digital Timing Relationships of the SMPTE-274M and -296M standards show, the period of time for the HIGHSYNC also varies when moving from 1080i mode to 720p mode. In this first case, the HIGHSYNC output level will be active for 44 clock periods. For 1080i, 44 clock periods * (1/74.25 MHz) = 592.6 ns. In 720p resolution, the HIGHSYNC output signal will be active for 40 clock periods per output line. For 720p, 40 clock periods * (1/74.25 MHz)= 538.7 ns, so the HIGHSYNC signal will only be active for 538.7 ns per output line.

Due to these discrepancies, the data master will need to program the CX25874/5's RASTER_SEL[1:0] bits properly so the encoder knows exactly which ATSC format it is going to encode. The encoder will then take care of outputting the proper analog voltage levels (see Figures E-5 through E-9) for the appropriate amounts of time depending on the resolution.

Table E-7 summarizes the different permutations of the RASTER_SEL[1:0] bits and the resolutions/modes supported with each option.

Table E-7. CX25874/5/CX25871 RASTER_SEL[1:0] Bit Functionality

RASTER_SEL[1]	RASTER_SEL[0]	HDTV/ATSC Mode	LOWSYNC period (ns)	HIGHSYNC period (ns)
1	1	1080i = SMPTE 274M(1)	44 clock periods = 592.6 ns	44 clock periods = 592.6 ns
1	0	720p = SMPTE 296M(2)	40 clock periods = 538.7ns	40 clock periods = 538.7 ns
0	1	480p = SMPTE 293M	63 clock periods = 2.36 µs.	No HIGHSYNC period
0	0	Trilevel sync periods dictated by HSYNC*&VSYNC* input levels	LOWSYNC period = width of VSYNC* input	HIGHSYNC period = width of HSYNC* input

GENERAL NOTE: To obtain any of these SMPTE specifications, visit Global Engineering Documents at: http://global.ihs.com/

FOOTNOTE:

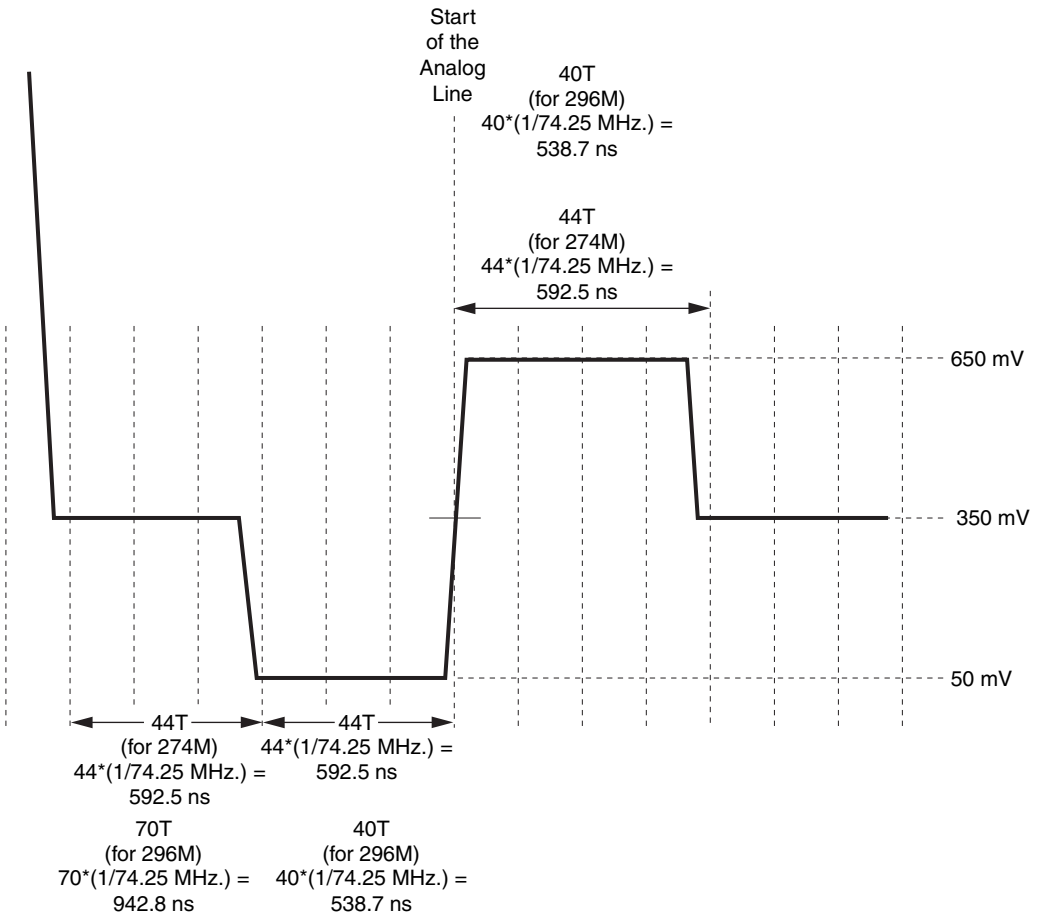
(1) The CX25874/5 can also be programmed for EIA-770.3 1080i format compliance. To do so, set RASTER_SEL[1:0] = 11 and set the BPB_SYNC_DIS and RPR_SYNC_DIS bits to 1 to disable the trilevel sync on the PB and PR signals.

(2) The CX25874/5 can also be programmed for EIA-770.3 720p format compliance. To do so, set RASTER_SEL[1:0] = 10 and set the BPB_SYNC_DIS and RPR_SYNC_DIS bits to 1 to disable the trilevel sync on the PB and PR signals.

The inserted syncs will adhere to Figure E-3 and the analog and digital timing relationships found in the various SMPTE specifications. All lines of the First and Second Fields of an Interlaced System will contain the trilevel syncs. This includes lines #1-5 and #564-567 of the 1080i format. Line 563 is an extraordinary case and the reader should defer to the SMPTE 274M specification for more details on this topic.

An illustration of the typical trilevel sync output from the CX25874/5 is shown on the next page. Note that the CX25874/5 cannot transmit negative voltages. As a result, the video output is offset by +350 mV to accommodate the negative sync levels listed in the governing specifications.

Figure E-3. 1080i and 720p Trilevel Sync provided by CX25874/5



GENERAL NOTE:

1. Tri-Level Sync applies to Y P_B, P_R output signals as well as HD RGB output signals.
2. 720p Tri-Level Sync timing differences are listed with the notation "(for 296 M)".

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E.6 Allowable Resolutions

Table E-8 summarizes the most popular HD resolutions or ATSC video formats supported by the CX25874/5. This encoder accepts digital data in a RGB, YPrPb, or YCrCb format.

Table E-8. CX25874/5 HDTV Supported Formats

Active Format (H x V)	Governing Standards	Input Data Format (can be muxed or nonmuxed)	Output Aspect Ratio	Frame Rate
1920x1080 = 1080i (contains trilevel syncs)	SMPTE-274M and EIA-770.3	15-, 16-, or 24-bit RGB or 16- or 24-bit Digital YP_BP_R or 16- or 24-bit YCrCb	16:9	30 Hz interlaced
1280x720 = 720p (contains trilevel syncs)	SMPTE-296M and EIA-770.3	15-, 16-, or 24-bit RGB or 16- or 24-bit Digital YP_BP_R or 16- or 24-bit YCrCb	16:9	60 Hz noninterlaced
720x480 = 480p (does not contain trilevel syncs)	SMPTE-293M and IUT-RBT.1358	15-, 16-, or 24-bit RGB or 16- or 24-bit Digital YP_BP_R or 16- or 24-bit YCrCb	16:9	60 Hz noninterlaced
720x576 = 625p (does not contain trilevel syncs)	ITU-RBT.1358	15-, 16-, or 24-bit RGB or 16- or 24-bit Digital YP_BP_R or 16- or 24-bit YCrCb	16:9	50 Hz noninterlaced
1920x1035-1035i (contains trilevel syncs)	ITU-RBT.709-4	15-, 16-, or 24-bit RGB or 16- or 24-bit Digital YP_BP_R or 16- or 24-bit YCrCb	16:9	30 Hz interlaced

Conceivably, any HD format with a clock less than or equal to 80 MHz can be displayed with the RASTER_SEL[1:0] = 00 option. This flexibility allows the CX25874/5 to receive and convert resolutions not yet standardized. All HDTV Output Mode resolutions will generate the new wide screen format that provides an aspect ratio of 16:9 yielding a movie-theatre like viewing experience.

When the encoder is in HDTV Output Mode, the internal FIFO and flicker filter blocks are bypassed. Therefore, the $Y/P_B/P_R$ and R/G/B video outputs do not have any flickering filtering nor any overscan compensation applied to them. For 480p, 720p, and other progressive input formats, the lack of flicker filtering causes no degradation whatsoever in the video output quality as compared to the digital input. For 1080i and other interlaced input formats, the lack of flicker filtering sets off the appearance of minor flickering in screen regions with small vertical dimensions.

The lack of overscan compensation in HDTV Output Mode results in the outer horizontal and vertical edges of the active image to appear behind the bezel of the television. This annoyance can be overcome by the insertion of a solid colored border around the active image itself by the data master in the digital domain.

E.7 720p Support with Character Clock Based Data Masters

Character clock based graphics controllers with 8 pixel clocks per character will experience difficulty supporting the 720p ATSC resolution. The reason for this is because the total line length (i.e., Samples per Total Line = S/TL) of 1650 pixels for 720p is not evenly divisible by 8. Thus, each line is comprised of an amount of characters that contains a non-zero fraction (206 + ¼ of a character or 206.25 total characters). To get around this shortcoming, the graphics controller must set its total line length to 1648 (HTOTAL) pixels and change the pixel clock frequency to 74.1600 MHz instead of the values of 1650 pixels and 74.2500 MHz, respectively, as specified in the SMPTE-296M standard that governs the 720p resolution.

All of the analog timing will then fall within the guidelines listed in the SMPTE-296M specification and the CX25874/5 will generate the desired analog representation of the 720p ATSC resolution.

Internal analysis of different portions of the 720p R/G/B and $Y/P_B/P_R$ waveforms has revealed that this approach is valid. All of the analog timing falls within the tolerances of the SMPTE-296M standard including the length of the broad pulse. In terms of clock periods, using the 74.1600 MHz clock yields a broad pulse length in time of 20.766 µs in duration. Using a 74.2500 MHz clock yields a broad pulse of 20.741 µs in duration. This tiny deviation will not cause a problem for any High-Definition television set.

To change the pixel clock frequency the encoder transmits and expects in return, the CX25874/5's PLL_INT and PLL_FRACT registers must be modified. For 720p support with Character Clock Based Data Masters, change the PLL_INT[5:0] bit field from 21 hex (for 74.25 MHz) to 20hex for 74.1600 MHz operation. Furthermore, reduce the 2-byte wide PLL_FRACT[15:0] from 0000 hex (for 74.25 MHz) to F5C3 hex for 74.1600 MHz operation. This reduction in the PLL_INT and PLL_FRACT registers will ensure the encoder transmits the modified 720p clock of 74.1600 MHz to the data master through CLKO and expects to receive data at this frequency coming back (via CLKI). This step must be done to render 720p via Character Clock Based Data Masters with the CX25874/5. Programming the data master's HTOTAL register to 1648 is vital as well. Modifying the CX25874/5's H_CLKI register to 1648 decimal is optional because this register will have no effect while the encoder is outputting HDTV.

In summary, for data masters which are character clock based with 8 and 9 pixel clocks per character and wish to support the 720p resolution, slow down the pixel input clock frequency (CLKI) by 90 kHz. to 74.1600 MHz and compensate by reducing HTOTAL by 2 pixels per line to 1648 pixels.

E.8 Automatic Insertion of Broad Pulses

In HD televisions, a frame shall begin with five vertical sync lines each containing a broad pulse. Broad pulses are the HD equivalent to the vertical synchronizing Serration and Equalization pulses used with present-day analog TVs. In response to the correct timing provided through the VSYNC* input which triggers the start of a new frame, the CX25874/5 will automatically insert broad pulses and trilevel syncs on the first 5 lines of the First Field(#1-#5) and the first 5 lines in the Second Field (563-568 for 1080i format). These broad pulses will adhere to the timing and voltage amplitudes found in various SMPTE specifications.

Figure E-7 illustrates the proper interface timing between the HDTV Source Device (master) and CX25874/5 (timing slave) during lines that include a BROAD PULSE in 1080i format. Figure E-9 shows the relationship between the digital input signals and HDTV output for lines that include a broad pulse in 720p format.

E.9 HDTV Output Mode Register and Bit Definitions

Table E-9. Register Bit Map for HDTV-Specific Registers

8-Bit Address	D7	D6	D5	D4	D3	D2	D1	D0
2E	HDTV_EN*	RGB2YPRPB*	RPR_SYNC_DIS*	GY_SYNC_DIS*	BPB_SYNC_DIS*	HD_SYNC_EDGE*	RASTER_SEL[1:0]*	
32	AUTO_CHK	Reserved		SETUP_HOLD_ADJ	IN_MODE[3]	DATDLY_RE	OFFSET_RGB*	CSC_SEL*

GENERAL NOTE:
1. * = HDTV-specific bits
2. ** The 625LINE bit is address Bit 2 of Register A2 and is not included in this table.

Table E-10. CX25874/5 Registers 0x2E and 0x32–HDTV Output Mode Bit Descriptions

Bit/Register Names	Bit/Register Definition
HDTV_EN	Enable HDTV Output Mode. OUT_MODE[1:0] register bits must be set to 11(VGA Mode). 0 = Enables VGA mode. DACs will output analog R, G, B with standard bilevel (–40 IRE) analog syncs. (DEFAULT) 1 = Enables HDTV Output mode. DACs will output HDTV compatible R/G/B or component video (Y/PR/PB) outputs. Trilevel syncs and vertical synchronizing/broad pulses will be inserted automatically if RASTER_SEL[1:0] = nonzero. ***GENERAL NOTE:*** EN_SCART bit must be 0 for HDTV Output Mode to be functional.
RGB2YPRPB	HDTV output switching bit. This bit is only effective when HDTV_EN = 1 and IN_MODE[3:0] = an RGB Input format. 0 = Digital RGB Input to Analog HDTV RGB Output (DEFAULT) 1 = Digital RGB Input to Analog HDTV YP_RP_B Output
RPR_SYNC_DIS	0 = Enables trilevel sync on Red or PR output. (DEFAULT) 1 = Disables trilevel sync on Red or PR output. This bit will have to be set manually for EIA-770.3 compliance.
GY_SYNC_DIS	0 = Enables trilevel sync on Green or Y output. (DEFAULT) 1 = Disables trilevel sync on Green or Y output
BPB_SYNC_DIS	0 = Enables trilevel sync on Blue or PB output. (DEFAULT) 1 = Disables trilevel sync on Blue or PB output. This bit will have to be set manually for EIA-770.3 compliance.
HD_SYNC_EDGE	This bit is only effective when HDTV_EN = 1 and RASTER_SEL is nonzero. 0 = Trilevel sync edges transition time is equal to 4 input clocks. (DEFAULT) 1 = Trilevel sync edges transition time is equal to 2 input clocks.
RASTER_SEL[1:0]	This bit is only effective when HDTV_EN = 1. 00 = Device does not generate trilevel sync automatically in HDTV output mode. Trilevel sync periods dictated by active HSYNC* input signal (as HIGHSYNC) and active VSYNC* input signal (as LOWSYNC). (DEFAULT) 01 = Bilevel sync generation for 480p, 525p, 625p formats 10 = Trilevel sync generation for 720p format 11 = Trilevel sync generation for 1080i, 1035i formats
OFFSET_RGB	0 = Standard RGB graphic digital input. Range is 0–255 decimal (DEFAULT) 1 = HDTV OFFSET RGB graphic digital input. Range is 16–235 decimal.
CSC_SEL	0 = Standard color space conversion for RGB to Y (R-Y) (B-Y) based on Y = 0.299R + 0.587G + 0.114B (DEFAULT) 1 = HDTV color space conversion for RGB to Y (R-Y) (B-Y) based on Y = 0.2126R + 0.7152G + 0.0722B
625LINE	When HDTV_EN = 1, this bit is only effective when RASTER_SEL = 01. 0 = Encoder generates 525-line HD formats (480p, 525p). 1 = Encoder generates 625-line HD format (576p, 625p).

E.10 Color Space Conversion Functionality to Support Analog RGB or YP_BP_R Component Video Outputs

The CX25874/5 has the ability to receive a digital RGB stream prevalent in graphics controllers or chipsets with integrated graphics with a width of 15-,16-, or 24-bits per pixel and transform it to a set of HDTV-compatible analog YP_BP_R component video outputs.

The option of not converting the digital RGB stream to analog YP_BP_R is available as well. In this case, the CX25874/5 would output a set of HDTV-compatible analog RGB component video outputs based on the same 15/16/or 24-bits per pixel RGB digital input.

The CX25874/5 can support the conversion from the HDTV color-difference digital YP_BP_R color space directly to analog YP_BP_R component video outputs seamlessly. No color space conversion nor register reprogramming is necessary for this case.

However, the HDTV color-difference digital YP_BP_R color space is slightly different from the standard digital 4:2:2 YCrCb (i.e., CCIR601) stream found within consumer applications such as set-top boxes. As a result, the CX25874/5 must be reprogrammed to new register values not found in Table E-3 to accommodate for the differences in the two formats. For this complete register set, contact your local Conexant Field Applications Engineer. Once obtained, program up the CX25874/5 as specified and it will provide analog YP_BP_R video outputs based on standard 4:2:2 YCrCb MPEG2 input data. The resulting outputs will be of high quality and viewable on SMPTE274M and SMPTE 296M standard HDTVs.

The reference equations for YP_RP_B:

$Y = 0.2126R' + 0.7152G' + 0.0722B'$

$Pb = \{0.5 / (1 - 0.0722)\} (B' - Y)$

$Pr = \{0.5 / (1 - 0.2126)\} (R' - Y)$

NOTE: The CX25874/5's MCOMPU register must contain a value of 45 hex prior to performing a color space conversion from digital RGB to analog YPBPR. The CX25874/5's MCOMPV register must contain a value of 51 hex prior to performing a color space conversion from digital RGB to analog YPBPR.

Digital Y, $P_{b,}$ and Pr are expressed as Y', P'_B and P'_R in the SMPTE specifications.

Finally, the CX25874/5 cannot provide analog RGB/HDTV video outputs from either color-difference digital YPrPb or 4:2:2 YCrCb MPEG2 input data. The encoder will not perform this color space conversion whatsoever. For analog RGB component HD out, a digital RGB input stream must be sent by the data master.

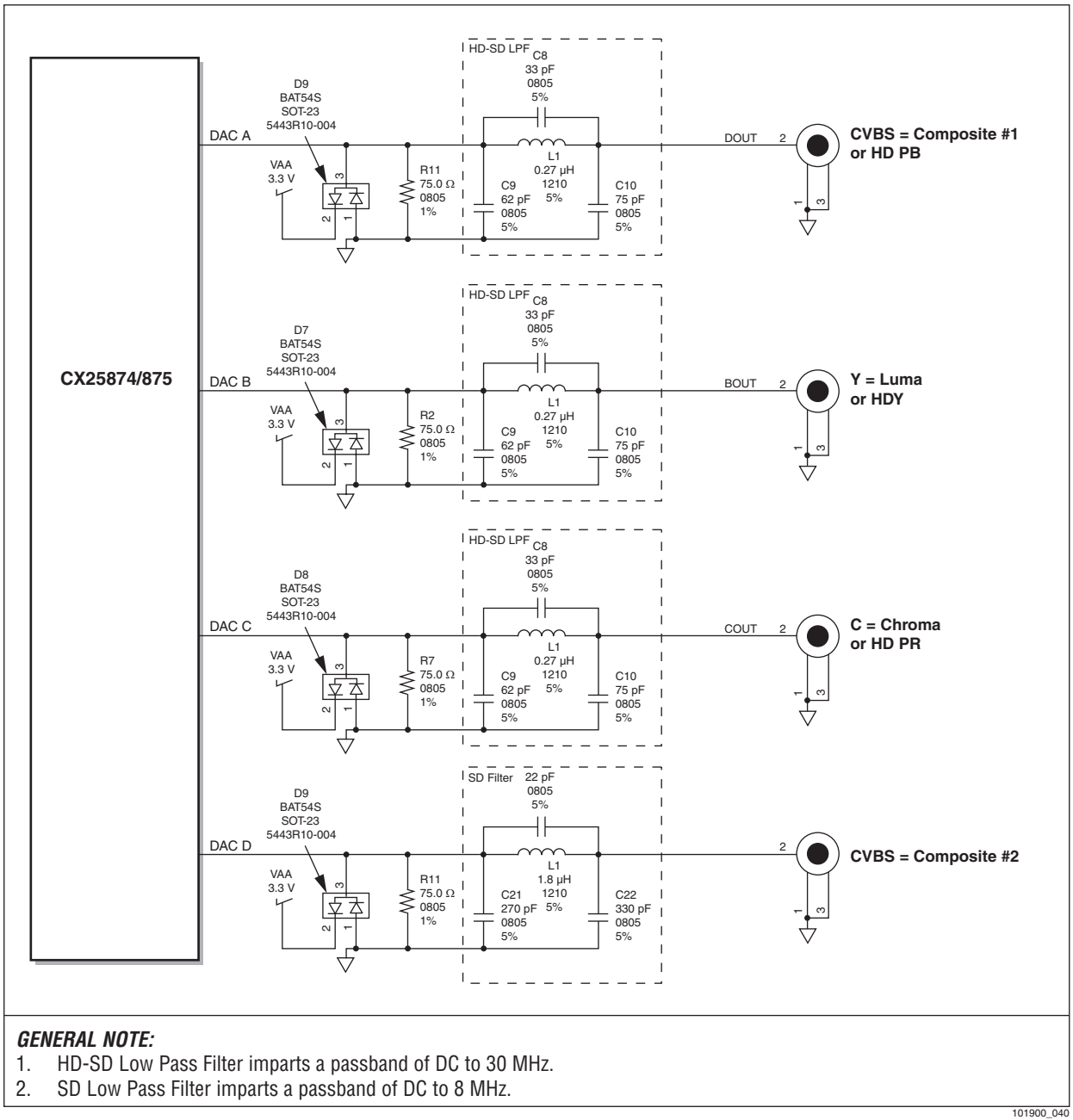
E.11 Recommended Output Filters for HDTV and SDTV

According to the SMPTE274M standard that governs the 1080i ATSC resolution, “the Y signal for Component HD video output shall have a bandwidth nominally of 30 MHz. In addition, the P_R and P_B signals shall have the same bandwidth as that of the associated Y signal at the analog originating equipment.” Other filter criteria found in the various SMPTE standards include the amplitude limit for ripple tolerance in the passband of $\pm$0.5 dB relative to insertion loss at 100 kHz. For Group-Delay, SMPTE states that the “group delay in the filters (should be) sufficiently tight to produce good performance while allowing the practical implementation of the filters themselves” (from SMPTE 274M and SMPTE293M(720p) standards).

As result of these criteria, during High-Definition Output Mode, each CX25874/5 DAC output requires a low-pass filter with a passband from DC to 30 MHz while adhering to the aforementioned group delay and passband ripple tolerances. Unfortunately, the filtering requirements for standard-definition television are quite different in several areas than filtering for HDTV. The most important difference is that standard-definition standards such as NTSC, PAL, and SECAM require a much lower 8 MHz passband starting at DC than HDTV.

This bandwidth difference coupled with the differing voltage amplitudes of the signals themselves forced Conexant to design a new low-pass filter with a wider passband to accommodate the HD outputs. After extensive testing and cost/benefit trade-offs, the company recommends that any customer using the encoder for both its standard-definition and high-definition capabilities design-in the HD-SD low-pass filter found in Figures 3-2, 3-5, 3-6, and E-4. This filter has been shown to exhibit many of the desired roll off, ripple, and passband characteristics defined in the aforementioned SMPTE standards. A frequency response plot of the HD-SD filter can be found in Figure 3-4.

Figure E-4. Recommended Low-Pass Filter Configuration for each CX25874/5 DAC for Generation of High-Definition and NTSC/PAL/SECAM TV Outputs



GENERAL NOTE:

1. HD-SD Low Pass Filter imparts a passband of DC to 30 MHz.
2. SD Low Pass Filter imparts a passband of DC to 8 MHz.

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E.12 Timing Diagrams for HDTV Output Mode

Figures E-5 through E-9 illustrate the relationship between the digital inputs received by the CX25874/5 and the HDTV Output signals transmitted by the encoder while in HDTV Output Mode.

Figure E-5. Proper Interface Timing between the HDTV Source Device (Master) and CX25874/5 (Timing Slave): Active Line in 1080i and 720p ATSC Format (RASTER SEL[1:0] = 11 or 10) for R, G, B, and Y Analog Outputs

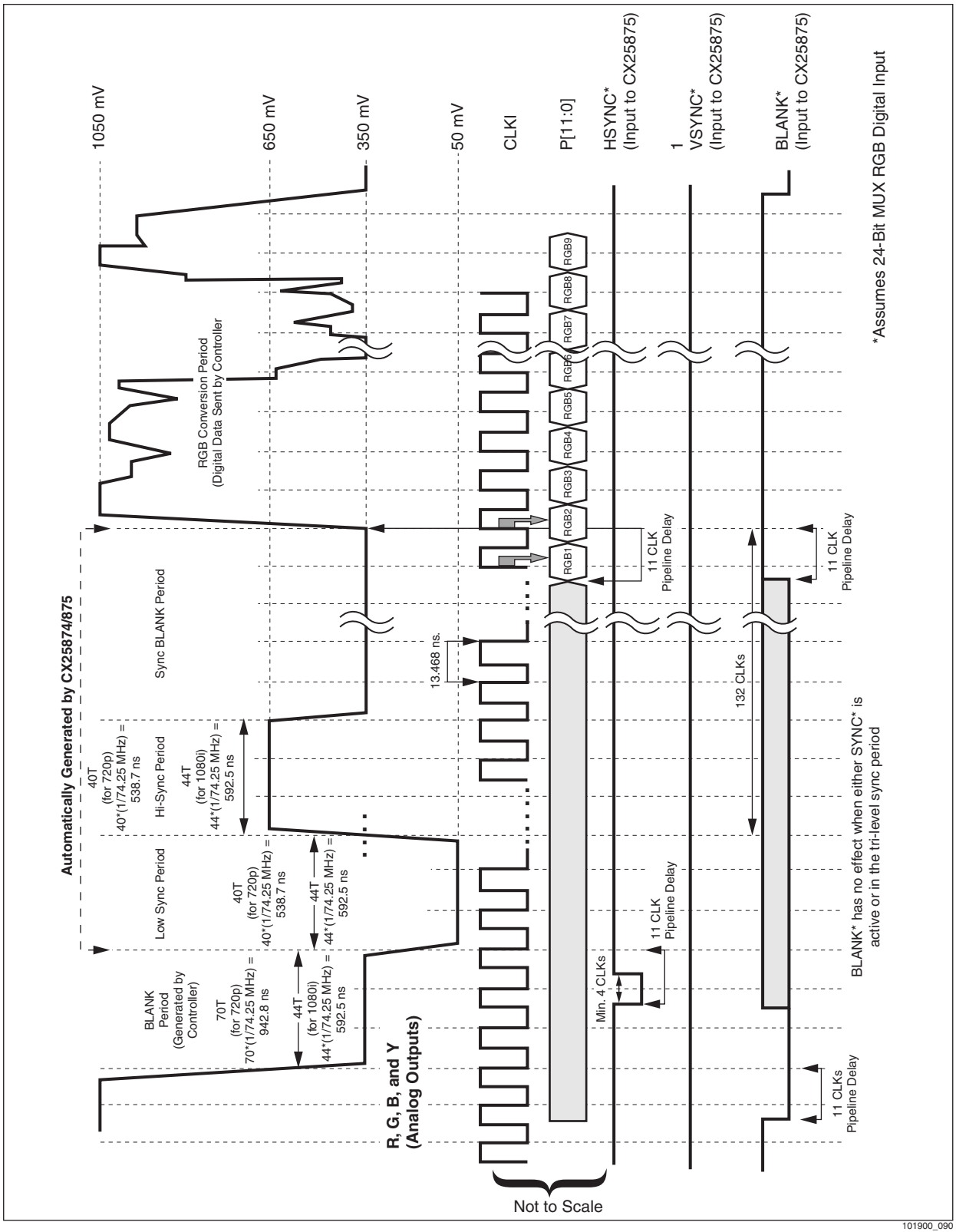


Figure E-6. Proper Interface Timing between the HDTV Source Device (Master) and CX25874/5 (Timing Slave): Active Line in 1080i and 720p ATSC Format (RASTER SEL[1:0] = 11 or 10) for P_B and P_R Analog Outputs

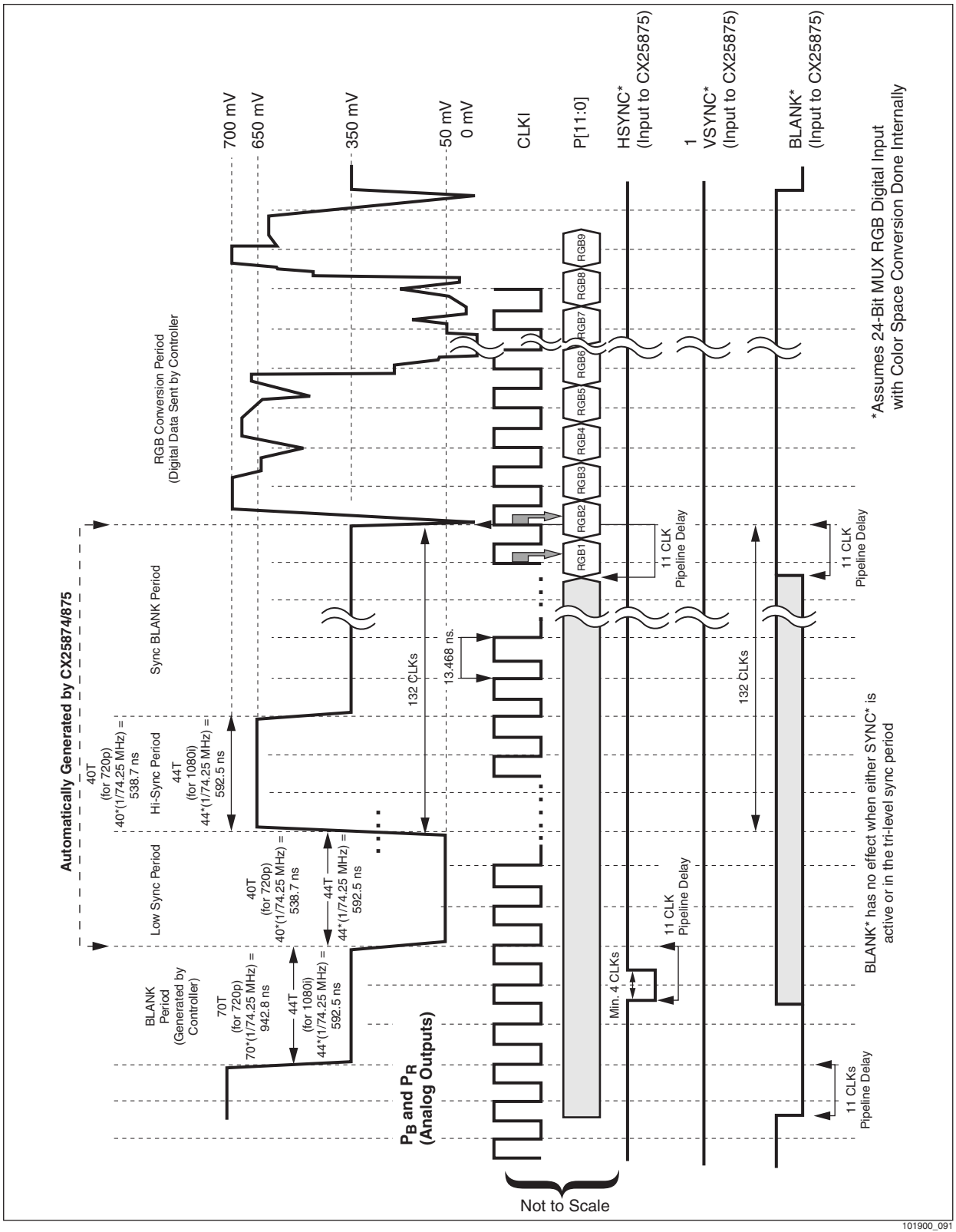


Figure E-7. Proper Interface Timing between the HDTV Source Device (Master) and CX25874/5 (Timing Slave): Broad Pulse Line in 1080i ATSC Format (RASTER SEL[1:0] = 11)—Odd Field

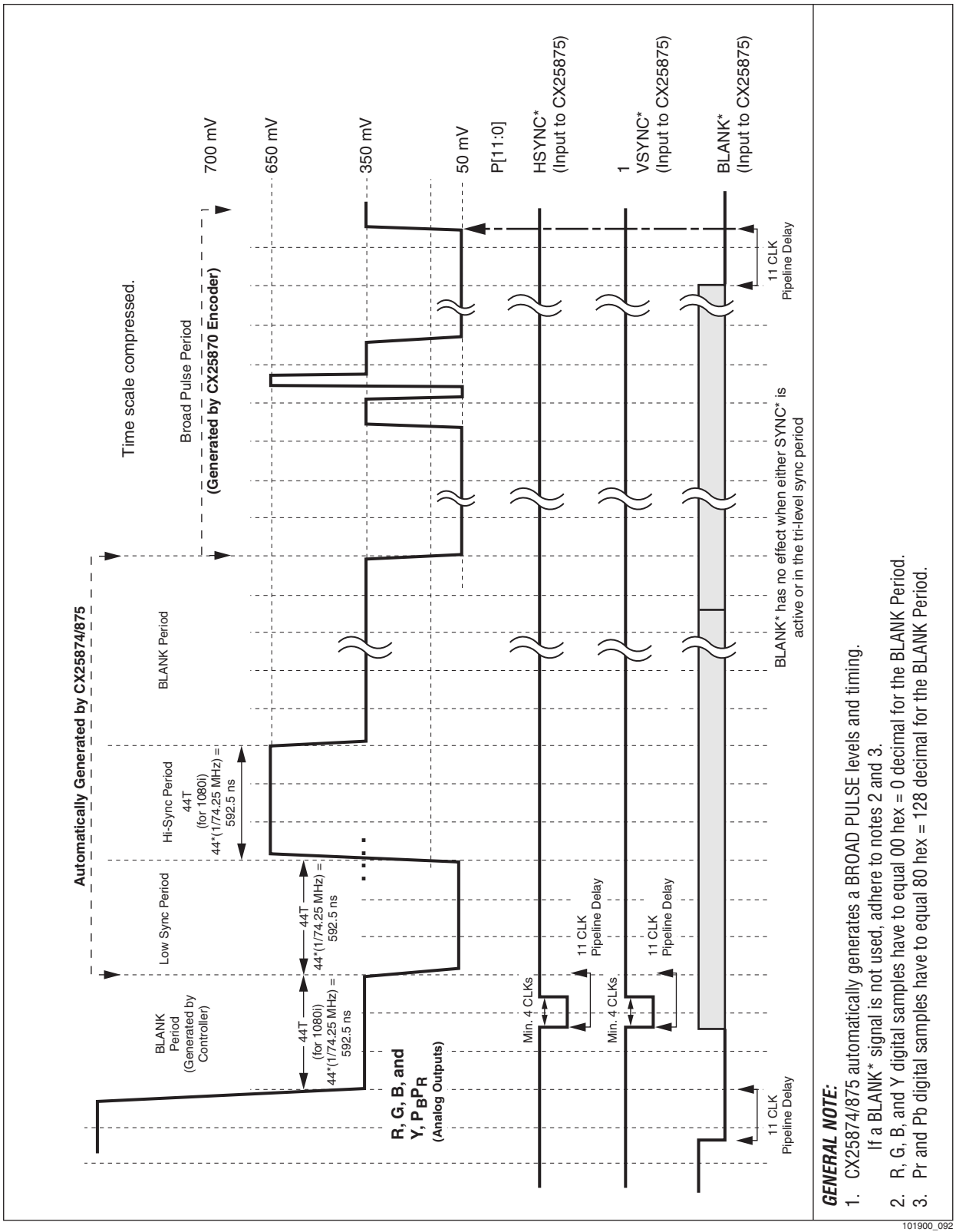
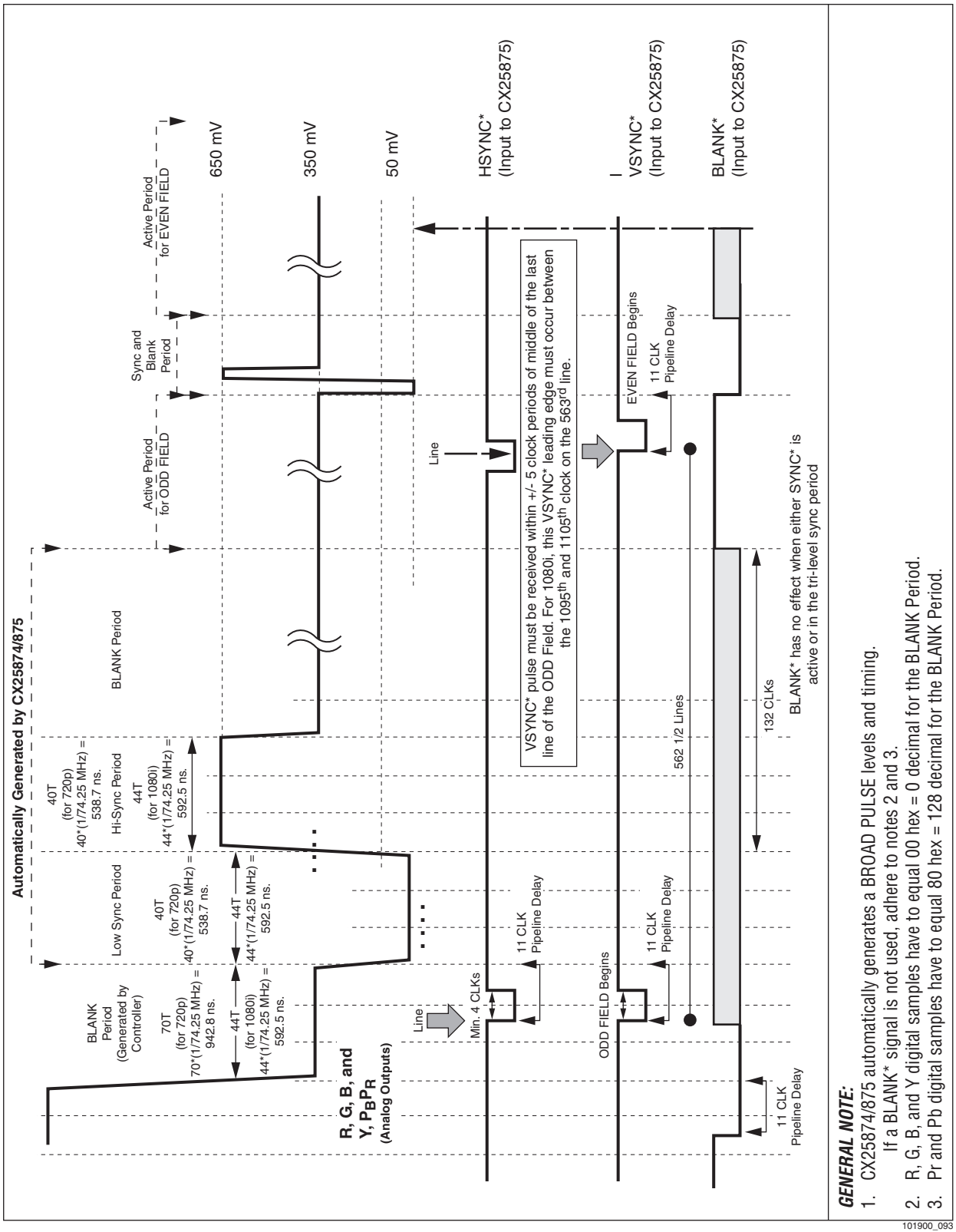


Figure E-8. Proper Interface Timing between the HDTV Source Device (Master) and CX25874/5 (Timing Slave): Two Successive Active Fields in 1080i ATSC Format (RASTER SEL[1:0] = 11)



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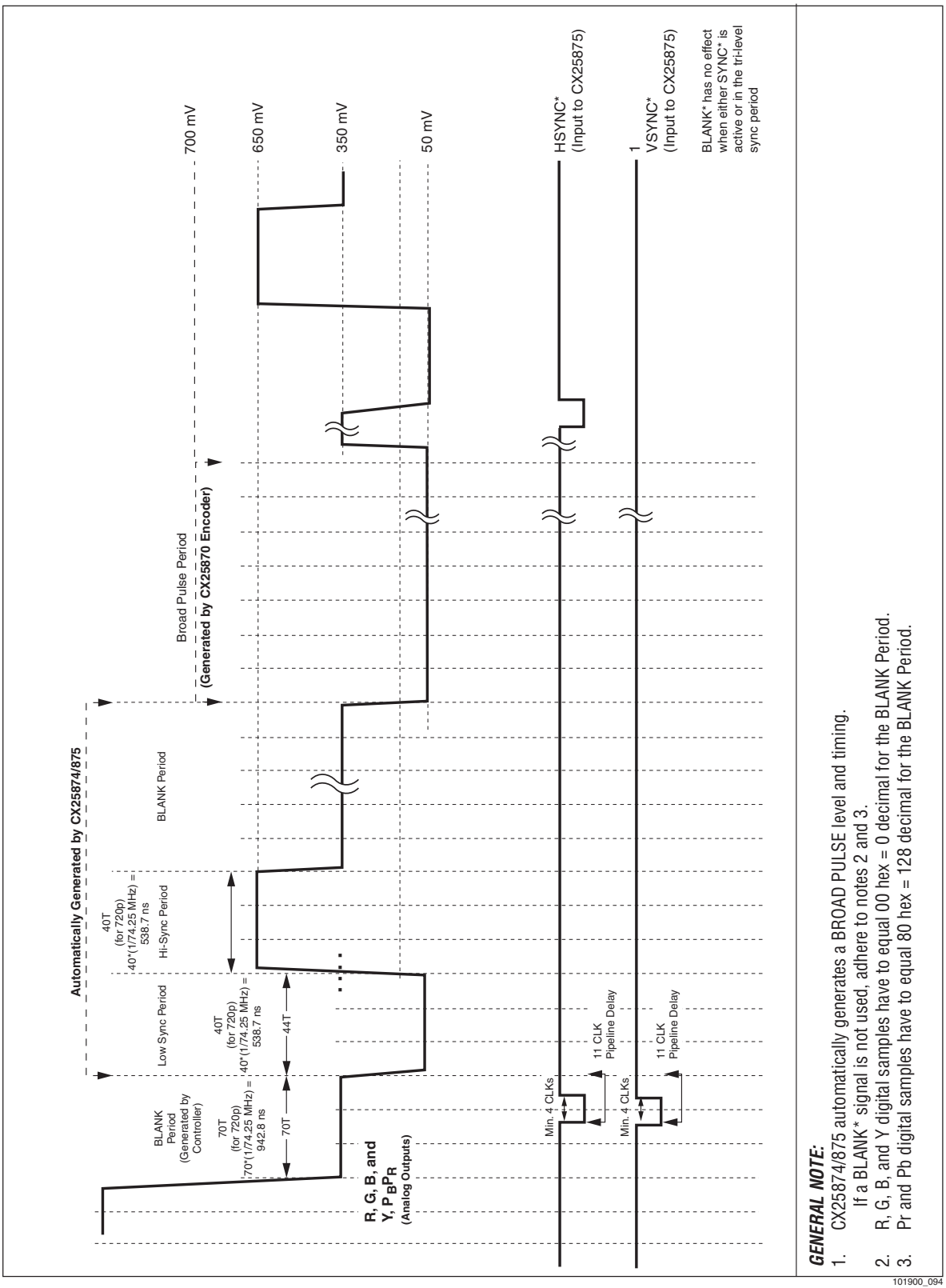
GENERAL NOTE:

1. CX25874/875 automatically generates a BROAD PULSE levels and timing.
   If a BLANK* signal is not used, adhere to notes 2 and 3.
2. R, G, B, and Y digital samples have to equal 00 hex = 0 decimal for the BLANK Period.
3. Pr and Pb digital samples have to equal 80 hex = 128 decimal for the BLANK Period.

Figure E-9. Proper Interface Timing between the HDTV Source Device (Master) and CX25874/5 (Timing Slave): Broad Pulse Line in 720p ATSC Format (RASTER SEL[1:0] = 10)



F

Complete Register Sets for All Desktop Resolutions

F.1 640x480, 800x600, 1024x768 NTSC-M and J, and PAL-M Register Sets

Using any of the 48 autoconfiguration modes in the CX25874/5 is the easiest method for bringing up the most popular desktop, game/Direct X, DOS boot-up screen, and DVD resolutions and TV out modes. However, sometimes the overscan ratios available through these autoconfiguration modes are not sufficient for some features such as a TV out size slider or some video applications in general. In these cases, use of a custom register set with a different overscan ratio is appropriate.

To give the software engineer maximum flexibility in enabling TV Out with various custom overscan ratios, Conexant has compiled Tables F-1 through F-7. These tables contain fully tested and working NTSC-M, -J, and PAL-M register sets for the three major desktop resolutions: 640x480, 800x600, and 1024x768. Some of these register sets are based on autoconfiguration modes and some are purely custom solutions. Note that each desktop resolution is supported with no less than four register sets corresponding to different overscan ratios that vary by approximately ±2 percent overscan compensation.

The default digital input format for the CX25874/5 will be IN_MODE[3:0] = 0000 = 24-bit RGB multiplexed and this is reflected in the table. Changing the encoder over to expect a different input format requires that the designer write a nonzero value to the IN_MODE[3:0] field. If this is necessary, perform this step after the entire register set has been programmed into the encoder.

Descriptions of many of the registers and bits are included in the last column within the spreadsheet itself.

Other settings shared by these register sets are as follows:

- Adaptive Flicker Filter has been programmed optimally for the specific input resolution.
- Physical interface used by the encoder is Master Interface with a BLANK* Input. This is not the default pseudo-master interface commonly used with the CX25874/5. The different interfaces are explained in the Autoconfiguration and Interface Bits section.
- SLAVE bit = 0. The state of the SLAVE bit dictates whether the CX25874/5 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. Since SLAVE = 0, the syncs will be generated by the encoder and sent to the master device.
- EN_OUT = 1 ensuring CLKO and other outputs enabled from the encoder.
- EN_BLANKO is high (=1), signifying the CX25874/5's BLANK* port is an output or that NO BLANK* signal is used as part of the system.

- EN_DOT = 0 telling the CX25874/5 to use its internal counters to determine the active versus the blanking regions.
- DAC routing configures DAC C as Luma, DAC B as Chroma, and DACA as Composite outputs. The DAC routing through register CE may need to be adjusted for each customer's particular set of outputs.
- Register 0xB8 is the autoconfiguration register. Do not program this or you will overwrite register values from 0x00 to 0xB6 with new, unwanted values.

The end user of any of these register sets may need to change various interface bits to make the CX25874/5 work with the particular GPU or master device it is connected to. If you wish the encoder to be in pseudo-master interface, as explained in the Autoconfiguration and Interface Bits section, then you will need to reprogram the SLAVE(bit 5 of 0xBA), EN_BLANKO(MSb of register 0xC6), EN_DOT(bit 6 of register 0xC6), and EN_OUT(LSb of register 0xC4) bits to the required values.

In addition to the register sets in the following tables, it is suggested that interested designers alter these video-quality centric register values tested to yield the best 640x480 NTSC picture quality into their software driver. Similar settings can be used for 800x600 and 1024x768 resolutions.

- Reg 0x34 = Adaptive FF register 1 on
- Reg 0x36 = Adaptive FF register 2 on
- Reg 0x96. CLPF[1:0] = bypass, YLPF[1:0] = bypass
- Reg 0xC8. DIS_YFLPF = 1= Enabled. Std. Y&C Flicker Filter set appropriately.
- Reg 0xCA = C3 so YATTEN = Brightness/Contrast switched to 3/4 gain.
- Reg 0xCC = C2 so CATTEN = Saturation = 7/8 gain.
- Reg 0xD8 = 60 so CHROMA_BW = off, BY_YCCR ON, PK_FIL = 10 for 2 dB gain

For more programming instructions see Section 1.3.21. It is not possible to reprogram only the encoder to enable a new TV out solution. To achieve VGA compatibility, the controller must manipulate some of its own VGA register settings in order to produce a high-quality dual display on both the computer monitor and TV. It should be noted that the encoder has no way of knowing that a different VGA mode has been selected. As a result, it relies on the serial bus master device to reconfigure it via an autoconfiguration mode or complete register set rewrite to make adjustments in its timing.

When the two devices are programmed correctly, regardless of the interface, the required input HSYNC*/VSYNC* to first input active pixel or line spacing matches the output HSYNC*/VSYNC* to first output active pixel or line spacing. When this occurs, the graphics controller always transmits active data at the time the CX25874/5 expects to receive it. Superior TV out quality is achieved only when this type of timing symmetry exists.

Table F-1. Complete Register Sets for 640x480 Input—NTSC-M Video Outputs *(1 of 4)*

MODE	640x480 NTSC-M			
Purpose of mode:	Complete CX25875 Reg. Set for NTSC-M output	Complete CX25875 Reg. Set for NTSC-M output	Complete CX25875 Reg. Set for NTSC-M output	Complete CX25875 Reg. Set for NTSC-M output
Active Resolution:	640x480 Default = MID OVERSCAN	640x480 MIN OVERSCAN	640x480 MAX OVERSCAN	640x480 MAX OVERSCAN
Auto Configuration Mode # used:	0	Custom Reg Set	Custom Reg Set	32
Horizontal Overscan Comp (HOC):	13.79	9.97	16.76	18.34
Vertical Overscan Comp (VOC):	13.58	11.11	14.82	19.34
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	640	640	640	640
Number of active lines/frame(V_ACTIVEI)	480	480	480	480
H_CLKI = HTOTAL(pixels)	784	770	800	770
VLINES_I = VTOTAL(lines)	600	585	609	645
H_BLANKI = Horizontal Blanking Region(pixels)	126	113	140	113
V_BLANKI = Vertical Blanking Region(lines)	75	69	81	100
Frequency of CLK (MHz)	28.195793	27.000000	29.202793	29.769241
Type of Video Output:	NTSC-M	NTSC-M	NTSC-M	NTSC-M
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	0	0	0
Read Only: 0x02	00	0	0	0
Read Only: 0x04	00	0	0	0
Read Only: 0x06	00	0	0	0
0x2E	00	0	0	0
0x30	00	0	0	0
0x32	00	0	0	0
0x34	9B	9B	9B	9B
0x36	C0	C0	C0	C0
0x38	00	0	0	00
0x3A	00	0	0	0
0x3C	80	80	80	80
0x3E	80	80	80	80

Table F-1. Complete Register Sets for 640x480 Input—NTSC-M Video Outputs *(2 of 4)*

MODE	640x480 NTSC-M			
0x40	80	80	80	80
0x42	00	0	0	0
0x44	00	0	0	0
0x46	00	0	0	0
0x48	00	0	0	0
0x4A	65	A3	36	36
0x4C	6D	9F	46	46
0x4E	25	25	25	25
0x50	65	A3	36	36
0x52	6D	9F	46	46
0x54	25	25	25	25
0x56	00	0	0	0
0x58	00	0	0	0
0x5A	00	0	0	0
0x5C	00	0	0	0
0x5E	00	0	0	0
0x60	00	0	0	0
0x62	00	0	0	0
0x64	00	0	0	0
0x66	06	E8	C8	C8
0x68	00	0	0	0
0x6A	00	0	0	0
0x6C	46	46	46	46
0x6E	00	0	0	0
0x70	0F	0F	0F	0F
0x72	00	0	0	0
0x74	01	1	1	1
0x76	00	B4	40	64
0x78	80	80	80	80
0x7A	84	7E	8A	8C
0x7C	96	90	9A	9E
0x7E	60	58	68	6E
0x80	7D	53	A1	B5

Table F-1. Complete Register Sets for 640x480 Input—NTSC-M Video Outputs *(3 of 4)*

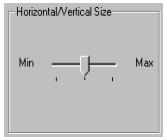
MODE	640x480 NTSC-M			
0x82	22	20	24	2A
0x84	D4	D9	D1	C5
0x86	27	26	27	27
0x88	00	0	0	00
0x8A	10	2	20	02
0x8C	7E	71	8C	71
0x8E	03	3	3	03
0x90	58	49	61	85
0x92	4B	45	51	64
0x94	E0	E0	E0	E0
0x96	06	6	6	06
0x98	92	A8	1F	50
0x9A	54	53	55	57
0x9C	0E	0	A1	14
0x9E	88	0	FA	3B
0xA0	0C	0C	0C	0D
0xA2	0A	0A	0A	0A
0xA4	E5	E5	E5	E5
0xA6	76	76	75	75
0xA8	79	79	79	79
0xAA	44	44	44	44
0xAC	85	85	85	85
0xAE	00	1F	7C	F2
0xB0	00	7C	1A	40
0xB2	80	F0	61	C8
0xB4	20	21	1F	1E
0xB6	00	0	0	0
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface**: 0xBA**	00	0	0	0
0xBC	00	0	0	0
0xBE	00	0	0	0

Table F-1. Complete Register Sets for 640x480 Input—NTSC-M Video Outputs *(4 of 4)*

MODE	640x480 NTSC-M			
0xC0	00	0	0	0
0xC2	00	0	0	0
LSb helps to control interface: **0xC4**	01	1	1	1
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	92	92	92	92
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	0	0	0
0xD2	00	0	0	0
0xD4	00	0	0	0
0xD6	00	0	0	0
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-2. Complete Register Sets for 640x480 Input—PAL-M Video Outputs *(1 of 4)*

MODE	640x480 PAL-M			
Purpose of mode:	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output
Active Resolution:	640x480 Default = MID OVERSCAN	640x480 MIN OVERSCAN	640x480 MAX OVERSCAN	640x480 MAX OVERSCAN
Auto Configuration Mode # used:	0	Custom Reg Set	Custom Reg Set	32
Horizontal Overscan Comp (HOC):	13.79	9.97	16.76	18.34
Vertical Overscan Comp (VOC):	13.58	11.11	14.82	19.34
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	640	640	640	640
Number of active lines/frame(V_ACTIVEI)	480	480	480	480
H_CLKI = HTOTAL(pixels)	784	770	800	770
VLINES_I = VTOTAL(lines)	600	585	609	645
H_BLANKI = Horizontal Blanking Region(pixels)	126	113	140	113
V_BLANKI = Vertical Blanking Region(lines)	75	69	81	100
Frequency of CLK (MHz)	28.195793	27.000000	29.202793	29.769241
Type of Video Output:	PAL-M	PAL-M	PAL-M	PAL-M
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	9B	9B	9B	9B
0x36	C0	C0	C0	C0
0x38	00	00	00	00
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80

Table F-2. Complete Register Sets for 640x480 Input—PAL-M Video Outputs *(2 of 4)*

MODE	640x480 PAL-M			
0x40	80	80	80	80
0x42	0	0	0	0
0x44	0	0	0	0
0x46	0	0	0	0
0x48	0	0	0	0
0x4A	65	A3	36	1C
0x4C	6D	9F	46	31
0x4E	25	25	25	25
0x50	65	A3	36	1C
0x52	6D	9F	46	31
0x54	25	25	25	25
0x56	0	0	0	0
0x58	0	0	0	0
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	6	E8	C8	96
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	00	B4	40	64
0x78	80	80	80	80
0x7A	84	7E	8A	8C
0x7C	A4	9D	A9	AD
0x7E	6A	60	72	78
0x80	7D	52	A1	B5

Table F-2. Complete Register Sets for 640x480 Input—PAL-M Video Outputs *(3 of 4)*

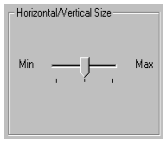
MODE	640x480 PAL-M			
0x82	22	20	24	2A
0x84	D4	D9	D1	C5
0x86	27	26	27	27
0x88	00	00	00	00
0x8A	10	02	20	02
0x8C	7E	71	8C	71
0x8E	03	03	03	03
0x90	58	49	61	85
0x92	4B	45	51	64
0x94	E0	E0	E0	E0
0x96	06	06	06	06
0x98	92	A8	1F	50
0x9A	54	53	55	57
0x9C	0E	0	A1	14
0x9E	88	0	FA	3B
0xA0	0C	0C	0C	0D
0xA2	2A	2A	2A	2A
0xA4	F0	F0	F0	F0
0xA6	57	57	57	57
0xA8	80	80	80	80
0xAA	48	48	48	48
0xAC	8C	8C	8C	8C
0xAE	6E	E3	9F	16
0xB0	DB	EF	46	98
0xB2	76	E6	58	BF
0xB4	20	21	1F	1E
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: **0xBA**	00	00	00	00
0xBC	00	00	00	00
0xBE	00	00	00	00

Table F-2. Complete Register Sets for 640x480 Input—PAL-M Video Outputs (4 of 4)

MODE	640x480 PAL-M			
0xC0	00	00	00	00
0xC2	00	00	00	00
LSb helps to control interface: **0xC4**	01	01	01	01
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	92	92	92	92
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-3. Complete Register Sets for 800x600 Input—NTSC-M Video Outputs *(1 of 4)*

MODE	800x600 NTSC-M			
Purpose of mode:	Complete CX25875 Reg. Set for NTSC output	Complete CX25875 Reg. Set for NTSC output	Complete CX25875 Reg. Set for NTSC output	Complete CX25875 Reg. Set for NTSC output
Active Resolution:	800x600 Default = MID OVERSCAN	800x600 = MIN OVERSCAN	800x600 = MAX OVERSCAN	800x600 = MAX OVERSCAN
Auto Configuration Mode # used:	18	Custom	40	34
Horizontal Overscan Comp (HOC):	13.78	11.57	15.59	19.26
Vertical Overscan Comp (VOC):	13.58	11.52	15.63	19.34
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	800	800	800	800
Number of active lines/frame(V_ACTIVEI)	600	600	600	600
H_CLKI = HTOTAL(pixels)	1176	1170	1170	1170
VLINES_I = VTOTAL(lines)	750	735	770	805
H_BLANKI = Horizontal Blanking Region(pixels)	329	323	323	323
V_BLANKI = Vertical Blanking Region(lines)	94	86	105	125
Frequency of CLK (MHz)	52/867138	51.545448	54.000000	56.454552
Type of Video Output:	NTSC-M	NTSC-M	NTSC-M	NTSC-M
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	0	0	00
Read Only: 0x02	00	0	0	00
Read Only: 0x04	00	0	0	00
Read Only: 0x06	00	0	0	00
0x2E	00	0	0	00
0x30	00	0	0	00
0x32	00	0	0	00
0x34	80	80	80	80
0x36	92	92	92	92
0x38	20	20	20	20
0x3A	00	0	0	00
0x3C	80	80	80	80

Table F-3. Complete Register Sets for 800x600 Input—NTSC-M Video Outputs *(2 of 4)*

MODE	800x600 NTSC-M			
0x3E	80	80	80	80
0x40	80	80	80	80
0x42	00	0	0	0
0x44	00	0	0	0
0x46	00	0	0	0
0x48	00	0	0	0
0x4A	51	6D	3A	don't reprogram, default state ok
0x4C	8A	A1	77	don't reprogram, default state ok
0x4E	1C	1C	1C	1C
0x50	51	6D	3A	don't reprogram, default state ok
0x52	8A	A1	77	don't reprogram, default state ok
0x54	1C	1C	1C	1C
0x56	00	0	0	0
0x58	00	0	0	0
0x5A	00	0	0	00
0x5C	00	0	0	00
0x5E	00	0	0	00
0x60	00	0	0	00
0x62	00	0	0	00
0x64	00	0	0	00
0x66	5	5A	EE	don't reprogram, default state ok
0x68	00	0	0	00
0x6A	00	0	0	00
0x6C	46	46	46	46
0x6E	00	0	0	00
0x70	0F	0F	0F	0F
0x72	00	0	0	00
0x74	01	1	1	01
0x76	C0	88	F0	58
0x78	20	20	20	20
0x7A	A6	A2	AA	B0
0x7C	BA	B6	BE	C8
0x7E	98	92	9E	AC

Table F-3. Complete Register Sets for 800x600 Input—NTSC-M Video Outputs *(3 of 4)*

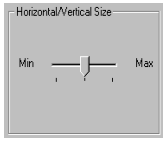
MODE	800x600 NTSC-M			
0x80	D9	B9	F3	2D
0x82	22	20	25	2A
0x84	D4	D8	CE	C5
0x86	38	38	38	39
0x88	00	0	0	00
0x8A	98	92	92	92
0x8C	49	43	43	43
0x8E	0C	0C	0C	0C
0x90	EE	DF	2	25
0x92	5E	56	69	7D
0x94	58	58	58	58
0x96	0A	0A	0B	0B
0x98	B7	CD	EF	11
0x9A	5D	5C	5E	A1
0x9C	1B	BA	0	46
0x9E	7F	E8	0	17
0xA0	17	16	18	19
0xA2	0A	0A	0A	0A
0xA4	E5	E5	E5	E5
0xA6	74	75	74	74
0xA8	78	78	78	77
0xAA	43	43	43	43
0xAC	85	85	85	85
0xAE	0	AB	17	21
0xB0	0	AA	5D	0B
0xB2	0	AA	74	59
0xB4	1A	1A	19	18
0xB6	00	0	0	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: **0xBA**	00	0	0	0
0xBC	00	0	0	0

Table F-3. Complete Register Sets for 800x600 Input—NTSC-M Video Outputs (4 of 4)

MODE	800x600 NTSC-M			
0xBE	00	0	0	0
0xC0	00	0	0	0
0xC2	00	0	0	0
LSb helps to control interface: **0xC4**	01	1	1	1
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	9B	9B	9B	9B
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	0	0	0
0xD2	00	0	0	0
0xD4	00	0	0	0
0xD6	00	0	0	0
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-4. Complete Register Sets for 800x600 Input—PAL-M Video Outputs *(1 of 4)*

MODE	800x600 PAL-M			
Purpose of mode:	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output	Complete CX25875 Reg. Set for PAL-M output
Active Resolution:	800x600 Default = MID OVERSCAN	800x600 = MIN OVERSCAN	800x600 = MAX OVERSCAN	800x600 = MAX OVERSCAN
Auto Configuration Mode # used:	18	Custom	40	34
Horizontal Overscan Comp (HOC):	13.78	11.57	15.59	19.26
Vertical Overscan Comp (VOC):	13.58	11.52	15.63	19.34
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	800	800	800	800
Number of active lines/frame(V_ACTIVEI)	600	600	600	600
H_CLKI = HTOTAL(pixels)	1176	1170	1170	1170
VLINES_I = VTOTAL(lines)	750	735	770	805
H_BLANKI = Horizontal Blanking Region(pixels)	329	323	323	323
V_BLANKI = Vertical Blanking Region(lines)	94	86	105	125
Frequency of CLK (MHz)	52/867138	51.545448	54.000000	56.454552
Type of Video Output:	PAL-M	PAL-M	PAL-M	PAL-M
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	80	80	80	80
0x36	92	92	92	92
0x38	20	20	20	20
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80

Table F-4. Complete Register Sets for 800x600 Input—PAL-M Video Outputs (2 of 4)

MODE	800x600 PAL-M			
0x40	80	80	80	80
0x42	0	0	0	0
0x44	0	0	0	0
0x46	0	0	0	0
0x48	0	0	0	0
0x4A	51	6D	3A	0B
0x4C	8A	A1	77	50
0x4E	1C	1C	1C	1C
0x50	51	6D	3A	0B
0x52	8A	A1	77	50
0x54	1C	1C	1C	1C
0x56	0	0	0	0
0x58	0	0	0	0
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	5	5A	EE	B7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	C0	88	F0	58
0x78	20	20	20	20
0x7A	A6	A2	AA	B0
0x7C	CC	C7	D1	DA
0x7E	A6	9E	AC	BA
0x80	D8	B9	F3	2D

Table F-4. Complete Register Sets for 800x600 Input—PAL-M Video Outputs *(3 of 4)*

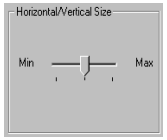
MODE	800x600 PAL-M			
0x82	22	20	25	2A
0x84	D4	D8	CE	C5
0x86	38	38	38	39
0x88	00	00	00	00
0x8A	98	92	92	92
0x8C	49	43	43	43
0x8E	0C	0C	0C	0C
0x90	EE	DF	2	25
0x92	5E	56	69	7D
0x94	58	58	58	58
0x96	0A	0A	0B	0B
0x98	B7	CD	EF	11
0x9A	5D	5C	5E	A1
0x9C	1B	BA	0	46
0x9E	7F	E8	0	17
0xA0	17	16	18	19
0xA2	2A	2A	2A	2A
0xA4	F0	F0	F0	F0
0xA6	56	56	56	56
0xA8	7F	7F	7F	7E
0xAA	47	47	47	47
0xAC	8C	8C	8C	8C
0xAE	8B	33	EB	A9
0xB0	AF	2A	33	31
0xB2	F8	A3	6D	52
0xB4	19	1A	19	18
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	00	00	00	00
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00

Table F-4. Complete Register Sets for 800x600 Input—PAL-M Video Outputs *(4 of 4)*

MODE	800x600 PAL-M			
0xC2	00	00	00	00
LSb helps to control interface: **0xC4**	01	01	01	01
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	9B	9B	9B	9B
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-5. Complete Register Sets for 1024x768 Input—NTSC-M Video Outputs (1 of 4)

MODE	1024x768 NTSC-M			
Purpose of mode:	CX25875 Reg. Set for NTSC-M output	CX25875 Reg. Set for NTSC-M output	CX25875 Reg. Set for NTSC-M output	CX25875 Reg. Set for NTSC-M output
Active Resolution:	1024x768 Default = MIN OVERSCAN	1024x768 = MID OVERSCAN	1024x768 = MAX OVERSCAN	1024x768 = LOWEST OVERSCAN
Auto Configuration Mode # used:	26	10	42	Custom
Horizontal Overscan Comp (HOC):	11.97	15.11	18.04	10.17
Vertical Overscan Comp (VOC):	11.93	14.81	18.11	7.82
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	1024	1024	1024	1024
Number of active lines/frame(V_ACTIVEI)	768	768	768	768
H_CLKI = HTOTAL(pixels)	1170	1176	1170	1204
VLINES_I = VTOTAL(lines)	945	975	1015	900
H_BLANKI = Horizontal Blanking Region(pixels)	127	133	127	157
V_BLANKI = Vertical Blanking Region(lines)	115	130	150	92
Frequency of CLK (MHz)	66.272724	68.727275	71.181827	64.951034
Type of Video Output:	NTSC-M	NTSC-M	NTSC-M	NTSC-M
TV Out Size:	LOW/MIN	MID	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	0	0	0
Read Only: 0x02	00	0	0	0
Read Only: 0x04	00	0	0	0
Read Only: 0x06	00	0	0	0
0x2E	00	0	0	0
0x30	00	0	0	0
0x32	00	0	0	0
0x34	80	80	80	80
0x36	F6	F6	F6	F6
0x38	20	20	20	20
0x3A	00	0	0	0
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-5. Complete Register Sets for 1024x768 Input—NTSC-M Video Outputs (2 of 4)

MODE	1024x768 NTSC-M			
0x42	00	0	0	0
0x44	00	0	0	0
0x46	00	0	0	0
0x48	00	0	0	0
0x4A	71	52	35	83
0x4C	D3	B9	A1	E1
0x4E	13	13	13	13
0x50	71	52	35	83
0x52	D3	B9	A1	E1
0x54	13	13	13	13
0x56	00	0	0	0
0x58	00	0	0	0
0x5A	00	0	0	0
0x5C	00	0	0	0
0x5E	00	0	0	0
0x60	00	0	0	0
0x62	00	0	0	0
0x64	00	0	0	0
0x66	7F	4	A2	57
0x68	00	0	0	0
0x6A	00	0	0	0
0x6C	46	46	46	46
0x6E	00	0	0	0
0x70	0F	0F	0F	0F
0x72	00	0	0	0
0x74	01	1	1	1
0x76	F8	60	C8	C0
0x78	0	0	0	0
0x7A	D0	D8	E0	CC
0x7C	EA	F2	FC	E6
0x7E	E0	EE	FA	DA
0x80	37	71	AB	17
0x82	21	24	28	1C

Table F-5. Complete Register Sets for 1024x768 Input—NTSC-M Video Outputs (3 of 4)

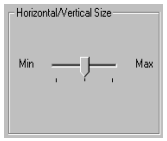
MODE	1024x768 NTSC-M			
0x84	D7	D0	C8	E1
0x86	4A	4B	4B	4A
0x88	00	0	0	0
0x8A	92	98	92	B4
0x8C	7F	85	7F	9D
0x8E	04	4	4	4
0x90	B1	CF	F7	84
0x92	73	82	96	5C
0x94	0	0	0	0
0x96	0F	0F	0F	0F
0x98	9A	6E	DE	DB
0x9A	A9	AB	AD	A6
0x9C	5D	A3	E8	FC
0x9E	74	8B	A2	DD
0xA0	1D	1E	1F	1C
0xA2	0A	0A	0A	0A
0xA4	E5	E5	E5	E5
0xA6	74	74	74	74
0xA8	77	77	77	77
0xAA	43	43	43	43
0xAC	85	85	85	85
0xAE	2F	0	C2	A7
0xB0	A1	0	72	AC
0xB2	BD	0	4F	29
0xB4	14	14	13	15
0xB6	00	0	0	0
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: **0xBA**	00	0	0	0
0xBC	00	0	0	0
0xBE	00	0	0	0
0xC0	00	0	0	0
0xC2	00	0	0	0

Table F-5. Complete Register Sets for 1024x768 Input—NTSC-M Video Outputs (4 of 4)

MODE	1024x768 NTSC-M			
LSb helps to control interface: **0xC4**	01	1	1	1
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	80	80	80	80
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	0	0	0
0xD2	00	0	0	0
0xD4	00	0	0	0
0xD6	00	0	0	0
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-6. Complete Register Sets for 1024x768 Input—PAL-M Video Outputs (1 of 4)

MODE	1024x768 PAL-M			
Purpose of mode:	CX25875 Reg. Set for PAL-M output	CX25875 Reg. Set for PAL-M output	CX25875 Reg. Set for PAL-M output	CX25875 Reg. Set for PAL-M output
Active Resolution:	1024x768 Default = MIN OVERSCAN	1024x768 = MID OVERSCAN	1024x768 = MAX OVERSCAN	1024x768 = LOWEST OVERSCAN
Auto Configuration Mode # used:	26	10	42	Custom
Horizontal Overscan Comp (HOC):	11.97	15.11	18.04	10.17
Vertical Overscan Comp (VOC):	11.93	14.81	18.11	7.82
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	1024	1024	1024	1024
Number of active lines/frame(V_ACTIVEI)	768	768	768	768
H_CLKI = HTOTAL(pixels)	1170	1176	1170	1204
VLINES_I = VTOTAL(lines)	945	975	1015	900
H_BLANKI = Horizontal Blanking Region(pixels)	127	133	127	157
V_BLANKI = Vertical Blanking Region(lines)	115	130	150	92
Frequency of CLK (MHz)	66.272724	68.727275	71.181827	64.951034
Type of Video Output:	PAL-M	PAL-M	PAL-M	PAL-M
TV Out Size:	LOW/MIN	MID	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	80	80	80	80
0x36	F6	F6	F6	F6
0x38	24	24	2C	20
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-6. Complete Register Sets for 1024x768 Input—PAL-M Video Outputs (2 of 4)

MODE	1024x768 PAL-M			
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	71	52	35	83
0x4C	D3	B9	A1	E1
0x4E	13	13	13	13
0x50	71	52	35	83
0x52	D3	B9	A1	E1
0x54	13	13	13	13
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	7F	4	A2	57
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	F8	60	C8	C0
0x78	0	0	0	0
0x7A	D0	D8	E0	CC
0x7C	0	0A	13	FB
0x7E	F0	FE	0A	E8
0x80	37	71	AC	17
0x82	21	24	28	1C

Table F-6. Complete Register Sets for 1024x768 Input—PAL-M Video Outputs (3 of 4)

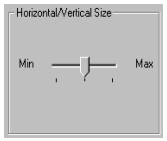
MODE	1024x768 PAL-M			
0x84	D7	D0	C8	E1
0x86	4A	4B	4B	4A
0x88	00	00	00	00
0x8A	92	98	92	B4
0x8C	7F	85	7F	9D
0x8E	04	04	04	04
0x90	B1	CF	F7	84
0x92	73	82	96	5C
0x94	0	0	0	0
0x96	0F	0F	0F	0F
0x98	9A	6E	DE	DB
0x9A	A9	AB	AD	A6
0x9C	5D	A3	E9	FC
0x9E	74	8B	A2	DD
0xA0	1D	1E	1F	1C
0xA2	2A	2A	2A	2A
0xA4	F0	F0	F0	F0
0xA6	56	56	56	56
0xA8	7E	7E	7E	7E
0xAA	47	47	47	47
0xAC	8C	8C	8C	8C
0xAE	7D	A6	13	8F
0xB0	CB	5F	4	B8
0xB2	B7	FA	4A	23
0xB4	14	13	13	15
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: **0xBA**	00	00	00	00
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00
0xC2	00	00	00	00

Table F-6. Complete Register Sets for 1024x768 Input—PAL-M Video Outputs *(4 of 4)*

MODE	1024x768 PAL-M			
LSb helps to control interface: **0xC4**	01	01	01	01
Several interface bits here: **0xC6**	80	80	80	80
Many Standard Flicker Filter(FF) bits here: 0xC8	80	80	80	80
Brightness Bits Found Here: 0xCA	C3	C3	C3	C3
Saturation Bits Found Here: 0xCC	C2	C2	C2	C2
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

Table F-7. Comments on Why Different Register Values Are Necessary for NTSC-M versus PAL-M Video Outputs *(1 of 5)*

MODE	NTSC-M vs. PAL-M
Purpose of mode:	
Active Resolution:	
Auto Configuration Mode # used:	
Horizontal Overscan Comp (HOC):	
Vertical Overscan Comp (VOC):	
Input Format	
Type of Clock:	
Type of Interface:	
Number of active pixels/line(H_ACTIVE)	
Number of active lines/frame(V_ACTIVEI)	
H_CLKI = HTOTAL(pixels)	
VLINES_I = VTOTAL(lines)	
H_BLANKI = Horizontal Blanking Region(pixels)	
V_BLANKI = Vertical Blanking Region(lines)	
Frequency of CLK (MHz)	
Type of Video Output:	
TV Out Size:	
[CX25874/5 register addresses]	
Read Only: 0x00	
Read Only: 0x02	
Read Only: 0x04	
Read Only: 0x06	
0x2E	
0x30	
0x32	
0x34	Adaptive FF set up optimally for all modes. Many Adaptive FF bits here.
0x36	Adaptive FF optimal settings the same for 640x480 NTSC & PAL-M, 800x600 NTSC & PAL-M, and 1024x768 NTSC & PAL-M
0x38	HBURST_BEGIN[8] changes
0x3A	
0x3C	

Table F-7. Comments on Why Different Register Values Are Necessary for NTSC-M versus PAL-M Video Outputs *(2 of 5)*

MODE	NTSC-M vs. PAL-M
0x3E	
0x40	
0x42	
0x44	
0x46	
0x48	
0x4A	
0x4C	
0x4E	
0x50	
0x52	
0x54	
0x56	
0x58	
0x5A	
0x5C	Hue Adjust register
0x5E	
0x60	
0x62	
0x64	
0x66	
0x68	
0x6A	
0x6C	
0x6E	

Table F-7. Comments on Why Different Register Values Are Necessary for NTSC-M versus PAL-M Video Outputs *(3 of 5)*

MODE	NTSC-M vs. PAL-M
0x70	
0x72	
0x74	
0x76	
0x78	
0x7A	
0x7C	HBURST_BEGIN later for PAL-M.Burst Start = 5.80 us. after analog leading SYNC* edge
0x7E	HBURST_END later for PAL-M. Burst End for M= 8.32 us analog leading SYNC* edge
0x80	H_BLANKO[7:0]
0x82	
0x84	
0x86	
0x88	
0x8A	
0x8C	
0x8E	
0x90	
0x92	
0x94	
0x96	
0x98	
0x9A	
0x9C	PLL_FRACT[7:0]
0x9E	
0xA0	

Table F-7. Comments on Why Different Register Values Are Necessary for NTSC-M versus PAL-M Video Outputs (4 of 5)

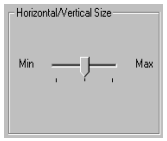
MODE	NTSC-M vs. PAL-M
0xA2	PAL_MD bit enabled for PAL-M. VSYNC duration 3.0 lines for PAL-M. 7.5 IRE setup on for PAL-M. 625 line bit disabled.
0xA4	Sync amplitude for PAL-M slightly greater.
0xA6	Minor change in burst amplitude. Negligible effect.
0xA8	Tiny change in multiplication factor for Cr. Negligible effect.
0xAA	Tiny change in multiplication factor for Cb. Negligible effect.
0xAC	Tiny change in multiplication factor for Y. Negligible effect.
0xAE	Least significant byte of Subcarrier increment. MSC[7:0] different for PAL-M or NTSC-M
0xB0	MSC[15:8] different for PAL-M or NTSC-M. Used in conjunction with PLL_INT, and PLL_FRACT to
0xB2	change FSC from 3.579545 MHz.(NTSC) to 3.5761 MHz.(PAL-M).
0xB4	This byte is MSC[31:24]
0xB6	
AUTO CONFIG register: 0xB8	**THIS IS THE AUTO-CONFIGURATION bit fields. DO NOT PROGRAM OR YOU WILL OVERWRITE bit fields VALUES FROM 0X00 TO 0XB6 WITH NEW, UNWANTED VALUES.**
bit5 helps to control interface: **0xBA**	Master interface. SLAVER bit = 0
0xBC	
0xBE	
0xC0	
0xC2	
LSb helps to control interface: **0xC4**	Encoder set up for master interface right now. EN_OUT = 1, CLKO and other outputs enabled.
Several interface bits here: **0xC6**	EN_BLANKO = 1, EN_DOT = 0, 24bit multiplexed RGB input format.
Many Standard Flicker Filter(FF) bits here: 0xC8	DIS_YFLPF = 1, Std. Flicker Filter = 3line for 640x480, 4line for 800x600, 5line for 1024x768
Brightness Bits Found Here: 0xCA	YATTEN = Brightness = 3/4 gain for all sets.
Saturation Bits Found Here: 0xCC	CATTEN = Saturation = 7/8 gain for all sets.

Table F-7. Comments on Why Different Register Values Are Necessary for NTSC-M versus PAL-M Video Outputs *(5 of 5)*

MODE	NTSC-M vs. PAL-M
DAC Routing Controlled Here: 0xCE	DAC routing may need to be adjusted for customer's particular set of outputs. This configures DAC Deaf CX25875 used) = Composite #1, DAC C = Luma, DAC B = Chroma, and DACA = Composite #2
0xD0	
0xD2	
0xD4	
0xD6	
Text Sharpener bits here: 0xD8	BY_YCCR = 1, Text Sharpener bits found here.PKFIL = 10 for 2 dB gain

Key:
Bold Text Denotes registers that are reprogrammed to establish different interfaces(master, pseudo-master, or slave)
Denotes register values that change from NTSC-M output format to PAL-M output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN setting.
MID OVERSCAN for MID setting.
MAX OVERSCAN for MAX setting.
At least 3 overscan solutions are included for every mode.



GENERAL NOTE: NTSC-J solutions are not listed separately from NTSC-M. All that is required to come up with an optimal register set for a NTSC-J output for Japan is to program the desired NTSC-M register set into the encoder and then turn off the setup bit within the encoder. This is bit 1 of register 0xA2.

F.2 640x480, 800x600, and 1024x768 PAL-B, D, G, H, I, N, and Nc Register Sets

To assist the software engineer in enabling TV Out with various custom overscan ratios, Conexant has compiled Tables F-8 through F-17. This table contains fully tested and working PAL-B, -D, -G, -H, -I, -N, -Nc register sets for the three major desktop resolutions: 640x480, 800x600, and 1024x768. Some of these register sets are based on autoconfiguration modes and some are purely custom solutions. Note that each desktop resolution is supported with no less than four register sets corresponding to different overscan ratios that vary by approximately ±2 percent overscan compensation.

The default digital input format for the CX25874/5 will be IN_MODE[3:0] = 0000 = 24-bit RGB multiplexed and this is reflected in the table. Changing the encoder over to expect a different input format requires that the designer write a nonzero value to the IN_MODE[3:0] field. If this is necessary, perform this step after the entire register set has been programmed into the encoder.

Descriptions of many of the registers and bits are included in the last column within the spreadsheet itself.

Other settings shared by these register sets are as follows:

- Adaptive Flicker Filter has been programmed optimally for the specific input resolution.
- Physical interface used by the encoder is Master Interface with a BLANK* Input. This is not the default pseudo-master interface commonly used with the CX25874/5. The different interfaces are explained in the Autoconfiguration and Interface Bits section.
- SLAVE bit = 0. The state of the SLAVE bit dictates whether the CX25874/5 is the timing master or timing slave by controlling the direction of the HSYNC* and VSYNC* ports. Since SLAVE = 0, the syncs will be generated by the encoder and sent to the master device.
- EN_OUT = 1 ensuring CLKO and other outputs enabled from the encoder.
- EN_BLANKO is high (=1), signifying the CX25874/5's BLANK* port is an output or that NO BLANK* signal is used as part of the system.
- EN_DOT = 0 telling the CX25874/5 to use its internal counters to determine the active versus the blanking regions.
- DAC routing configures DAC C as Luma, DAC B as Chroma, and DACA as Composite outputs. The DAC routing through register CE may need to be adjusted for each customer's particular set of outputs.
- Register 0xB8 is the Autoconfiguration register. Do not program this or you will overwrite register values from 0x00 to 0xB6 with new, unwanted values.

The end user of any of these register sets may need to change various interface bits to make the CX25874/5 work with the particular GPU or master device it is connected to. If you wish the encoder to be in pseudo-master interface, as explained in the Autoconfiguration and Interface Bits section, then you will need to reprogram the SLAVE(bit 5 of 0xBA), EN_BLANKO(MSb of register 0xC6), EN_DOT(bit 6 of register 0xC6), and EN_OUT(LSb of register 0xC4) bits to the required values.

In addition to the register sets above, it is suggested that interested designers alter these video-quality centric register values tested to yield the best 640x480 PAL

picture quality into their software driver. Similar settings can be used for 800x600 and 1024x768 resolutions.

- Reg 0x34 = Adaptive FF register 1 on
- Reg 0x36 = Adaptive FF register 2 on
- Reg 0x96. CLPF[1:0] = bypass, YLPF[1:0] = bypass
- Reg 0xC8. DIS_YFLPF = 1= Enabled. Std. Y&C Flicker Filter set appropriately.
- Reg 0xCA = C2 so YATTEN = Brightness/Contrast switched to 7/8 gain.
- Reg 0xCC = C1 so CATTEN = Saturation = 15/16 gain.
- Reg 0xD8 = 60 so CHROMA_BW = off, BY_YCCR ON, PK_FIL = 10 for 2 dB gain

Consult Section 1.3.21 for more programming instructions. It is not possible to reprogram only the encoder to enable a new TV Out solution. To achieve VGA compatibility, the controller must manipulate some of its own VGA register settings in order to produce a hi-quality dual display on both the computer monitor and TV. It should be noted that the encoder has no way of knowing that a different VGA mode has been selected. As a result, it relies on the serial bus master device to reconfigure it via an autoconfiguration mode or complete register set rewrite to make adjustments in its timing.

When the two devices are programmed correctly, regardless of the interface, the required input HSYNC*/VSYNC* to first input active pixel or line spacing matches the output HSYNC*/VSYNC* to first output active pixel or line spacing. When this occurs, the graphics controller always transmits active data at the time the CX25874/5 expects to receive it. Superior TV Out quality is achieved only when this type of timing symmetry exists.

Table F-8. Complete Register Sets for 640x480 Input—PAL-BDGHI Video Outputs *(1 of 4)*

MODE	640x480 PAL-BDGHI			
Purpose of mode:	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output
Active Resolution:	640x480 Default = MID OVERSCAN	640x480 MIN OVERSCAN	640x480 MAX OVERSCAN	640x480 LOWEST OVERSCAN
Auto Configuration Mode # used:	1	17	33	Custom
Horizontal Overscan Comp (HOC):	16.56	13.63	20.27	9.88
Vertical Overscan Comp (VOC):	16.67	13.19	19.79	9.38
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	640	640	640	640
Number of active lines/frame(V_ACTIVEI)	480	480	480	480
H_CLKI = HTOTAL(pixels)	944	950	950	950
VLINES_I = VTOTAL(lines)	625	600	650	575
H_BLANKI = Horizontal Blanking Region(pixels)	266	271	271	271
V_BLANKI = Vertical Blanking Region(lines)	90	76	104	64
Frequency of CLK (MHz)	29.500008	28.500011	30.875015	27.312492
Type of Video Output:	PAL-BDGHI	PAL-BDGHI	PAL-BDGHI	PAL-BDGHI
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	9B	9B	9B	9B
0x36	E4	E4	E4	E4
0x38	00	00	00	00
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-8. Complete Register Sets for 640x480 Input—PAL-BDGHI Video Outputs *(2 of 4)*

MODE	640x480 PAL-BDGHI			
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	28	57	ED	92
0x4C	3B	61	0A	91
0x4E	25	25	24	25
0x50	28	57	ED	92
0x52	3B	61	0A	91
0x54	25	25	24	25
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	3C	98	51	D7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	20	B8	D4
0x78	80	80	80	80
0x7A	8A	86	92	80
0x7C	A6	A0	AC	98
0x7E	68	60	72	56
0x80	C1	9D	F3	71
0x82	2E	29	33	24

Table F-8. Complete Register Sets for 640x480 Input—PAL-BDGHI Video Outputs *(3 of 4)*

MODE	640x480 PAL-BDGHI			
0x84	F2	FC	E9	07
0x86	27	27	27	A6
0x88	00	00	00	00
0x8A	B0	B6	B6	B6
0x8C	0A	0F	0F	0F
0x8E	0B	0B	0B	0B
0x90	71	58	8A	3F
0x92	5A	4C	68	40
0x94	E0	E0	E0	E0
0x96	06	06	06	06
0x98	00	B8	48	71
0x9A	50	4E	51	4D
0x9C	72	AB	E4	8E
0x9E	1C	AA	B8	23
0xA0	0D	0C	0D	0C
0xA2	24	24	24	24
0xA4	F0	F0	F0	F0
0xA6	58	58	58	59
0xA8	81	82	81	82
0xAA	49	49	48	49
0xAC	8C	8C	8C	8C
0xAE	0C	2C	3D	92
0xB0	8C	25	E7	69
0xB2	79	D3	C2	8E
0xB4	26	27	24	29
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*	*00*
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00

Table F-8. Complete Register Sets for 640x480 Input—PAL-BDGHI Video Outputs *(4 of 4)*

MODE	640x480 PAL-BDGHI			
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	92	92	92	92
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

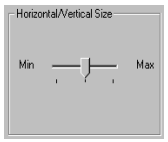


Table F-9. Complete Register Sets for 640x480 Input—PAL-Nc Video Outputs (1 of 4)

MODE	640x480 PAL-Nc			
Purpose of mode:	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output
Active Resolution:	640x480 Default = MID OVERSCAN	640x480 MIN OVERSCAN	640x480 MAX OVERSCAN	640x480 LOWEST OVERSCAN
Auto Configuration Mode # used:	47	17	33	Custom
Horizontal Overscan Comp (HOC):	16.56	13.63	20.27	9.88
Vertical Overscan Comp (VOC):	16.67	13.19	19.79	9.38
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	640	640	640	640
Number of active lines/frame(V_ACTIVEI)	480	480	480	480
H_CLKI = HTOTAL(pixels)	944	950	950	950
VLINES_I = VTOTAL(lines)	625	600	650	575
H_BLANKI = Horizontal Blanking Region(pixels)	266	271	271	271
V_BLANKI = Vertical Blanking Region(lines)	90	76	104	64
Frequency of CLK (MHz)	29.500008	28.500011	30.875015	27.312492
Type of Video Output:	PAL-Nc	PAL-Nc	PAL-Nc	PAL-Nc
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	9B	9B	9B	9B
0x36	E4	E4	E4	E4
0x38	00	00	00	00
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-9. Complete Register Sets for 640x480 Input—PAL-Nc Video Outputs (2 of 4)

MODE	640x480 PAL-Nc			
0x42	0	0	0	0
0x44	0	0	0	0
0x46	0	0	0	0
0x48	0	0	0	0
0x4A	28	57	ED	92
0x4C	3B	61	0A	91
0x4E	25	25	24	25
0x50	28	57	ED	92
0x52	3B	61	0A	91
0x54	25	25	24	25
0x56	0	0	0	0
0x58	0	0	0	0
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	3C	98	51	D7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	20	B8	D4
0x78	80	80	80	80
0x7A	8A	86	92	80
0x7C	A6	A0	AC	98
0x7E	70	68	7A	5E
0x80	C1	9D	F3	71
0x82	2E	29	33	24

Table F-9. Complete Register Sets for 640x480 Input—PAL-Nc Video Outputs *(3 of 4)*

MODE	640x480 PAL-Nc			
0x84	F2	FC	E9	7
0x86	27	27	27	A6
0x88	00	00	00	00
0x8A	B0	B6	B6	B6
0x8C	0A	0F	0F	0F
0x8E	0B	0B	0B	0B
0x90	71	58	8A	3F
0x92	5A	4C	68	40
0x94	E0	E0	E0	E0
0x96	06	06	06	06
0x98	00	B8	48	71
0x9A	50	4E	51	4D
0x9C	72	AB	E4	8E
0x9E	1C	AA	B8	23
0xA0	0D	0C	0D	0C
0xA2	24	24	24	24
0xA4	F0	F0	F0	F0
0xA6	57	57	57	57
0xA8	80	80	7F	80
0xAA	48	48	48	48
0xAC	8C	8C	8C	8C
0xAE	1E	43	51	51
0xB0	C0	F8	5B	19
0xB2	15	2C	B3	93
0xB4	1F	20	1D	21
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*	*00*
0xBC	00	00	00	00

Table F-9. Complete Register Sets for 640x480 Input—PAL-Nc Video Outputs *(4 of 4)*

MODE	640x480 PAL-Nc			
0xBE	00	00	00	00
0xC0	00	00	00	00
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	92	92	92	92
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:

Denotes register values that change for the different PAL output formats.

Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).

Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:

Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

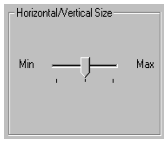


Table F-10. Complete Register Sets for 640x480 Input—PAL-N Video Outputs *(1 of 4)*

MODE	640x480 PAL-N			
Purpose of mode:	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output
Active Resolution:	640x480 Default = MID OVERSCAN	640x480 MIN OVERSCAN	640x480 MAX OVERSCAN	640x480 LOWEST OVERSCAN
Auto Configuration Mode # used:	1	17	33	Custom
Horizontal Overscan Comp (HOC):	16.56	13.63	20.27	9.88
Vertical Overscan Comp (VOC):	16.67	13.19	19.79	9.38
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	640	640	640	640
Number of active lines/frame(V_ACTIVEI)	480	480	480	480
H_CLKI = HTOTAL(pixels)	944	950	950	950
VLINES_I = VTOTAL(lines)	625	600	650	575
H_BLANKI = Horizontal Blanking Region(pixels)	266	271	271	271
V_BLANKI = Vertical Blanking Region(lines)	90	76	104	64
Frequency of CLK (MHz)	29.500008	28.500011	30.875015	27.312492
Type of Video Output:	PAL-N	PAL-N	PAL-N	PAL-N
TV Out Size:	MID	LOW/MIN	HI/MAX	
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	9B	9B	9B	9B
0x36	E4	E4	E4	E4
0x38	00	00	00	00
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-10. Complete Register Sets for 640x480 Input—PAL-N Video Outputs *(2 of 4)*

MODE	640x480 PAL-N			
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	28	57	ED	92
0x4C	3B	61	0A	91
0x4E	25	25	24	25
0x50	28	57	ED	92
0x52	3B	61	0A	91
0x54	25	25	24	25
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	3C	98	51	D7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	20	B8	D4
0x78	80	80	80	80
0x7A	8B	86	91	80
0x7C	A5	A0	AD	99
0x7E	68	60	72	56
0x80	AB	87	DD	5D
0x82	2E	29	33	24

Table F-10. Complete Register Sets for 640x480 Input—PAL-N Video Outputs *(3 of 4)*

MODE	640x480 PAL-N			
0x84	F2	FC	E9	07
0x86	27	27	27	A6
0x88	00	00	00	00
0x8A	B0	B6	B6	B6
0x8C	0A	0F	0F	0F
0x8E	0B	0B	0B	0B
0x90	71	58	8A	3F
0x92	5A	4C	68	40
0x94	E0	E0	E0	E0
0x96	06	06	06	06
0x98	00	B8	48	71
0x9A	50	4E	51	4D
0x9C	72	AB	E4	8E
0x9E	1C	AA	B8	23
0xA0	0D	0C	0D	0C
0xA2	2E	2E	2E	2E
0xA4	F0	F0	F0	F0
0xA6	58	58	58	59
0xA8	81	82	81	82
0xAA	49	49	48	49
0xAC	8C	8C	8C	8C
0xAE	0C	2C	3D	92
0xB0	8C	25	E7	69
0xB2	79	D3	C2	8E
0xB4	26	27	24	29
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*	*00*
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00

Table F-10. Complete Register Sets for 640x480 Input—PAL-N Video Outputs *(4 of 4)*

MODE	640x480 PAL-N			
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	92	92	92	92
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

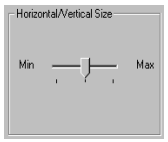


Table F-11. Complete Register Sets for 800x600 Input—PAL-BDGHI Video Outputs *(1 of 4)*

MODE	800x600 PAL-BDGHI		
Purpose of mode:	Complete CX25875 Reg. Set for NTSC output	Complete CX25875 Reg. Set for NTSC output	Complete CX25875 Reg. Set for NTSC output
Active Resolution:	800x600 Default = MID OVERSCAN	800x600 = MIN OVERSCAN	800x600 = MAX OVERSCAN
Auto Configuration Mode # used:	19	3	35
Horizontal Overscan Comp (HOC):	16.42	14.52	19.03
Vertical Overscan Comp (VOC):	15.97	13.19	18.40
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Character or Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	800	800	800
Number of active lines/frame(V_ACTIVEI)	600	600	600
H_CLKI = HTOTAL(pixels)	950	960	950
VLINES_I = VTOTAL(lines)	775	750	800
H_BLANKI = Horizontal Blanking Region(pixels)	131	140	131
V_BLANKI = Vertical Blanking Region(lines)	109	95	122
Frequency of CLK (MHz)	36.812507	36.000000	37.999992
Type of Video Output:	PAL-BDGHI	PAL-BDGHI	PAL-BDGHI
TV Out Size:	MID	LOW/MIN	HI/MAX
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00
Read Only: 0x02	00	00	00
Read Only: 0x04	00	00	00
Read Only: 0x06	00	00	00
0x2E	00	00	00
0x30	00	00	00
0x32	00	00	00
0x34	80	80	80
0x36	D2	D2	D2
0x38	00	00	00
0x3A	00	00	00
0x3C	80	80	80
0x3E	80	80	80

Table F-11. Complete Register Sets for 800x600 Input—PAL-BDGHI Video Outputs *(2 of 4)*

MODE	800x600 PAL-BDGHI		
0x40	80	80	80
0x42	00	00	00
0x44	00	00	00
0x46	00	00	00
0x48	00	00	00
0x4A	22	3A	1
0x4C	63	77	48
0x4E	1C	1C	1C
0x50	22	3A	1
0x52	63	77	48
0x54	1C	1C	1C
0x56	00	00	00
0x58	00	00	00
0x5A	00	00	00
0x5C	00	00	00
0x5E	00	00	00
0x60	00	00	00
0x62	00	00	00
0x64	00	00	00
0x66	55	E3	F2
0x68	00	00	00
0x6A	00	00	00
0x6C	46	46	46
0x6E	00	00	00
0x70	0F	0F	0F
0x72	00	00	00
0x74	01	01	01
0x76	34	00	80
0x78	20	20	20
0x7A	AE	AA	B2
0x7C	CE	CA	D4
0x7E	A0	9A	AA
0x80	2B	0D	57

Table F-11. Complete Register Sets for 800x600 Input—PAL-BDGHI Video Outputs *(3 of 4)*

MODE	800x600 PAL-BDGHI		
0x82	2D	29	31
0x84	F4	FC	EC
0x86	39	39	39
0x88	00	00	00
0x8A	B6	C0	B6
0x8C	83	8C	83
0x8E	03	03	03
0x90	7	EE	20
0x92	6D	5F	7A
0x94	58	58	58
0x96	0B	0A	0B
0x98	AE	66	F6
0x9A	97	96	98
0x9C	72	0	8E
0x9E	5C	0	E3
0xA0	10	10	10
0xA2	24	24	24
0xA4	F0	F0	F0
0xA6	57	57	57
0xA8	80	80	7F
0xAA	48	48	48
0xAC	8C	8C	8C
0xAE	1	18	E1
0xB0	4	28	5B
0xB2	D5	87	DE
0xB4	1E	1F	1D
0xB6	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*
0xBC	00	00	00
0xBE	00	00	00

Table F-11. Complete Register Sets for 800x600 Input—PAL-BDGHI Video Outputs *(4 of 4)*

MODE	800x600 PAL-BDGHI		
0xC0	00	00	00
0xC2	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	9B	9B	9B
Brightness Bits Found Here: 0xCA	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18
0xD0	00	00	00
0xD2	00	00	00
0xD4	00	00	00
0xD6	00	00	00
Text Sharpener bits here: 0xD8	60	60	60

Key:
Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

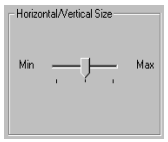


Table F-12. Complete Register Sets for 800x600 Input—PAL-Nc Video Outputs *(1 of 4)*

MODE	800x600 PAL-Nc		
Purpose of mode:	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output
Active Resolution:	800x600 Default = MID OVERSCAN	800x600 = MIN OVERSCAN	800x600 = MAX OVERSCAN
Auto Configuration Mode # used:	19	3	35
Horizontal Overscan Comp (HOC):	16.42	14.52	19.03
Vertical Overscan Comp (VOC):	15.97	13.19	18.40
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Character or Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	800	800	800
Number of active lines/frame(V_ACTIVEI)	600	600	600
H_CLKI = HTOTAL(pixels)	950	960	950
VLINES_I = VTOTAL(lines)	775	750	800
H_BLANKI = Horizontal Blanking Region(pixels)	131	140	131
V_BLANKI = Vertical Blanking Region(lines)	109	95	122
Frequency of CLK (MHz)	36.812507	36.000000	37.999992
Type of Video Output:	PAL-Nc	PAL-Nc	PAL-Nc
TV Out Size:	MID	LOW/MIN	HI/MAX
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00
Read Only: 0x02	00	00	00
Read Only: 0x04	00	00	00
Read Only: 0x06	00	00	00
0x2E	00	00	00
0x30	00	00	00
0x32	00	00	00
0x34	80	80	80
0x36	D2	D2	D2
0x38	00	00	00
0x3A	00	00	00
0x3C	80	80	80
0x3E	80	80	80
0x40	80	80	80

Table F-12. Complete Register Sets for 800x600 Input—PAL-Nc Video Outputs (2 of 4)

MODE	800x600 PAL-Nc		
0x42	0	0	0
0x44	0	0	0
0x46	0	0	0
0x48	0	0	0
0x4A	22	3A	1
0x4C	63	77	48
0x4E	1C	1C	1C
0x50	22	3A	1
0x52	63	77	48
0x54	1C	1C	1C
0x56	0	0	0
0x58	0	0	0
0x5A	00	00	00
0x5C	00	00	00
0x5E	00	00	00
0x60	00	00	00
0x62	00	00	00
0x64	00	00	00
0x66	55	E3	F2
0x68	00	00	00
0x6A	00	00	00
0x6C	46	46	46
0x6E	00	00	00
0x70	0F	0F	0F
0x72	00	00	00
0x74	01	01	01
0x76	34	00	80
0x78	20	20	20
0x7A	AE	AA	B2
0x7C	CE	CA	D4
0x7E	AA	A4	B4
0x80	2B	0D	57
0x82	2D	29	31

Table F-12. Complete Register Sets for 800x600 Input—PAL-Nc Video Outputs *(3 of 4)*

MODE	800x600 PAL-Nc		
0x84	F4	FC	EC
0x86	39	39	39
0x88	00	00	00
0x8A	B6	C0	B6
0x8C	83	8C	83
0x8E	03	03	03
0x90	7	EE	20
0x92	6D	5F	7A
0x94	58	58	58
0x96	0B	0A	0B
0x98	AE	66	F6
0x9A	97	96	98
0x9C	72	0	8E
0x9E	5C	0	E3
0xA0	10	10	10
0xA2	24	24	24
0xA4	F0	F0	F0
0xA6	56	56	56
0xA8	7F	7F	7E
0xAA	47	47	47
0xAC	8C	8C	8C
0xAE	44	35	32
0xB0	2	EF	BA
0xB2	E9	78	21
0xB4	18	19	18
0xB6	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*
0xBC	00	00	00
0xBE	00	00	00
0xC0	00	00	00

Table F-12. Complete Register Sets for 800x600 Input—PAL-Nc Video Outputs *(4 of 4)*

MODE	800x600 PAL-Nc		
0xC2	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	9B	9B	9B
Brightness Bits Found Here: 0xCA	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18
0xD0	00	00	00
0xD2	00	00	00
0xD4	00	00	00
0xD6	00	00	00
Text Sharpener bits here: 0xD8	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

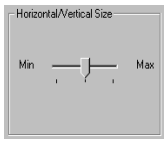


Table F-13. Complete Register Sets for 800x600 Input—PAL-N Video Outputs *(1 of 4)*

MODE	800x600 PAL-N		
Purpose of mode:	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output
Active Resolution:	800x600 Default = MID OVERSCAN	800x600 = MIN OVERSCAN	800x600 = MAX OVERSCAN
Auto Configuration Mode # used:	19	3	35
Horizontal Overscan Comp (HOC):	16.42	14.52	19.03
Vertical Overscan Comp (VOC):	15.97	13.19	18.40
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Pixel	Character or Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	800	800	800
Number of active lines/frame(V_ACTIVEI)	600	600	600
H_CLKI = HTOTAL(pixels)	950	960	950
VLINES_I = VTOTAL(lines)	775	750	800
H_BLANKI = Horizontal Blanking Region(pixels)	131	140	131
V_BLANKI = Vertical Blanking Region(lines)	109	95	122
Frequency of CLK (MHz)	36.812507	36.000000	37.999992
Type of Video Output:	PAL-N	PAL-N	PAL-N
TV Out Size:	MID	LOW/MIN	HI/MAX
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00
Read Only: 0x02	00	00	00
Read Only: 0x04	00	00	00
Read Only: 0x06	00	00	00
0x2E	00	00	00
0x30	00	00	00
0x32	00	00	00
0x34	80	80	80
0x36	D2	D2	D2
0x38	00	00	00
0x3A	00	00	00
0x3C	80	80	80
0x3E	80	80	80
0x40	80	80	80

Table F-13. Complete Register Sets for 800x600 Input—PAL-N Video Outputs (2 of 4)

MODE	800x600 PAL-N		
0x42	0	0	0
0x44	0	0	0
0x46	0	0	0
0x48	0	0	0
0x4A	22	3A	1
0x4C	63	77	48
0x4E	1C	1C	1C
0x50	22	3A	1
0x52	63	77	48
0x54	1C	1C	1C
0x56	0	0	0
0x58	0	0	0
0x5A	00	00	00
0x5C	00	00	00
0x5E	00	00	00
0x60	00	00	00
0x62	00	00	00
0x64	00	00	00
0x66	55	E3	F2
0x68	00	00	00
0x6A	00	00	00
0x6C	46	46	46
0x6E	00	00	00
0x70	0F	0F	0F
0x72	00	00	00
0x74	01	01	01
0x76	34	00	80
0x78	20	20	20
0x7A	AD	A9	B3
0x7C	CE	CA	D5
0x7E	A1	9B	AA
0x80	0F	F3	3B
0x82	2D	29	31

Table F-13. Complete Register Sets for 800x600 Input—PAL-N Video Outputs *(3 of 4)*

MODE	800x600 PAL-N		
0x84	F4	FC	EC
0x86	39	39	39
0x88	00	00	00
0x8A	B6	C0	B6
0x8C	83	8C	83
0x8E	03	03	03
0x90	7	EE	20
0x92	6D	5F	7A
0x94	58	58	58
0x96	0B	0A	0B
0x98	AE	66	F6
0x9A	97	56	98
0x9C	72	0	8E
0x9E	5C	0	E3
0xA0	10	10	10
0xA2	2E	2E	2E
0xA4	F0	F0	F0
0xA6	57	57	57
0xA8	80	80	7F
0xAA	48	48	48
0xAC	8C	8C	8C
0xAE	1	18	E1
0xB0	4	28	5B
0xB2	D5	87	DE
0xB4	1E	1F	1D
0xB6	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*
0xBC	00	00	00
0xBE	00	00	00
0xC0	00	00	00

Table F-13. Complete Register Sets for 800x600 Input—PAL-N Video Outputs *(4 of 4)*

MODE	800x600 PAL-N		
0xC2	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	9B	9B	9B
Brightness Bits Found Here: 0xCA	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18
0xD0	00	00	00
0xD2	00	00	00
0xD4	00	00	00
0xD6	00	00	00
Text Sharpener bits here: 0xD8	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

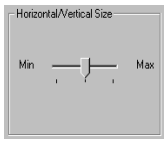


Table F-14. Complete Register Sets for 1024x768 Input—PAL-BDGHI Video Outputs *(1 of 4)*

MODE	1024x768 PAL-BDGHI			
Purpose of mode:	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output	CX25875 Reg. Set for PAL-BDGHI output
Active Resolution:	1024x768 Should Be Default = MIN OVERSCAN	1024x768 = MID OVERSCAN	1024x768 = MAX OVERSCAN	1024x768 Should Be Default = MIN OVERSCAN
Auto Configuration Mode # used:	11	43	Custom	Custom
Horizontal Overscan Comp (HOC):	13.44	16.20	19.62	10.23
Vertical Overscan Comp (VOC):	14.24	16.67	20.49	14.24
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	1024	1024	1024	1024
Number of active lines/frame(V_ACTIVEI)	768	768	768	768
H_CLKI = HTOTAL(pixels)	1400	1410	1400	1350
VLINES_I = VTOTAL(lines)	975	1000	1050	975
H_BLANKI = Horizontal Blanking Region(pixels)	329	337	329	285
V_BLANKI = Vertical Blanking Region(lines)	131	147	171	131
Frequency of CLK (MHz)	68.249988	70.499988	73.500011	65.8125
Type of Video Output:	PAL-BDGHI	PAL-BDGHI	PAL-BDGHI	PAL-BDGHI
TV Out Size:	MID	HI/MAX	ALTERNATE	LOW/MIN
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	80	80	80	80
0x36	F6	F6	F6	F6
0x38	20	24	2E	20
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80

Table F-14. Complete Register Sets for 1024x768 Input—PAL-BDGHI Video Outputs *(2 of 4)*

MODE	1024x768 PAL-BDGHI			
0x40	80	80	80	80
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	58	3C	1B	78
0x4C	BE	A7	8C	D8
0x4E	13	13	13	13
0x50	58	3C	1B	78
0x52	BE	A7	8C	D8
0x54	13	13	13	13
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	1C	BE	F5	C7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	C0	40	F8
0x78	0	0	0	0
0x7A	D6	DC	E6	CE
0x7C	FE	8	12	F6
0x7E	E6	F0	0	D8
0x80	87	BF	7	4D

Table F-14. Complete Register Sets for 1024x768 Input—PAL-BDGHI Video Outputs *(3 of 4)*

MODE	1024x768 PAL-BDGHI			
0x82	2B	2F	34	2B
0x84	F8	F1	E6	F8
0x86	4B	4B	4C	4A
0x88	00	00	00	00
0x8A	78	82	78	46
0x8C	49	51	49	1D
0x8E	0D	0D	0D	0D
0x90	CF	E8	1A	CF
0x92	83	93	AB	83
0x94	0	0	0	0
0x96	0F	0F	0C	0F
0x98	EC	33	C3	EC
0x9A	A1	A3	E5	A1
0x9C	55	55	AB	0
0x9E	55	55	AA	40
0xA0	1E	1F	20	1D
0xA2	24	24	24	24
0xA4	F0	F0	F0	F0
0xA6	56	56	56	56
0xA8	7F	7E	7E	7F
0xAA	47	47	47	47
0xAC	8C	8C	8C	8C
0xAE	57	9B	51	CC
0xB0	F8	29	D4	7C
0xB2	F1	26	29	DE
0xB4	18	18	17	19
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*	*00*
0xBC	00	00	00	00
0xBE	00	00	00	00

Table F-14. Complete Register Sets for 1024x768 Input—PAL-BDGHI Video Outputs *(4 of 4)*

MODE	1024x768 PAL-BDGHI			
0xC0	00	00	00	00
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	80	80	80	80
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:
Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

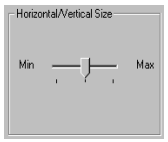


Table F-15. Complete Register Sets for 1024x768 Input—PAL-Nc Video Outputs *(1 of 4)*

MODE	1024x768 PAL-Nc			
Purpose of mode:	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output	CX25875 Reg. Set for PAL-Nc output
Active Resolution:	1024x768 Default = MIN OVERSCAN	1024x768 = MID OVERSCAN	1024x768 = MAX OVERSCAN	1024x768 = MAX OVERSCAN
Auto Configuration Mode # used:	11	43	Custom	Custom
Horizontal Overscan Comp (HOC):	13.44	16.20	19.62	10.23
Vertical Overscan Comp (VOC):	14.24	16.67	20.49	14.24
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	1024	1024	1024	1024
Number of active lines/frame(V_ACTIVEI)	768	768	768	768
H_CLKI = HTOTAL(pixels)	1400	1410	1400	1350
VLINES_I = VTOTAL(lines)	975	1000	1050	975
H_BLANKI = Horizontal Blanking Region(pixels)	329	337	329	285
V_BLANKI = Vertical Blanking Region(lines)	131	147	171	131
Frequency of CLK (MHz)	68.249988	70.499988	73.500011	65.8125
Type of Video Output:	PAL-Nc	PAL-Nc	PAL-Nc	PAL-Nc
TV Out Size:	MID	HI/MAX		LOW/MIN
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	80	80	80	80
0x36	F6	F6	F6	F6
0x38	20	24	2E	20
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-15. Complete Register Sets for 1024x768 Input—PAL-Nc Video Outputs (2 of 4)

MODE	1024x768 PAL-Nc			
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	58	3C	1B	78
0x4C	BE	A7	8C	D8
0x4E	13	13	13	13
0x50	58	3C	1B	78
0x52	BE	A7	8C	D8
0x54	13	13	13	13
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	1C	BE	F5	C7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	C0	40	F8
0x78	0	0	0	0
0x7A	D6	DC	E6	CE
0x7C	FE	8	12	F6
0x7E	F2	FE	0E	E4
0x80	87	BF	7	4D
0x82	2B	2F	34	2B

Table F-15. Complete Register Sets for 1024x768 Input—PAL-Nc Video Outputs *(3 of 4)*

MODE	1024x768 PAL-Nc			
0x84	F8	F1	E6	F8
0x86	4B	4B	4C	4A
0x88	00	00	00	00
0x8A	78	82	78	46
0x8C	49	51	49	1D
0x8E	0D	0D	0D	0D
0x90	CF	E8	1A	CF
0x92	83	93	AB	83
0x94	0	0	0	0
0x96	0F	0F	0C	0F
0x98	EC	33	C3	EC
0x9A	A1	A3	E5	A1
0x9C	55	55	AB	0
0x9E	55	55	AA	40
0xA0	1E	1F	20	1D
0xA2	24	24	24	24
0xA4	F0	F0	F0	F0
0xA6	56	56	56	56
0xA8	7E	7E	7E	7E
0xAA	47	47	47	47
0xAC	8C	8C	8C	8C
0xAE	AE	1E	FD	A2
0xB0	6B	C2	E3	82
0xB2	27	82	B6	E6
0xB4	14	13	12	14
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*00*	*00*	*00*
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00

Table F-15. Complete Register Sets for 1024x768 Input—PAL-Nc Video Outputs *(4 of 4)*

MODE	1024x768 PAL-Nc			
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	80	80	80	80
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

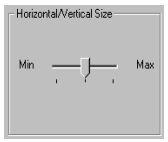


Table F-16. Complete Register Sets for 1024x768 Input—PAL-N Video Outputs *(1 of 4)*

MODE	1024x768 PAL-N			
Purpose of mode:	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output	CX25875 Reg. Set for PAL-N output
Active Resolution:	1024x768 Default = MIN OVERSCAN	1024x768 = MID OVERSCAN	1024x768 = MAX OVERSCAN	1024x768 = MAX OVERSCAN
Auto Configuration Mode # used:	11	43	Custom	Custom
Horizontal Overscan Comp (HOC):	13.44	16.20	19.62	10.23
Vertical Overscan Comp (VOC):	14.24	16.67	20.49	14.24
Input Format	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed	24bit RGB multiplexed
Type of Clock:	Character or Pixel	Pixel	Pixel	Pixel
Type of Interface:	CX25875 as Master	CX25875 as Master	CX25875 as Master	CX25875 as Master
Number of active pixels/line(H_ACTIVE)	1024	1024	1024	1024
Number of active lines/frame(V_ACTIVEI)	768	768	768	768
H_CLKI = HTOTAL(pixels)	1400	1410	1400	1350
VLINES_I = VTOTAL(lines)	975	1000	1050	975
H_BLANKI = Horizontal Blanking Region(pixels)	329	337	329	285
V_BLANKI = Vertical Blanking Region(lines)	131	147	171	131
Frequency of CLK (MHz)	68.249988	70.499988	73.500011	65.8125
Type of Video Output:	PAL-N	PAL-N	PAL-N	PAL-N
TV Out Size:	MID	HI/MAX		LOW/MIN
[CX25874/5 register addresses]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]	[CX25874/5 register values]
Read Only: 0x00	00	00	00	00
Read Only: 0x02	00	00	00	00
Read Only: 0x04	00	00	00	00
Read Only: 0x06	00	00	00	00
0x2E	00	00	00	00
0x30	00	00	00	00
0x32	00	00	00	00
0x34	80	80	80	80
0x36	F6	F6	F6	F6
0x38	20	24	2E	20
0x3A	00	00	00	00
0x3C	80	80	80	80
0x3E	80	80	80	80
0x40	80	80	80	80

Table F-16. Complete Register Sets for 1024x768 Input—PAL-N Video Outputs (2 of 4)

MODE	1024x768 PAL-N			
0x42	00	00	00	00
0x44	00	00	00	00
0x46	00	00	00	00
0x48	00	00	00	00
0x4A	58	3C	1B	78
0x4C	BE	A7	8C	D8
0x4E	13	13	13	13
0x50	58	3C	1B	78
0x52	BE	A7	8C	D8
0x54	13	13	13	13
0x56	00	00	00	00
0x58	00	00	00	00
0x5A	00	00	00	00
0x5C	00	00	00	00
0x5E	00	00	00	00
0x60	00	00	00	00
0x62	00	00	00	00
0x64	00	00	00	00
0x66	1C	BE	F5	C7
0x68	00	00	00	00
0x6A	00	00	00	00
0x6C	46	46	46	46
0x6E	00	00	00	00
0x70	0F	0F	0F	0F
0x72	00	00	00	00
0x74	01	01	01	01
0x76	60	C0	40	F8
0x78	0	0	0	0
0x7A	D6	DD	E6	CE
0x7C	FF	7	12	F6
0x7E	E5	F1	1	D8
0x80	65	9B	E3	2B
0x82	2B	2F	34	2B

Table F-16. Complete Register Sets for 1024x768 Input—PAL-N Video Outputs *(3 of 4)*

MODE	1024x768 PAL-N			
0x84	F8	F1	E6	F8
0x86	4B	4B	4C	4A
0x88	00	00	00	00
0x8A	78	82	78	46
0x8C	49	51	49	1D
0x8E	0D	0D	0D	0D
0x90	CF	E8	1A	CF
0x92	83	93	AB	83
0x94	0	0	0	0
0x96	0F	0F	0C	0F
0x98	EC	33	C3	EC
0x9A	A1	A3	A5	A1
0x9C	55	55	AB	0
0x9E	55	55	AA	40
0xA0	1E	1F	20	1D
0xA2	2E	2E	2E	2E
0xA4	F0	F0	F0	F0
0xA6	56	56	56	56
0xA8	7F	7E	7E	7F
0xAA	47	47	47	47
0xAC	8C	8C	8C	8C
0xAE	57	9B	51	CC
0xB0	F8	29	D4	7C
0xB2	F1	26	29	DE
0xB4	18	18	17	19
0xB6	00	00	00	00
AUTO CONFIG register: 0xB8	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values	CONFIG[5:3] & CONFIG[2:0] bit fields Don't program 0xB8. This overwrites other register values
bit5 helps to control interface: *0xBA*	*00*	*20*	*20*	*20*
0xBC	00	00	00	00
0xBE	00	00	00	00
0xC0	00	00	00	00

Table F-16. Complete Register Sets for 1024x768 Input—PAL-N Video Outputs *(4 of 4)*

MODE	1024x768 PAL-N			
0xC2	00	00	00	00
LSb helps to control interface: *0xC4*	*01*	*01*	*01*	*01*
Several interface bits here: *0xC6*	*80*	*80*	*80*	*80*
Many Standard Flicker Filter(FF) bits here: 0xC8	80	80	80	80
Brightness Bits Found Here: 0xCA	C2	C2	C2	C2
Saturation Bits Found Here: 0xCC	C1	C1	C1	C1
DAC Routing Controlled Here: 0xCE	18	18	18	18
0xD0	00	00	00	00
0xD2	00	00	00	00
0xD4	00	00	00	00
0xD6	00	00	00	00
Text Sharpener bits here: 0xD8	60	60	60	60

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

Slider:
Activate MIN OVERSCAN ratio when slider is on MIN Setting
MID OVERSCAN for MID setting
MAX OVERSCAN for MAX setting
At least 3 overscan solutions are included for every mode

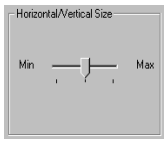


Table F-17. Comments on Why Different Register Values Are Necessary for PAL-BDGHI versus PAL-Nc versus PAL-N Video Outputs *(1 of 4)*

MODE	PAL-BDGHI vs. PAL-Nc vs. PAL-N
Purpose of mode:	
Active Resolution:	
Auto Configuration Mode # used:	
Horizontal Overscan Comp (HOC):	
Vertical Overscan Comp (VOC):	
Input Format	
Type of Clock:	
Type of Interface:	
Number of active pixels/line(H_ACTIVE)	
Number of active lines/frame(V_ACTIVEI)	
H_CLKI = HTOTAL(pixels)	
VLINES_I = VTOTAL(lines)	
H_BLANKI = Horizontal Blanking Region(pixels)	
V_BLANKI = Vertical Blanking Region(lines)	
Frequency of CLK (MHz)	
Type of Video Output:	
TV Out Size:	
[CX25874/5 register addresses]	
Read Only: 0x00	
Read Only: 0x02	
Read Only: 0x04	
Read Only: 0x06	
0x2E	
0x30	
0x32	
0x34	Adaptive FF set up optimally for all modes. Many Adaptive FF bits here.
0x36	Adaptive FF optimal settings the same for 640x480 PAL-BDGHI & PAL-Nc & PAL-N, 800x600 PAL-BDGHI & PAL-Nc & PAL-N, and 1024x768 PAL-BDGHI & PAL-Nc & PAL-N
0x38	
0x3A	
0x3C	
0x3E	

Table F-17. Comments on Why Different Register Values Are Necessary for PAL-BDGHI versus PAL-Nc versus PAL-N Video Outputs (2 of 4)

MODE	PAL-BDGHI vs. PAL-Nc vs. PAL-N
0x40	
0x42	
0x44	
0x46	
0x48	
0x4A	
0x4C	
0x4E	
0x50	
0x52	
0x54	
0x56	
0x58	
0x5A	
0x5C	Hue Adjust register
0x5E	
0x60	
0x62	
0x64	
0x66	
0x68	
0x6A	
0x6C	
0x6E	
0x70	
0x72	
0x74	
0x76	
0x78	
0x7A	
0x7C	HBURST_BEGIN begins slightly earlier for PAL-N HBURST_END later for PAL-Nc. Burst End for Nc= 8.11 us. PAL-M and PAL-N active begin time is 9.40 us after falling HSYNC* edge compared to 10.5 us for PAL-BDGHI
0x7E	
0x80	

Table F-17. Comments on Why Different Register Values Are Necessary for PAL-BDGHI versus PAL-Nc versus PAL-N Video Outputs (3 of 4)

MODE	PAL-BDGHI vs. PAL-Nc vs. PAL-N
0x82	
0x84	
0x86	
0x88	
0x8A	
0x8C	
0x8E	
0x90	
0x92	
0x94	
0x96	
0x98	
0x9A	Vertical scaling coefficent(V_SCALE) most significant bits here. Most significant bits of HBLANKO change for PAL-N
0x9C	
0x9E	
0xA0	
0xA2	For PAL-N, VSYNC_DUR will be set, 625LINE will be set, SETUP will be set(=1), and PAL_MD will be set.
0xA4	
0xA6	Minor change in burst amplitude. Negligible effect.
0xA8	Tiny change in multiplication factor for Cr. Negligible effect.
0xAA	Tiny change in multiplication factor for Cb. Negligible effect.
0xAC	Tiny change in multiplication factor for Y. Negligible effect.
0xAE	Least significant byte of Subcarrier increment. MSC[7:0] different for PAL-BDGHI or PAL-Nc
0xB0	MSC[15:8] different for PAL-BDGHI or PAL-Nc. Used in conjunction with PLL_INT, and PLL_FRACT to
0xB2	change FSC from 4.433 MHz.(PAL-BDGHI & PAL-N) to 3.582 MHz.(PAL-Nc) and
0xB4	This byte is MSC[31:24]
0xB6	
AUTO CONFIG register: 0xB8	THIS IS THE AUTO-CONFIGURATION REGISTER. DO NOT PROGRAM OR YOU WILL OVERWRITE REGISTER VALUES FROM 0X00 TO 0XB6 WITH NEW, UNWANTED VALUES.
bit5 helps to control interface: *0xBA*	Master interface. SLAVER bit = 0
0xBC	
0xBE	
0xC0	

Table F-17. Comments on Why Different Register Values Are Necessary for PAL-BDGHI versus PAL-Nc versus PAL-N Video Outputs *(4 of 4)*

MODE	PAL-BDGHI vs. PAL-Nc vs. PAL-N
0xC2	
LSb helps to control interface: *0xC4*	Encoder set up for master interface right now. EN_OUT = 1, CLKO and other outputs enabled.
Several interface bits here: *0xC6*	*EN_BLANKO = 1, EN_DOT = 0, 24bit multiplexed RGB input format.*
Many Standard Flicker Filter(FF) bits here: 0xC8	DIS_YFLPF = 1, Std. Flicker Filter = 3line for 640x480, 4line for 800x600, 5line for 1024x768
Brightness Bits Found Here: 0xCA	YATTEN = Brightness = 7/8 gain for all sets.
Saturation Bits Found Here: 0xCC	CATTEN = Saturation = 15/16 gain for all sets.
DAC Routing Controlled Here: 0xCE	DAC routing may need to be adjusted for customer's particular set of outputs. This configures DAC Deaf CX25875 used) = Composite #1, DAC C = Luma, DAC B = Chroma, and DACA = Composite #2
0xD0	
0xD2	
0xD4	
0xD6	
Text Sharpener bits here: 0xD8	BY_YCCR = 1, Text Sharpener bits found here.PKFIL = 10 for 2 dB gain

Key:

Denotes register values that change for the different PAL output formats.
Italicized Text Denotes registers that are reprogrammed for different interfaces(master, pseudo-master, or slave).
Bold Text Denotes register values that change from PAL-BDGHI output format to PAL-N video output format.

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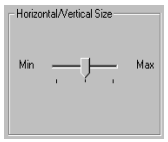

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