CX25836/7
Video Decoder

Data Sheet

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102267A
September 2004

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Ordering Information

Model Number	Description	Package
CX25836-3X	Worldwide video decoder without component input and VIP host port	64-pin lead-free
CX25837-3X	Worldwide video decoder with component input and VIP host port	64-pin lead-free
CX25837-4X	Worldwide video decoder with component input and VIP host port	80-pin lead-free

Revision History

Revision	Level	Date	Description
A		September 2004	Initial Release

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CX25836/7

Video Decoder

The CX25836 and CX25837 video decoders incorporate Conexant Systems' fourth generation high-quality analog video decoding technology. The device integrates all the analog front-end functions: clamping, AGC and ADCs, along with complete 10-bit video decoding logic required for digitizing video into ITU-R BT.656 or SPI-compliant video streams.

Eight analog inputs are provided that can be flexibly configured to support composite, S-Video, and component video inputs, ideal for capturing video from TV tuners, DVD players, camcorders, VCRs, game consoles, and security cameras. Digitized video output is provided by a configurable output port that can support 8-bit and 10-bit sample sizes, embedded sync codes, external timing strobes, and ancillary sliced or raw VBI data.

Worldwide decoding for all common video standards with automatic format detection and configuration is incorporated for minimizing software development and the addition of a hardware interrupt pin eliminates the need for the system to poll the device for status. Also included are high-quality processing functions such as five-line adaptive comb filtering, arbitrary horizontal and 5-tap vertical scaling, hue, brightness, saturation, and contrast control.

The CX25836/7 has multiple-power-down modes to fit your application and power budget needs. The CX25836 is available in one package size: a 64-pin, 7x7 mm TQFP. The CX25837 is available in two package sizes: a 64-pin, 7x7 mm TQFP and an 80-pin, 12x12 mm TQFP package. The CX25837-4x is pin-compatible with the CX25843/2/1/0 series of products.

Distinguishing Features

- Worldwide video standards—NTSC (M, J, 4.43), PAL (B, D, G, H, I, M, N, Nc), SECAM (K, L),PAL-60
- Full 10-Bit ADCs and data path
- Flexible video input mux supporting composite, S-Video, and component inputs with integrated anti-alias filtering
- Five-line adaptive comb filter for NTSC and PAL
- Flexible video output port—27 MHz ITU-R BT.656; VIP1.1, VIP2, or SPI video with separate syncs for square pixel rates
- Macrovision® 1.0 detection compliant
- Programmable VBI data slicer for data services such as closed caption, WSS, Teletext, and program guides
- Power-up configurable two-wire serial command interface or two-wire VIP1.1 or VIP2 host port interface
- Hardware interrupt to eliminate polling
- Auto-detection and configuration for video
- Fast locking mode for security camera applications
- Auxiliary clock output—for providing an oversample audio clock. The PLL can be locked to the video or used as a general purpose PLL output
- Infrared transmit and receive logic
- Internal voltage regulation for single supply operation
- The CX25837 is pin-compatible with the CX24840/1/2/3

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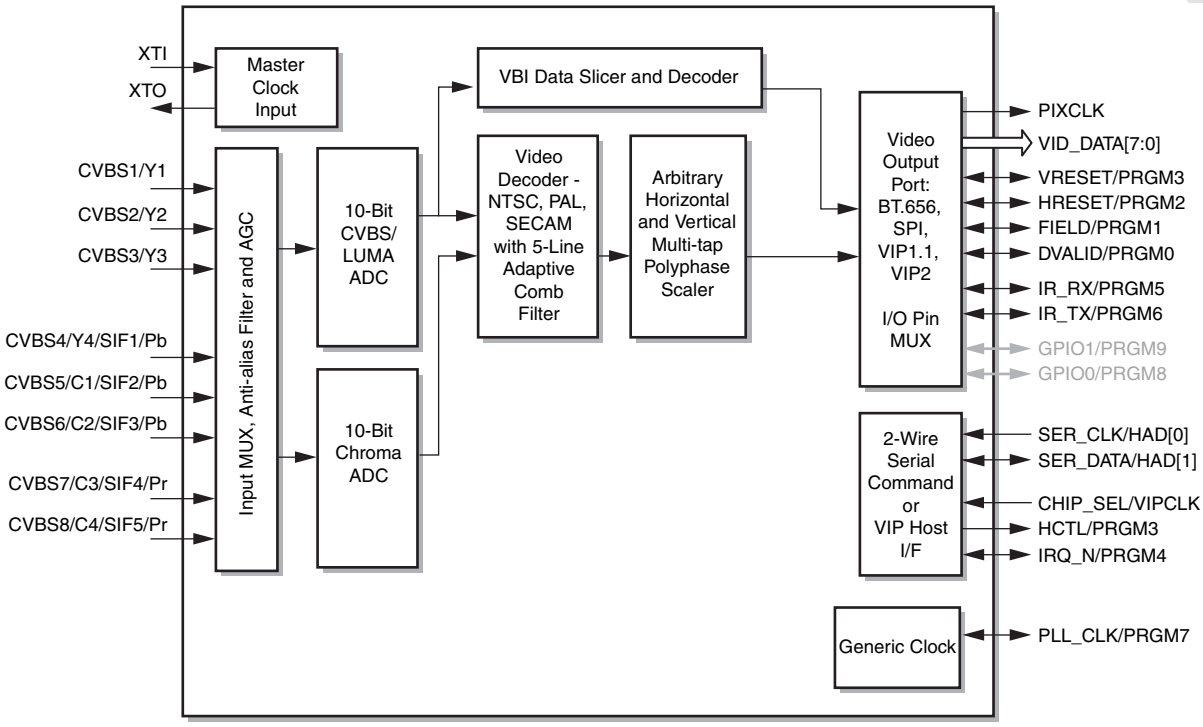
Functional Block Diagram



GENERAL NOTE:

PRGMx pins are labeled with their default reset functions; however, they can be programmed to provide any of the following internal functions: horizontal active, vertical active, Cb flag, 10-bit video data bits[1:0], or GPIO.

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1 Functional Overview

1.1 Analog Video Inputs

The CX25836/7 integrates two high-performance 10-bit Analog-to-Digital Converters (ADCs) and provides a full 10-bit data path through the video decoder to maintain optimum end-to-end video quality. Eight analog video inputs are provided with flexible analog muxing that can be configured for one or a combination of the following:

- Eight composite inputs
- Four Y/C inputs
- Three composite with one Y/C and one YPbPr
- Two composite with two YPbPr

Time multiplexing the various inputs to the chroma ADC allows for the simultaneous digitalization of Pb and Pr inputs in component mode. All video inputs have integrated anti-alias filters, eliminating the need for external filter components.

1.2 Integrated Clamping and Automatic Gain Control

DC restoration and Automatic Gain Control (AGC) are provided to compensate for sources with differing average picture levels. Manual gain control is also supported. Gain values can be read from and written to the device, allowing for the calibration of each input and facilitating fast switching from one source to another.

1.3 Flexible Decoder Rates

The video data path includes a sample rate converter to enable multiple pixel rates and to track any timing fluctuations that may be present within the video source. With the sample rate converter, the user can program the device to decode video at output pixel rates of either 13.5 MHz for an ITU-R BT.656 compliant output stream or at 12.27 MHz and 14.75 MHz for NTSC and PAL/SECAM square pixel rates, respectively. The sample rate converter with internal FIFO monitors the horizontal timing of the input source to create a fixed number of samples per line. It controls a PLL to slowly adjust the FIFO level such that short-term jitter in the input source is filtered out of the digitized video stream. This provides stable video data and output clocks, even with sources like VCRs that can have inherently unstable timing.

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1.4 High-Quality Filtering

Luma/chroma separation of composite video sources is accomplished through a 5-line adaptive chroma comb filter for NTSC and PAL standards. The adaptive comb filter looks across five lines of incoming video and determines which of the five lines are appropriately correlated enough to average together. Depending on the amount of correlation among the lines, two or three lines are averaged together to form the resulting combed filtered line. In the case where no correlation exists between lines, the decoder automatically falls back to chroma band-pass and luma notch filtering. The output of the chroma comb filter is also remodulated and fed back into the luma channel. The result is a high quality image with reduced cross-chrominance and cross-luminance artifacts—such as dot crawl, hanging dots, rainbow effects—that restore full bandwidth to luminance data from composite sources. Additionally, we have a SECAM "Bell" filter to improve SECAM luminance and chroma separation. This is because SECAM uses an FM modulated signal carrier that is always present, regardless of whether or not there is color information being broadcast. This results in a visible artifact in the luminance at the carrier frequency. To eliminate this effect, an "inverse Bell" filter is applied at the encoder to attenuate color frequencies near the Dr and Db carriers. Thus, if little or no color information is present in the signal, the carriers will be reduced in amplitude.

1.5 Video Processing Functions

Back-end video processing functions include contrast, brightness, hue, saturation, and scaling. In addition, the luma data path provides white crush compensation for sources that exceed sync tip to white level ratios. The decoder also provides four sets of selectable peaking filters for sharpening the image. The luma data output range is selectable so that luma codes can be limited to the nominal ITU-R BT.656 code range, or can support values below black level, or can use the entire 10-bit range of values where 0 is black level, and 1023 is nominal white. Additional chroma functions include AGC to compensate for attenuated color subcarriers, a color killer for true black and white sources, and coring for limiting low-level chroma noise.

1.6 High-Quality Scaling

Arbitrary horizontal and vertical scaling is available, from full resolution down to an 8:1 ratio (icon size). Scaling can be accomplished in both VIP and BT.601 square pixel formats. To maintain a high quality scaled image, multitap polyphase interpolation is used. The horizontal luma scaler uses 6-tap, 63-phase FIR interpolation between horizontal source samples, while the horizontal chroma scaler uses 4-tap, 63-phase interpolation. Line store memory is integrated into the decoder so that the vertical scaler—depending on the horizontal scaling ratio—can use from 2-tap to 5-tap, seven-phase interpolation between lines.

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1.7 Configurable Pixel Output Interface

The pixel output format is user-configurable and can conform to 4:2:2 ITU-R BT.656 with embedded timing codes, VIP1.1, VIP2, with embedded timing codes, or SPI-coded video samples with separate sync signals. The pixel output interface can also be set up for 8-bit or 10-bit sample widths, where 8-bit data is derived from the rounded 10-bit value. In addition to providing decoded video data during the active region, raw sample data can be obtained during the horizontal region of the vertical blanking interval. The raw data is from the luma/composite ADC after it has been sample-rate converted and 2x upsampled. This data can be used for capturing high-bit rate VBI services like Teletext for later use by software decoders. The pixel output port also makes use of ancillary data streams by inserting sliced VBI data during the horizontal blanking interval.

1.8 Vertical Blanking Interval Data Slicing and Decoding

An integrated VBI data slicer supports a variety of data standards: WST, Closed Caption, WSS, VITC, as well as programming guide information like Gemstar 1x, Gemstar 2x, and VPS. Decoded data for closed caption, WSS, and Gemstar services is available through either a register read or can be inserted as ancillary data within the ITU-R BT.656 data stream. For high-bit rate services such as WST, NABTS, VPS, and VITC, data is provided on the pixel output port and can be inserted as ancillary data as well. There is independent control of what data service is to be sliced/decoded for every line of each field in the vertical interval. Programmability is also provided such that custom data slicing can be accomplished for data services that do not comply with one of the standards already supported.

1.9 Communications Port and General Functions

Communication with the device is configurable through a pin strap option at power-up reset. Two methods of communication are available: either a 400 kHz two-wire serial command interface or a 2-bit VIP host port interface. A hardware interrupt pin is available along with a maskable interrupt status register so that the device can notify the system when internal events occur without the need to implement polling schemes.

Other convenience features consist of the following:

- Programmable infrared transmitter/receiver logic, able to modulate or demodulate low data rate consumer remote control protocols
- General purpose I/O pins
- Power-down pin or register-controlled power-down levels
- Single 3.3 V power supply configuration available with an external pass transistor
- PLL output for either supplying a video locked 256x/384x oversample audio clock or a general purpose user programmable clock for minimizing PCB component count
- Small package size options: a 64-pin, 7x7 mm TQFP and an 80-pin 12x12 mm TQFP
- Lead-free package

The CX25836 is also offered in a pin-compatible version for solutions that want to offer a video-only product through stuff options using the same PCB.

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2 Pin Descriptions

2.1 Pin Descriptions

See Table 2-1 for pin descriptions.

Table 2-1. Pin Descriptions *(1 of 4)*

Pin Name	64 Pin Pkg	80 Pin Pkg	Dir	Type	Description: {20} ADC Analog
CVBS{1:3}/Y{1:3}	46, 48, 49	58, 60, 61	I	As	Composite or Luma signal input to ADC1. The signal passes through on-chip analog multiplexers before passing through a gain stage, an anti-alias filter stage, and into ADC1. Unused inputs should be left floating.
CVBS{4:6}/Y4/C{1:2}/ SIF{1:3}/Pb{1:2}	51, 53, 55	63, 65, 67	I	As	Chroma, Sound IF, or Pb signal input to ADC2 or Luma, Composite signal input to ADC1. This signal passes through on-chip analog multiplexers before passing through a gain stage, an anti-alias filter stage, and into either ADC1 or ADC2. In color component (Pb, Pr) input mode (available only on CX25837), the Pb component should be connected to one of these pins, and the Pr component should be connected to the Pr{1:2} pins. Unused inputs should be left floating.
CVBS{7:8}/C{3:4}/ SIF{4:5}/Pr{1:2}	57, 59	69, 71	I	As	Chroma, Sound IF, or Pr signal input to ADC2 or Luma, Composite signal input to ADC1. This signal passes through on-chip analog multiplexers before passing through a gain stage, an anti-alias filter stage, and into either ADC1 or ADC2. In color component (Pb, Pr) input mode (available only on CX25837), the Pr component should be connected to this pin, and the Pb should be connected to a Pb{1:2} pin. Unused inputs should be left floating.
IREF	54	66	I/O	Ar	Current reference pin. Connect 30 kΩ, 5% precision resistor to ground.
VAA_ADC{1:2}	44, 41	56, 53	I	Ap	ADC core power, one for each ADC. VAA_ADC = 3.3 V nominal.
VSS_ADC{1:2}	43, 42	55, 54	I	Ap	ADC core ground, one for each ADC.
VAA_CH{1:2}	50, 58	62, 70	I	Ap	Analog channel 1 and 2 (clamp, single-to-diff, VGA, filter) power. VAA_CH = 3.3 V nominal.
VSS_CH{1:2}	52, 60	64, 72	I	Ap	Analog channel 1 and 2 (clamp, single-to-diff, VGA, filter) ground.
ASUB	45	57	I	Ap	ADC core substrate ground.
S2D_NEG{1:2}	47, 56	59, 68	I	Ar	Negative input of single-to-differential converter. Tie to analog ground through AC coupling capacitor for common mode noise rejection. The capacitor should match the value used on the analog inputs.

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Table 2-1. Pin Descriptions *(2 of 4)*

Pin Name	64 Pin Pkg	80 Pin Pkg	Dir	Type	Description: {10} Crystal and PLLs
XTI	62	74	I	As	28.63636 MHz crystal oscillator input, or single-ended clock oscillator input. Used for PLL clock reference and ADC sample clock.
XTO	63	75	I/O	As	Crystal buffer return, or DC reference input for single-ended clock oscillator mode.
VAA_XTAL	64	76	I	Ap	Crystal oscillator power. VAA_XTAL = 3.3 V nominal. Couple to VAA.
VSS_XTAL	61	73	I	Ap	Crystal oscillator ground. Couple to VSS_A.
VPP{0:1}	37, 36	49, 48	O	Ap	Internal PLL power decoupling node. Decouple through 0.1uF capacitor to ground.
VSS_PLL	38	50	I	Ap	Shared PLL ground. Couple to VSS_A.
VDDO_PLL	35	47	I	Dp	Output pad ring power for PLL_CLK pad. Isolated from the rest of the pad ring for noise immunity. VDDO_PLL = 3.3 V nominal. Refer to Note (1) in Figure 4-4 for more information.
PLL_CLK/PRGM7	34	46	O	D	General purpose output clock from a second PLL or can also be used for 256x (or 384x) oversampled clock for external Sigma-Delta Audio ADCs and DACs.
Pin Name	**64 Pin Pkg**	**80 Pin Pkg**	**Dir**	**Type**	**Description: {12} Digital Power Supply**
REG_IN	39	51	I	As	Regulator In. An internal regulator monitors this voltage level from the emitter/drain of an external voltage drop transistor.
REG_OUT	40	52	O	As	Regulator Out. An internal 1.2 V regulator drives this signal out to control the base/gate of an external voltage drop power transistor. When using an externally provided 1.2 V for VDD tie REG_OUT to REG_IN.
VDD {1:3}	10, 16, 27	14, 20, 31	I	Dp	Digital core power. VDD = 1.2 V, nominal. Connect to regulator-generated voltage REG_IN pin or external power supply.
VSS {1:3}	9, 15, 26	13, 19, 30	I	Dp	Digital core ground.
VDDO{1:2}	7, 24	11, 28	I	Dp	I/O pad ring power, VDDO = 3.3 V, nominal.
VSSO{1:2}	8, 25	12, 29	I	Dp	I/O pad ring ground.
VSSO_PLL	33	45	I	Dp	Output pad ring ground for PLL_CLK pad. Isolated from the rest of the pad ring for noise immunity. Couple to VSS_A.

Product Preview

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Table 2-1. Pin Descriptions *(3 of 4)*

Pin Name	64 Pin Pkg	80 Pin Pkg	Dir	Type	Description: {4} Control interface: Serial or VIP Host Port
SER_CLK/HAD[0]	12	16	I/O	Od	Serial communications clock or VIP host address/data bit 0. Used for accessing internal registers. VIP host port available only on CX25837.
SER_DATA/HAD[1]	11	15	I/O	Od	Serial communications data or VIP host address/data bit 1. Used for accessing internal registers. VIP host port available only on CX25837.
CHIP_SEL/VIPCLK	13	17	I	D	Serial communications mode chip select. Selects 7-bit serial chip address: 0: 1000100 (0x88 write, 0x89 read) 1: 1000101 (0x8A write, 0x8B read) VIP host port clock in VIP host mode. VIP host port available only on CX25837. Can also be configured for GPIO and video timing control if interrupt not needed. In VIP Host port mode, this also acts as the IRQ_N signal. Also acts as pin strap option during reset. If the IRQ_N/PRGM4 pin is low during the de-assertion of RESET_N the device will respond to the alternate two-wire serial communications address: 0x8C/0x8D when CHIP_SEL/VIPCLK pin is low 0x8E/0x8F when CHIP_SEL/VIPCLK pin is high If the IRQ_N/PRGM4 pin is high during the de-assertion of RESET_N the device will respond to the default two-wire serial communications addresses: 0x88/x89 when CHIP_SEL/VIPCLK pin is low 0x8A/0x8B when CHIP_SEL/VIPCLK pin is high
VRESET/HCTL/ PRGM3	14	18	I/O	D, R	In VIP host port mode acts as control pin that is used to begin, end, or throttle data transfers. VIP host port available only on CX25837. When the device is in serial communications mode the pin acts as VRESET or can be configured for alternate pin functions.
Pin Name	**64 Pin Pkg**	**80 Pin Pkg**	**Dir**	**Type**	**Description: {12} Video Output Signals**
PIXCLK	32	36	O	D	Pixel clock. Operates at 27.0 MHz and for square pixel formats, 29.5 MHz (625-line) and 24.545 MHz (525-line).
VID_DATA[7:0]	20 21, 22, 23, 28, 29, 30, 31	24 25, 26, 27, 32, 33, 34, 35	O	D	Eight most significant bits of rounded video data. Data is output in a YCrCb 4:2:2 format. For 10-bit mode, the fractional, least significant two bits can be programmed to be output on any of the PRGMx pins
HRESET/PRGM2	17	21	I/O	D	Horizontal reset timing indication is the default pin function. Alternatively, the pin can be programmed to function as a different video timing control, least significant video data bits, or GPIO. See Table 2-2 and Figures 2-1 and 2-2 for the available programmable alternative functions.
FIELD/PRGM1	18	22	I/O	D	Field indication is the default pin function. Alternatively, the pin can be programmed to function as a different video timing control, least significant video data bits, or GPIO. See Table 2-2 and Figures 2-1 and 2-2 for the available programmable alternative functions.
DVALID/PRGM0	19	23	I/O	D	Data valid indication is the default pin function. Alternatively, the pin can be programmed to function as a different video timing control, least significant video data bits, or GPIO. See Table 2-2 and Figures 2-1 and 2-2 for the available programmable alternative functions.

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Table 2-1. Pin Descriptions *(4 of 4)*

Pin Name	64 Pin Pkg	80 Pin Pkg	Dir	Type	Description: {2} Infrared
IR_TX/PRGM6	4	8	O	D, R	Infrared remote control transmit output. Can also be configured for GPIO and video timing control if infrared control is not needed. Also acts as a pin strap option during reset. If the pin is low during the de-assertion of RESET_N the device will boot-up in VIP host port communications mode. If the pin is high during the de-assertion of RESET_N the device will boot-up in two-wire serial communications mode.
IR_RX/PRGM5	5	9	I	D	Infrared remote control receive input. Can also be configured for GPIO and video timing control if infrared control is not needed.
Pin Name	**64 Pin Pkg**	**80 Pin Pkg**	**Dir**	**Type**	**Description: {4} Chip Control**
IRQ_N/PRGM4	6	10	O	D, R	Interrupt output, active low. Can also be configured for GPIO and video timing control if interrupt not needed. In VIP Host port mode, this also acts as the VIRQ_N signal. Also acts as a pin strap option during reset. If the pin is low during the de-assertion of RESET_N the device will respond to the alternate two-wire serial communications address: 0x8C/0x8D when CHIP_SEL/VIPCLK pin is low 0x8E/0x8F when CHIP_SEL/VIPCLK pin is high If the pin is high during the de-assertion of RESET_N the device will respond to the default two-wire serial communications addresses: 0x88/x89 when CHIP_SEL/VIPCLK pin is low 0x8A/0x8B when CHIP_SEL/VIPCLK pin is high
RESET_N	2	2	I	D	Global chip reset, active low.
SLEEP	3	3	I	D	A logic high state on this pin puts the chip in power-down mode.
TEST	1	1	I	D	Puts chip in test mode. Pin is tied low for normal operation.

Legend for Pin Type

R	Active resistive pullup
Od	Open-drain pads with glitch filters
As	Analog signal
Ap	Analog power or ground
Dp	Digital power or ground
Ar	Analog reference, for connection to external component
D	Digital signal

GENERAL NOTE:

1. All signal I/O are LVTTL compatible.
2. All inputs are Schmitt unless otherwise noted.
3. All outputs have drive capability IOL = 4 mA unless otherwise noted.

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The following set of common pins are multifunctional and can have signals routed in and out. Table 2-2 lists these common pins. Figure 2-1 shows the registers to which any signal can be routed.

Figure 2-1 shows the signals that can be routed to any pin in the common list. The CHIP_SEL/VIPCLK pin can also be routed to the signals in Figure 2-2. Refer to Section 3.14, I/O Pin Configuration, for details.

Table 2-2. Common Pins

DVALID/PRGM0
FIELD/PRGM 1
HRESET//PRGM2
VRESET/HCTL/PRGM3
IRQ_N/PRGM4
IR_TX/PRGM6
IR_RX/PRGM5
PLL_CLK/PRGM7

Figure 2-1. Pin Routing

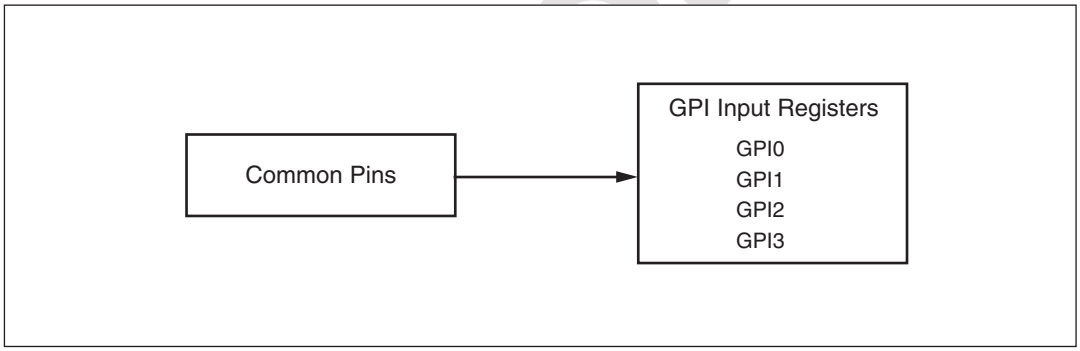
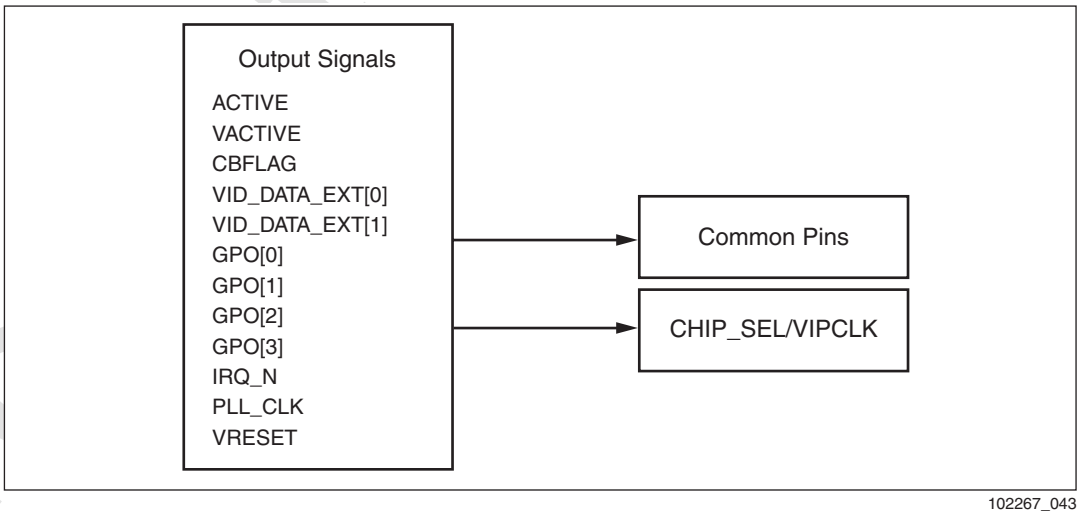


Figure 2-2. CHIP_SEL/VIPCLK Pin Routing



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Pinout drawings are provided in Figures 2-3 and 2-4.

Figure 2-3. CX25836 and CX25837 Pinout (64-Pin)

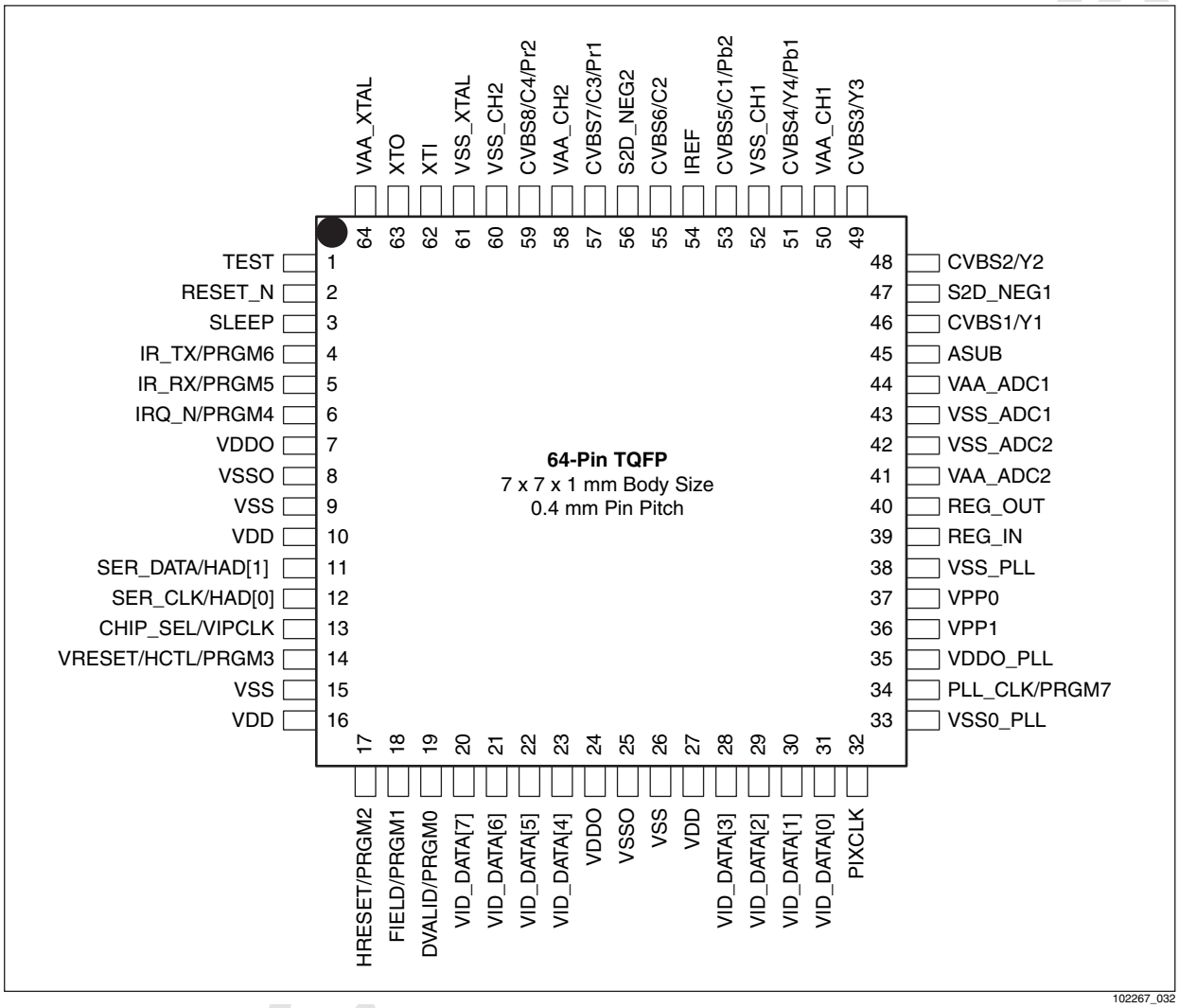

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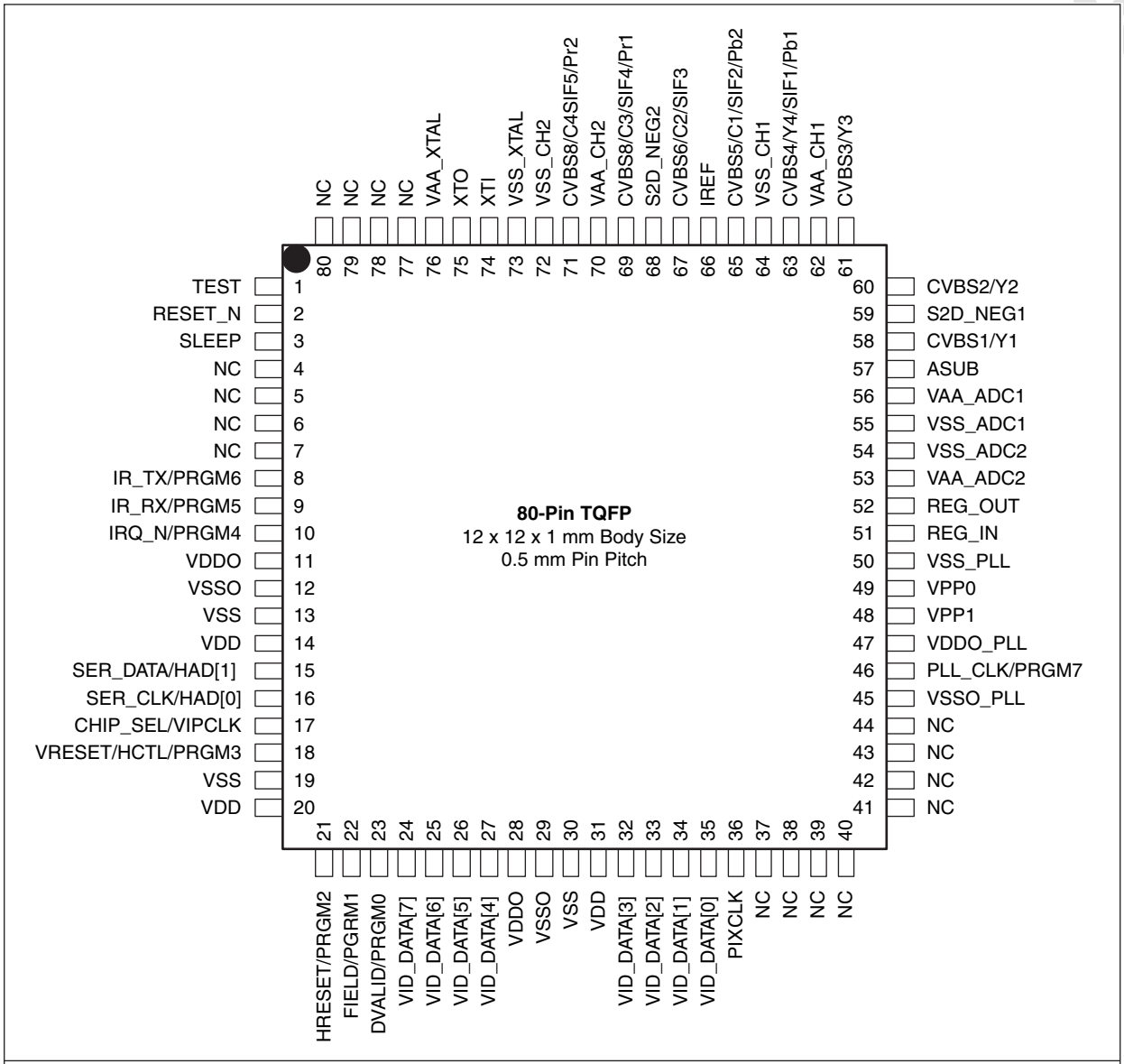
Figure 2-4. CX25837 Pinout (80-Pin)



GENERAL NOTE: NC = No connect.

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3 Detailed Functional Description

3.1 Analog Subsystem Overview

The CX25836 and CX25837 integrate all Analog Front-end (AFE) functions required for filtering, gaining, clamping, and digitizing an analog video signal. The AFE is comprised of the following blocks:

- Three analog muxes
- Clamping and impedance boosting circuitry
- Three single-ended to differential converters
- Three Variable Gain Amplifiers (VGA)
- Three anti-alias filters
- A bandgap reference
- Two Analog-To-Digital Converters (ADC)
- A crystal oscillator amplifier
- Two Phase Locked Loops (PLL)

A block diagram of the signal flow through the analog subsystem is shown in Figure 3-1.

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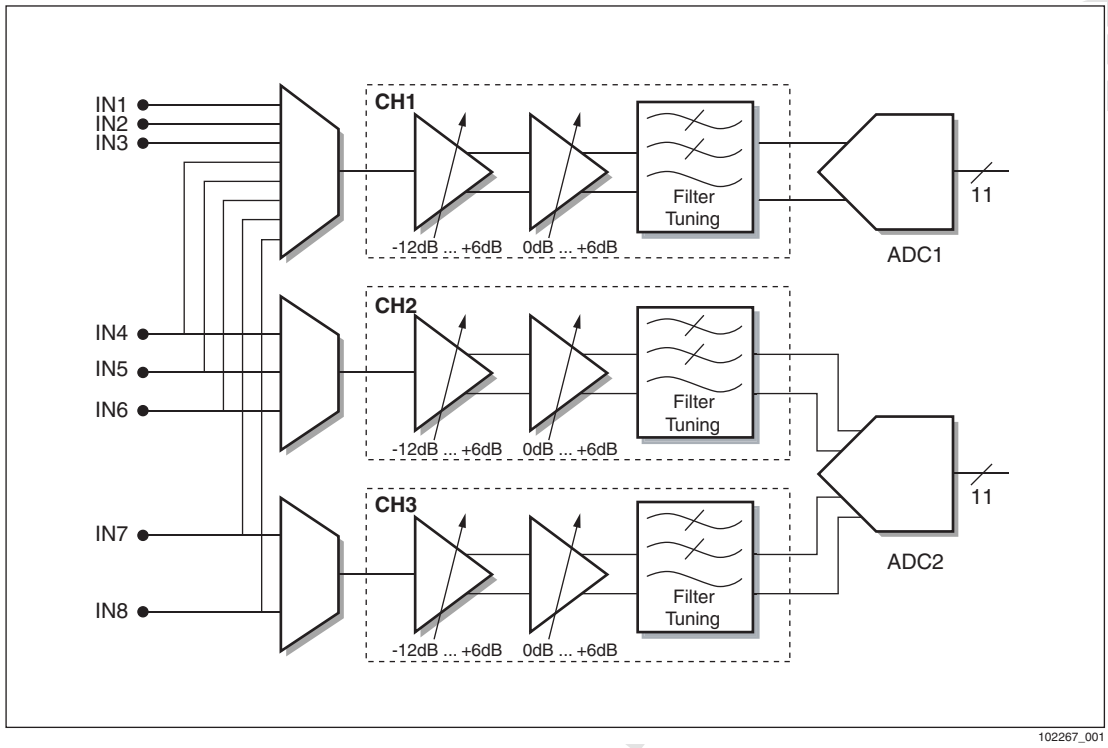
Figure 3-1. AFE Overview



The AFE receives eight video inputs that are multiplexed to produce inputs for the three analog channels: CH1, CH2, or CH3. Each analog channel has a variable gain amplifier and anti-alias filter that can be independently configured. The CH1 signal is routed through ADC1, while CH2 and CH3 can be statically shared or time-multiplexed on ADC2.

After the input mux, the video signal is clamped to the midpoint of the single-to-differential amplifier for DC restoration. Next, the signal is converted from single-ended to differential, and then amplified or attenuated through the two gain stages. The gain settings for the VGA come from the video decoder feedback loop, although this can be disabled and a manual gain value set instead.

The output of the VGA is then low-pass filtered prior to the ADC to prevent high-frequency noise near the sampling frequency from being aliased back onto the signal by the sampling process. The bandwidth of the anti-alias filter is programmable for either 8 MHz, half this bandwidth, or completely bypassed.

ADC1 then samples the DC-restored and gained differential video waveform using the external crystal frequency. ADC2 also samples its differential inputs at the crystal frequency, but the video input can be enabled to time multiplex between the CH{2} and CH{3} inputs. An internal mux switches between the two channels fast enough to support the sampling of the Pb and Pr chroma signals of an interlaced component video input through one ADC.

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The clock for the video decoder's digital domain comes from a fractional PLL that converts the crystal frequency to a clock that is a multiple of the video pixel rate. For example, in ITU-R BT.656 mode, the internal clock runs at 8 times the 13.5 MHz pixel rate, 108 MHz. The digital logic adjusts the frequency in small increments to track the field rate of the decoded video signal, producing a video-locked clock.

Additionally, a second PLL output, AUX_CLK, is provided and can be used as a video-locked oversample audio clock reference for any external audio components. This clock would usually be programmed to be either 384 or 256 times the audio sample rate, but may be any desired multiple of the audio sample rate. The PLL can also be used as a general clock source, unlocked to the video input and programmable to any arbitrary frequency.

A bandgap design is used as an internal voltage reference generator. Its output is connected to a pin for external filtering. Another circuit converts this bandgap reference voltage to a precision current reference. This circuit relies upon an external high-precision resistor connected to the IREF pin to generate this current.

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3.2 Video Mux Inputs

3.2.1 General Muxing Scheme

The analog front-end of the decoder supports up to eight composite video inputs (In1–In8), four S-Video inputs, or two component inputs. Analog muxes connect the inputs to CH{1}, CH{2}, or CH{3} so that any one of eight inputs can be connected to CH{1}, any one of inputs In4, In5, or In6 can be connected to CH{2}, and any one of inputs In7 or In8 can be connected to CH{3}. The muxes are controlled through the Video Input Control register (0x103) with bits CH{1}_SRC, CH{2}_SRC, and CH{3}_SRC, as shown in Tables 3-1 through 3-3.

Table 3-1. Muxing Scheme for CH{1}

Video Input Control (0x103) CH{1}_SRC Bits [2:0]	Input Connected to CH{1}
000	In1
001	In2
010	In3
011	In4
100	In5
101	In6
110	In7
111	In8

Table 3-2. Muxing Scheme for CH{2}

Video Input Control (0x103) CH{2}_SRC Bits [5:4]	Input Connected to CH{2}
00	In4
01	In5
10	In6
11	None

Table 3-3. Muxing Scheme for CH{3}

Video Input Control (0x103) CH{3}_SRC Bits [7:6]	Input Connected to CH{3}
00	In7
01	In8
10	None
11	None

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Although it is possible to connect inputs In4-In8 to two channels simultaneously, this is not recommended.

When an internal input is not connected to any channel, it is connected to a voltage approximately one half of the supply voltage through a high resistance. The maximum allowed input signal amplitude is 2.0 Vp-p.

3.2.2 Configuring for Composite Inputs

In this usage scenario, up to eight composite inputs can be connected to the decoder. As shown in the Figure 3-1, it is possible to connect all eight composite inputs to CH{1} so that only one ADC is being used. Since ADC2 is not being used, it can be turned off to conserve power. It is important to note that although all inputs IN1 through IN8 can be connected, only one input can be active at any one time.

To configure the decoder to accept one of eight possible composite video inputs using just one ADC, the Video Input Control (0x103) register must be programmed as described in Table 3-4.

Table 3-4. Example Composite Mux Configuration

Active Input	Control Bits	Bit Value
CVBS {1}	CH{1}_SRC	000
CVBS {2}		001
CVBS {3}		010
CVBS {4}		011
CVBS {5}		100
CVBS {6}		101
CVBS {7}		110
CVBS {8}		111
	CH{3}_SRC	10 OR 11
	CH{2}_SRC	11

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3.2.3 Configuring for S-Video

It is possible to configure the input mux to accept an S-Video input source. In this case, two channels of the AFE must be used. The luma portion of the S-Video input must be routed to CH{1} and the chroma signal routed to CH{2} or CH{3}. There are enough inputs and analog channels to support multiple S-Video inputs. For example, up to four S-Video inputs can be connected at the same time by using inputs In1 to In4 as luma inputs and In5 to In8 as chroma inputs, as shown in Table 3-5.

Table 3-5. Example S-Video Mux Configuration

Active Input	Control Bits	Bit Value
Y1	CH{1}_SRC	000
C1	CH{2}_SRC	01
Y2	CH{1}_SRC	001
C2	CH{2}_SRC	10
Y3	CH{1}_SRC	010
C3	CH{3}_SRC	00
Y4	CH{1}_SRC	011
C4	CH{3}_SRC	01

To configure the rest of the AFE for S-Video mode, see Section 3.4.1.

3.2.4 Configuring for Component Video

In this scenario, the input mux is used to route component video, YPbPr signals to each of the analog channels. To support component video, all three channels of the AFE are used. CH{1} handles the luma (Y) signal, and CH{2} and CH{3} handle the Pb and Pr color-difference signals. The chroma inputs are time-multiplexed to carry out dual sampling using ADC2. A total of two component inputs can be supported, although only one can be active at any time. For example, In1 and In2 are Y inputs, In4 and In5 are Pr inputs, and In7 and In8 are Pb inputs. The Video Input Control (0x103) register must be programmed as shown in Table 3-6.

Table 3-6. Example Component Video Mux Configuration

Active Input	Control Bits	Bit Value
Y1	CH{1}_SRC	000
Pr1	CH{2}_SRC	00
Pb1	CH{3}_SRC	00
Y2	CH{1}_SRC	001
Pr2	CH{2}_SRC	01
Pb2	CH{3}_SRC	01

To configure the rest of the AFE for component video mode, see Section 3.4.1.

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3.3 Analog Channel

The features described in this section are automatically configured by default, but they can be manually configured as described below.

3.3.1 Input Impedance

Each of the video inputs should be AC-coupled to the source. The minimum size of the coupling capacitor depends on the input resistance of the first circuit block of the signal channel. This resistance is nominally 15 kΩ To allow smaller coupling capacitor values, an active impedance boosting circuit can be activated by setting signal DROOP_COMP_CHx to logical 1 in the AFE Control 3 register (0x106). This increases the resistance value to the 70 kΩ–200 kΩ range. It is not recommended that impedance boosting be used without analog clamping because the boosting circuit may add an offset to the signal, and this offset voltage can be as high as 200 mV. The offset can be eliminated with clamping. For most video applications, the DROOP_COMP_CHx bit should be enabled to use the recommended 1 µF AC-coupling value.

3.3.2 Clamping

Since the video inputs are AC coupled, the sync and back-porch levels of the signal at the channel input varies with the overall average picture level. This requires extra voltage head room, which reduces the maximum achievable signal-to-noise ratio, both in the ADC and the analog signal processing blocks before it. Therefore, the analog subsystem provides a clamping feature to force the sync voltage to a predefined level.

The clamping circuit is by default enabled, but can be disabled by setting the CLAMP_EN_CHx bit in the AFE Control 2 and 3 (0x105 and 0x106) registers to 0. When the clamp is enabled, it pulls the input voltage toward the desired level. A clamp strobe from the digital logic is activated during the sync pulse and remains clamped for a minimum of 1 µs per line. Since the channel gain is variable, the clamping level seen at the ADC output depends on the gain settings. To provide a suitable clamping level across different gain settings, the clamping level can be set with signal CLAMP_LEVEL_CHx[2:0] according to Table 3-7.

Table 3-7. Clamping Levels

CLAMP_LEVEL_CHx	Clamp Voltage (relative to mid-level)	Clamp Code (when gain is set to 0 dB)
000	–1.05 V	–160 (out of ADC range)
001	–0.80 V	0
010	–0.606 V	124
011	–0.460 V	218
100	–0.348 V	289
101	–0.264 V	343
110	–0.2 V	384
111	0 V	512

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3.3.3 Negative Reference Input

The signal inputs are single-ended, but to reduce the effect of board level noise, the negative input terminal of the first gain stage can be taken out of the chip and grounded on the PCB. This external board connection must be AC coupled.

3.3.4 Variable Gain Amplifiers

The variable gain is realized in two stages. The first stage has a gain range from –12 dB to +6 dB in 6 dB steps, and the second stage covers the 6 dB range between the first stage steps by providing 16 linear steps. In addition, the digital control can enable an extra 12 dB of gain by setting the signal EN_12DB_CHx to 1 in the AFE Control (0x104) register. Normally, the video decoder automatically chooses the correct gain value, depending on the amplitude of the input signal. However, if manual control over the gain is desired, the value can be programmed through the VGA_GAIN bits in the VGA Gain Control (0x488) register. It is also necessary to disable the automatic function of the VGA by setting the VGA_AUTO_EN bit in the Digital Front-End (DFE) Control (0x48B) register to 0. The possible gain settings are shown in Table 3-8.

Table 3-8. Gain Settings *(1 of 3)*

Gain[5:4]	Gain[3:0]	Gain
0	0	0.25
0	1	0.265625
0	2	0.28125
0	3	0.296875
0	4	0.3125
0	5	0.328125
0	6	0.34375
0	7	0.359375
0	8	0.375
0	9	0.390625
0	10	0.40625
0	11	0.421875
0	12	0.4375
0	13	0.453125
0	14	0.46875
0	15	0.484375
1	0	0.5
1	1	0.53125

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Table 3-8. Gain Settings *(2 of 3)*

Gain[5:4]	Gain[3:0]	Gain
1	2	0.5625
1	3	0.59375
1	4	0.625
1	5	0.65625
1	6	0.6875
1	7	0.71875
1	8	0.75
1	9	0.78125
1	10	0.8125
1	11	0.84375
1	12	0.875
1	13	0.90625
1	14	0.9375
1	15	0.96875
2	0	1
2	1	1.0625
2	2	1.125
2	3	1.1875
2	4	1.25
2	5	1.3125
2	6	1.375
2	7	1.4375
2	8	1.5
2	9	1.5625
2	10	1.625
2	11	1.6875
2	12	1.75
2	13	1.8125
2	14	1.875
2	15	1.9375
3	0	2

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Table 3-8. Gain Settings *(3 of 3)*

Gain[5:4]	Gain[3:0]	Gain
3	1	2.125
3	2	2.25
3	3	2.375
3	4	2.5
3	5	2.625
3	6	2.75
3	7	2.875
3	8	3
3	9	3.125
3	10	3.25
3	11	3.375
3	12	3.5
3	13	3.625
3	14	3.75
3	15	3.875

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3.3.5 Anti-Alias Filtering

Anti-aliasing filtering is integrated within the analog input channels of the device. The anti-alias filter is designed to reject frequencies within 6 MHz of the sampling frequency to prevent these frequencies from producing aliases in the pass band. The cutoff frequency is set to 8 MHz to provide the flattest possible response for PAL, and the stop band is defined as 22.0 MHz and above where the signal is attenuated at least 25 dB. The time-domain impulse response avoids ringing so that sharp luma transitions do not create ringing in the filter output. Furthermore, the delay through this filter differs by no more than 6 ns across the range from 3.0 MHz to 5.0 MHz.

The filter is automatically tuned to the correct –3 dB frequency by using the ADC clock as a reference. Nominally, this is about 1/3 times the ADC clock frequency. To allow sampling at half-rate, the filter bandwidth can be halved by setting HALF_BW_CHx to 1 in the AFE Control 1 register (0x104). Alternatively, the filter can be completely bypassed by setting BYPASS_CHx to 1 in the AFE Control 3 (0x106) register.

Table 3-9 provides a summary of the anti-alias filter characteristics. Figure 3-2 illustrates a transfer function of the realized filter.

Table 3-9. Anti-Alias Filter Characteristics Summary

Parameter	Requirement
Cutoff Frequency (3 dB)	8.0 MHz
Differential Delay, 3.0 MHz to 5.0 MHz	6 ns
Ripple below 3 MHz	±0.1 dB

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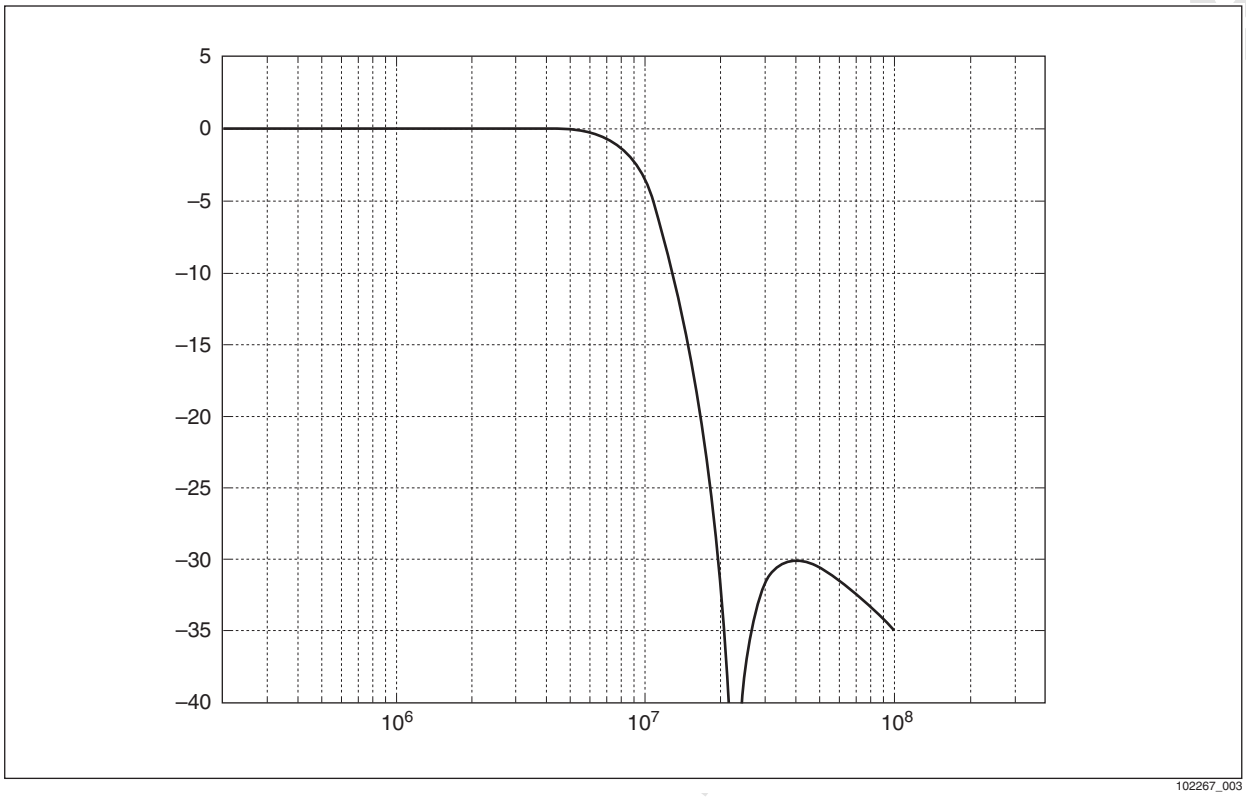
Figure 3-2. A Transfer Function of the Realized Filter



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3.3.6 Channel Performance

The RMS noise voltage in the ADC input depends on the filter bandwidth, gain setting, and temperature. The worst-case noise voltages (not including the ADC noise) for different bandwidth settings are shown in Table 3-10.

Table 3-10. Analog Channel Performance

EN_12DB_CHx	Filtering	RMS Noise Voltage	RMS Noise (dBFS)
0	Normal	750 µV	–57.5
0	Half bandwidth	700 µV	–58
0	Bypass	1.0 mV	–55
1	Normal	2.7 mV	–46.5
1	Half bandwidth	1.9 mV	–49
1	Bypass	3.9 mV	–43

The total harmonic distortion in the ADC input is always smaller than –65 dBFS.

3.3.7 Analog to Digital Converter

Specifications for the ADC are listed in Table 3-11.

Table 3-11. ADC Specifications

Parameter	Symbol	Minimum	Typ	Maximum	Units
Sample Frequency	Fs		27.0	29.5	MHz
Differential Input Voltage Range	Vin			1.6	V p-p
Input Bandwidth	Fb			12	MHz
Output Word Width	R			11	bits
Integral Linearity	INL		±1.0		LSB
Differential Linearity	DNL		±0.7		LSB
SINAD			55		dB
Input Capacitance	Ci		TBD		pF

The second ADC (ADC2) can be configured to sample either CH{2} or CH{3} at nominal clock rate, or it can be put in dual mode, in which samples are alternated between CH{2} and CH{3}. Channel selection is controlled by signal CH_SEL_ADC2: 0=CH{2}, 1=CH{3}, and dual mode is enabled by setting DUAL_MODE_ADC2 to 1. These control bits are found in the ADC2 Configuration (0x102) register.

The ADC is fed a buffered version of the crystal frequency, where it then generates a clock that is five times the crystal clock. This clock is generated using a DLL based clock multiplier.

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3.4 Digital Video Processing

The CX25836 and CX25837 integrate all mixed-signal integrated circuit functions required for decoding broadcast video television standards. They decode all common broadcast analog video formats—(all NTSC, PAL, and SECAM variations) in addition to the nonbroadcast NTSC-4.43 and PAL-60 formats.

The devices decode standard-definition baseband video, formatted as either a composite video baseband signal (CVBS), S-Video (Y/C) format, or as component (YPbPr) format.

For composite video inputs, excellent luma/chroma separation is achieved through the use of an adaptive 5-line comb filter.

All video formats are decoded to either a 10-bit or 8-bit ITU-R BT.656 digital video stream with embedded sync bytes, VIP 2 scale-able digital video stream, or as SPI-coded video stream with separate sync pins.

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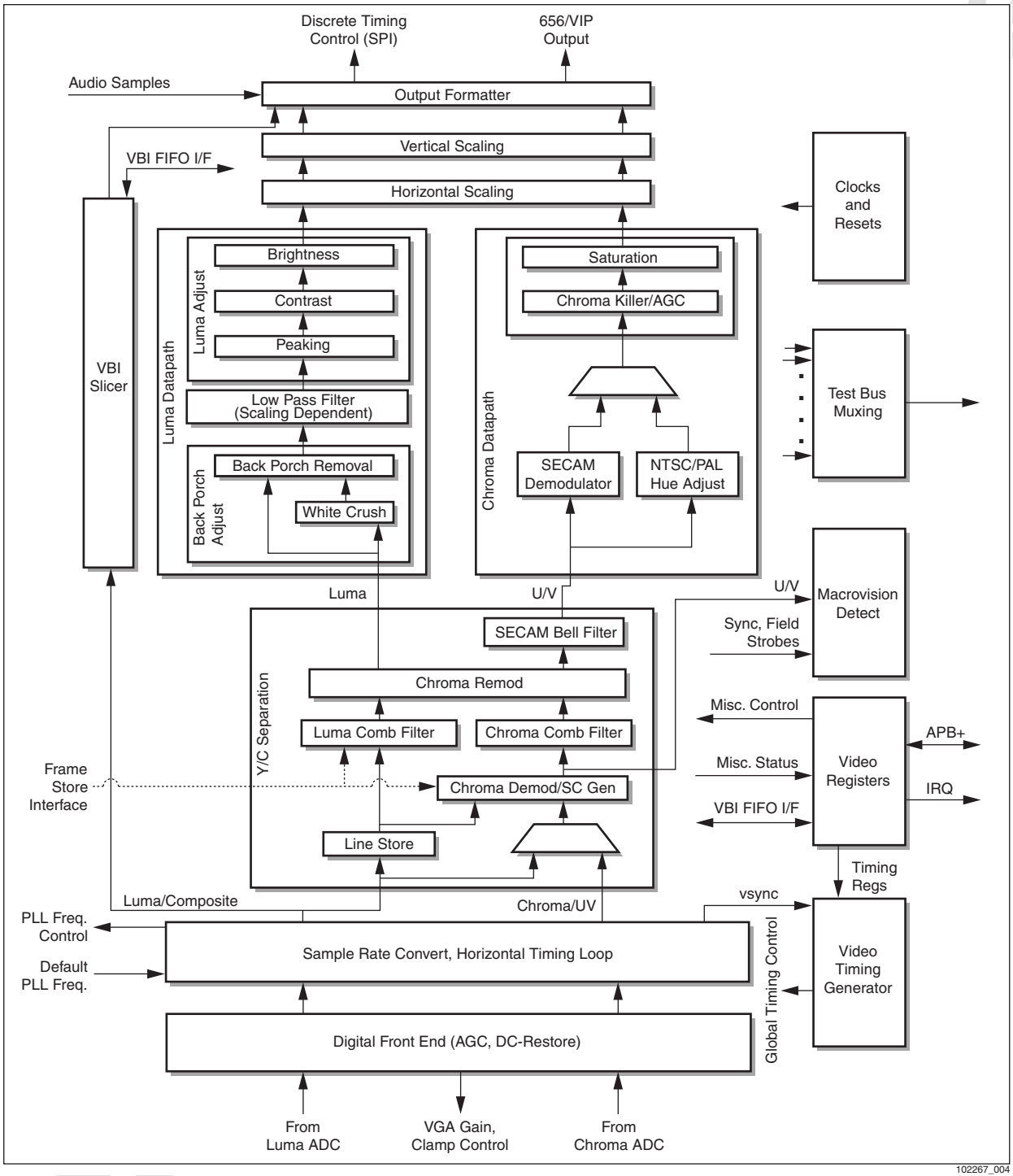
Figure 3-3 illustrates the video decoding functions and data flow.

Figure 3-3. Video Decoder Functional Block Diagram



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3.4.1 Video Signal Format

The input waveform to the video decoder can be in either composite (CVBS), S-Video (Y/C), or component (YPbPr) format. For any of the composite video inputs, ADC1 and ADC2 can be used to sample the video waveform. If desired, the analog front-end of channel 2 can be powered down in situations that do not require S-Video or component video decoding. When an S-Video signal is applied, ADC1 samples the luma signal, and ADC2 samples the chroma signal. When a component waveform signal is applied, the Pb and Pr values are interleaved on ADC2.

The selection of the type of video format to decode is made by programming the appropriate value to the INPUT_MODE bits of the VIDEO MODE CONTROL 2 register (0x401). Once INPUT_MODE is programmed, the video format registers in Table 3-16 are auto programmed. These registers can be manually programmed as well. In cases where S-Video or component formats are to be decoded, the VGA for the chroma channels must be programmed to clamp at the mid-code of the input waveform. This is programmed through the CLAMP_SEL_CHx bits in the AFE Control 2 register (0x105). Additionally, for decoding component signals, the second ADC must be programmed for dual sampling mode. The DUAL_MODE_ADC2 bit of the ADC2 Configuration register (0x102) should be set high to enable multiplexed sampling for the Pb and Pr inputs.

For reducing the integrated anti-alias filter bandwidth on chroma channels, the HALF_BW_CH{1}/2/3 bits are provided. Setting this bit high halves the input bandwidth for that particular channel and prevents the occurrence of any anti-aliasing artifacts. This bit should be set when the channels are used for the chroma waveforms in component video format. Table 3-12 lists the video format register settings.

Table 3-12. Video Format Register Settings

Video Format	INPUT_MODE	CLAMP_SEL_CH{1}	CLAMP_SEL_CH{2}	CLAMP_SEL_CH{3}	DUAL_MODE_ADC2	HALF_BW_CH{2}/3
Composite	00	0	0	0	0	0
S-Video	01	0	1	1	0	0
Component	11	0	1	1	1	1

For power savings measures, the analog front-end associated with chroma inputs can be powered down when decoding only composite input signals. Control over powering down the second ADC and its associated VGAs can be found in the Power Control 1 register (0x130).

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3.4.2 AFE and Video Auto-Config

AFE and Video Auto-Config is enabled by default, but can be overridden in the Miscellaneous Chip Control Configuration register (0x102), by setting bit 4 to a 1.

3.4.2.1 AFE Control Auto-Config

Several control ports to the AFE from the digital core must be adjusted based on the input mode, that is, the content received into the dual ADCs.

To provide some background, the chip contains the two ADCs, but three pre-ADC channels. The pre-ADC channels contain conditioning circuits, Variable-Gain Amplifiers (VGAs), and anti-alias filters. ADC1 is fed by one channel, Channel 1, and ADC2 is fed by two channels (Channel 2 and Channel 3). Either Channel 2 or Channel 3 can be selected to drive ADC2 statically, but the AFE also supports a dual mode in which the ADC2 alternates between samples from Channel 2 and Channel 3 on each sample clock. This supports component video mode, where it is acceptable to digitize the Pb/Pr input streams at half the normal bandwidth. It also supports a mode which allows us to support S-Video and audio IF simultaneously, by digitizing the chroma stream and the audio stream at half of the normal bandwidth.

Table 3-13 shows the supported input formats. Naturally, the chip supports mapping of any given input stream to either ADC1 or ADC2, but when auto-config mode is enabled, default assumptions are made according to Table 3-13. To reverse the input streams between ADC1 and ADC2 channels, the auto-config bit should be disabled.

Table 3-13. AFE Input Modes

Video Mode Control 2 (0x401) INPUT_MODE (Bits 2:1)	Mode Description	ADC1	ADC2
00	Composite Video/Audio	CVBS	Audio
01	Y/C, S-Video	Luma	Chroma
11	Y/Pb/Pr, Component Video	Y	Pb/Pr

Each input mode requires that several AFE control ports be adjusted, either to achieve the required functionality, or to optimize performance. The register fields that control these ports are not register bits that the user generally needs to adjust. Therefore, the auto-config feature is designed to allow the user to just specify the input mode, without having to develop software that knows how to fine-tune the AFE controls. The register logic will automatically adjust the register fields upon writing the INPUT_MODE field in the Video Mode Control 2 register (0x0401). The auto-config will happen immediately upon writing the INPUT_MODE field. If desired by the customer, software may overwrite any fields that were set by the auto-config logic by directly writing to that field. However, the auto-config logic will again modify the register fields if software again writes the INPUT_MODE field. To disable the auto-config features altogether, write the CHIP_ACFG_DIS (ADC2 Configuration register, 0x102) bit.

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Table 3-14 shows how the register field in the ADC2 Configuration and AFE Control (N) registers will be configured based on the INPUT_MODE field of the Video Mode Control 2 register (0x0401).

Table 3-14. AFE Control Auto-Config

Field Name	Register	Bits	CVBS (Default)	Y/C	Y/Pb/Pr
INPUT_MODE	0x401	2:1	00	01	11
DUAL_MODE_ADC2	0x102	2	0	0	1
DROOP_COMP_CH3	0x106	4	0	0	1
DROOP_COMP_CH2	0x106	3	0	0	1
CLAMP_EN_CH3	0x106	1	0	0	1
CLAMP_EN_CH2	0x106	0	0	0	1
VGA_SEL_CH3	0x105	0	1	0	0
VGA_SEL_CH1	0x104	7	1	0	0
HALF_BW_CH3	0x104	5	0	0	1
HALF_BW_CH2	0x104	4	0	0	1

3.4.2.2 Video PLL Auto-Config

Similar to the AFE Control Auto-Config feature, the Video PLL frequency is also automatically configured based on the video operating mode. The Video PLL must be programmed to eight times the pixel rate. The pixel rate in turn depends on whether the chip is in square pixel mode, and if so, whether it is currently decoding a 525-line format or a 625-line format.

Table 3-15. Pixel Frequency Modes

Mode	Pixel Frequency (MHz)	8x Video PLL Frequency (MHz)	Sq_pixel bit	Lines-per-frame
BT.656	13.5000	108.0000	0	Don't-care
525-line square pixel	12.2727	98.1818	1	525
625-line square pixel	14.7500	118.0000	1	625

When auto-config is enabled, the video PLL frequency will be automatically configured based on whether the chip is in square pixel mode, and if so, whether the decoder is decoding a 525-line or 625-line format. The auto-config logic will immediately re-program the video PLL frequency controls whenever either of the following events happens:

1. The SQ_PIXEL bit 4 in Video Mode Control 1 (address = 0x400) is written;
2. The video format changes, whether due to a register write to the VID_FMT_SEL field bits 3:0 of Video Mode Control 1, or due to a format change while in auto-detection mode.

If desired by the customer, software may overwrite any fields that were set by the auto-config logic by directly writing to that field. However, the auto-config logic will again modify the register fields if one of the auto-config events listed above happens. To disable the auto-config feature altogether, write the CHIP_ACFG_DIS (ADC2

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Configuration, 0x102) bit. This is the same bit described above, that disables the AFE Control Auto-Config.

Table 3-16 shows how the registers are configured based on the pixel frequency mode.

Table 3-16. Video PLL Auto-Config

Field Name	Register	Bit(s)	BT.656 timing (Default)	525-line Square Pixel	625-line Square Pixel
VID_PLL_POST	0x109	5:0	0x04	0x04	0x04
VID_PLL_INT	0x108	5:0	0x0F	0x0D	0x10
VID_PLL_FRAC1	0x10C	7:0	0xFE	0xE6	0xB7
VID_PLL_FRAC2	0x10D	7:0	0xE2	0xB6	0x0F
VID_PLL_FRAC3	0x10E	7:0	0x2B	0x6D	0xF7
VID_PLL_FRAC4	0x10F	0	0x0	0x1	0x0

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3.4.3 Video Standard Autodetection

The CX25836 and CX25837 automatically detect and configure themselves to decode a variety of video standards found throughout the world. The auto-format detection logic uses information about the subcarrier frequency, number of video lines, and whether or not the video is alternating phase in order to determine the input standard. For cases where two standards are differentiated by the presence or absence of a pedestal (or setup), two user-programmable register bits, AFD_PAL_SEL and AFD_NTSC_SEL, are required to differentiate the standards. Table 3-17 illustrates how this information is used to automatically determine the video standard.

Table 3-17. Auto Format Detection Parameters

	NTSC-M	NTSC-J	PAL-BDGHI	PAL-N	PAL-M	PAL-NC	SECAM	PAL-60	NTSC-443
Video Lines	525	525	625	625	525	625	625	525	525
Subcarrier Frequency	3.58	3.58	4.43	4.43	3.58	3.58	4.25/ 4.40	4.43	4.43
AFD_PAL SEL	N/A	N/A	0	1	N/A	N/A	N/A	N/A	N/A
AFD_NTSC_SEL	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Video standards supported include NTSC-M, NTSC-J, NTSC-4.43, PAL-BDGHI, PAL-M, PAL-N, PAL-N combination, PAL-60, and SECAM. After a device reset, the video decoder comes up in auto-detect mode and automatically configures the Vertical Blanking, Vertical Active, Horizontal Blanking, Horizontal Active, Burst Gate Delay, Band-pass Filter, Comb Error Limit, SRC Decimation Ratio, Subcarrier Step Size, and VBI Offset registers based upon the active input and whether the SQ_PIXEL bit is set in the VIDEO MODE CONTROL 1 register (0x400).

Refer to Tables 5-4 and Tables 5-5, which show the register values when auto-detect mode is selected for both BT.656 decoding and square pixel rate decoding.

Two video standards, NTSC-J and PAL-N, require additional configuration to discern between NTSC-M and PAL-BDGHI, respectively. For properly decoded black levels with NTSC-J and PAL-N, the AFD_NTSC_SEL or AFD_PAL_SEL bit in the VIDEO MODE CONTROL 1 register (0x400) must be set high to indicate to the decoder that no pedestal is present on the input waveform.

The autodetection can also be manually over-ridden by programming the VID_FMT_SEL bits in the VIDEO MODE CONTROL 1 register (0x400) to the desired video standard to be decoded. Writing these VID_FMT_SEL bits to a forced standard still enables automatic configuration of the registers to their respective values but disables the function to automatically switch should a different video standard be input. To completely disable the automatic register configuration, the ACFG_DIS bit in the Video Mode Control register (0x400) should be set high.

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3.4.4 Signal Level Adjust in the Digital Front End

When a video signal is first applied, the Digital Front End (DFE) block receives 8x NTSC subcarrier, oversampled waveforms from the ADCs that have unknown amplitude and offsets. The block then applies offset and gain to the input such that the output of the DFE is aligned with expected levels for black and white. The DFE controls the amplitude of the signal into the ADCs by implementing an AGC algorithm to gain the signal based on the reference sync tip amplitude. This AGC algorithm coarsely controls the signal amplitude by adjusting the VGA gain in discrete steps. Next, fine adjustment of the amplitude is accomplished by applying a digital multiplier to the incoming signal.

Since some video equipment provides a less-than-standard sync tip, the decoder must also adapt the gain accordingly. If the input signal contains white levels that exceed the expected normal level, the luma processing block detects the occurrence of these excursions past the normal peak white and updates the sync tip height reference.

The DFE is also responsible for aligning the back porch to a standard level. It measures the average level of the back porch level in the incoming signal, and then adds an offset to the ADC data after it has passed through the gain stage.

For S-Video and component formats, the chroma and Pb/Pr ADC data must have its own gain and offset applied. For these cases, the DFE uses the same gain value that was determined from the luma channel for the chroma and Pb/Pr channels. However, for the offset, different assumptions apply. In the case of S-Video, it assumes that the chroma signal is balanced around the ADC's mid-code value of 0x200. Any DC offset from this ideal value should not matter once the AC waveform is passed through the chroma demodulation stage. In the case of YPbPr video format, the offset is such that the chroma value during the sync tip is clamped to the mid-code value of 0x200 (which is logically equivalent to U/V = 0).

The DFE is also partly responsible for determining when the input waveform is clamped. The AFE attempts to clamp the sync tip to a level such that after passing through the VGA stage, it is roughly the correct level. This requires the DFE to provide both the clamping strobe during the sync pulse and a clamping level to the AFE. The clamping level is provided through mapping based on the VGA setting. These functions also serve to maximize the dynamic range of the ADC.

Alternatively, the automatic function of the VGA and AGC can be disabled by setting the auto enable bits, VGA_AUTO_EN and AGC_AUTO_EN, in the DFE CONTROL register (0x48B) low and manually setting the gain values through the VGA Gain Control register (0x488) and AGC Gain Control registers (0x489 and 0x48A). The auto clamping function can be disabled as well through the CLAMP_AUTO_EN bit in the DFE Control register (0x48B). Manual control of the VGA, AGC, and clamp can be useful for specialized applications such as security cameras, but is not recommended for applications where the sources, formats, and standards of the video equipment providing the signal can vary from one use to another.

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3.4.5 Sample Rate Conversion

After the levels of the ADC samples are adjusted, the sample points must be adjusted in time. The Sample Rate Conversion (SRC) blocks convert the signal from the ADC crystal clock domain to the pixel clock rate. Three pixel clock rates are supported. as shown in Table 3-18.

Table 3-18. Pixel Sample Rates

Pixel Rate	Usage
13.5 MHz	ITU-R BT.656 Pixel Frequency
14.75 MHz	PAL and SECAM 625-line Square Pixel Frequency
12.272715 MHz	NTSC 525-line Square Pixel Frequency

This conversion is more involved than a static sample rate conversion. The sample points must be adjusted so the SRC provides not only the same number of pixels per line (for example, 858 in 13.5 MHz mode), but sample points placed such that the first sample is aligned with the leading horizontal sync edge.

VCRs often have timing glitches during the vertical blanking interval caused by head switches, and camera sources can have inter-field and intra-field drift in their line timing due to the manner in which their video timing is derived. The SRC is designed to maintain pixel alignment with these types of nonstandard timing sources by quickly locking to these line-to-line timing variations and smoothing out these variations so that a consistent amount of pixels is output from the decoder.

3.4.6 Source Locked Pixel Clock Generation

The sample rate conversion stage also controls the pixel clock generated by the video PLL. This PLL should be programmed to generate a clock that is 8 times the pixel rate. The internal video decoder logic is clocked with either this 8x clock, or a divided-down 2x version of the same clock.

An important aspect of the SRC and video PLL is that these two blocks work together to provide an internal clock that is locked to the video source. The BT.656 output format requires a fixed number of clocks per field, which is the driving requirement for a pixel clock that is locked to the video source. Not only must there be a constant number of clocks per field, but the PLL-generated clock must be stable. This is required to support MPEG video codec devices connected to the pixel output interface. Similarly, analog video encoders that derive their time base from the pixel clock that we provide can result in inaccurate hue if there is substantial clock drift over the short term.

The video PLL clock directly controls the post-SRC pipeline of the video decoder all the way to the output pixel interface. The frequency creates an exact data rate requirement from the SRC, although the data rate out of the polyphase decimation filter rate is generated independently of the PLL pixel clock. The polyphase filter output rate and the PLL frequency are nevertheless locked, because both the SRC filter and the PLL are both locked to a constant number of pixels per line. The difference is that the SRC has a locking time constant of a few lines, while the PLL has a locking time constant of hundreds to thousands of lines. This means that the PLL and SRC effective sample rates can deviate from each other over the short term.

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To accommodate these short-term clock rate deviations, a synchronization FIFO large enough to hold a line's worth of pixels is implemented. The nominal FIFO-level is half-full. The FIFO level can rise above the midpoint as the SRC quickly outputs more sample points to keep up with short lines. The FIFO level can fall below midpoint as the SRC slows down to accommodate longer lines, but the rate at which samples are read from the FIFO is relatively constant.

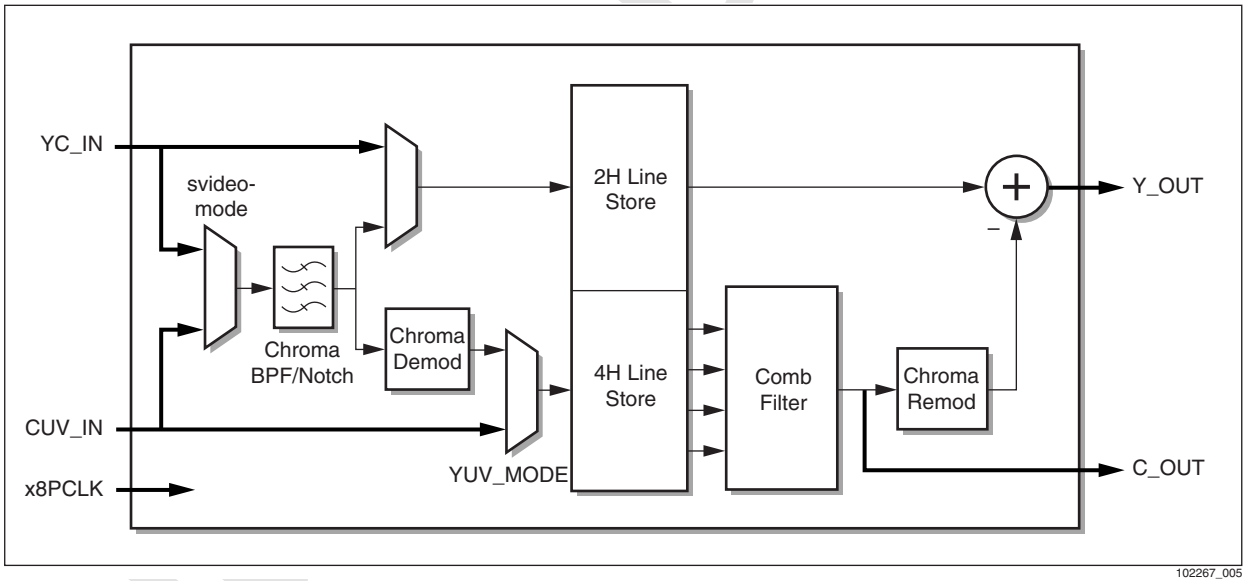
3.4.7 Vertical Sync Detection

The sample rate converter has one more task. It detects transitions in the data that indicate vertical sync pulses (VSYNC). The timing generator circuitry uses the VSYNC pulse to synchronize its vertical counters, and determine what field is currently being decoded.

3.4.8 Luma and Chroma Separation

After the data passes through the DFE level adjust and sample rate converter stages, the next step is to separate the luma from the chroma for composite signal sources (see Figure 3-4). For S-Video and component signal source, the chroma is already separated out, and these ADC samples simply bypass the separation stage and go to the chroma demodulator.

Figure 3-4. YC Separation Block Diagram



A digital PLL is used to track the color subcarrier frequency, F_{sc}, as each line is decoded. It is the responsibility of the subcarrier tracking loop logic to exactly match the phase frequency of the subcarrier in order to properly decode the color information. The $2\omega t$ components of the U and V are then removed by a low-pass filter, resulting in baseband chroma components.

The Y/C separation block implements a 5-line adaptive comb filter, with adaptive fallback to a chroma notch filter. The comb filter implements two algorithms, one for NTSC and one for PAL. The two algorithms are required because the NTSC color carrier has a 180-degree phase shift between adjacent lines, while the PAL color

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carrier has only a 90-degree phase shift. However, the comb filter takes advantage of these phase shifts in the color subcarrier from line to line to recover luminance data from the bandwidth occupied by the chrominance data.

The CX25836/7 separates luminance and chrominance components of the composite video signal with a flexible combination of a luma comb, chroma comb and notch filter. A total of five lines are used in the chroma comb filter algorithm. Four lines are stored in on-chip memory, and the fifth line is the currently decoded line. The adaptation algorithms take advantage of the two additional lines to provide pixels that are in phase with the current pixel in NTSC mode, or to provide additional comb filter options in PAL mode. The luma comb uses only three lines, but which three depends on whether the signal is NTSC or PAL.

The chroma comb filter uses addition and subtraction to determine the lines with the highest degree of correlation with the current pixel and extract the chrominance from these pixels. Since any sample consists of both luma and chroma components, the difference between two pixels could be due to either luminance or chrominance difference, and there is not enough information to tell them apart. In other words, since on any adjacent line, the chroma is out of phase with the current line, subtracting the two pixels is not the difference between the pixels, but rather chroma plus the difference. For NTSC systems, the addition of another pair of lines above the usual three gives access to two lines that are in phase with the current line, making a true comparison possible. In PAL systems, the additional lines are 180 degrees out of phase with the current line, making it similar to NTSC with three lines. However, using a combination of all five lines, a comparison between the current line and the outer lines is possible. So the comb filter finds the combination of lines in which this difference is the smallest. If all the differences are above the programmed CCOMB_ERR_LIMIT threshold in the Chroma Comb Error Limit Max (0x49E) register, the chroma is passed through unaltered and the luminance is notch filtered.

The luma comb uses only the lines which have chroma 180 degrees out of phase, but it first low pass filters the signal to remove the chroma, then compares the remaining luma components. In addition, the chroma comb feeds the difference it has computed to the luma comb. If both errors are acceptably low (below LCOMB_ERR_LIMIT) the luma comb averages the pixels over the entire signal bandwidth. This greatly reduces cross luma in color transitions and high frequency chroma sources such as DVD players.

In SECAM mode, or when the adaptation algorithm determines that an unacceptable error would be created by the comb filter algorithm, it simply notch-filters the color subcarrier out of the luma. Since SECAM uses an FM modulated signal, a carrier is always present, regardless of whether or not there is color information being broadcast. This results in a visible artifact in the luminance at the carrier frequency. To minimize this effect, an “inverse bell” filter is applied at the encoder to attenuate color frequencies near the Dr and Db carriers. Thus, if little or no color information is present in the signal, the carriers will be reduced in amplitude. In order to properly decode the color information, a “bell” filter is applied to the chroma data when in SECAM mode.

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3.4.9 Luma Processing

The luma data path logic processes the luma waveform that comes from the Y/C separation module to produce SPI luma samples. These decoded luma samples are then sent through logic blocks that can perform post-processing functions such as white crush, peaking for sharpness control, contrast, and brightness adjustment before they are passed along to the scaling block.

White Crush

The "white crush" term refers to Conexant's algorithm for adapting to luma overflow in the presence of nonstandard sync-tip-to-white ratios. The luma samples are first passed through the white crush circuitry, which works with the front-end to automatically fine-tune the video levels. This circuitry adjusts the overall gain of the input signal such that excursions above nominal 100 or 110 IRE peak white-level are compensated for to reduce video-blooming artifacts. The white crush processing is by default enabled but can be disabled by writing a 0 to the WCEN bit of Mode Control register 2 (0x401). The 110 IRE threshold can be enabled by setting the WTW_EN bit high in the White Crush Control 3 register (0x4A2).

Following white crush, the back porch of the luma waveform is removed, and for some video formats, the setup (or pedestal) value is removed as well. The luma samples are then multiplied by scale factors to match SPI defined luma levels. Setup removal is determined by the video standard.

Luma Low-Pass Filtering

Next, the luma is optionally low-pass filtered to remove any high frequency content that could cause alias artifacts associated with horizontal scaling. The filter has four different transfer functions based upon the desired horizontal scaling factor. The appropriate transfer characteristic is automatically selected by deriving from the value that is programmed in the Horizontal Scaling registers (0x418 to 0x41A). One of these four transfer functions is nothing more than a filter bypass. This is automatically chosen when no scaling is enabled.

Figure 3-5 shows the luma filter responses for the other three transfer characteristics when scaling is performed.

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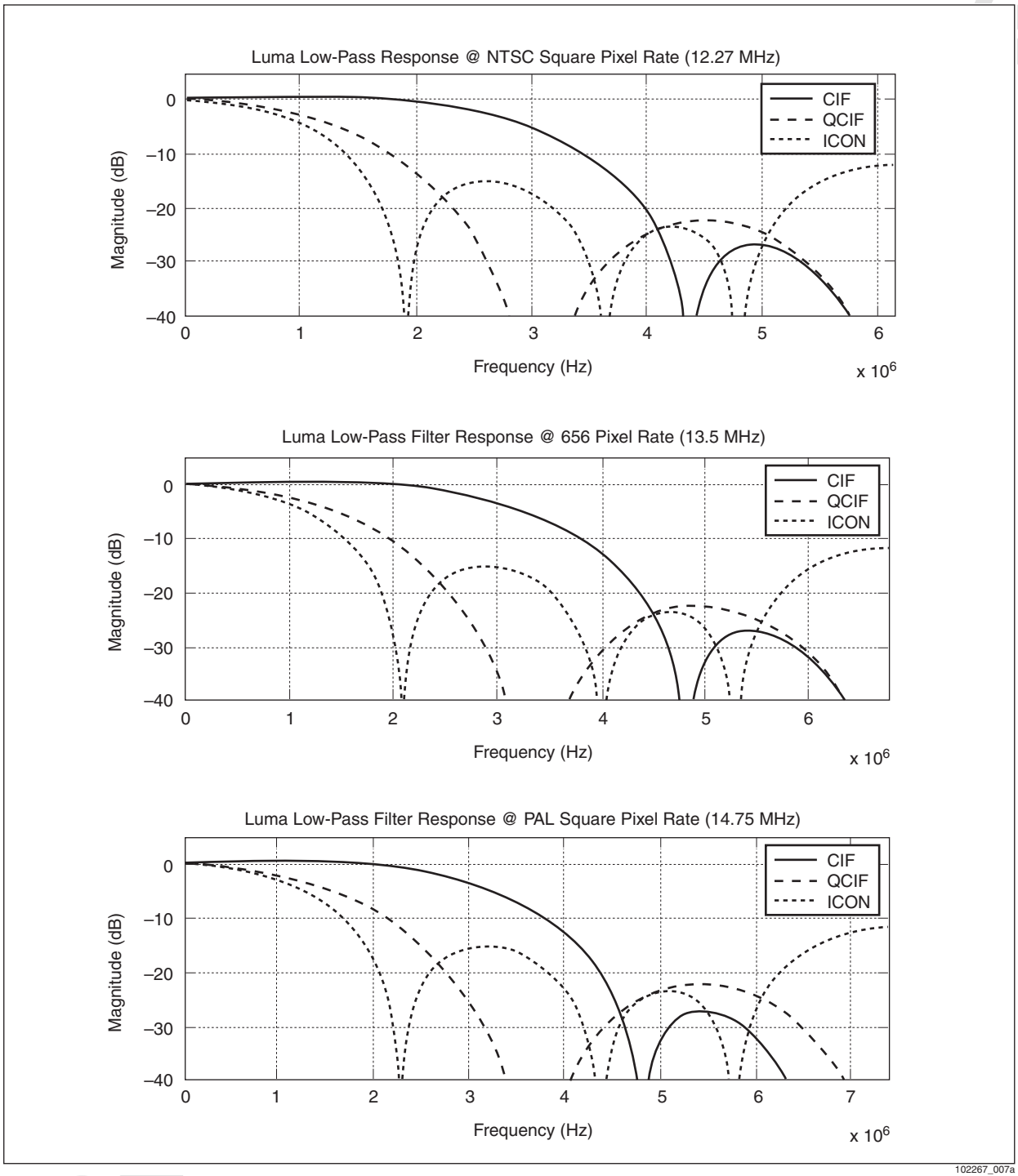
Figure 3-5. Luma Filter Responses



Luma Peaking

Following the low-pass filter is another filter, the peaking or sharpness filter. The peaking filter can be used to improve the high-frequency response of the luma near its corner frequency. As with the luma low-pass filter, this filter has multiple response functions. There is a bypass mode and four modes with non-0 gains, increasing from +2.0 dB to +6.0 dB. The larger the programmed gain of the filter, the greater the luma

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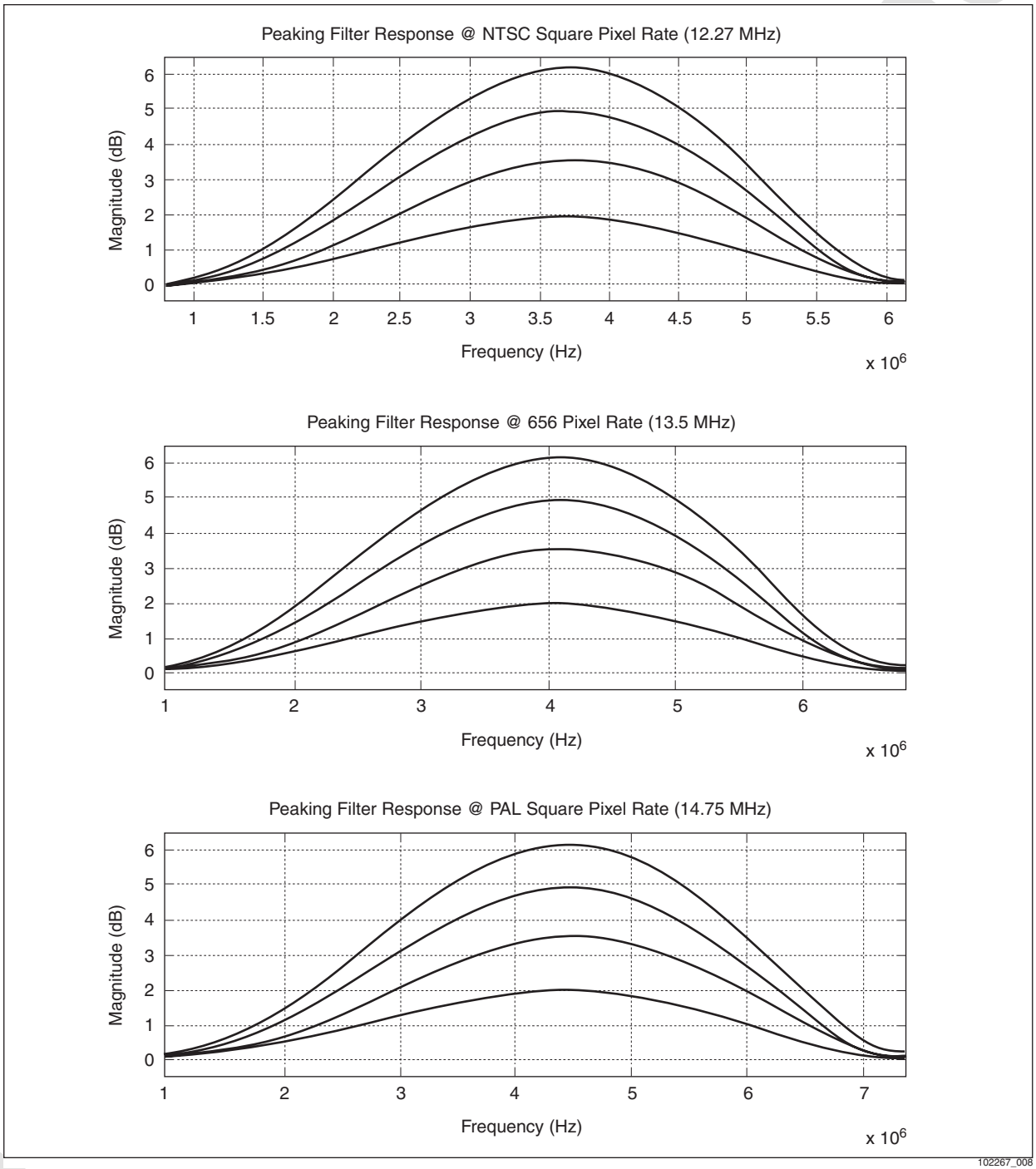
high frequency adjustment. The filter is enabled through the PEAK_EN bit in the Luma Control register (0x416). The gain of the filter is selected through the PEAK_SEL bits, which selects between the four positive gain values, +2.0 dB, +3.5 dB, +5.0 dB, and +6.0 dB. Figure 3-6 shows the peaking filter characteristics for the various pixel rates.

Figure 3-6. Peaking Filter Responses



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Contrast

Contrast adjustment follows the peaking filter. This block multiplies the luma samples by the contrast value that is programmed into the Contrast register (0x415). The multiplication value is represented by a 2s complement number, thus values above 0x80 increase the contrast, and values below 0x80 decrease the contrast. This is followed by color-space conversion, which converts the luma from YUV color space to YCrCb color space. The function involves multiplying the incoming luma data by the color-space conversion factor. The incoming video standard and the desired output range of luma codes determine the multiplication factor. The RANGE bits of the Luma Control register (0x416) determine the number of 10-bit codes, out of 1024, that are allowed for the nominal luma range. This does not mean that the luma is limited to this range. It just means that this range is used in the color space conversion process. multiplying

Brightness

Following the contrast and color-space conversion multiplication operations, the brightness adjustment is performed, which is an addition of the luma samples with 8 times the value found in the BRIGHTNESS register (0x414). This register value is represented by a 2s complement number, allowing the overall video level to be adjusted down by as much as 1024, or up by as much as 1016 on a 10-bit scale. This results in a luma signal that has been offset by an amount equal to the brightness value.

The next step is the coring operation, which serves to remove low-level noise by zeroing-out any values whose magnitude is below a user-selected threshold. This threshold is selected through the LUMA_CORE_SEL bits in the Luma Control register (0x416). This coring threshold can range from 0, which would have no effect, to 64, which would zero-out the 7 LSBs of the luma output.

The final process of the luma data path is the range saturation. The range adjustment enables the user to select one of three allowed luma output ranges. The first range is compliant to the SPI specification that allows for a nominal 64–940 range with excursion up to 1016 but not below 16-black level. The second range is similar in that it allows for a nominal 64–940 with excursions up to 1016 but in addition it allows for excursions below 16. This is to support blacker-than-black values which are possible on systems with a pedestal. The final range places no restrictions on the data in that it allows all value from 0 to 1023 to pass. Table 3-19 illustrates the output range of the luma data for the various RANGE bits in the Luma Control register (0x416).

Table 3-19. Luma Output Ranges

RANGE[5:4]	Nominal Range After Color-Space Conversion (decimal)	Allowed 8-bit Output Range (decimal)	Allowed 10-bit Output Range (decimal)	Description
00	64–940	16–235	64–1016	Nominal range with excursions allowed but no blacker than black levels
01	64–940	1–235	4–1016	Nominal range with excursions and blacker than black allowed
1x	0–1023	0–255	0–1023	0–1023 nominal with no limiting

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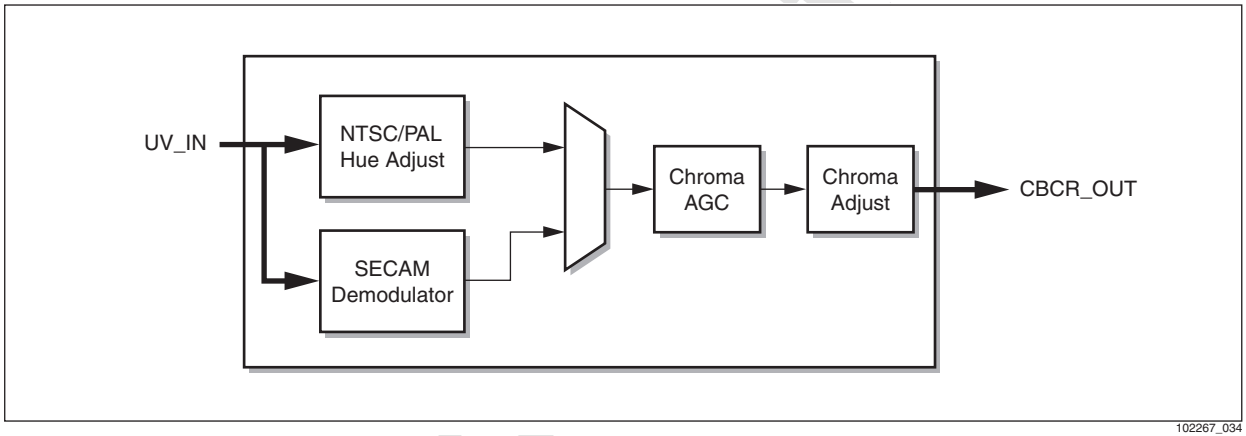
3.4.10 Chroma Processing

The Chroma Data Processing (CDP) block receives chrominance U/V data from the Y/C Separation (YCS) block. Although the SECAM demodulator is located in the CDP, the demodulator for NTSC and PAL is located in the YCS because of the comb filtering in these formats. The U/V input is also used to support component video (YUV) formats. The component format U/V data is merged into the U/V data path in the YCS block.

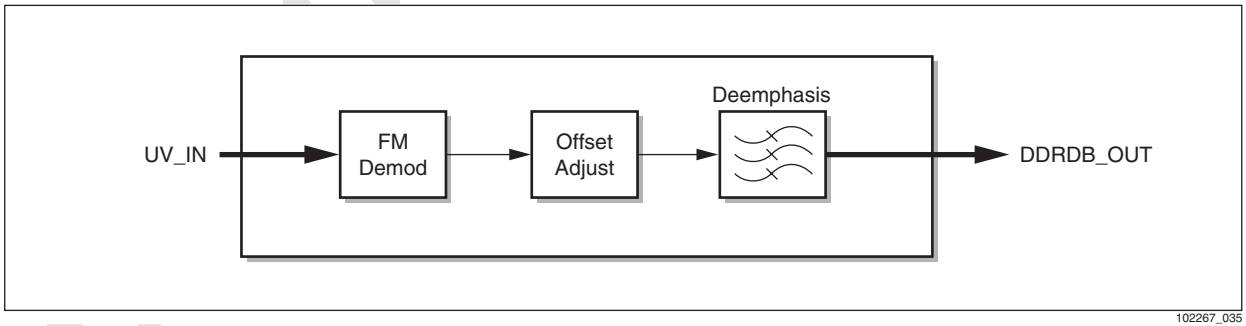
Figure 3-7 illustrates the major components of the CDP. When in SECAM mode, the CDP must demodulate the SECAM chroma to obtain the Db/Dr baseband components. Otherwise, hue adjustment is done for the NTSC and PAL formats. The CDP performs AGC on the signals, for NTSC and PAL formats, based on the value of the U component during the color burst. Adjustments are made for saturation, color space conversion for the Cb/Cr space, and finally chroma coring. The chroma data path also contains a programmable delay of ±2 pixels to allow alignment adjustments relative to the luma data path.

Figure 3-7. Chroma Processing



Some amount of SECAM pre-processing is performed in the YCS block. The SECAM complex down converter or frequency mixer and the Bell filter function is performed in the YCS block. The CDP processing for SECAM is shown in Figure 3-8.

Figure 3-8. SECAM Chroma Demod



The first step is to perform FM demodulation. FM demodulation is implemented with a CORDIC rotator followed by a differentiator filter. Next, an adjustment is made to the output of the FM demod to account for the frequency offset introduced by using the fixed frequency mixer. A fixed de-emphasis filter is then applied according to the SECAM standard.

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Hue can be adjusted for NTSC video standards through the Hue register (0x422). The register value represents a signed 8-bit value that is used to rotate the subcarrier phase in increments of 0.35 degrees with a range of –45 degrees to +45 degrees.

Chroma AGC

The chroma AGC logic is used to correct for nonstandard chrominance information in NTSC and PAL, typically found in VCRs, by multiplying the chrominance information by a computed gain value. The chroma AGC logic is a feedback loop that continually adjusts the gain applied to the chrominance data to produce the standard level for the given television format. Each horizontal line, the value of the U data during the color burst is compared to the standard value, and the difference accumulated over four samples. If the error is greater than or equal to –8, or less than or equal to 7 for 32 consecutive lines, the chroma AGC enters an idle state. Once in this idle state, the chroma AGC does not make any gain corrections until the accumulated error is greater than or equal to 32, or less than or equal to –32 for 32 consecutive lines. At this point, corrections are made until the idle state is entered once again. This gain update only occurs once per line. The chroma AGC is enabled by default but can be disabled by setting the CAGCEN bit of the Video Mode Control 2 register (0x401) to 0. The chroma AGC is also disabled automatically if the video input format is component, YPrPb, or if the video standard is SECAM.

Chroma Kill

The chroma kill function disables the chroma demodulation function if the color burst is detected to be below a certain threshold. This allows for the case in which either no color exists or a greatly attenuated color subcarrier exists on the video input. This prevents the chroma AGC loop from falsely detecting noise as chroma and amplifying it.

The NTSC and PAL chroma killer is accomplished by logic that detects a low color burst value for 127 consecutive lines. The chroma killer state machine monitors chroma samples that are accumulated during the color burst. If the accumulated chroma samples have a magnitude smaller than 7 percent of the nominal NTSC burst amplitude, or 10 percent of the nominal PAL burst amplitude, the color kill function is asserted. If the accumulated chroma sample value has a greater magnitude than 14 percent of nominal NTSC burst amplitude, or 19 percent of nominal PAL burst amplitude for 127 consecutive lines, the color killer function is automatically disabled. The SECAM chroma killer is accomplished by using the subcarrier frequency detect information from the DFE. If no subcarrier exists for 127 consecutive lines, the chroma killer logic is activated. To permanently disable the color killer function, the CKILLEN bit in the Video Mode Control 2 register (0x401) should be set low.

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Saturation

Saturation can be adjusted through the Saturation-U (0x420) and Saturation-V (0x421) registers. These register values are doubled internally and then multiplied with the U and V data. The result is then rounded and clamped to a 10-bit value. To maintain proper U and V saturation ratios, these registers should be written in tandem with the same value. Table 3-20 illustrates the range of saturation adjustment available.

Table 3-20. Chroma Saturation Range

Decimal Value	Hex Value	Percent of Original Signal
255	0xFF	199.22
254	0xFE	198.44
. . .	. . .	. . .
129	0x81	100.78
128	0x80	100.00
127	0x7F	99.22
. . .	. . .	. . .
1	0x01	0.78
0	0x00	0.00

Chroma Coring

Chroma coring can be enabled to remove low-level chroma noise by zeroing out any values whose magnitude is below a user-selected threshold. This threshold is selected through the CHROMA_CORE_SEL bits in the Chroma Control register (0x423). This coring threshold can range from 0, which would have no effect, to ±31, which would zero out the 6 LSBs of the chroma output. Table 3-21 shows the range of possible chroma coring values.

Table 3-21. Chroma Coring Range

CHROMA_CORE_SEL[1:0]	Coring Range
00	No coring
01	–7 <= x <= +7
10	–15 <= x <= +15
11	–31 <= x <= +31

Lastly, the chroma data can be delayed by ± 2 pixels relative to the luma data. The CHR_DELAY bits of Chroma Control register (0x423) specify the delay. The values can be thought of as signed 3-bit numbers that represent the pixel delay. Positive values mean the chroma data will be delayed more than the 0 value. Negative values mean the chroma data will be delayed less than the 0 value.

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3.4.11 Copy Protection Detect

The copy protection logic detects the presence of the pseudo-sync pulses and color striping in the video waveform according to the Macrovision copy protection detection specification. If more than a minimum specified number of pseudo-sync pulses (PSP) in a field are detected, the MV_PSP status bit is set in the Copy Protection Status register (0x40C). If Macrovision color striping is detected for more than a specified minimum number of lines, the logic sets a status bit indicating that color striping has been detected and additional status bits indicating what type of color striping is detected, type 2 or type 3. The MV_CS bit indicates the presence of color striping, the MV_T3CS bit indicates the presence of type 3 color striping, and MV_TYPE2_PAIR indicates a type 2 pair detected. These status bits can be found in the Copy Protection Status register (0x40C).

Additionally, the pseudo-sync pulse and color striping status indicators are encoded to form a 2-bit Macrovision Copy Control status as described in the Macrovision detection specification. This code is represented by the MV_CDAT bits in the Copy Protection Status register (0x40C). The host processor can be automatically informed of changes in the presence of copy protection on the source material through the interrupt pin. A MV_CHANGE_STATE interrupt status with mask is available in the Interrupt Status 2 and Interrupt Mask 2 registers (0x411 and 0x413), respectively. If the MV_CHANGE_STATE mask is 0, any change to the status bit is reflected on the interrupt pin. This alleviates the host processor from having to continually poll the status register to see if copy protection is present on the incoming video waveform.

3.4.12 Timing Generator

The timing generator provides all the timing control strobes for video decoder paths that follow the sample rate converter block. It outputs both horizontal and vertical timing control, including blanking and burst gate control. The SRC module provides vertical sync (VSYNC) and horizontal sync (HSYNC) reference pulses to synchronize the timing generator.

In auto-detect mode, the timing generator is also responsible for controlling the format search. Based on the lines-per-frame count, the subcarrier frequency, and the presence of phase alternation, the mode is selected. When video lock is lost and re-acquired, the default assumption is that the video broadcast standard remains unchanged. It is only when differences in the key format metrics are detected that the format selection is changed.

Upon selecting a mode, the timing generator automatically sets all of the timing parameters required for the selected video broadcast standard. There is also a manual mode where the timing parameters are produced directly from the programmable register set.

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3.4.13 Fast Channel Switching

Fast channel switching is when you grab a field (or frame) from an input and then switch to another input and try to grab the first correct field available and then switch again to another input and so on.

To determine if the decoder can grab a field after a channel switch, the decoder must lock on the signal. To lock on the new input signal, it is necessary to have Horizontal Lock, Vertical Lock, and Color lock on the video input.

The CX25840/1/2/3 uses optimized hardware to reduce the time needed to switch between different signal sources. This new technology now achieves much higher frame rates when switching inputs continuously.

This is achieved through the following:

- Fast Horizontal Lock
- Fast Vertical Lock
- Fast Color Lock
- Fast adjustment of gain for input signal

Fast Horizontal Lock (HLOCK) is a feature that is already optimized in the decoder. There are no registers to enable. The General Status 2 (0x40E) register has an HLOCK bit that notifies the application that horizontal lock has been achieved. Even under line length variations fast horizontal locking is achieved.

Fast Vertical Lock (VLOCK) can be achieved by setting FAST_LOCK_MD bit of the Video Mode Control 3 (0x402) register to high to enable the fast locking algorithm. The fast locking algorithm locks onto the first vertical sync it encounters, regardless of where the internal timing counters expect a vertical sync to occur. It also disables the hysteresis that is used for the field detection logic. As soon as the even/odd field is detected, the field signal is updated to reflect that status. Vertical lock can be determined by reading the VLOCK and VPRES status bits in the General Status 2 (0x40E) register.

To achieve Fast Color Lock (CSC_LOCK), the chroma subcarrier lock speed must be set to fast mode. To do this, the auto mode of the subcarrier lock must first be disabled by setting the AUTO_SC_LOCK bit low and then setting the subcarrier lock speed to “fast” by setting the MAN_SC_FAST_LOCK bits in the Video Mode Control 2 (0x401) and Interrupt Status 1 (0x410) registers, respectively. Status of subcarrier lock can be determined by reading the CSC_LOCK and CSC_LOCK_CHANGE_STAT bits in the General Status 2 (0x40E) and Interrupt Status 1 (0x410) registers, respectively.

To achieve a fast adjustment of gain for the input signal (AGC_LOCK), enable the AGC_AUTO_EN and VGA_AUTO_EN functions in the Digital Front-End Control (0x48B) register. By doing so, the decoder has the ability to automatically acquire gain value for all eight composite inputs. This is particularly useful because the AGC presents a problem for doing fast channel switching. Since all sources require different gain values when we switch from one video input to another, it takes time for the gain to adjust. The adjustment time can prevent how fast the application can switch between inputs. After enabling the AGC_AUTO_EN and VGA_AUTO_EN functions, the application would then enable each input, read the AGC_GAIN and VGA_GAIN values for that source, and save the values for later use. Next, the application would set AGC_AUTO_EN and VGA_AUTO_EN bits to manual mode, and write the saved AGC value that is associated with a particular input to the

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AGC_GAIN and VGA_GAIN fields. This technique of restoring predetermined gain values eliminates the amount of time needed to adjust the AGC for the new video input. The General Status 2 (0x40E) register has an AGC_LOCK bit that notifies the application that the correct gain has been selected.

Finally, auto format detection should be disabled for fast channel switching. This is accomplished by setting the VID_FMT_SEL bits in the Video Mode Control 1 register (0x400) to the appropriate video standard to be decoded.

3.4.14 Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when full frame rate cannot be supported due to bandwidth and system restrictions.

The device provides temporal decimation on either a field or frame basis. The temporal decimation register (TDEC) is loaded with a value from 1 to 60 (NTSC) or 1 to 50 (PAL/SECAM). This value represents the number of fields or frames skipped by the chip during a sequence of 60 for NTSC, or 50 for PAL/SECAM. Skipped fields and frames are considered inactive, indicated by the ACTIVE pin remaining low. Consequently, if QCLK is programmed to depend on ACTIVE, QCLK becomes inactive as well.

Examples:

- TDEC = 0x02 Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding.
  - Frames 1–29 are output normally, then ACTIVE remains low for one frame. Frames 30–59 are then output, followed by another frame of inactive video.
- TDEC = 0x9E Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding.
  - This value outputs every other field, or every odd field of video, starting with field one in frame one.
- TDEC = 0x01 Decimation is performed by frames. One frame is skipped per 50 frames of video, assuming PAL/SECAM decoding.
- TDEC = 0x00 Decimation is not performed. Full frame rate video is output by the device.

When changing programming in the temporal decimation register, 0x00 should be loaded first, and then the decimation value. This ensures the decimation counter is reset to zero. If zero is not first loaded, the decimation may start on any field or frame in the sequence of 60 (or 50 for PAL/SECAM). On power-up, this preload is not necessary because the counter is internally reset. When decimating fields, the FLDALN bit in the TDEC register can be programmed to choose whether the decimation starts with an odd field or an even field. If the FLDALN bit is set to logical 0, the first field dropped during the decimation process will be an odd field. Conversely, setting the FLDALN bit to logical 1 causes the even field to be dropped first in the decimation process.

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3.5 Scaling and Cropping

The scaling engine consists of both horizontal and vertical scalers. The purpose of the scaling engine is to scale down the image by a programmable factor. This is useful when viewing video on a PC desktop and when saving video to disk. The scaling engine supports arbitrary and independent downscaling only with vertical and horizontal scaling factors that are controlled through separate registers to allow different scaling values—anamorphic scaling.

The horizontal scaler supports the following requirements:

- Supports scaling from 1 to 15.999755859375 in 1/4096 steps.
- Supports 63 phases between source samples. The filter rejects aliases by 60 dB.

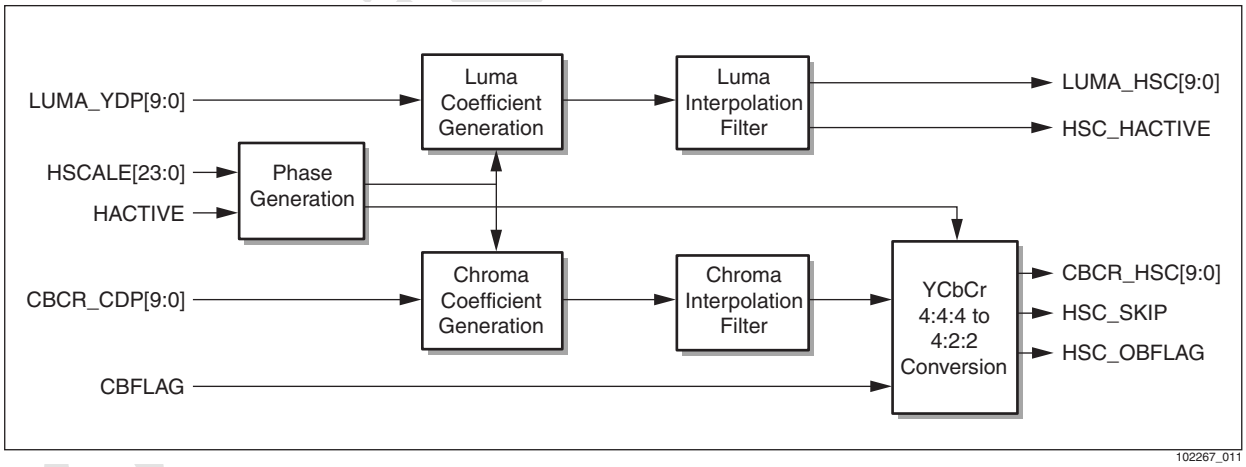
The vertical scaler supports the following requirements:

- Supports scaling from 1 to 7.998046875 in 1/512 steps.
- Supports 7 phases between horizontal lines.

3.5.1 Horizontal Scaling

The horizontal scaling function is shown in Figure 3-9. The primary purpose of this block is to scale down horizontally or reduce the number of pixels in each line. Horizontal scaling is implemented through multitap, poly-phase interpolation. Six taps of luma and four taps of chroma, each with 64 different phases, are used to accurately interpolate the value of a scaled pixel. In simple pixel- and line-dropping algorithms, noninteger scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position, providing more accurate information. This results in more aesthetically pleasing video and higher compression ratios in bandwidth-limited applications. In addition, the chroma path has a YCrCb 4:4:4 to 4:2:2 conversion block. It is important to note that prior to horizontal scaling the luma data path pre-filters the data to prevent aliasing artifacts

Figure 3-9. Horizontal Scaling Block Diagram



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The amount of horizontal scaling performed is based on two factors, the number of active pixels in a line entering the scaler along with the desired number of pixels leaving the scaler. The ratio of these two values determines the scaling ratio to be used in the following HSCALE formula:

Horizontal Scale Value (HSCALE) = (Scaling Ratio-1) x 2^{20}

For example, to achieve horizontal scaling of a BT.656 full-resolution (720 active pixels) image down to a half-resolution (360 active pixel) image, the scaling ratio would simply be 2, Scaling Ratio = 720/360. Using this value in the horizontal scaling equation yields a value of HSCALE = 2^{20} (0x100000). For 4:1 scaling the scale factor would be 4, Scaling Ratio = 720/180. Thus, the HSCALE register (0x418 to 0x41A) value must be set to 3 x 2^{20}, 0x300000.

For square pixel scaling, the same calculation is involved, except in this case, full-resolution has 640 active pixels for NTSC and 768 active pixels for PAL and SECAM. The scaling ratios and the HSCALE values are the same as in the BT.656 calculations (see Table 3-22).

Table 3-22. Common Scaling Resolutions: HSCALE and VSCALE Values

Resolution	HSCALE (0x418 to 0x41A) Value	VSCALE (0x41C to 0x41D) Value
Full-resolution Square Pixel 1:1	0x000000	0x10000
CIF 2:1	0x100000	0xFE00
QCIF 4:1	0x300000	0xFA00
Icon 8:1	0x700000	0xF200

Note that there is no dependence on the horizontal blanking delay (HBLANK) value that is programmed, as there have been in some previous generation video decoders.

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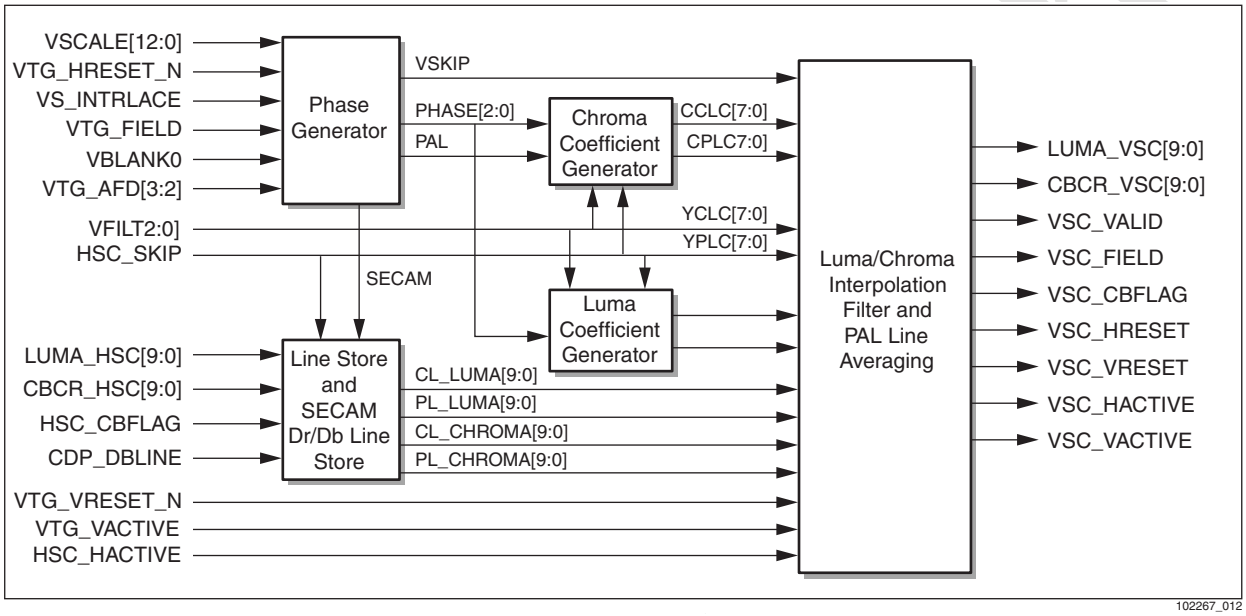
3.5.2 Vertical Scaling

The vertical scaling function is shown in Figure 3-10. The primary purpose of this block is to scale down vertically by reducing the number of lines. In addition, special functions are performed during SECAM mode for Dr/Db line-store and during PAL mode for line averaging.

Figure 3-10. Vertical Scaling Block Diagram



Valid video data does not start until line 21 for NTSC and line 33 for PAL/SECAM. In autoconfiguration mode, the default value for the vertical blanking delay, VBLANK (0x474 an 0x475) is set to 22 and 34, respectively, for each video standard. This register value, VBLANK, represents the number of half lines between the trailing edge of a vertical reset (after the first nine lines, which contain equalization and serration pulses) and the start of active video, while the VACTIVE (0x475 and 0x476) registers represents the number of half lines in the vertical active region that enter the vertical scaler.

As in the horizontal scaler, the two factors that determine the scaling process are the number of active lines going into the vertical scaler and the number of desired lines out of the scaler. The ratio of these two values determines the scaling ratio to be used in the VSCALE formula below:

Vertical Scale Value (VSCALE) = 216 – (Scaling Ratio-1) x 2^9

Thus, the vertical scaling ratio is determined by VACTIVE, the number of half lines coming into the scaler and desired number of half lines output from the scaler. For example, to achieve vertical scaling of an NTSC BT.656 full-resolution (487 active half lines) image down to a half-resolution (244 active pixel) image, the scaling ratio would simply be 2, Scaling Ratio = 487/244. Using this value in the horizontal scaling equation yields a value of VSCALE = 2^{16} - 2^9 (0xFE00). For 4:1 vertical scaling, the scale factor would be 4, Scaling Ratio = 487/122. Thus, the VSCALE register (0x41C and 0x41D) value must be set to 2^{16} – 3 x 2^9, 0xFA00.

For square pixel scaling, the same calculation is involved, except in this case, full-resolution has 480 active lines for NTSC and 576 active lines for PAL and SECAM.

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The scaling ratios and the VSCALE values are the same as in the BT.656 calculations (see Table 3-22).

There are two modes to the vertical scaler: interlaced and noninterlaced vertical scaling. In interlaced mode, the two fields are treated as part of a whole image to be displayed. Since the lines are interlaced, the scaling coefficients are set to reflect this by resetting the coefficients to 0 and VSCALE/2 to generate that offset. In noninterlaced mode, each field is treated independently and the scaling coefficients are always reset to 0. Control of these modes is accomplished through the VS_INTRLACE bit in the Vertical Scaling Control (0x41E) register.

3.5.3 Interpolation Filter and PAL Line Averaging

A multitap, polyphase filter is provided for vertical scaling of both luma and chroma data. The number of vertical taps is programmed by the user through the VFILT bits in the Vertical Scaling Control (0x41F) register. Care should be taken when selecting the number of taps for the vertical filter. The user may select 2, 3, 4, or 5 taps. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure that the needed data can fit in the internal line-store memory.

The line-store contains enough memory for 768 active pixels per line. When horizontally scaling, not all of the line-store memory needs to be used. This left-over memory can be used to store up to three additional lines of data, for a total of five lines worth. The amount of excess memory is determined by the horizontal scaling ratio. When there is no horizontal scaling, the line-store can hold one line, and provide for 2-tap filtering. When a horizontal ratio of 2:1 or greater is used, the line-store can hold two lines, allowing 3-tap filtering. When a horizontal ratio of 3:1 or greater is used, the line-store can hold three lines, allowing a 4-tap filtering.

Finally, when a horizontal ratio of 4:1 or greater is used, the line-store can hold four lines, allowing 5-tap filtering. Figure 3-11 illustrates this selection. Table 3-23 defines the vertical scaler tap selection.

Figure 3-11. Interpolation Filter Tap Selection Diagram

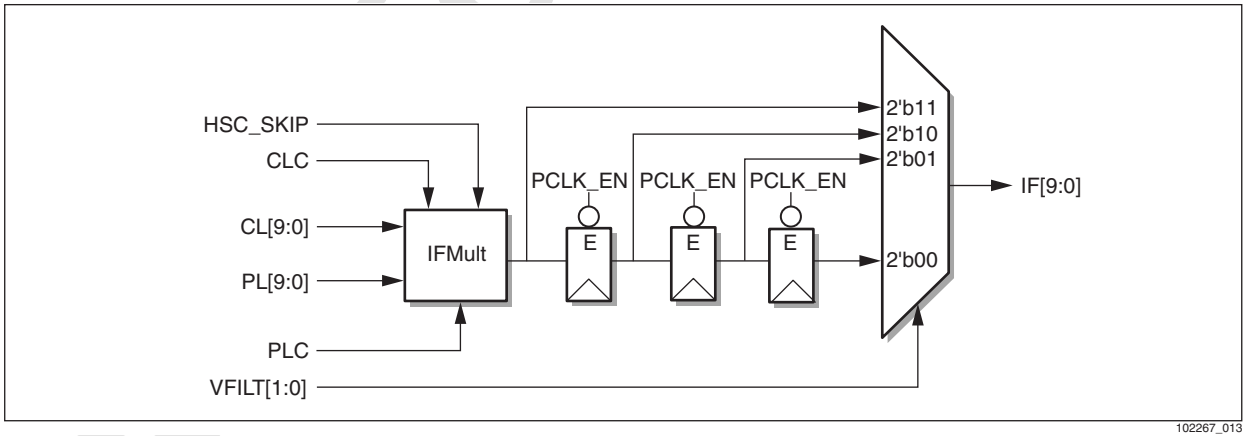

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Table 3-23. Vertical Scaler Tap Selection

Resolution	VFILT[2:0] Bits	Description
Full Resolution and Below	000	2-Tap Interpolation
½ Resolution (less than 384 active pixels per line) or below	001	3-Tap Interpolation
¼ Resolution (less than 193 active pixels per line) or below	010	4-Tap Interpolation
1/8 Resolution	011	5-Tap Interpolation

Two other functions take advantage of the line-store memory. There is line averaging in PAL mode and Dr/Db line storage in SECAM mode. In SECAM mode, Dr/Db values are passed through the chroma channel on alternating lines, thus a line-store is necessary so that Cr/Cb pairs can be obtained from combining the demodulated Dr/Db values.

In PAL mode, line averaging is done to enhance the color accuracy by averaging the chroma values of adjacent lines. The PAL line averaging and vertical scaling are done in the same filter. The coefficient generator for the chroma module has an input that indicates PAL operation and sets the coefficients to the 50 percent point. Line averaging can be disabled for sharper vertical transitions by setting the LINE_AVG_DIS bit in the Vertical Line Control register (0x41F).

3.5.4 Chrominance Interpolation Filter and Resampling

A 4-tap, 64-phase chroma interpolation filter is applied to YCbCr 4:4:4 chroma data. The output of the filter is offset by 512 (for 10-bit chroma data) and passed to the chroma resampling block. The chroma input to the scaler block is in 4:4:4 YCbCr format and is downsampled to 4:2:2 YCbCr after the data has been scaled. The resampling at half the rate can be done without a downsample filter because Cr and Cb signals are typically limited to approximately 1.3 MHz.

3.5.5 Image Cropping

Cropping enables the user to output any subsection of the video image. The HACTIVE and VACTIVE values can be programmed to start and stop at any position on the video frame, as illustrated in Figure 3-12. The start of the active area in the vertical direction is referenced to vertical reset, (the beginning of a new field). In the horizontal direction, it is referenced to horizontal reset (the beginning of a new line). The dimensions of the active video region are defined by HBLANK, HACTIVE, VBLANK, and VACTIVE. The vertical and horizontal blanking delay values determine the position of the cropped image within a frame, while the horizontal and vertical active values set the pixel dimensions of the cropped image.

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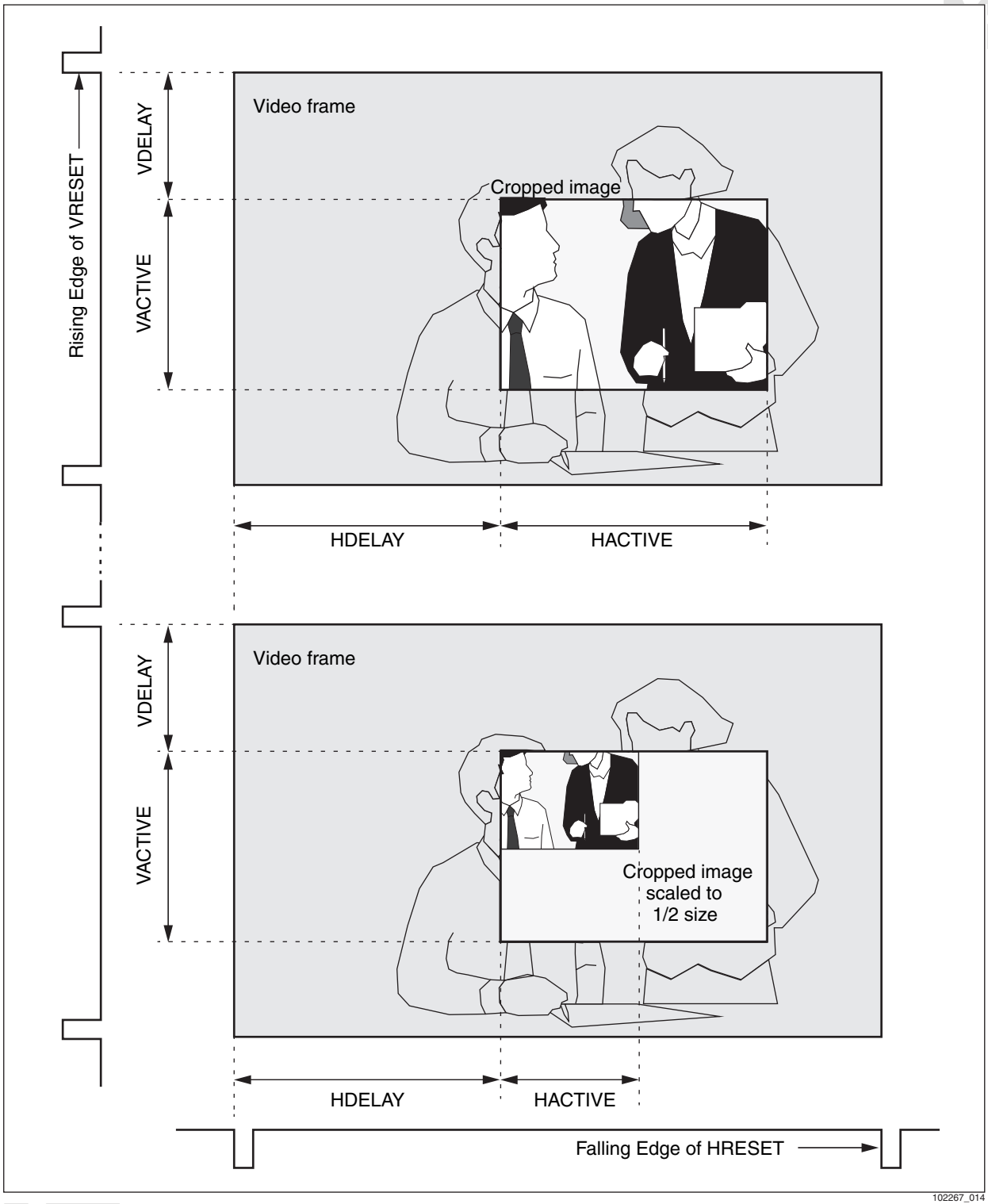
Figure 3-12. Effect of the Cropping and Active Registers



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3.5.6 Horizontal Cropping

To horizontally crop an image, the values of HBLANK (0x470 and 0x471) and HACTIVE (0x471 and 0x472) are adjusted. To maintain proper image location, the cropped values of HBLANK and HACTIVE should sum to less than or equal to the value of HBLANK + HACTIVE without cropping. To crop the left side of an image, increase HBLANK by the number of pixels desired. To crop the right side of the image, decrease HACTIVE by the number of pixels desired.

3.5.7 Vertical Cropping

To vertically crop an image, the values of VBLANK (0x474 and 0x475) and VACTIVE (0x475 and 0x476) are adjusted. To maintain proper image location, the cropped value of VACTIVE plus (VDELAY) should be less than or equal to the value without cropping.

The units of VBLANK and VACTIVE are half lines. To crop the top of the image, increase VBLANK by the number of desired lines multiplied by two. To crop the bottom of the image, decrease VACTIVE by the number of desired lines multiplied by two.

3.5.8 Scaling and Cropping Effects on SPI

The decoder has the following external timing signals available, which are affected by scaling and cropping as described below:

- Vertical Sync: Not affected by scaling or cropping
- Horizontal Sync: Occurs at the beginning of each line and is not affected by horizontal scaling
- Vertical Active: This signal is used to determine when the analog active video is valid. When vertical scaling occurs, this signal goes to its inactive state for the lines that should not be stored into the video memory. When image cropping is taking place, the length of Vertical Active is adjusted to provide fewer lines per field.
- Horizontal Active: This signal is used to determine when the analog active video is valid. Since horizontal video is always scaled, Horizontal Active contains more clocks than the pixels programmed into the Horizontal Active register. This signal is affected by the value programmed into the scaling register. When image cropping is taking place, the length of Horizontal Active is adjusted to provide fewer valid pixels per line.
- Valid Pixel Indicator: To determine which clocks are valid for storage into a video buffer, the Valid Pixel signal is high for valid pixels and low for invalid pixels. The Valid Pixel Indicator toggles throughout the entire line time to include blanking and synchronizing intervals even with cropping. This signal is affected by the value programmed into the scaling register.
- Odd/Even Field Indicator: Not affected by scaling or cropping
- Cb/Cr Indicator: Informs the user whether the pixel is Cb or Cr. When invalid pixels are encountered, the Cr, Cb order is therefore maintained from valid pixel to valid pixel, as flagged by this signal pin. This signal is affected by the value programmed into the scaling register.

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3.6 VBI Data Slicer

3.6.1 VBI Data Slicer Overview

The output of the SRC stage bypasses the Y/C separation block and passes data to the VBI slicer block. Once in the VBI slicer, the ADC data can be VBI sliced or output directly to the video output formatter in a raw mode.

From the SRC, the ADC samples are passed to the VBI block at the pixel rate, where the data is upsampled to 2x the pixel rate. Here, the data is oversampled at a 4x rate and then filtered with a –5.54 MHz to 5.54 MHz bandpass filter to reduce quantization noise. Filtered data is then passed through the data bit slicer—which detects VBI data according to the format for each standard. Finally, the data goes to a FIFO for output on the 656 interface or can be read from the VBI data registers.

Note that the parameters described in this section can be manually controlled through custom modes, but they are configured automatically in the autoconfiguration mode.

3.6.2 VBI Standards Supported

The VBI block is capable of slicing the world's VBI data standards. All sliced data can be inserted into the BT.656 or VIP video streams as an ancillary data stream. The BT.1364 specification discusses the specific formatting of ancillary data. The following VBI standards are available as ancillary data in BT.656 and VIP modes:

- Closed Caption/Extended Data Services (EIA-608)
- Wide Screen Signaling (625 line: ITU-R BT.1119, 525 line: EIAJ CPR-1204) including the Copy Generation Management System (CGMS)
- Gemstar1x
- Gemstar2x

The following VBI standards are available as ancillary data on BT.656 mode only:

- World System Teletext (ITU-R BT.653)
- North American Basic Teletext Spec. (NABTS EIA-516)
- Video Programming System using Enhanced Teletext Standard (VPS ETS-300-231)
- VITC/SMPTE (ITU-R BT.1366)
- Moji (ARIB STD-B5)

Where applicable, both 625-line and 525-line versions are supported.

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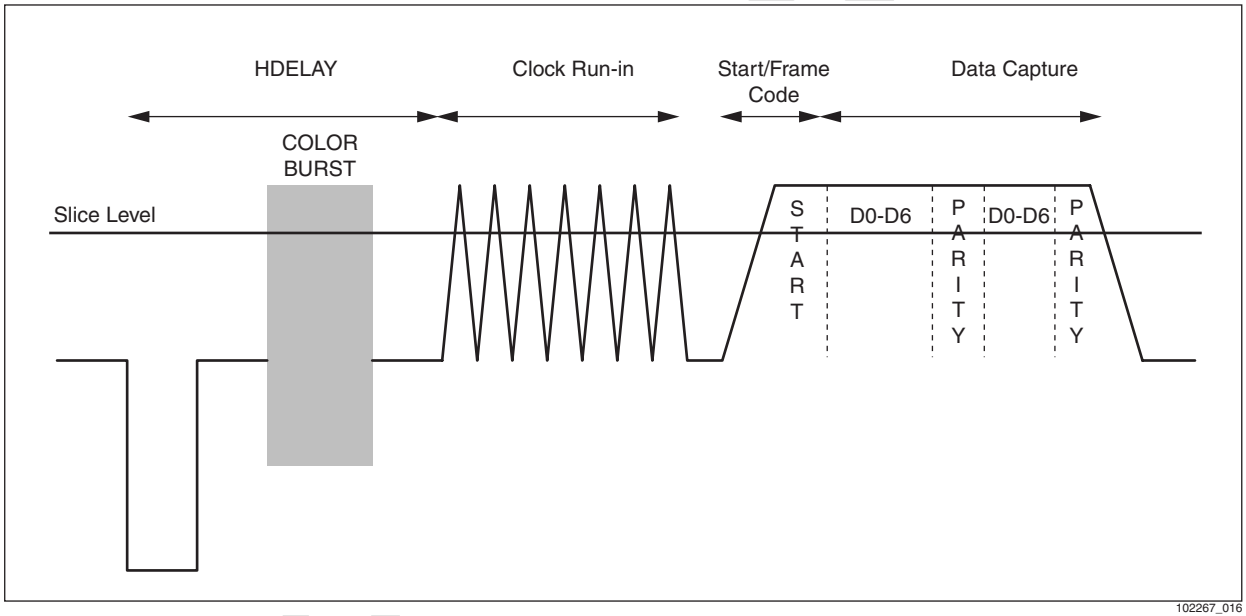
3.6.3 VBI Waveform Description

A detailed description of the incoming waveform will help to better understand the VBI function blocks. The model that is being used for the VBI block implementation is based on four basic input data formats: Closed Caption (CC), Wide Screen Signaling (WSS), Teletext (TTX), and VITC. All other signaling standards should fit into the format of these signals.

Figure 3-13 depicts a Closed Caption waveform. The main purpose of this figure is to illustrate the various signaling formats and how the various sections of the signal play a part into the VBI engine. The VBI engine starts when one of the following three events occurs: a vertical reset, time-out of data run-in, or the end of the previous line's data capture mode.

There are exceptions to the typical VBI waveform shown in Figure 3-13. For example, VBI standards such as WSS525, VITC525, and VITC625 do not have clock run-in periods. Another VBI standard that differs from the example given is the WSS625 VBI standard. It is a biphase modulated signal.

Figure 3-13. Typical VBI Waveform



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3.6.4 VBI Data Output

Low bit-rate VBI standards can be read back from the memory-mapped registers that are accessible by either the two-wire serial communication or VIP host port. The VBI data registers, which contain data for both even and odd fields, are updated every frame during the vertical blanking interval after capturing and decoding the data. The data standards available through the memory-mapped registers are the following:

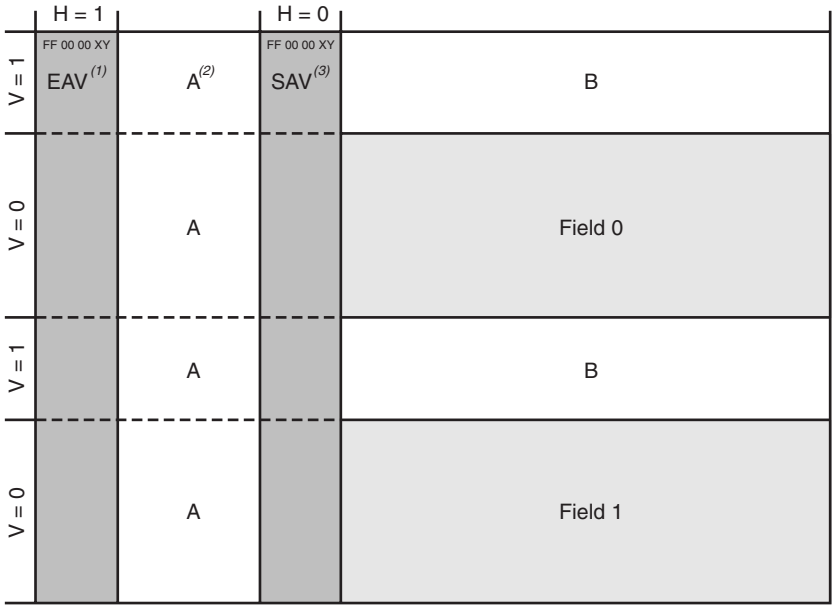
- Closed Caption/Extended Data Services (EIA-608)
- Wide Screen Signaling (625 line: ITU-R BT.1119, 525 line: EIAJ CPR-1204) including the Copy Generation Management System (CGMS)
- Gemstar1x
- Gemstar2x

There are four payload data FIFOs for Closed Caption, Gemstar 1x, Gemstar 2x, and WSS standards. The CC and Gemstar 1x FIFOs are 10 bytes deep, the Gemstar 2x are 20 bytes deep, and the WSS FIFO are 6 bytes deep. By reading the Closed Caption Data (0x445), Gemstar 1x Data (0x447), Gemstar 2x Data (0x449) and WSS Data (0x44B) registers, the user can access the FIFOs for each of these standards.

After the data is read, the data FIFO pointer is automatically incremented to the next byte of information. With each data byte loaded to a register for reading, a status byte is updated accordingly. The status byte indicates whether a parity error has occurred for CC, Gemstar 1x, Gemstar 2x. It also indicates if the byte was captured from the odd or even field (CC or XDS), and the byte number. Two bits indicating FIFO overflow or empty are also included in the status byte.

Both high bit-rate and low bit-rate sliced data can be inserted in the video output stream during horizontal blanking intervals (areas labeled A in Figure 3-14) as ancillary data. The VBI slicer uses a FIFO and related control signals to pass the data to the video output formatter for insertion. Ancillary data insertion is enabled by setting high the ANC_DATA_EN bit in the Video Out Control 1 (0x404) register.

Figure 3-14. Blanking Regions



Footnotes:
(1) EAV = End of active video
(2) A = Ancillary data
(3) SAV = Start of active video

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3.6.5 Preprogrammed VBI Standards

The VBI slicer block can operate in a predefined/autoconfiguration mode or in a user-defined custom mode. The VBI slicer provides access to 34 VBI lines in one frame of video; 17 lines are provided per odd and even field. The VBI decoder block can be assigned a VBI standard to be sliced on a line-by-line basis. Each VBI line can be individually programmed to use either the predefined autoconfiguration VBI settings or the user programmable custom settings.

There are eight preprogrammed settings of VBI decoding for 525-line mode and six preprogrammed settings for the 625-line mode. Each line, in either odd or even field, can be decoded for each of the modes listed in by programming the VBI Line Control 1 to VBI Line Control 17 (0x424 to 0x434) registers. The VBI block can decode any combination of the available 34 lines of VBI information and output the information to the memory mapped data registers or through the BT.656/VIP data stream. Due to the higher bit-rates of Teletext, this data is only available as ancillary data within the BT.656/VIP stream.

There are a total of five configuration registers consisting of 17 total lines; each fieldname in the configuration register is defined as an odd and even line. The decoding of each line is defined by an 8-bit register value programmed by the user through the VBI Line Control [1:17] registers. Available preprogrammed VBI slice standards are listed in Table 3-24.

Table 3-24. Available Preprogrammed VBI Slice Standards

525 Line Modes VBI Line Control Value		625 Line Modes VBI Line Control Value	
0000	No VBI Data Slicing	0000	No VBI Data Slicing
0001	WST525-B	0001	WST625-B
0010	WST525-C (NABTS)	0010	WST625-A
0011	WST525-D (Moji)	0011	RESERVED
0100	WSS525	0100	WSS625
0101	VITC525	0101	VITC625
0110	CC525	0110	CC625
0111	Gemstar 1x	0111	RESERVED
1000	Gemstar 2x	1000	RESERVED
1001	RESERVED	1001	VPS
1010	Custom VBI 1	1010	Custom VBI 1
1011	Custom VBI 2	1011	Custom VBI 2
1100	Custom VBI 3	1100	Custom VBI 3

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For each control register, the fieldname is defined as an 8-bit value with the most significant nibble of the fieldname used to indicate the odd field and the least significant nibble used define the even field. To program the VBI engine to decode a specific standard or a particular line, both the odd and the even registers of the fieldname must be programmed to decode that set standard.

For example, upon reset, VBI_LINE_CONTROL4 (0x427) is set to a default value of 0x00 or "No VBI data slicing" on line 4 for odd or even field. However, if the user wished to decode line 4 from the odd video field with WST525 and the even video field of line 4 with Gemstar 1x, then VBI_LINE_CONTROL4 would need to be programmed as 0x47. For a complete list of options, refer to the description of the various VBI registers in Section 5 of this document.

3.6.6 Custom Data Transmission of VBI Data

The VBI decoding block also provides the flexibility for the user to define each parameter through various registers and fieldnames. Once programmed, the decoder extracts the VBI information from the video stream and outputs the decoded data to the video output formatter (VOF) block or to the memory mapped registers. To initiate custom program mode, the control register, VBI Line Control {1:17}, for a particular line must be set to Custom VBIx mode.

Three programmable registers are available for customization and are Autoconfigure by default. These registers, VBI Custom{1:3} Horizontal Delay, VBI Custom{1:3} Time-out, and VBI Custom{1:3} Increment, can be custom-configured individually to support specific user-defined VBI requirements. In the default configuration, the VBI Custom 1 registers are set to decode Closed Caption 525; VBI Custom 2 registers are set to decode WSS625; and VBI Custom 3 registers are set to decode WST525, System C.

Each of these registers can be custom-configured through the two-wire serial communications port or VIP host interfaces. Refer to Section 5 for the Custom {1:3} settings and their fieldnames. Each of these fieldname values is programmable and allows the user to custom-modify the VBI decode engine.

3.6.7 Miscellaneous VBI Configuration

Additionally, there are miscellaneous configuration registers, VBI Miscellaneous Config 1, TTX Packet Address {1:3} (0x43C to 0x43F), used to customize Teletext decoding and reset the VBI FIFOs for Gemstar 1x/2x, WSS, and CC. In the case of Teletext decoding, the upper and lower limits of the Teletext packet information can be specified through these registers and fieldnames, as well as the programming of alternative framing packets. Furthermore, the registers can be programmed to enable hamming comparison.

Alternatively, the miscellaneous configuration registers can also be used for modifying the parameters in the predefined or autoconfiguration modes. A different frame code can be substituted for the autoconfiguration mode with little user effort. For example, modifying the VBI Miscellaneous Configuration 1 (0x43C) register, bits FC_ALT1_TYPE, with the same code as the VBIMODE, does this.

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3.6.8 VBI Controller

Control of the VBI engine is through a state machine, which monitors the incoming video and nonvideo data and initiates the VBI decoding process based on user defined parameters of HDELAY, CRILK, FCBIT, and VBx_BYTE_COUNT. Other inputs to the VBI state machine are from the Vertical Timing Generator (VTG), which outputs both the vertical and horizontal reset. See Table 3-13 in Section 3.6.3. The CC waveform consists of four major sections: hdelay, clock run-in, data run-in, (start/frame code) and data payload (data capture).

Through the state machine, the VBI engine starts when either one of three conditions occurs: vertical reset, a time-out of data run-in, or at the end of the previous line's data capture mode. When a horizontal reset occurs, the VBI engine goes into BREEZE state for HDELAY clock cycles. Once HDELAY counter expires, it goes into a Clock run-in state (CRILK) for the number of programmed clock run-in cycles to be captured. It then switches to data run-in state (FCBIT). The VBI engine stays in this state for FCBIT to capture the start bits, or the framing code in case of the Teletext format. Then it switches to Data Capture mode to capture as many bits or bytes specified by VBIx_CAP_COUNT. Note that the parameters described here can be manually controlled through the custom modes, but they are configured automatically in the autoconfiguration modes.

A discrete time oscillator determines the sample rate and positioning of the sample points for each of the various VBI standards. A 14-bit counter, incremented by VBIx_BITINC with each VBI clock, generates a pulse to mark each sample point. This is used to measure sample periods as the state machine sequences through the different stages of the VBI waveform.

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3.6.9 Clock Run-In Synchronization

During the clock run-in cycles, the logic performs three functions:

1. Measures the slice level
2. Synchronizes the slice timing to the clock run-in edges
3. Determines whether the clock run-in cycle has the expected frequency.

The slice level detector determines the "slice level" used to distinguish between a logical 1 or 0 data sample. At the start of the clock run-in signal, an initial assumption of 1.75 x the back-porch level is made for the initial slice level. This number is used as a seed to the slice level calculation engine. Samples are taken at VBIx_SLCNT clocks apart. Starting with the first zero crossing of the clock run-in, four samples are taken, and the average of those samples is data and data run-in slice level.

During clock run-in, the logic detects the number of clock run-in cycles specified by VBIx_CRILK. These clocks are detected in terms of rising edges on the input waveform. At the end of this search, frequency lock is declared if the elapsed time lies within the range specified by the VBIx_CKRGH and VBIx_CKRGL registers. These registers specify time in terms of the VBI sample rate period. The DTO that is controlled by the VBIx_BITINC parameter is used to count the sample periods. In other words, the logic determines whether a defined number of clock run-in cycles (VBIx_CRILK) elapsed in the expected time (VBIx_CKRGH and VBIx_CKRGL).

If frequency lock is determined, the sample period DTO is synchronized one more time to the last negative edge of the clock run-in cycles. In the absence of frequency lock, the state machine is reset to idle and waits for the next line.

3.6.10 VBI Special Cases

There are some exceptions to the typical example of the CC VBI, as follows:

- For WSS525, VITC 525, and VITC625 VBIx_SKIP_DRI should be set to 1. This implies that only one clock run-in cycle is detected, and the data run-in stage should be skipped. Instantly, the VBI state machine switches to data capture mode.
- WSS625 uses biphase modulation, where the VBI engine groups the decoded bits into a 24-bit words, which are sent to the Output Formatter block. The detected bits are decoded into a 1 or 0 bit, depending if 111000 or 000111, respectively.
- For Teletext, if Hamming checks are enabled through VBIx_HAM_EN, bits 3 through 0 of the framing code are used to match the odd bits of a byte detected in transmission order. The packet address range is also checked, and if it is not valid, the captured data is not stored into the FIFO.

3.6.11 Raw Mode VBI

In raw mode, data samples are sent through the VBI slicer without any processing directly to the video output formatter. Raw VBI data is passed directly from the SRC output to the output formatter during the active video region of the VBI lines for decoding and or processing by an external processor or software. Within the VBI block, the raw ADC samples are converted to a decoder sample rate of 2x oversampled VBI samples of 2 bytes each. Raw mode VBI is enabled by setting the VBIHACTRAW_EN bit high in the Video Out Control 1 (0x404) register. The order of the raw samples presented on the 8 VID_DATA pins is configurable through the SWAPRAW bit in the Video Out Control 2 (0x405) register.

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3.7 Video Output Formatting

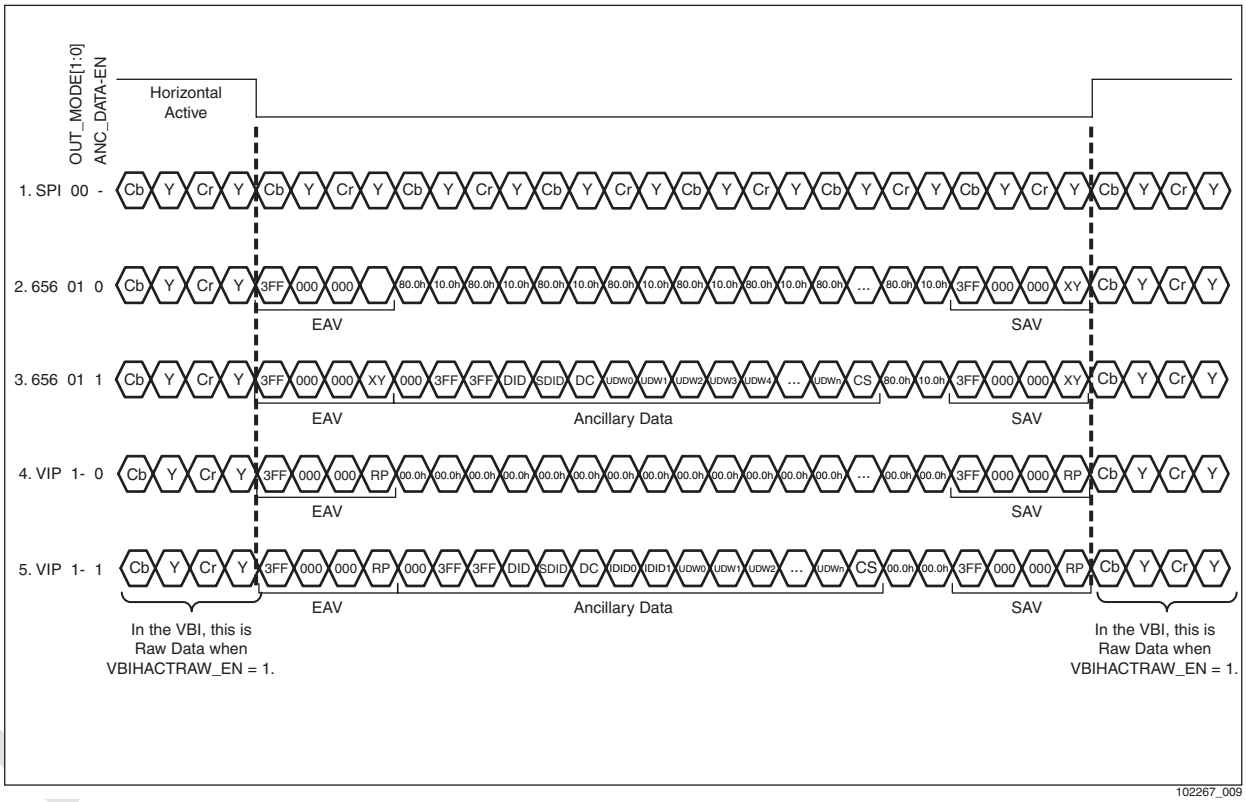
The Video Output Formatter (VOF) module is at the end of the data processing pipeline. It is responsible for formatting the 10-bit luma and 10-bit chroma data into one of the following video output stream formats:

- Synchronous Pixel Interface (SPI) mode where the video is SPI coded, 4:2:2 subsampled, and timing information is provided through separate sync signals
- ITU-R BT.656 mode where timing control codes are embedded within the data stream
- VIP1.1 and VIP2 modes, both a super set of ITU-R BT.656 that supports advanced features such as square pixel sample rates and scaled video. VIP1.1 and VIP2 are very similar, with minor differences in control code formatting.

3.7.1 Output Format Options

The OUT_MODE bits in the Video Out Control 1 register (0x404) select which of the video output formats to enable. Also, the video data in the output stream can be represented as either 8-bits or 10-bits wide depending on the setting of the MODE10B bit in the same register. In 8-bit mode, the internal 10-bit video data is rounded to 8 bits and presented on the upper most significant bits of the VID_DATA pins. The VOF is also responsible for inserting sliced and raw VBI data into the pixel stream embedded as ancillary data. Figure 3-15 shows the various output formats along with ancillary data.

Figure 3-15. Output Stream Formats



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3.7.2 Synchronous Pixel Interface Mode

In the Synchronous Pixel Interface (SPI) mode, the device outputs all pixels synchronous with PIXCLK, both horizontal and vertical blanking interval pixels and active pixels. Unlike the BT.656 or VIP output modes where timing control codes are embedded in the digital data stream, SPI video timing information is conveyed through the following external synchronization signals, available on separate output pins:

- Vertical Sync
- Horizontal Sync
- Vertical Active
- Horizontal Active
- Valid Pixel Indicator
- Odd/Even Field Indicator
- Cb/Cr Indicator

The polarity of each of these signals is independently selectable using the POLAR bit in the Video Out Control 4 register (0x407).

Figure 3-16 illustrates the relationship of the external timing signals over fields. Figure 3-17 illustrates the relationship of Horizontal Reset and the active portion of the line. Figure 3-18 illustrates the operation of the VALID and CBFLAG indicators.

The VOF also provides the pixel clock output, PIXCLK, which can be inverted using the CLK_INVERT register bit. The pixel clock output can be set to run continuously or to be gated by either the VALID pixel indicator or by the logical AND of the VALID pixel indicator with ACTIVE indicator. The clock-gating scheme is selected using the CLK_GATING bits of the Video Out Control 2 register (0x405). Note that the ACTIVE indicator in the same register can be set to represent either composite-active-vertical and horizontal-active, or simply horizontal-active. The VALID indicator can similarly be configured to represent either nonscaled pixels or represent the logical AND of the VALID indicator and the ACTIVE video indicator. This is controlled by the VALIDFMT bit in the same Video Out Control 2 register (0x405).

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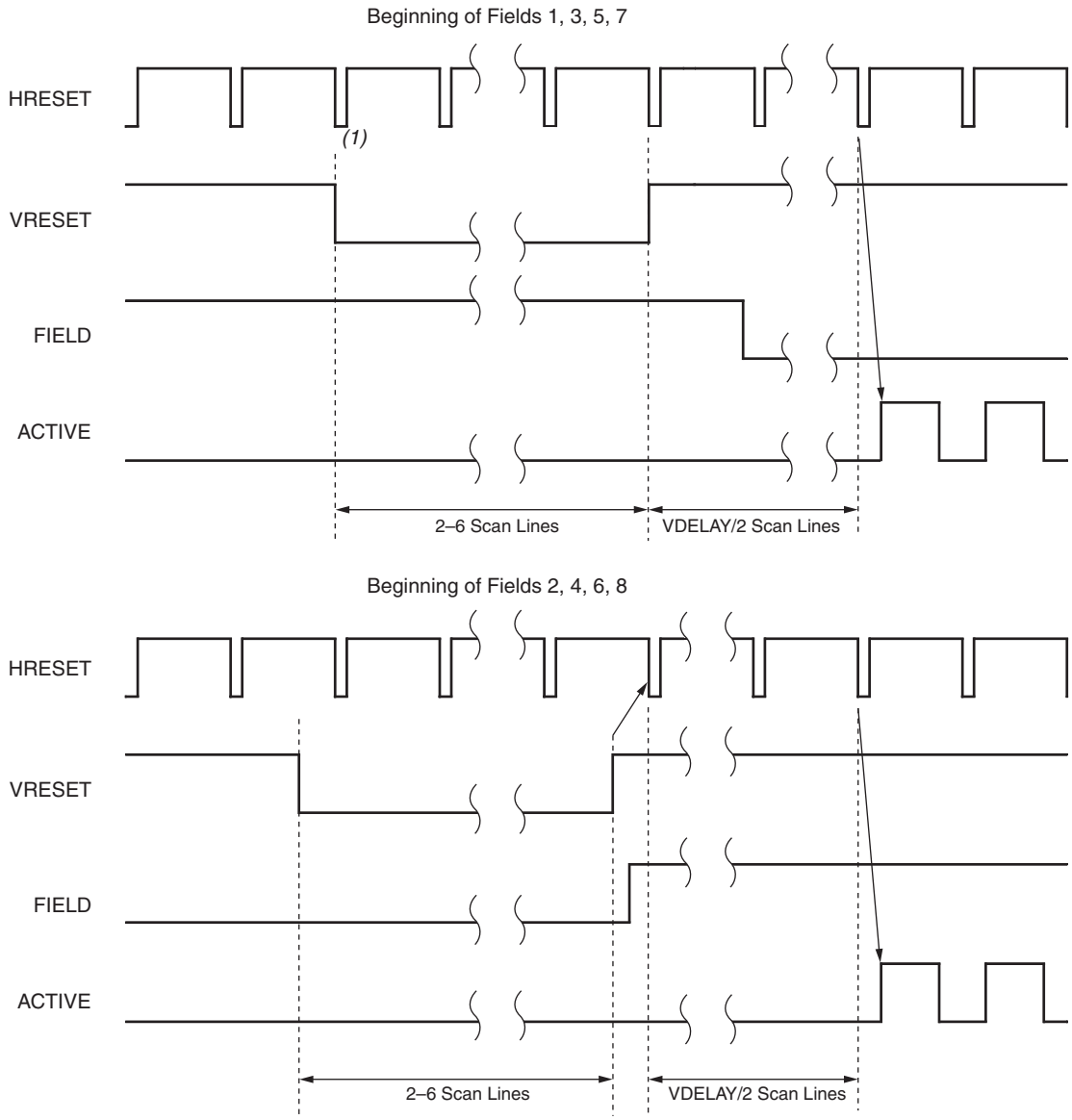
Figure 3-16. SPI Mode External Field Timing Signals



GENERAL NOTE:

1. ACTIVE pin may be programmed to be composite ACTIVE or horizontal ACTIVE.
2. ACTIVE, HRESET, VRESET, and FIELD are shown here with their default polarity. the polarity is programmable via the VPOLE register.
3. FIELD translations with the end of horizontal active video defined by HDELAY and HACTIVE.

FOOTNOTE:

(1) HRESET Precedes VRESET by two clock cycles at the beginning of fields 1, 3, 5, and 7 to facilitate external field generation.

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Figure 3-17. SPI Mode External Line Timing Signals

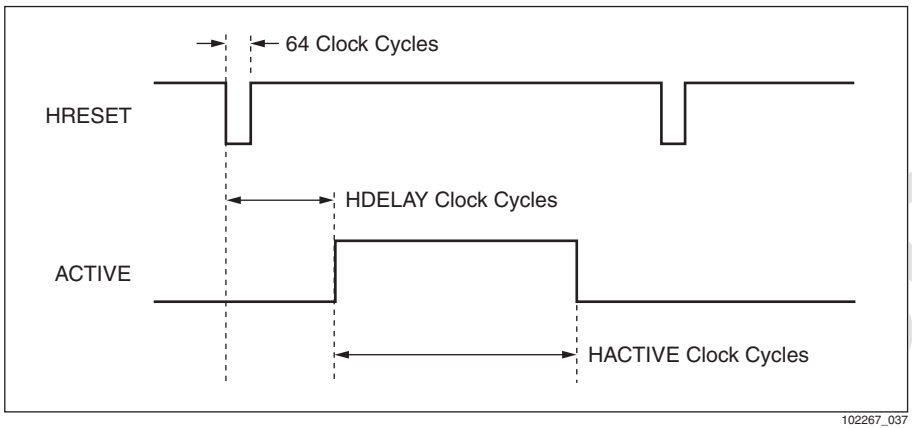
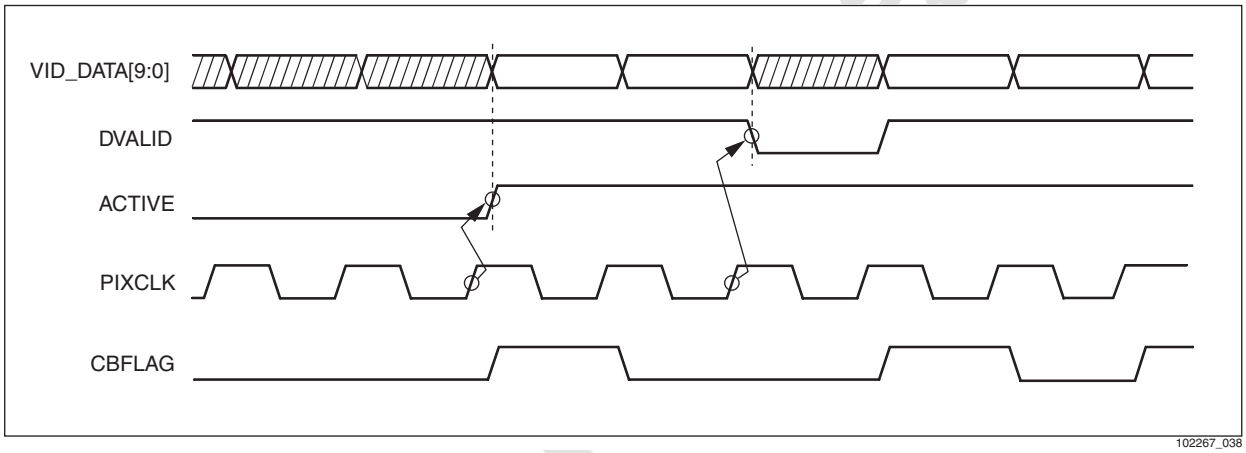


Figure 3-18. SPI Mode VALID and CBFLAG Indicators



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3.7.3 Control Codes

For the BT.656 and VIP modes, Start of Active Video (SAV) and End of Active Video (EAV) control codes are inserted into the output video stream. The 8-bit SAV/EAV codes are comprised of four timing reference bits: Task (T), Field ID (F), Vertical Blanking (V), and Horizontal Blanking (H). The T, F, and V bits only change during EAV codes. The remaining four bits are Hamming-coded error protection and correction bits in BT.656 mode or 0x0 in VIP modes. If 10-bit output mode is enabled, 0s are appended as LSBs to the end of the SAV/EAV codes.

The value of the task (T) bit depends on the output mode. In BT.656 mode, the T bit is 1. For VIP 2 mode, the T bit is determined by the TASKBIT_VAL bit in the Video Out Control register (0x404). In VIP 1.1 mode, the T bit is 0 during the vertical blanking interval if raw data is being substituted and is 1 otherwise.

The value of the field ID (F) bit toggles in the EAV code after an "end-of-field" signal from the video timing generator is asserted.

The value of the vertical blanking (V) bit switches to 1 in the EAV code when the end of vertical active is detected. The time at which the V bit switches to 0 in the EAV code is dependant on whether the output formatter is in VIP or BT.656 mode. In VIP mode, the line at which the V bit switches to 0 is determined by the Vertical Blanking Delay registers (0x474 an 0x475). In BT.656 mode, the line at which the V bit switches to 0 is determined by the Vertical 656 Blanking Delay register (0x477). The values programmed into these registers must represent the number of half-lines after a vertical reset. When the VIP_OPT_AL bit is set high in the Video Out Control 3 register (0x406), this forces the V bit to switch to 0 in the EAV code after the Vertical 656 Blanking Delay time when in VIP output mode.

The value of the horizontal blanking (H) bit is 0 in an SAV and 1 in an EAV.

In BT.656 or VIP modes, the video output formatter can limit the 8 MSBs of luma and chroma samples to the range 1–254. This is done to ensure the upper eight bits do not contain 0x00 or 0xFF, which are used in these modes to indicate the presence of control codes. This is accomplished by setting the VIPCLAMP_EN bit of the Video Out Control 3 register (0x406) high. Also, when VIPBLANK_EN is set high, the output formatter will blank (Y=16, Cb and Cr=128) the luma and chroma samples for the following conditions.

- During the horizontal blanking interval (i.e., between EAV and SAV)
- When V bit is 1 between SAV and EAV (if VBIHACTRAW_EN is not set)

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3.7.4 Ancillary Data Insertion

Sliced vertical blanking data can be inserted into the pixel stream output during the horizontal blanking interval as ancillary data. The ancillary data will be prepended by the appropriate control codes for the output format that is enabled, BT.656 or VIP. Table 3-25 is an example of 10 bytes of ancillary data, along with the control codes and headers that are used for each of the formats.

Table 3-25. Example 10-Byte Ancillary Data Packet

	BT.656 / BT.1364			VIP		
	A	**B**	**C**	**D**	**E**	**F**
MODE10B	0 (8-bit)	0 (8-bit)	1 (10-bit)	0 (8-bit)	0 (8-bit)	1 (10-bit)
DCMODE	0	1	n/a	0	1	n/a
1. ADF0	0x00	0x00	0x00.0	0x00	0x00	0x00.0
2. ADF1	0xFF	0xFF	0xFF.C	0xFF	0xFF	0xFF.C
3. ADF2	0xFF	0xFF	0xFF.C	0xFF	0xFF	0xFF.C
4. DID	0x55 or 0x91	0x55 or 0x91	0x55.0 or 0x91.0	0x55 or 0x91	0x55 or 0x91	0x55.0 or 0x91.0
5. SDID	n,e,00,dt[3:0]	n,e,00,dt[3:0]	n,e,00,dt[3:0],00	n,e,00,dt[3:0]	n,e,00,dt[3:0]	n,e,00,dt[3:0],00
6. DC	n,e,00 0011	n,e,00 1010	n,e,00 0010 10	n,e,00 0011	n,e,00 1010	n,e,00 0011 00
7.	UDW0	UDW0	UDW0	IDID0	IDID0	IDID0
8.	UDW1	UDW1	UDW1	IDID1	IDID1	IDID1
9.	UDW2	UDW2	UDW2	UDW0	UDW0	UDW0
10.	UDW3	UDW3	UDW3	UDW1	UDW1	UDW1
11.	UDW4	UDW4	UDW4	UDW2	UDW2	UDW2
12.	UDW5	UDW5	UDW5	UDW3	UDW3	UDW3
13.	UDW6	UDW6	UDW6	UDW4	UDW4	UDW4
14.	UDW7	UDW7	UDW7	UDW5	UDW5	UDW5
15.	UDW8	UDW8	UDW8	UDW6	UDW6	UDW6
16.	UDW9	UDW9	UDW9	UDW7	UDW7	UDW7
17.	Fill Byte	CS	CS	UDW8	UDW8	UDW8
18.	Fill Byte	—	—	UDW9	UDW9	UDW9
19.	Checksum	—	—	Checksum	CS	Checksum
20.	—	—	—	Fill Byte	—	Fill Byte
UDW Clamp:	1-254	1-254	1-254.75	Not Required	Not Required	Not Required

Key:
n: not e
e: even parity of remaining bits
dt: data type of ancillary data (sent from VBI slicer)

The ancillary data insertion can be enabled by setting high the ANC_DATA_EN bit of the Video Out Control 1 register (0x404). For the VIP modes, the IDID0 and IDID1 values that are embedded within the stream can be customized by programming the Ancillary IDID0 and IDID1 registers (0x408 to 0x40B) with the desired value. Alternatively, the VBI slicer line count can be used as the IDID0 bytes by setting the

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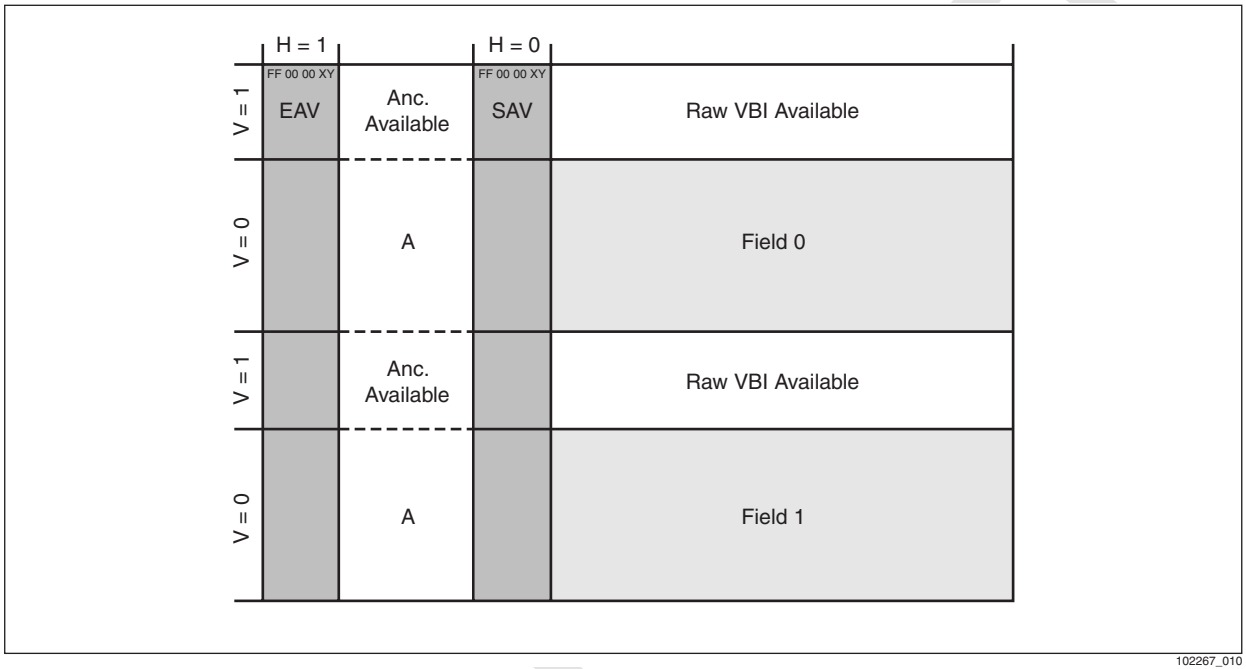
IDID0_SOURCE bit high in the Video Out Control 3 register (0x406). The data count (DC) byte can be configured to represent either 4-byte blocks of UDWs—with byte padding to remain DWORD aligned or the actual number of UDWs. This option is selected through the DCMODE bit of the Video Out Control 3 register (0x406).

In addition to providing sliced VBI data as ancillary packets, raw VBI sample data can be substituted into the horizontal active region of the vertical blanking interval. Figure 3-19 shows the ancillary region along with the raw VBI regions.

Figure 3-19. Ancillary Region and Raw VBI Regions



This raw data is from the luma/composite output of the ADC after it has been sample-rate converted to 13.5 MHz and 2x upsampled by the VBI decoder/slicer. Raw data substitution is selected by setting the VBIHACTRAW_EN bit high in the Video Out Control 1 (0x404) register. In the SPI mode, the raw data is substituted when VACTIVE is 0 and HACTIVE is 1. In BT.656 or VIP modes, the raw data is substituted between SAV and EAV codes when the V bit is 1.

By default, the even samples are placed where the chroma samples would occur, and the odd samples are placed where the luma samples would occur. If the SWAPRAW bit of the Video Out Control 2 (0x405) register is set high, odd raw samples are placed where chroma samples would occur and the even raw samples are placed where the luma samples would occur.

3.7.5 Blue Field Generation

The video output formatter also contains a blue field generator. This function replaces the input luma and chroma samples with a field of blue pixels, Y=35, Cb=212, Cr=114. The blue field generator can be set to automatically output these pixels' value when the video decoder determines that there is no lock-able signal on the input. This is configured by setting high the BLUE_FIELD_EN bit in the Video Out Control 1 (0x410) register. The blue field generation can be forced on by setting the BLUE_FIELD_ACT bit in the same register, regardless of the state of the input video waveform.

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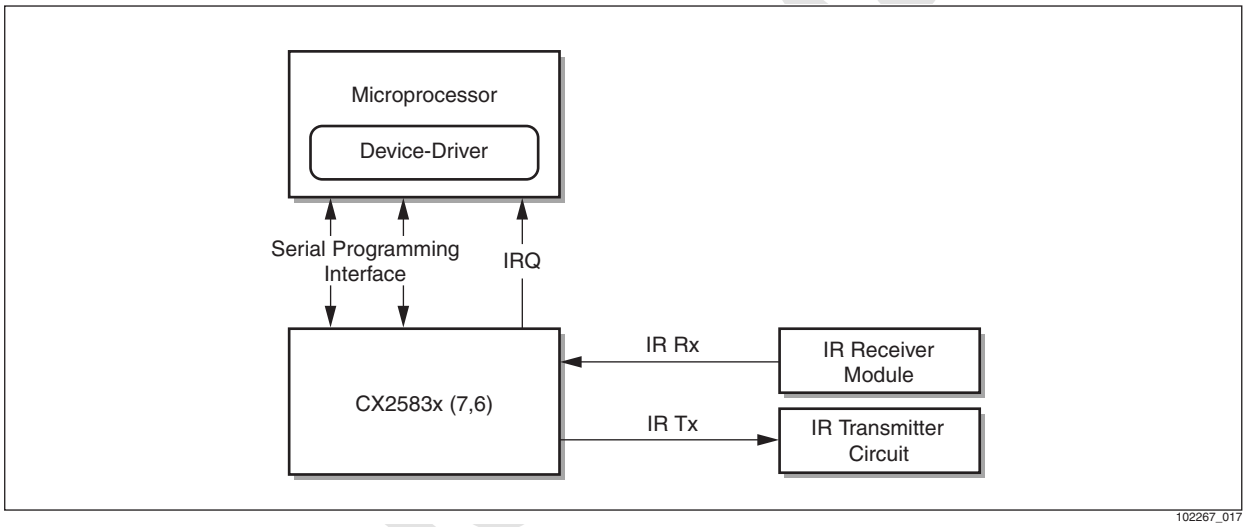
3.8 Infrared Remote Controller

3.8.1 Architecture Overview

The Infrared Remote (IR) controller, shown in Figure 3-20, is a generic interface that can be used to communicate with a wide variety of commercial infrared remote control units. This interface provides modulation and demodulation logic, a set of programmable pulse timers, and a set of FIFOs. Enough hardware support is provided to off-load the microprocessor from performing individual bit modulation and demodulation and data transmission and reception. However, individual infrared protocols are not decoded or encoded by the hardware, such as Sharp ASK or Universal Remote. Instead, this task is left to the device driver software that controls the port. This division between hardware and software alleviates the microprocessor from performing the time-consuming bit manipulation.

Figure 3-20. Infrared System Diagram



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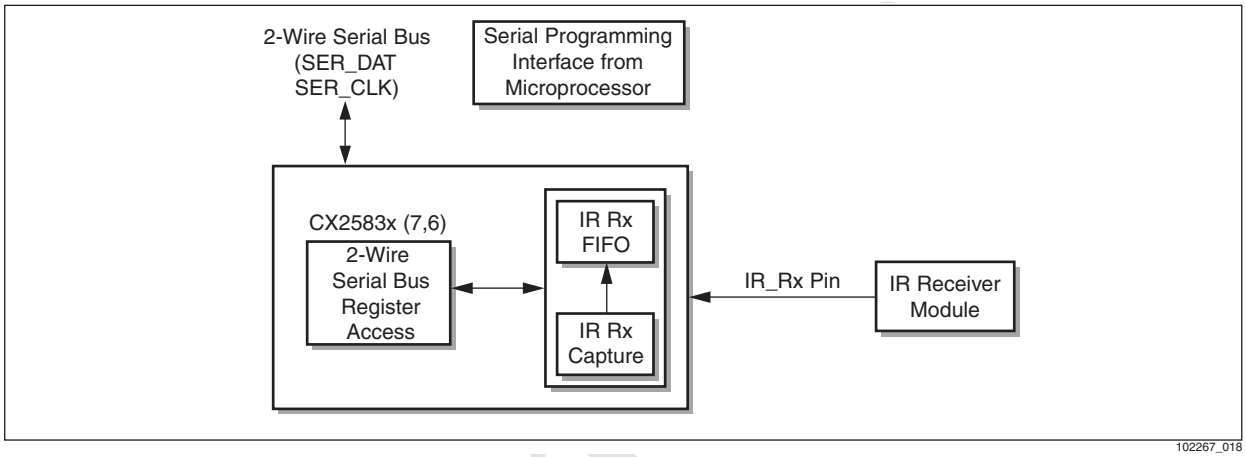
3.8.2 IR Receiver

The IR receiver block, shown in Figure 3-21, captures bits and timing information from the IR receiver module. Data can either be in the form of a modulated or an unmodulated signal. For modulated signals, the IR port contains a demodulator which can be enabled. The demodulated signal is then used to start and stop a counter which measures the width of the pulse. The frequency of the clock which drives the pulse width counter can be varied, depending on the total duration of the longest pulse which must be measured. Next the timing value from the pulse width counter is stored to the receive FIFO, along with the level of the pulse just measured and a tag to indicate the data is valid. When data stops being received, the input no longer transitions, and the pulse width counter overflows. This overflow signals the end of the transmission.

Figure 3-21. IR Receiver Block Diagram



3.8.2.1 Receive Data Demodulation

A modulated signal encodes 1s and 0s through the use of a carrier which either transitions at a high frequency (compared to the rate of the incoming data stream), or does not transition. In most circumstances, a high frequency transition, called a mark, represents a logical 1, while the absence of any input signal transitions, called a space, represents a logical 0. The IR port is programmable such that both a mark and a space can represent either a 0 or a 1. An unmodulated signal is simply represented by the logic level received on the IR_RX pin. As with modulated signals, the polarity of an unmodulated signal is programmable and can be programmed for inverse sense.

A programmable clock is used for all receive logic. The frequency ranges from 27 MHz down to 823.97 Hz. If the demodulation logic is used, this programmable clock rate must be 16 times the frequency of the input carrier. All incoming data is first synchronized to the IR port's internal clock. This 16-bit Receive Clock Divider bit field is used to control the IR port's receive clock rate. The receive clock is used to drive both the demodulation logic and the receive pulse width timer. The IR RX Clock Divider (0x208 and 0x209) registers are used as the modulus for a 16-bit down counter and is decremented at half the video clock rate (108 MHz/2). Each time the counter reaches 0 or the IR RX Clock Divider registers are written, the contents of this register are reloaded to the counter. Each time the counter wraps to 0, a receive clock pulse is signaled to the demodulation logic and the RX pulse width timer. The IR RX Clock Divider bit fields can be programmed with any value from 0x01 to 0xFFFF.

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The RX clock rate, given a set Receive Clock Divider value, is calculated using the equation below:

$$RxClkFreq = \frac{108/2}{(RxClkDivider + 1)}$$

Next, the demodulation logic looks for rising-edges on the input signal. Once a rising-edge is detected, the logic expects another rising-edge every 16 RX clock cycles. To compensate for jitter in the receive carrier or if the carrier frequency is a noninteger multiple of the RX clock, a programmable window function is implemented which allows the next rising-edge to fall within a range of 16 clock cycles plus or minus three to four clocks. If the edge occurs within the programmed limits, the demodulator passes the data to a persistence counter. The persistence counter ensures that the receiver encounters four consecutive rising-edges at the predicted time in order for a mark to be output from the demodulator. Likewise, when the carrier burst stops, the demodulator does not output a space until four time periods elapse and a rising-edge has not been detected. This filtering function makes the demodulator somewhat resistant to noise if carrier transitions are occasionally missed. Marks and spaces are then output to the low-pass filter.

3.8.2.2 Low-Pass Filter

Ambient light can cause high-frequency noise to be picked up by infrared receivers. To eliminate this noise, a low-pass filter is used. A programmable 16-bit down counter measures the duration of each demodulated or raw unmodulated pulse which is input to the receiver.

The 16-bit IR Low-Pass Filter (0x218 and 0x219) registers are used to prevent pulses under a minimum width from being measured by the receive pulse counter. These registers are used as the modulus for a 16-bit down counter that is decremented at half the video clock rate (108 MHz/2). The counter reloads using the value programmed to this register each time a qualified edge is detected as programmed through the EDG bits in the IR Control 1 (0x200) register. Once the reload occurs, the counter begins decrementing. If the next programmed edge occurs before the counter reaches 0, the pulse measurement value is discarded, the filter modulus value is reloaded, and the next pulse measurement begins. Thus, any pulse measurement that ends before the counter reaches 0 is ignored.

For pulses that are greater than the minimum selected, the filter counter decrements to 0, and remains at 0 until the next qualified edge is encountered. Pulse measurements are only stored to the RX FIFO when the filters counter reaches 0. The equation below is used to calculate the minimum pulse width that can be measured, given the filter register modulus value. To enable the filter, the IR Low-Pass Filter register can be programmed with any value from 0x0004 to 0xFFFF (4 to 65535), which filters pulses using the equation below for minimum allowable pulse duration. Values of 0x0001 through 0x0003 are not allowed. This register is reset to 0 (0x0000), which disables the filter function.

$$MinPulseMeasured = \frac{LowPassFilter\,\mathrm{Re}\,gValue}{vclk/2}$$

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3.8.2.3 Pulse Width Timer

The demodulated or unmodulated raw data is then applied to an 18-bit pulse width timer. The RX pulse width timer uses the same programmable clock used by the demodulation logic to measure the duration between edge transitions on the incoming demodulated signal. If the input signal is not modulated, meaning the RX clock does not need to be 16 times the carrier frequency, it can be programmed such that the longest symbol width does not cause the RX pulse width counter to overflow at the given RX clock frequency. This allows each pulse to be measured at its greatest resolution, using the full 18-bit range of the counter.

The IR port can be programmed to measure the time between rising-edges, falling edges, or both edge types. The pulse width timer starts when the first programmed edge type is detected and stops when the next edge is detected. At this point, the most significant 16 bits of the 18-bit timer value is transferred to bits 15–0 at the top of the 8-entry x 18-bit receive FIFO. The logic level of the pulse (as programmed by the polarity bit) is stored in bit 16, and bit 17 is set in the next FIFO location to denote that the next FIFO entry contains valid data. Next the RX pulse width timer is cleared and again begins to increment at the programmed clock rate to measure the width of the next pulse.

When the demodulated input signal no longer transitions, the RX pulse width timer overflows, which indicates the end of data transmission. When this occurs, the timer value contains all 1s. This value can be stored to the RX FIFO, to indicate the end of the transmission if the Rx FIFO load on Timer Overload disable is not set. Additionally, a status bit is set which can interrupt the microprocessor, if it is enabled within the IR port. The time duration of each pulse measured can be calculated using the following equation (the multiplication by four takes place due to the use of the most significant 16 bits of the pulse width timer):

$$PulseDuration = \frac{(RxFIFOCountValue * 4)}{RxClockFreq}$$

The RX FIFO load on Timer Overload Disable allows the user to choose whether to store or not store Rx pulse with times overflows. Noise starts the Rx pulse width Counter and can produce overloads when not desired as in a Com mode wakeup operation.

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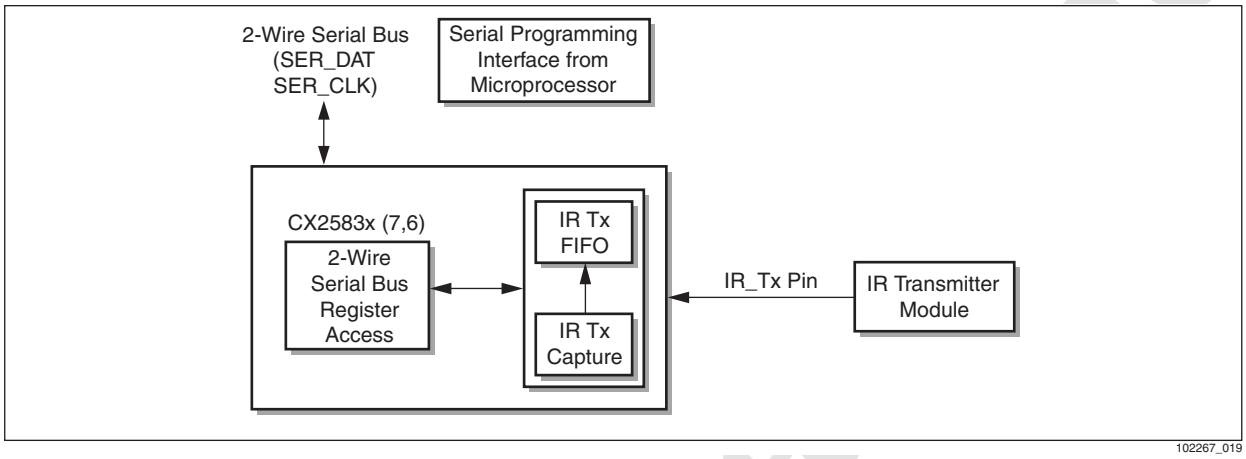
3.8.3 IR Transmitter

The IR transmitter block, shown in Figure 3-22,accepts bits for transmission from the microprocessor and is responsible for formatting the output data into a desired transmission specification prior to placement into the TX FIFO buffer.

Figure 3-22. IR Transmitter Block Diagram



For IR transmission, pulse duration count values are calculated by the microprocessor using the same equation,

$$PulseDuration = \frac{(TxFIFOCountValue * 4)}{TxClockFreq}$$

and written to the transmit FIFO. The TX FIFO is 8 entries by 17 bits. Bits 15–0 contain the timer count value, and bit 16 contains the logic level that is to be output during the duration of the pulse. These count values are taken from the bottom of the FIFO one at a time and are loaded to the most significant 16 bits of the 18-bit TX pulse width counter. The counter decrements using a separate TX clock which is independent of the RX clock described above. Similarly, its frequency is programmable with a range determined by the frequency of the host clock. If the transmit modulation logic is enabled, this programmable clock rate must also be 16 times the frequency of the output carrier.

If the output is not modulated, a clock frequency can be selected such that the longest pulse duration does not cause the 18-bit TX pulse width timer to overflow. Again, this provides the best resolution for each pulse that is transmitted. Once a value is loaded into the TX pulse width counter, the programmed logic level is either driven onto the IR_TX pin, if modulation is disabled, or is passed to the modulation logic, if it is enabled. When the counter reaches 0, the next value is taken from the bottom of the TX FIFO, and the whole process starts once again. When the counter reaches 0 and no more data is available within the TX FIFO, it is assumed that the end of the data stream has been reached. At this point, the IR_TX/PRGM6 pin is forced to the level which indicates a space, as programmed by the polarity bit.

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3.8.3.1 Transmit Data Modulation

If modulation is enabled, marks are represented by bursts of high frequency carrier transitions, and spaces are represented by the absence of carrier transitions. The duty cycle of the high-frequency transitions is programmable. Again, if modulation is enabled, the TX clock frequency must be 16 times the desired frequency of the carrier transitions. This 16-bit IR Transmit Clock Divider bit-field is used to control the IR port's transmit clock rate. The transmit clock is used to drive both the modulation logic and the transmit pulse width timer. This bit-field is used as the modulus for a 16-bit down counter, which is decremented at half the video clock rate (108 MHz/2). Each time the counter reaches 0 or the IR TX Clock Divider registers (0x204 and 0x205) are written, the contents of this register are reloaded to the counter. Each time the counter wraps to 0, a transmit clock pulse is signaled to the modulation logic and the TX pulse width timer.

If modulation is enabled, this field must be programmed such that the TX clock rate is 16 times the desired carrier frequency when a mark is transmitted. If modulation is disabled, a clock frequency can be selected such that the longest pulse duration does not cause the 18-bit TX pulse width timer to overflow. This provides the best resolution for each pulse that is transmitted. The IR TX Clock Divider bit-fields can be programmed with any value from 0x01 to 0xFFFF. The Transmit Clock Divider is reset to a value of 0xFFFF. The TX clock rate, given a set Transmit Clock Divider value, is calculated using the following equation:

$$TxClkFreq = \frac{108/2}{(TxClkDivider + 1)}$$

The period of one carrier transmitting is broken into 16 time periods. The duty cycle register provides a selection of one of 16 different carrier duty cycles. The carrier can be one TX clock period high and 15 low, two TX clock periods high and 14 low, and so on. The 4-bit IR TX Carrier Duty Cycle (0x20C) register selects the duty cycle (high time, then low time duration) of the transmit carrier when signaling a mark. The TX carrier frequency is established by programming the IR TX Clock Divider registers as described above. Again, the TX clock must be programmed to be 16 times the desired frequency of the TX carrier. The IR TX Carrier Duty Cycle value then selects one of 16 possible duty cycles: one TX clock high and 15 TX clocks low, or two TX clocks high and 14 TX clocks low, etc. This bit-field is ignored if modulation is disabled.

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3.8.4 IR FIFOs

The IR FIFO (0x23C and 0x23D) registers provide access to the IR port's transmit and receive FIFOs. Writes to this register access the top of the transmit FIFO, allowing it to be filled and count values to be transmitted. A write with a value of 0x0000 to the Tx FIFO is effectively 0xFFFF+1, or maximum pulse width. Reads of this register access the bottom of the receive FIFO, allowing incoming pulse width measurements to be removed. The transmit FIFO is 17 bits wide x 8 entries deep. Bits 15–0 contain the count value to be loaded to the TX pulse width counter, and bit 16 contains the state which should be driven to the modulation logic. The receive FIFO is 18 bits wide x 8 entries deep. Bits 15–0 contain the pulse width measurement from the RX pulse width counter, bit 16 contains the state of the ir_in pin at the end of the measurement, and bit 17 is a tag which indicates whether more valid data is present within the FIFO.

3.8.5 IR Controls

General control of the IR functions is programmable through the IR Control 1 (0x200) and IR Control 2 (0x201) registers. Features which are controlled using these registers include the following:

- RX FIFO load on timer overflow
- Loopback operation
- Carrier polarity
- FIFO service request levels
- Enabling/disabling of both the IR port's transmitter and receiver
- Enabling/disabling of the RX and TX FIFOs
- Selection of carrier modulation and demodulation
- Control of which type of edge to start and stop the pulse timer for demodulated receive data
- Control of a window which is used to predict when the next receive carrier transition is expected

The user can either program the IR port's six control registers, in any order, then write to the transmit FIFO to start operation, or first place data in the transmit FIFO, while the IR port is disabled, then configure the six control registers, programming this register last to enable the IR port. When changing any configuration in these registers, always disable the IR's transmitter and receiver first, then reprogram the mode of operation and enable the receiver and transmitter.

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3.8.6 IR Status and Interrupts

The IR Status (0x210) register contains six status bits, four that can interrupt the microprocessor and two that can be polled. Bits 5, 4, 1, and 0 are set and cleared automatically by hardware and signal when a hardware condition exists which must be handled by software. Any one of these four status bits produces an interrupt when set and its corresponding interrupt enable bit is set. Interrupt enable bits do not affect the setting and clearing of status bits. The transmit and receive busy flags are also set and cleared automatically by hardware, bits 2 and 3, but do not produce interrupts. They are polled by software to query whether the IR port is currently transmitting and/or receiving IR data. The Interrupt Enable Register (IR_IRQEN_REG) is programmed to enable/disable the transmit and receive FIFO service requests to signal interrupts to the interrupt controller. This register is read-only, writes have no effect.

The IR Interrupt Enable (0x214) register contains four bits which are used to mask or enable individual interrupt requests. Refer to the above IR Status (0x210) register for a description of each interrupt source. The interrupt enable bits do not effect the setting and clearing of the interrupt status bits. Each enable bit is logically ANDed with its corresponding status bit, and the resultant signals are all logically ORed to produce a single interrupt request to the interrupt controller.

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3.9 Auxiliary PLL, Video-Locked Master Clock

In addition to the PLL dedicated for clocking the video decoder data path, a second auxiliary PLL is provided for general-purpose use. The user can program the auxiliary PLL for any reference frequency desired. One intended use is to use this PLL as an audio master clock, or OSR (oversampled ratio) clock, to clock the audio DACs or ADCs in the system. If so, an optional feature is provided to enable the locking of this clock to the video pixel rate.

Many applications require synchronization between the video pixel rate and the audio sample rate. This is particularly important for applications that compress audio and video data into MPEG frames for subsequent playback. To support these applications, the device provides an audio master clock that is locked to the video pixel rate. This master clock can be divided down to generate the serial audio word clocks, bit clocks, and the OSR clocks. In the context of the video decoder, a "locked" audio clock means that there is a constant ratio between the number of video pixel clocks and audio sample clocks. This ratio is defined as any integer number of audio clocks to another integer number of video clocks. The EN_AV_LOCK bit in the Audio Lock 1 (0x12B) register controls the video-audio locking. Setting this register to 1 enables video-audio locking. When the locking is not enabled, the PLL values pass straight through the filter.

The audio clock is loosely coupled through a locking loop. Thus, for any given set of audio samples, there are not necessarily a fixed number of video samples. However, over the long term, the ratio will be maintained. Thus the sample-rate ratio is defined by defining two numbers that must equal each other over the long term. The AUD_COUNT (0x12C to 0x12E) register contains a 24-bit integer value representing the number of audio clocks, and the 24-bit VID_COUNT (0x128 to 0x12A) register represents the fractional number of video clocks that are expected in the time frame of the audio register. The VID_COUNT register contains 21 integer bits and 3 fractional bits. The locking loop will drive the audio PLL such that this ratio is maintained. Lock is maintained as long as the accumulated difference between audio samples and video pixels does not exceed one-half of a video field.

The locking algorithm counts a number of audio clocks from an audio clock reference, equal to the number programmed into the AUD_COUNT register. The reference for the audio clock is the AUX_PLL, which is always equal to 384 times the audio sample rate.

A video count register accumulates the number of video pixel clocks during this interval. The difference between the accumulated number of pixel clocks and the expected value in VID_COUNT defines the error term. The reference for the video clock is a clock that is 8 times the pixel rate. Since jitter can exist due to clock domain synchronization issues, and because the video pixel clock can be somewhat unstable in order to lock to sources such as VCRs, the error term is heavily filtered (a low loop gain) to maintain a clean audio clock.

The fractional portion of the VID_COUNT register provides a degree of flexibility in the required parameter in the AUD_COUNT register, and thus how often the loop updates. Without fractional capability, the value required in the AUD_COUNT register might have to be so large that the loop is updated too infrequently.

Table 3-26 contains examples of how these registers should be programmed for common audio sample rates and video pixel rates. Notice that the fractions can be exactly represented through binary numbers. These values demonstrate the minimum requirements. The user may want to multiply both AUD_COUNT and VID_COUNT

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numbers by a common integer such that all modes have similar loop update rates. The video pixels and audio samples columns show the minimum ratio of whole pixel to whole sample counts. However, because the actual clocks are multiples of the video pixel and audio sample rates, and because the video count can be specified to 3-bit fractional granularity, the logic does not have to wait for that long to measure the ideal ratio. Table 3-26 shows the minimum values of AUD_COUNT and VID_COUNT that will achieve the desired ratio. The VID_COUNT register value assumes an 8x pixel clock and a 21-bit integer, 3-bit fractional number. The AUD_COUNT register value assumes a 384 x sample rate clock.

Table 3-26. 43 Locking Register Values for Common Audio Sample Rate

Video Pixel Rate	Audio Sample Rate	Video Pixels	Audio Samples	Recommended VID_COUNT	Recommended AUD_COUNT
13.5 M	48 k	1,125	4	0x1193F8	0x05FFF
13.5 M	96 k	1,125	8	0x08CAF8	0x02FFF
13.5 M	32 k	2,250	8	0x0D2EF8	0x02FFF
13.5 M	44.1 k	4,500	147	0x057E38	0x01B8F
14.75 M	48 k	7,375	24	0x0733B8	0x023FF
14.75 M	96 k	7,375	48	0x0733B8	0x047FF
14.75 M	32 k	7,375	16	0x0733B8	0x017FF
14.75 M	44.1 k	147,500	441	0x0900A8	0x02957
12.27 M	48 k	818,181	3,200	0x0C7BFD	0x04AFF
12.27 M	96 k	818,181	6,400	0x0C7BFD	0x095FF
12.27 M	32 k	2,454,543	6,400	0x257407	0x095FF
12.27 M	44.1 k	272,727	980	0x04294F	0x016F7

The table entries show the exact ratio, and the event that generates an error happens faster than the field rate of 60 Hz. (NTSC square pixel with 32 kHz audio would have a worst-case update rate of 40 Hz. However, because the AUD_COUNT integer is divisible by eight, and there are still three bits of resolution in the VID_COUNT register, both numbers could be divided by eight to reduce the update frequency to 320 Hz.)

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3.10 Register Addressing

The user-programmable registers can be programmed through either a two-wire serial interface or the VIP Host port. In either method, there is a portion of the cycle in which a register subaddress is passed over the interface. The internal register space is based on a 16-bit subaddressing scheme. (The address space is currently limited to 12 bits based on VIP Host port limitations.) Table 3-27 shows how the address space is organized among the major submodules of the IC.

The first address space is used for the serial port mechanism, whether it is the two-wire interface or the VIP Host port. The mapping of these 256 bytes depends on which of the two interfaces is active. This space is used to configure the operation of the serial interface itself. It is also used for configuring power-down states. Since the serial interfaces receive their own external clocks, these modules can be used to shut down the other digital clocks.

See Section 5 for a full definition of the register address space.

Table 3-27. Register Subaddresses

Sub-Address[11:8]	Register File	Size (bytes)
0000	Two-wire serial/VIP	256
0001	Chip Config	256
0010	IR Blaster	256
0011	RESERVED	256
0100	Video and VBI	1K
1xxx	RESERVED	2K

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3.11 Two-Wire Communications Port

The device communicates over a 400 kHz, two-wire serial interface or a 2-bit VIP host interface. These two interfaces share pins and are mutually exclusive. The VIP_ENABLE reset strap selects either the VIP Host or the serial slave communication mode.

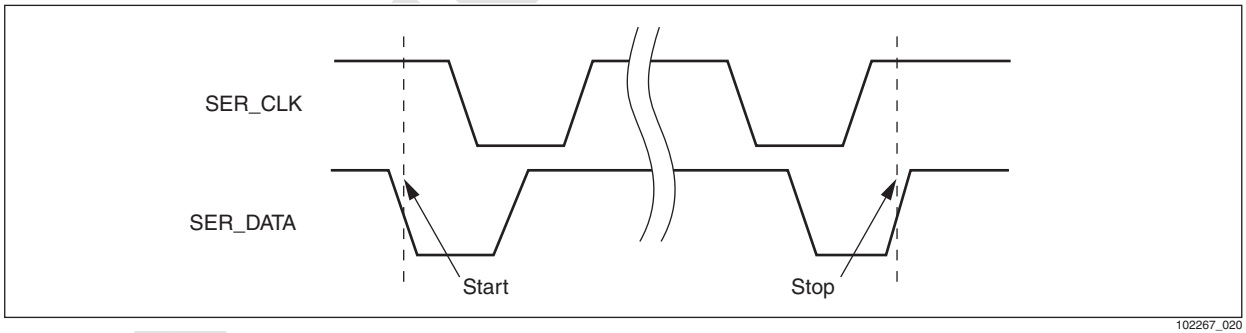
3.11.1 Serial Slave Interface

The registers can be accessed through a two-wire serial bus interface operating as a slave device. The serial clock and data lines SER_CLK and SER_DATA transfer data from the bus master. A CHIP_SEL/VIPCLK pin is available to configure the device for one of two possible chip addresses. The device address byte can be either 0x88 or 0x8A for write cycles, or 0x89 or 0x8B for read cycles. (The ALTADDR_SEL reset strap also enables a 0x8C/0x8D and 0x8E/0x8F option. See Section 3.16 for more details.)

3.11.2 Starting and Stopping

The relationship between SER_CLK and SER_DATA is decoded to provide both a start and stop condition on the bus. To initiate a transfer on the serial interface bus, the master must transmit a start pulse to the slave device by taking the SER_DATA line low while the SER_CLK line is held high. The master should only generate a start pulse at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SER_DATA line high while the SER_CLK line is held high. The master can issue a stop pulse at any time during a cycle. Since the interface interprets any transition on the SER_DATA line during the high phase of the SER_CLK line as a start or stop pulse, ensure that data is stable during the high phase of the clock. Figure 3-23 provides a timing diagram for the serial start and stop transaction.

Figure 3-23. Serial Start and Stop Transaction



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3.11.3 Chip Addressing

The device's serial interface chip address consists of two parts: a 7-bit base address and a single-bit R/W command. The R/W bit is appended to the base address to form the transmitted address.

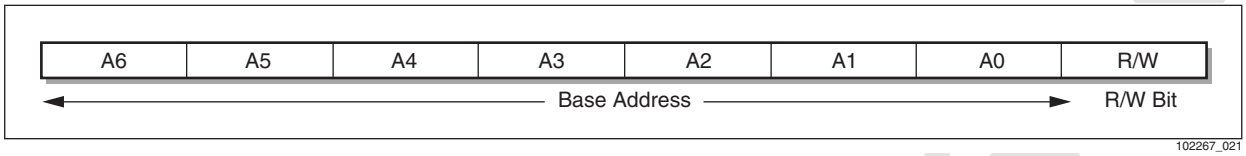

Table 3-28 defines chip addressing.

Table 3-28. Chip Addressing

Serial Address	CHIP_SEL/ VIPCLK Pin	IRQ_N/PRGM4 Pin	Base Address	R/W Bit	Action
88	0	1	1000100	0	Write
	0	1	1000100	1	Read
8A	1	1	1000101	0	Write
	1	1	1000101	1	Read
8C	0	0	1000100	0	Write
	0	0	1000100	1	Read
8E	1	0	1000101	0	Write
	1	0	1000101	1	Read

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3.11.4 Reading and Writing

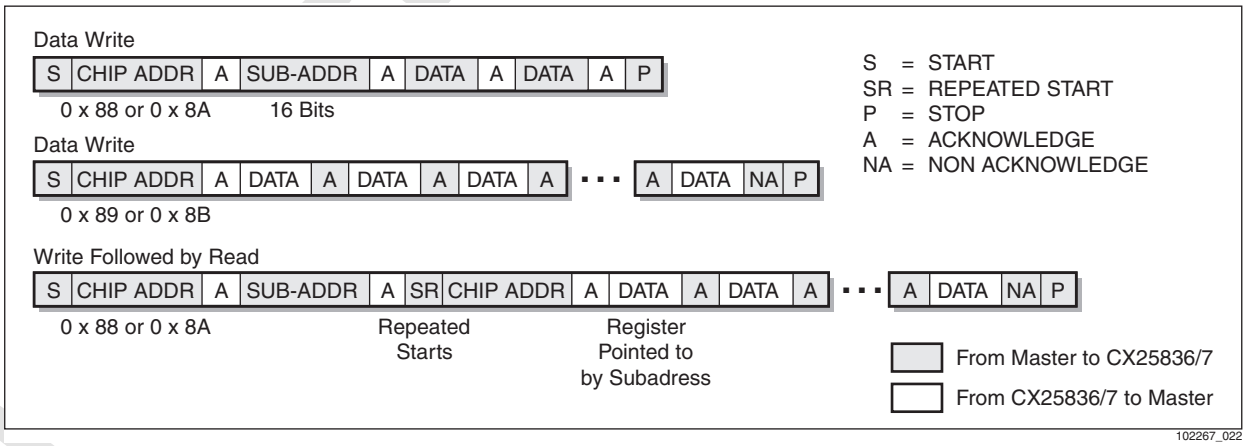
After transmitting a start pulse to initiate a cycle, the master must address the device. To do this, the master must transmit one of the four valid chip addresses, with the Most Significant Bit (MSB) transmitted first. After transmitting the address, the master must release the SER_DATA line during the low phase of the SER_CLK and wait for an acknowledge. If the transmitted address matches the selected chip address, the device responds by driving the SER_DATA line low, generating an acknowledge to the master. The master samples the SER_DATA line at the rising edge of the SER_CLK line, and proceeds with the cycle. If no device responds, the master transmits a stop pulse and ends the cycle.

If the slave address R/W bit is low, indicating a write, the master must transmit the 16-bit subaddress, MSB first. The device acknowledges the transfer and loads data into its internal address register. The master then issues a stop command, a start command, or transfers an 8-bit byte, MSB first, which is loaded into the register specified by the internal address register. The device then acknowledges the transfer and increments the address register in preparation for the next transfer. As before, the master may issue a stop command, a start command, or transfer another 8 bits to be loaded into the next location.

If the slave address R/W bit is high, indicating a read, the device transfers the contents of the register specified by its internal address register, MSB first. The master must acknowledge receipt of the data and pull the SER_DATA line low. As with the write cycle, the address register is auto incremented, in preparation for the next read. To stop a read transfer, the host must not acknowledge the last read cycle. The device then releases the data bus in preparation for a stop command. If an acknowledged pulse is received, the chip proceeds to transfer the next register.

When the master generates a read from the device, it starts its transfer from whatever location is currently loaded in the address register. Because the address register might not contain the address of the desired register, the master executes a write cycle and sets the address register to the desired location. After receiving an acknowledgment for the transfer of data into the address register, the master initiates a read of the device by starting a new serial interface cycle with an appropriate read address. The device then transfers the contents of the desired register. Serial communications protocol is illustrated in Figure 3-24.

Figure 3-24. Serial Communications Protocol



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3.12 VIP 2 Host Interface

The VIP 2 Host Interface provides a faster alternative interface to the two-wire serial communication interface. The VESA VIP 2 Host slave interface is a high-bandwidth, minimal-pin-count interface for connecting multiple video components. Refer to the *Video Electronics Standards Association (VESA) Video Interface Port*, *version 2* specification for full implementation details. The VIP 2 Host slave interface enables the chip to communicate with devices that are compliant with either the VIP 1.1 or 2 master specifications. The host interface provides Read/Write accesses to the register space.

The VIP Host Interface also supports the following:

- Burst reads of the registers with at most one wait phase per byte
- Power management configuration through writes into the command register
- Power reporting in the status registers

The VIP Host interface works on the VIPCLK pin, which doubles as CHIP_SEL/ VIPCLK in the two-wire serial mode. The VIP 2 Host interface block takes care of the serialization of the data flow from the device to the a VIP Master (graphics chip) and the serial to parallel conversion of the data flow from the VIP Master to the device. The VIP Host interface block follows the VIP 2 specification, which stipulates that, for reliable operation, all register accesses must be at most one wait phase per byte and no wait phases for FIFO operations.

3.12.1 Address Space

The VIP Master can address 4096 locations. VIP address spaces are defined in Table 3-29.

Table 3-29. VIP Address Spaces

Address Space	Block	Select Bit
000–00F	VIP configuration space	VIP_SEL
010–FFF	Local register space	REG_SEL

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3.12.2 VIP Power-Up Detection

On power-up, the VIP master asserts VRST. The device holds the HAD[0] line low until VRST remains asserted. Once the VRST is deasserted, the host interface drives the HAD[0] line to a three-state, indicating the signal's presence on the VIP bus.

3.12.3 VIP Power Modes

The VIP master can configure the device for different power modes. The device supports all four modes, as described in the VIP 2 specification. The master must write to bits [1:0] of the command register to configure the chip for these different power modes.

- P0: The device is operating in the normal power consumption mode without any part of the chip being put to sleep. This is the default mode.
- P1: In this mode, the digital part of the chip is shut down. It essentially turns off all the clocks to the digital part of device. This mode has a turn-on latency of less than 10 ms. The VIP clock will be on, and the graphics chip can access the configuration registers (000:00D addresses).
- P2: In this mode, the analog portions of the chip are shut down as well. The host interface turns off the power to the digital part and the analog portions of the chip. Turn-on latency is less than 1 second. The VIP master can turn off the VIPCLK in this mode. However, if the clock is supplied, the master will be able to access the configuration registers (000:00D address).
- P3: The device supports the P3 powered down mode where it consumes minimal power. The VIP master stops the VIPCLK to the block in a power-down mode. In this mode, the host interface will drive the VIP interface pins to a three-state. The host interface asserts a sleep signal, and this turns of the power to digital and the analog parts of the chip. This mode is the same as the power mode P2.

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3.13 Hardware Interrupt

The interrupt pin, IRQ_N (VIRQ_N in VIP mode) signals interrupt conditions that occur within the chip. An interrupt condition can be enabled through the Interrupt Mask 1 and Interrupt Mask 2 (0x412 and 0x413) register. Setting the appropriate video decoder or IR controller bits in the register masks the assertion of the interrupt pin. The Interrupt Status 1 and Interrupt Status 2 (0x410 and 0x411) registers allow the status of each of those interrupts to be checked separately. There is also an option to invert the polarity of the pin.

3.14 I/O Pin Configuration

3.14.1 Output Pin Configuration

The digital I/O pin functionality is extremely flexible. The CX25836 and CX25837 provide up to eight programmable pins. These configurable GPIOs are shared with the following pin/port groups so that the user can assign exactly which pins can be dedicated to specific functions versus general purpose I/O functions.

- Video Timing Control (VRESET/HCTL/PRGM3 is unavailable when VIP Host mode is selected)
- Interrupt pin
- Infrared Remote Transmit
- Infrared Remote Receive
- Auxiliary PLL Output Clock

Any of the programmable pins can be configured to provide alternate functions from their default state. This allows customization of the output interface in order to fit a wide variety of system requirements. Table 3-30 shows the default state of the programmable pins after reset.

Table 3-30. Default PRGM[0:7] Pin Configuration

Pin Name	Default Output Select	Description
DVALID/PRGM0	DVALID	Default function is a valid pixel data indicator. When asserted, indicates a valid pixel. Can be programmed for alternate functions in Table 3-31.
FIELD/PRGM1	FIELD	Default function is field indicator. Even/Odd Field indicator (0 = odd field, 1 = even field). Field resets to 0, odd, and toggles every new_field. Can be programmed for alternate functions in Table 3-31.
HRESET/PRGM2	HRESET	Default function is horizontal reset indicator. Asserted at 0H sync point, held for 32 or 64 clocks. Width can be configured through HR32 bit in MISC_TIM_CTRL register in video decoder core. Can be programmed for alternate functions in Table 3-31.
VRESET/HCTL/ PRGM3	VRESET	Default function is vertical reset indicator. Asserted from vsync begin (start of serration pulses) through end of equalization pulse period, nominally 5 or 6 lines depending on video standard. Can be programmed for alternate functions in Table 3-31. In VIP mode this pin becomes the Host Interface Reset Input and is not programmable.
IRQ_N/PRGM4	IRQ_N	Interrupt pin
IR_TX/PRGM6	IR_TX	Infrared Remote Transmit
IR_RX/PRGM5	GPO[2]	Infrared Remote Receive. This is by default an input, so the output select will be a don't care unless put in output mode.
PLL_CLK/PRGM7	GPO[3]	Auxiliary PLL output clock. This default mode is to select the PLL output from inside the analog domain, so this output select will be a don't care unless CLK_PAD_IN is selected from the digital core.

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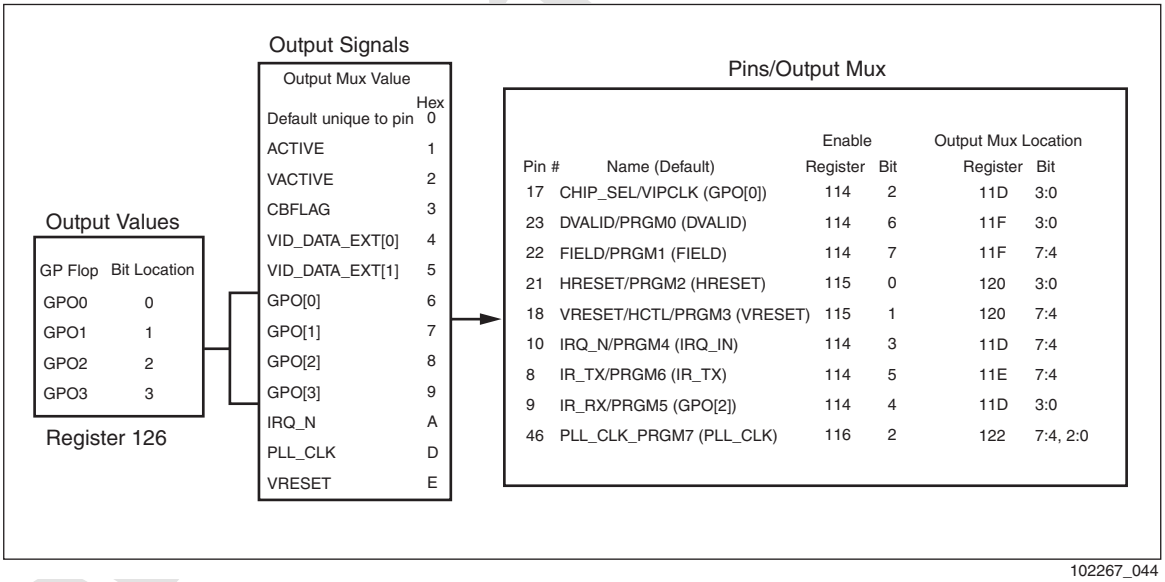
Alternatively, the following functions in Table 3-31 are available by programming the Pin Configuration registers (0x11C to 0x122). The XXX_OUT_SEL field select which internal signal is output on the PRGMx pin. The default output 0 value is determined by the specific output pin.

Table 3-31. Alternate PRGM[0:7] Pin Functions

0 = Pin Dependant
1 = ACTIVE (Composite active or horizontal active indicator. See ACTFMT bit of OUT_CTRL1 register in video decoder core.)
2 = VACTIVE (Vertical active indicator. Asserted during all vertical active lines.)
3 = CBFLAG (Cr/Cb indicator (0 = Cr, 1 = Cb) Cbflag is reset to cb at the beginning of each line and toggles every pixel clock period.)
4 = VID_DATA_EXT[0] (Extended Video Data. Least significant bits of internal 10-bit video bus. When enabled, 10-bit video is possible.)
5 = VID_DATA_EXT[1] (Extended Video Data. Least significant bits of internal 10-bit video bus. When enabled, 10-bit video is possible.)
6 = GPO[0] (Data from internal GPIO flops.)
7 = GPO[1] (Data from internal GPIO flops.)
8 = GPO[2] (Data from internal GPIO flops.)
9 = GPO[3] (Data from internal GPIO flops.)
A = IRQ_N/PRGM4 (Interrupt output: default active low polarity)
D = PLL_CLK
E = VRESET/HCTL/PRGM3 (vertical reset indicator)
F = RESERVED

Any signal shown in Figure 3-25 can be routed to any pin.

Figure 3-25. Output Signals Connection and Routing to Pins



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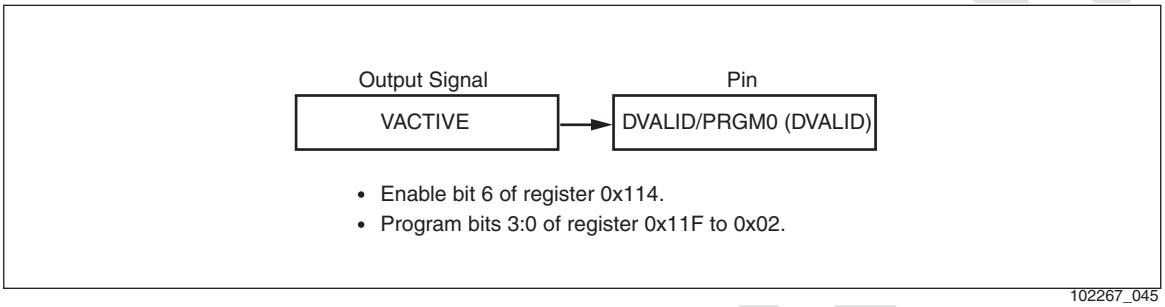
For example, if you want to read the signal VACTIVE on pin 23 (DVALID/PRGM0), enable the signal by programming the output mux to a decimal 2 on register 0x11F, bits 3:0. The signal VACTIVE can now be read on pin 23 (DVALID/PRGM0). However, if you want to read any signal on pin 46 (PLL_CLK/PRGM7), set bit 2 of register 0x115, then program the output mux to X11 (x = don't care) on register 0x122, bits 2:0, and finally, register 0x122, bits 7:4. See Figure 3-26.

Figure 3-26. Reading the VACTIVE Signal on Pin 23 (DVALID/PRGM0)



3.14.2 Input Pin Configuration

For general purpose inputs, there are four internal registers that can be programmed to receive their state from the pins shown in Table 3-32. The input pin for each general purpose input can be programmed through the GPIOx_IN_SEL bits in the Pin Configuration 9 and 10 registers (0x124 and 0x125). Bits 0x0 of GPIO{3:0}_IN_SEL select the pin input that is assigned to the internal GPIx input flip-flop.

Table 3-32. Alternate GPI0 Pin Functions

0 = DVALID/PRGM0
1 = FIELD/PRGM1
2 = HRESET/PRGM2
3 = VRESET/PRGM3
4 = IRQ_N/PRGM4
5 = IR_TX/PRGM6
6 = IR_RX/PRGM5
7 = RESERVED
8 = RESERVED
9 = RESERVED
0xA = RESERVED
0xB = PLL_CLK

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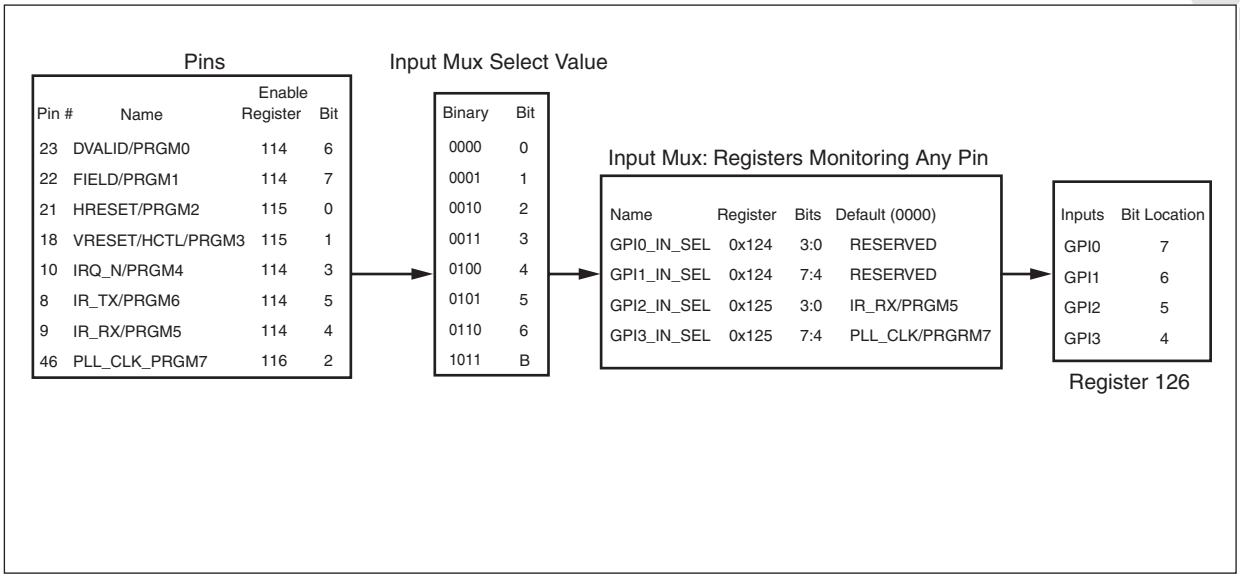
Any of the pins shown in Figure 3-27 can be routed to any four registers.

Figure 3-27. Input Signals Connection and Routing to Pins



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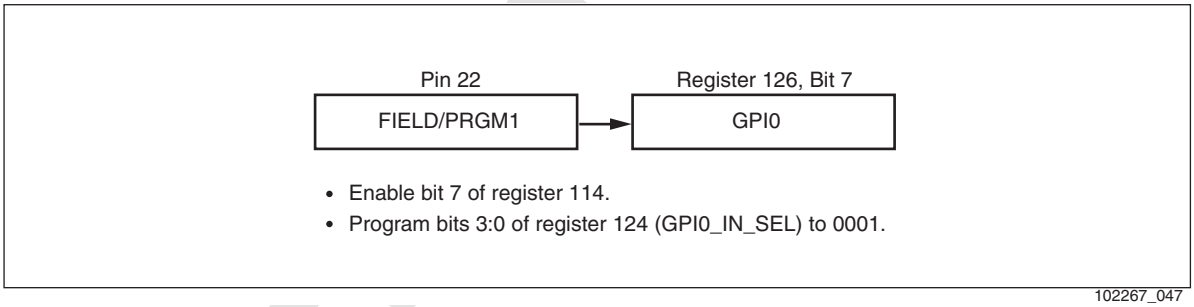
For example, if you want to read the value of pin 22 (FIELD/PRGM1) on register 0x126 (GPI0), enable the pin by setting bit 7 of register 0x114, then program the input mux to value 0001 of register 0x124, bits 3:0 (normally defaults to GPIO[0]. The value of pin 22 (FIELD/PRGM1) can now be read. See Figure 3-28.

Figure 3-28. Reading the Value of Pin 22 (FIELD/PRGM1) on Register 0x126 (GPI0)



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3.15 PLL Programming

The device contains two PLLs for generating the required divided-down clocks used by the video and master audio clock modules. Both PLLs are implemented with 25-bit fractional PLLs. The VID_PLL_CLK is used for video data path, and the PLL_CLK is a separate PLL used to provide an audio sample frequency clock that is rate matched to the incoming video. The PLL capabilities are outlined in Table 3-33.

Table 3-33. PLL Specifications

Clock	Min (MHz)	Typ (MHz)	Max (MHz)	Accuracy (ppm)	Duty Cycle (%)	Description
VID_PLL_CLK	98.18	108	118	100	50 ± 2%	Video and Audio master clock
PLL_CLK	8.19	12.29	54.00	100	50 ± 2%	Oversampling clock for external audio DAC

The video PLL frequency can be programmed as follows:

$Fpll\_clk = Fxtal \times (VID\_PLL\_INT + (VID\_PLL\_FRAC/2^{25}))/VID\_PLL\_POST$

Where

Fxtal is typically 28.63636 MHz

VID_PLL_POST (0x109) has a range of values from 2 to 63

VID_PLL_INT (0x108) has a range of value from 0 to 63

VID_PLL_FRAC (0x10C to 0x10F) has a range of values from 0 to $2^{25}-1$

The auxiliary PLL (PLL_CLK) is programmed in the same way with AUX_PLL_POST, AUX_PLL_INT, and AUX_PLL_FRAC. The range of values for the PLL's VCO, as determined by the PLL frequency times the post divide (VID_PLL_POST or AUX_PLL_POST), should remain between 200 MHz and 600 MHz.

The video decoder PLL (VID_PLL_CLK) is programmed for eight times the pixel rate. The default pixel rate is the ITU-R BT.656 standard of 13.5 MHz, or a default PLL frequency of 108 MHz. To produce square pixel rates, the SQ_PIXEL bit in the Video Mode Control 1 register (0x400) must be set high, and the video PLL frequency must be set to 8x 14.75 MHz or 12.272715 MHz for PAL/SECAM or NTSC, respectively. Table 3-34 gives the recommended values for the video PLL registers for the various standard pixel frequencies.

Table 3-34. Video PLL Programming Values

Desired Pixel Rate	Video PLL Frequency	VID_PLL_INT	VID_PLL_FRAC	VID_PLL_POST
13.5 MHz	108 MHz	0xF	0x2BE2FE	4
12.272715 MHz	98.181720 MHz	0xD	0x5B6D52	4
14.75 MHz	118 MHz	0x10	0x3DC3EE	4

The auxiliary PLL can be programmed for any reference frequency desired. However, see Section 3.9 for a description of how to enable the video locking feature, which enables the use of this clock output for an audio master clock that is locked to the video pixel rate.

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3.16 Device Reset and Reset Configuration

There is no mandatory power-up sequence. 1.2 V VDD can be powered up before 3.3 V VAA and 3.3 V VDDO, and vice versa, as long as the following reset steps are met. However, it is recommended that the 3.3 V VAA and 3.3 V VDDO supplies be powered up together.

After power-up, the device must be initialized in the following manner:

1. 100 ms after the both VAA and VDDO are stable, RESET_N pin should be held low for 350 µs. The rising edge of RESET_N will latch the correct state of the reset configuration pins (Table 3-35), configuring the device to use the VIP Host Port of two-wire serial and corresponding two-wire serial interface address. The power-strap pins are three-stated and pulled high internally (~100 kΩ) while reset is asserted.
2. Next, toggle the SLEEP bit, Host Register 1 (0x000) register, bit SLEEP, from a low to a high, then a high to a low. This will ensure that the PLL is initialized in the correct state. Note that this can also be accomplished by toggling the SLEEP pin instead of the SLEEP bit.
3. Next, to ensure the proper configuration of the Delay Lock Loop (DLL), used for clock generation, the following sequence of register writes must be provided. This sequence must be run after power-up or after the DLLs are powered down and powered back up; however, it is unnecessary to run this sequence only after a reset.
   a. Set DEPTH to 0 in register DLL1 Diagnostic Control 3 (0x15A).
   b. Set CURRSET to 3 in register DLL1 Diagnostic Control 4 (0x15B).
   c. Enable UP_OVRD in register DLL1 Diagnostic Control 2 (0x159).
   d. Wait at least 10 µs.
   e. Disable UP_OVRD in register DLL1 Diagnostic Control 2 (0x159).
   f. Set COMP_GT_LOW to a 3 in register DLL1 Diagnostic Control 2 (0x159).
   g. Disable FLD, and then re-enable FLD in register DLL1 Diagnostic Control 2 (0x159).
   h. Set CURRSET to an 8 in register DLL1 Diagnostic Control 4 (0x15B).

Table 3-35. Reset Configurations

<table>
<tr><th>Strap Name</th><th>Pin</th><th>Usage After Reset (when pulled down)</th></tr>
<tr><td>VIP_ENABLE_N</td><td>IR_TX</td><td>Select the VIP Host port as the default serial interface. Otherwise, the chip will respond to two-wire serial port transactions.</td></tr>
<tr><td>ALTADDR_SEL</td><td>IRQ_N/PRGM4</td><td>If IR_TX/PRGM6 is pulled high, selects serial address for the two-wire serial interface. If IR_TX/PRGM6 is pulled low, the serial address for the two-wire serial interface is a Don't Care.
<table>
<tr><th>VIP_ENABLE_N</th><th>ALTADDR_SEL</th><th>CHIP_SEL/VIPCLK</th><th>Write/Read Device Address Pair</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0x88/0x89</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0x8A/0x8B</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0x8C/0x8D</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0x8E/0x8F</td></tr>
</table>
</td></tr>
</table>

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3.17 Quick Start Video

First, perform the steps outlined in Section 3.16, "Device Reset and Reset Configuration." The chip can be configured to boot up in either two-wire serial interface or VIP host port mode. To bring up the chip in two-wire serial interface mode, the TEST pin must be driven low, the IR_TX pin driven high, and the CHIP_SEL/VIPCLK and IRQ_N pins driven to the appropriate state for the desired chip address. For immediate operation of the device, the SLEEP pin must be driven low. If a low-power state is desired upon the completion of the system boot-up, the SLEEP pin must be driven high. This may be useful for situations that require low-power consumption until the system has been enumerated.

To bring up the chip in VIP host port mode, the TEST and IR_TX/PRGM6 pins must be driven low. The SLEEP pin can be configured as desired.

To enable ITU-R BT.656 decoded video from a CVBS source, simply write the following two registers:

- Set the analog CH{1}_SOURCE to the mux in the appropriate video input pin through the Video Input Control (0x103) register.
- Enable the pixel clock and video outputs through the Pin Control 2 (0x115) register.

The auto-detection feature of the decoder sets up the remaining registers based upon the detected input waveform.

3.18 Power Down

The sleep mode is used to power down various blocks of the chip to decrease power consumption. It can be controlled through either hardware or software. The SLEEP pin or the equivalent SLEEP bit in the register powers down the chip by disabling digital clocks and analog circuits, subject to masking. There is also a redundant digital power-down bit to provide compatibility with VIP Host power-down states.

The power-down feature allows independent shut-down of power domains (such as an ADC). This option limits the domains that are shut down to provide speedy recovery from sleep mode, allows unused power domains to be shut off during normal operation, and allows chip diagnosis to measure power consumption by different analogy circuits and digital clock domains. Mask Registers allow software to control which analog circuits to shut down when the sleep signal is asserted. These various power-down options are available through the Power Control 1 and 2 (0x130 and 0x131) registers.

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4 Electrical Interfaces

4.1 Electrical Interface and Design Guidelines

4.1.1 Board Layout Guidelines

Please take special note of the following:

- Series Clock termination should be at the source.
- Place 0.1 μF ceramic bypass capacitors as close to the device as possible. This will insure that the power goes through the capacitors before power goes through the VIAs to the power plane.
- Digital traces should be routed away from analog traces.
- Shielded connectors should be used with all shields connected to the ground plane with low impedance connections.
- Minimize the ground path for the crystal.
- If possible power and ground should be on separate dedicated layers.

4.2 Split Power Planes

Please give careful attention to the power planes. Proper implementation produces good video and audio performance. The following guidelines should be considered in board layout:

- Digital terminating resistors should be connected to digital supplies.
- Components connected to analog pins should be connected to analog ground.
- Analog traces should be routed over analog planes wherever possible.
- Digital traces should be routed over digital planes wherever possible.
- Digital ground should be connected to chassis ground (bottom of the bracket and the connector shields).

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4.3 Latchup Avoidance

Latchup is possible with all CMOS devices. It is triggered when any signal pin exceeds the voltage on the power pins associated with that pin by more than 0.5 V or falling below the ground pins associated with that pin by more than 0.5 V. Latchup can occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

To avoid latchup of the device, follow these precautions:

- Apply power to the device before or at the same time as the interface circuit.
- Connect all Ground pins together through a low impedance plane.
- If a voltage regulator is used on the digital and or the analog power planes, protection diodes must be used.

4.4 Crystal Oscillator Reference Clock

The device integrates a crystal amplifier oscillator circuit to produce a low-jitter reference for all clocks on the chip. The master clock is generated by installing a high-precision 28.63636 MHz crystal across the XTI and XTO pins, or a single-ended clock oscillator can be fed into the XTI pin while a DC bias of VSS_XTAL is applied to the XTO pin. The single-ended method must be selected by writing REF_CLK_SEL bit of the Serial Host Register (0x000) to 0.

The master clock reference is used for the ADC sample clock and as the reference clock for the PLLs. This clock reference is also used by the front-end digital logic that directly interfaces to the ADC modules.

The crystal amplifier oscillator has a dedicated power supply pin, VAA_XTAL, which should be carefully decoupled to the VSS_XTAL pin in order to minimize board noise from coupling into the reference clock.

Table 4-1 lists the specifications for the crystal circuit. Figures 4-1 and 4-2 illustrate the connection of third overtone or fundamental mode crystals.

Table 4-1. External Crystal Circuit Specifications

Parameter	Value
Frequency	28.63636 MHz
Tolerance	± 30 ppm (CL = 16.5 and 19.5 pF)
Temperature stability	± 50 ppm (0 °C to 70 °C)
Aging stability	± 15 ppm / 4 yrs
Oscillator Mode	Third Overtone or Fundamental Mode
Calibration Mode	Parallel resonant
Load Capacitance	20 pF, nom
Shunt Capacitance	7 pF, max
Series Resistance	40 Ω max @500 µW drive level
Operating Temperature	0 °C to 70 °C
Storage Temperature	–40 °C to 85 °C

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Figure 4-1. Third Overtone Crystal Oscillator

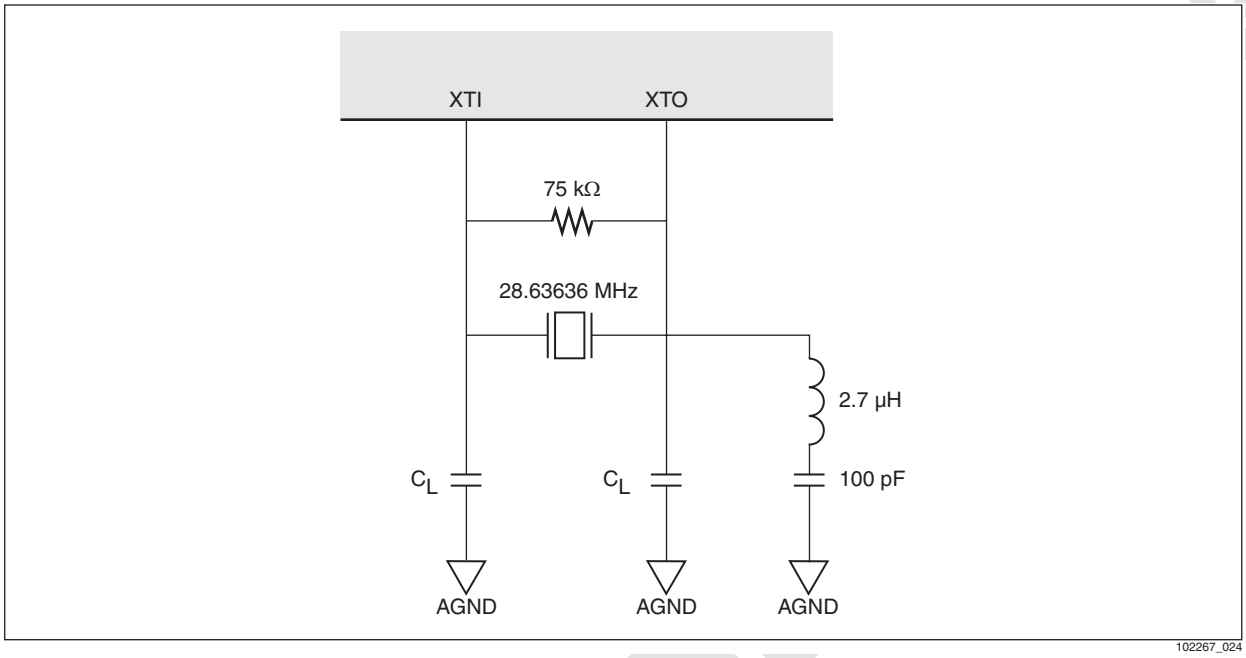

Figure 4-2. Fundamental Crystal Oscillator

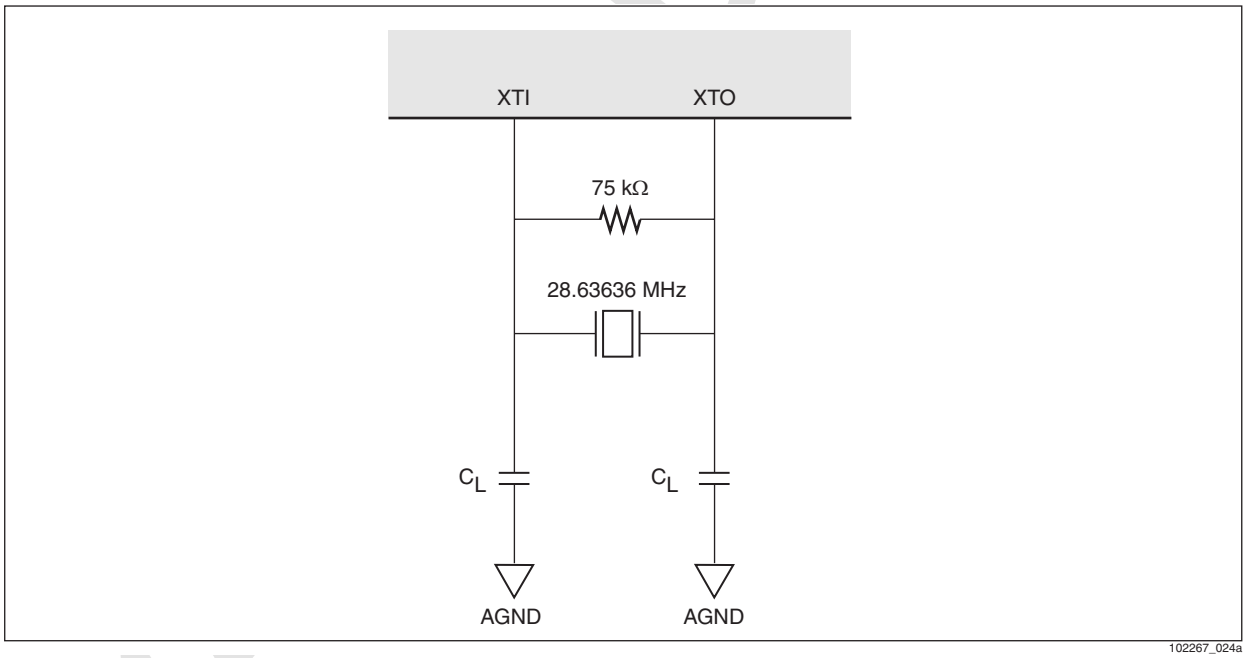

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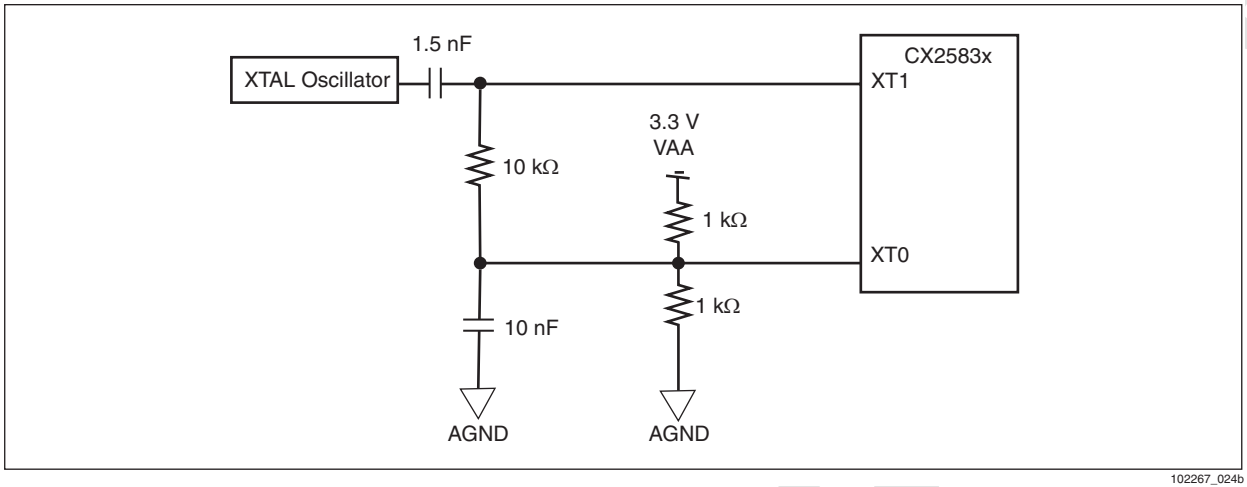
Figure 4-3. Single-Ended Clock Input



4.4.1 On-Chip Regulator

A linear voltage regulator is integrated on-chip in order to provide a means to convert the 3.3 V external power supply to a 1.2 V supply to be used for powering the core logic. This relieves the system of having to provide a separate 1.2 V supply for the decoder. The regulator is designed to only accommodate the power needs of the chip. This supply cannot be used for any other components on the board.

The regulator controls the base (or gate) of an external pass transistor such that the emitter (source/drain) is driven to 1.2 V. Specifications are listed in Table 4-2.

Table 4-2. Voltage Regulator Specifications

Parameter	Requirement	Units
Supply Range	3.0–3.6	V
Regulated Voltage	1.2–1.38	V
Regulated Voltage Tolerance	±100	mV
Current Output Range	0–250	mA

The regulator requires two external pins, REG_IN and REG_OUT, to be connected. The REG_OUT pin provides the base current for the external NPN. The REG_IN pin provides the feedback voltage from the emitter terminal of the external pass transistor. Figure 4-4 illustrates the external components required for using the on-chip regulator.

Additionally, the regulator can be bypassed and a system voltage of 1.2 V applied directly to the VDD pins if so desired. In this case the REG_OUT pin must be tied to REG_IN.

The advantage to using the on-chip regulator is that a localized regulator can be carefully monitored and controlled with registers. Advantages to not using the on-chip regulator are that better heat dissipation is achieved on the boards, and a lower bill of material results, assuming that another device is supplying the 1.2 V supply.

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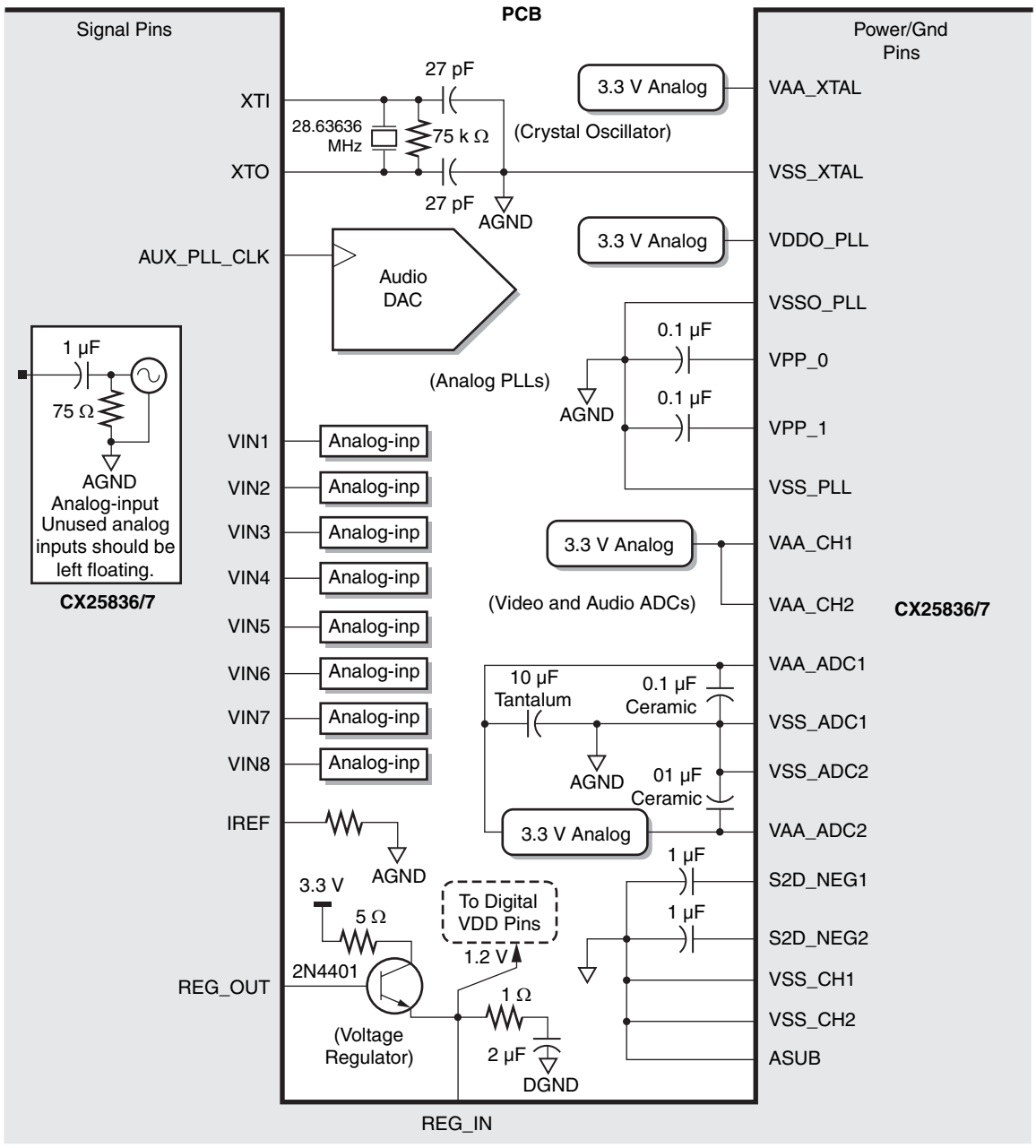
4.5 Electrical Hookup

Figure 4-4 shows the analog pin hookups.

Figure 4-4. Analog Pin Hookups



(1) VDDO_PLL and VSSO_PLL should be connected to an analog supply and ground if PLL_CLK pin is providing a sample clock for an external ADC or DAC. If PLL_CLK pin is used as a digital output, then VDDO_PLL should be connected to a digital supply.

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5 Register Map

5.1 Register Type Definitions

Table 5-1 documents each register type. These abbreviations indicate what is required for each bit position. The standard register type is RW for a simple read/write register bit.

Table 5-1. Register Types

Register Type	Description
RO	Read-only
RZ	Read zero only
RW	Read/Write
SC	Self-clearing on clock after write.
RR	Read with Reset on Write. Writing a 1 resets corresponding bit location. Writing 0 has no effect.
ISW	Internal Synchronized Write. Same as RW, but internal source can also write to register upon asserting a write strobe. This write must be synchronized to local clock domain.
PW	Pulse on Write. Same as RW, but detecting a write (byte granularity) generates a one-clock pulse.
PR	Pulse on Read. Same as RW, but detecting a read (byte granularity) generates a one-clock pulse.

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5.2 Register Map Summary

Table 5-2 shows the overall scheme for organizing the register space. The third nibble (bits 11:8) is used to select the register module. Note that the first 256 bytes of the map can be used for either the Serial Slave registers, or the VIP Host registers, depending on which serial interface is enabled. Table 5-3 provides a list of all registers and their addresses.

Table 5-2. Address Space Organization

Subaddress [11:8]	Register Domain	Size (Bytes)
0000	Serial Slave/VIP	256
0001	Chip Config	256
0010	IR Blaster	256
0011	RESERVED	256
01xx	Video Decoder	1K

Table 5-3. Register Map Summary *(1 of 8)*

Address (hex)	Register Name	Page Number
Serial Communications Host Registers:		
0x000	Host Register 1	page 5-10
0x001	Host Register 2	page 5-10
VIP Communications Host Registers:		
0x000	VIP Vendor ID	page 5-11
0x002	VIP Device ID	page 5-11
0x004	VIP Subsystem ID	page 5-11
0x006	VIP Subsystem Vendor ID	page 5-11
0x008	VIP Command	page 5-11
0x00A	VIP Status	page 5-12
0x00C	VIP Revision ID	page 5-12
0x00E	VIP Clock Status	page 5-12
Chip Configuration Registers:		
0x100	Device ID Low Byte	page 5-13
0x101	Device ID High Byte	page 5-13
0x102	Miscellaneous Chip Control Configuration	page 5-13
0x103	Video Input Control	page 5-14
0x104	AFE Control 1	page 5-14
0x105	AFE Control 2	page 5-15
0x106	AFE Control 3	page 5-15
0x107	AFE Control 4	page 5-16

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Table 5-3. Register Map Summary *(2 of 8)*

Address (hex)	Register Name	Page Number
0x108	Video PLL Integer	page 5-16
0x109	Video PLL Divider	page 5-16
0x10A	Aux PLL Integer	page 5-16
0x10B	Aux PLL Divider	page 5-16
0x10C	Video PLL Fractional 1	page 5-17
0x10D	Video PLL Fractional 2	page 5-17
0x10E	Video PLL Fractional 3	page 5-17
0x10F	Video PLL Fractional 4	page 5-17
0x110	Aux PLL Fractional 1	page 5-17
0x111	Aux PLL Fractional 2	page 5-17
0x112	Aux PLL Fractional 3	page 5-17
0x113	Aux PLL Fractional 4	page 5-17
0x114	Pin Control 1	page 5-18
0x115	Pin Control 2	page 5-19
0x116	Pin Control 3	page 5-19
0x117	Pin Control 4	page 5-20
0x118	Pin Control 5	page 5-20
0x119	Pin Control 6	page 5-20
0X11A	RESERVED (DEFAULT 0x00)	page 5-20
0x11C	RESERVED (DEFAULT 0x00)	page 5-20
0x11D	Pin Configuration 2	page 5-21
0x11E	Pin Configuration 3	page 5-22
0x11F	Pin Configuration 4	page 5-23
0x120	Pin Configuration 5	page 5-24
0x121	Pin Configuration 6	page 5-24
0x122	Pin Configuration 7	page 5-25
0x123	RESERVED	page 5-25
0x124	Pin Configuration 9	page 5-26
0x125	Pin Configuration 10	page 5-27
0x126	Pin Configuration 11	page 5-27
0x127	Pin Configuration 12	page 5-28
0x128	Video Count Low	page 5-28
0x129	Video Count Mid	page 5-28
0x12A	Video Count HIgh	page 5-28
0x12B	Audio Lock	page 5-29

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Table 5-3. Register Map Summary *(3 of 8)*

Address (hex)	Register Name	Page Number
0x12C	Audio Count Low	page 5-29
0x12D	Audio Count Mid	page 5-29
0x12E	Audio Lock 2	page 5-29
0x12F	Audio Lock 3	page 5-29
0x130	Power Control 1	page 5-30
0x131	Power Control 2	page 5-31
0x134	AFE Diagnostic Control 1	page 5-31
0x135	AFE Diagnostic Control 2	page 5-32
0x136	AFE Diagnostic Control 3	page 5-32
0x137	RESERVED	page 5-32
0x13C	AFE Diagnostic Control 5	page 5-33
0x13D	AFE Diagnostic Control 6	page 5-33
0x13E	AFE Diagnostic Control 7	page 5-33
0x13F	AFE Diagnostic Control 8	page 5-34
0x140	PLL Diagnostic Control 1	page 5-34
0x141	PLL Diagnostic Control 2	page 5-34
0x144–0x14F	Test Registers	page 5-35
0x158	RESERVED	page 5-35
0x159	DLL1 Diagnostic Control 2	page 5-35
0x15A	DLL1 Diagnostic Control 3	page 5-35
0x15B	DLL1 Diagnostic Control 4	page 5-36
0x15C	DLL2 Diagnostic Control 1	page 5-36
0x15D	DLL2 Diagnostic Control 2	page 5-36
0x15E	DLL2 Diagnostic Control 3	page 5-36
0x15F	DLL2 Diagnostic Control 4	page 5-37
Infrared Remote Registers:		
0x200	IR Control 1	page 5-37
0x201	IR Control 2	page 5-38
0x204	IR TX Clock Divider Low	page 5-39
0x205	IR TX Clock Divider High	page 5-39
0x208	IR RX Clock Divider Low	page 5-39
0x209	IR RX Clock Divider High	page 5-39
0x20C	IR Carrier Duty Cycle	page 5-40
0x210	IR Status	page 5-40
0x214	IR Interrupt Enable	page 5-41

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Table 5-3. Register Map Summary *(4 of 8)*

Address (hex)	Register Name	Page Number
0x218	IR Low-Pass Filter Low	page 5-41
0x219	IR Low-Pass Filter High	page 5-42
0x23C	IR FIFO Low	page 5-42
0x23D	IR FIFO High	page 5-42
0x23E	IR FIFO Level	page 5-42
Video Decoder Core Registers:		
0x400	Video Mode Control 1	page 5-43
0x401	Video Mode Control 2	page 5-44
0x402	Video Mode Control 3	page 5-45
0x403	Video Mode Control 4	page 5-46
0x404	Video Out Control 1	page 5-47
0x405	Video Out Control 2	page 5-48
0x406	Video Out Control 3	page 5-49
0x407	Video Out Control 4	page 5-49
0x408	Ancillary IDID-0	page 5-49
0x409	Ancillary IDID-1	page 5-50
0x40A	Ancillary IDID-0/1	page 5-50
0x40C	Copy Protection Status	page 5-50
0x40D	General Status 1	page 5-50
0x40E	General Status 2	page 5-51
0x410	Interrupt Status 1	page 5-51
0x411	Interrupt Status 2	page 5-52
0x412	Interrupt Mask 1	page 5-52
0x413	Interrupt Mask 2	page 5-53
0x414	Brightness	page 5-54
0x415	Contrast	page 5-54
0x416	Luma Control	page 5-54
0x418	Horizontal Scaling Low	page 5-55
0x419	Horizontal Scaling Mid	page 5-55
0x41A	Horizontal Scaling High	page 5-55
0x41B	Horizontal Scaling Control	page 5-55
0x41C	Vertical Scaling Low	page 5-55
0x41D	Vertical Scaling High	page 5-56
0x41E	Vertical Scaling Control	page 5-56
0x41F	Vertical Line Control	page 5-56

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Table 5-3. Register Map Summary *(5 of 8)*

Address (hex)	Register Name	Page Number
0x420	Saturation U	page 5-57
0x421	Saturation V	page 5-57
0x422	Hue	page 5-58
0x423	Chroma Control	page 5-58
0x424	VBI Line Control 1	page 5-59
0x425	VBI Line Control 2	page 5-59
0x426	VBI Line Control 3	page 5-60
0x427	VBI Line Control 4	page 5-60
0x428	VBI Line Control 5	page 5-60
0x429	VBI Line Control 6	page 5-60
0x42A	VBI Line Control 7	page 5-60
0x42B	VBI Line Control 8	page 5-60
0x42C	VBI Line Control 9	page 5-60
0x42D	VBI Line Control 10	page 5-61
0x42E	VBI Line Control 11	page 5-61
0x43F	VBI Line Control 12	page 5-61
0x430	VBI Line Control 13	page 5-61
0x431	VBI Line Control 14	page 5-61
0x432	VBI Line Control 15	page 5-61
0x433	VBI Line Control 16	page 5-61
0x434	VBI Line Control 17	page 5-62
0x438	VBI Frame Code Search Mode	page 5-62
0x439	VBI Alternate Frame Code Type	page 5-62
0x43A	VBI Alternate 1 Frame Code	page 5-62
0x43B	VBI Alternate 2 Frame Code	page 5-62
0x43C	VBI Miscellaneous Config 1	page 5-63
0x43D	TTX Packet Address 1	page 5-64
0x43E	TTX Packet Address 2	page 5-64
0x43F	TTX Packet Address 3	page 5-64
0x440	VBI 1 and 2 SDID	page 5-64
0x441	VBI 3 SDID	page 5-64
0x442	VBI FIFO Reset	page 5-64
0x443	VBI Hamming	page 5-65
0x444	Closed Caption Status	page 5-65
0x445	Closed Caption Data	page 5-65

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Table 5-3. Register Map Summary *(6 of 8)*

Address (hex)	Register Name	Page Number
0x446	GEMSTAR 1x Status	page 5-65
0x447	GEMSTAR 1x Data	page 5-66
0x448	GEMSTAR 2x Status	page 5-66
0x449	GEMSTAR 2x Data	page 5-66
0x44A	WSS Status	page 5-66
0x44B	WSS Data	page 5-66
0x44C	VBI Custom 1 Horizontal Delay	page 5-66
0x44D	VBI Custom 1 Bit Increment	page 5-67
0x44E	VBI Custom 1 Slice Distance	page 5-67
0x44F	VBI Custom 1 Clock Run-in Window	page 5-67
0x450	VBI Custom 1 Frame Code Low	page 5-68
0x451	VBI Custom 1 Frame Code Mid	page 5-68
0x452	VBI Custom 1 Frame Code High	page 5-68
0x453	VBI Custom 1 Frame Code Length	page 5-68
0x454	VBI Custom 1 Clock Run-in Period	page 5-68
0x455	VBI Custom 1 Clock Run-in Margin and Length	page 5-68
0x456	VBI Custom 1 Payload Length	page 5-69
0x457	VBI Custom 1 Miscellaneous	page 5-69
0x458	VBI Custom 2 Horizontal Delay	page 5-69
0x459	VBI Custom 2 Bit Increment	page 5-70
0x45A	VBI Custom 2 Slice Distance	page 5-70
0x45B	VBI Custom 2 Clock Run-in Window	page 5-70
0x45C	VBI Custom 2 Frame Code Low	page 5-70
0x45D	VBI Custom 2 Frame Code Mid	page 5-71
0x45E	VBI Custom 2 Frame Code High	page 5-71
0x45F	VBI Custom 2 Frame Code Length	page 5-71
0x460	VBI Custom 2 Clock Run-in Period	page 5-71
0x461	VBI Custom 2 Clock Run-in Margin and Length	page 5-71
0x462	VBI Custom 2 Payload Length	page 5-71
0x463	VBI Custom 2 Miscellaneous	page 5-72
0x464	VBI Custom 3 Horizontal Delay	page 5-72
0x465	VBI Custom 3 Bit Increment	page 5-72
0x466	VBI Custom 3 Slice Distance	page 5-73

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Table 5-3. Register Map Summary *(7 of 8)*

Address (hex)	Register Name	Page Number
0x467	VBI Custom 3 Clock Run-in Window	page 5-73
0x468	VBI Custom 3 Frame Code Low	page 5-73
0x469	VBI Custom 3 Frame Code Mid	page 5-73
0x46A	VBI Custom 3 Frame Code High	page 5-73
0x46B	VBI Custom 3 Code Length	page 5-74
0x46C	VBI Custom 3 Clock Run-in Period	page 5-74
0x46D	VBI Custom 3 Clock Run-in Margin and Length	page 5-74
0x46E	VBI Custom 3 Payload Length	page 5-74
0x46F	VBI Custom 3 Miscellaneous	page 5-75
0x470	Horizontal Blanking Delay Low	page 5-76
0x471	Horizontal Blanking Delay High	page 5-76
0x472	Horizontal Active HIgh	page 5-76
0x473	Burst Gate Delay	page 5-76
0x474	Vertical Blanking Delay Low	page 5-77
0x475	Vertical Blanking Delay High	page 5-77
0x476	Vertical Active High	page 5-77
0x477	Vertical Blanking Delay	page 5-77
0x478	SRC Decimation Ratio Low	page 5-77
0x479	SRC Decimation Ratio High	page 5-78
0x47A	Comb Filter Bandwidth Select	page 5-78
0x47B	Comb Filter Enable	page 5-79
0x47C	Subcarrier Step Size Low	page 5-80
0x47D	Subcarrier Step Size Mid	page 5-80
0x47E	Subcarrier Step Size High	page 5-81
0x47F	VBI Offset	page 5-81
0x480	Field Count Low	page 5-81
0x481	Field Count HIgh	page 5-81
Diagnostic Registers		
0x484	Temporal Decimation	page 5-82
0x485	Miscellaneous Timing Control	page 5-82
0x486	Test Register (DEFAULT 0x00)	page 5-82
0x487	Video Detect Configuration	page 5-83
0x488	VGA Gain Control	page 5-83
0x489	AGC Gain Control Low	page 5-83
0x48A	AGC Gain Control High	page 5-83
0x48B	Digital Front-End Control	page 5-84

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Table 5-3. Register Map Summary *(8 of 8)*

Address (hex)	Register Name	Page Number
0x48C	VGA Sync Control	page 5-84
0x48D	VGA Track Range	page 5-84
0x48E	VGA Acquire Range	page 5-84
0x490	DFE Control	page 5-84
0x491	Backporch Loop Gain	page 5-85
0x492	DFT Threshold	page 5-85
0x493	Backporch Percent	page 5-85
0x494	PLL Offset Low	page 5-85
0x495	PLL Offset High	page 5-85
0x496	PLL Indirect Loop Gain	page 5-85
0x497	PLL Direct Loop Gain	page 5-85
0x498	Horizontal Tracking Loop Indirect Gain	page 5-86
0x49C	Luma Comb Error Limit Max	page 5-86
0x49D	Luma Comb Threshold	page 5-86
0x49E	Chroma Comb Error Limit Max	page 5-86
0x49F	Luma Comb Error Limit Max	page 5-86
0x4A0	White Crush Increment	page 5-87
0x4A1	White Crush Decrement	page 5-87
0x4A2	White Crush Comparison Point	page 5-87
0x4A4	Soft Reset Mask 1	page 5-88
0x4A5	Soft Reset Mask 2	page 5-88
0x4B4	Version ID	page 5-89
0x4B8	MIscellaneous Diagnostic Control	page 5-89

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5.3 Serial Communications Host Registers

Host Register 1 **Address 0x000**

Bits	Type	Default	Name	Description
[7]	RW	0	FORCE_CHIP_SEL	Override the CHIP_SEL/VIPCLK pin for 12C address decode. 0 = Use the CHIP_SEL/VIPCLK pin for 12C decode 1 = The 12C chip select signal is forced to a 1 regardless of the CHIP_SEL/VIPCLK pin
[6]	RW	0	SLV_SI_DIS	Control the glitch filters and slew rate control in the 12C pads to enable a faster speed of operation. 0 = Glitch filters and slew rate control enabled 1= Glitch filters and slew rate control disabled
[5]	RW	0	AUTO_INC_DIS	Control auto-address increment after each byte transfer. 0 = Do the auto-address increment 1 = Do not increment the address
[4]	RW	0	PWR_DN_AUX_PLL	Power down the Auxiliary PLL. 0 = Do not power down 1 = Power down
[3]	RW	0	PWR_DN_VID_PLL	Power down the Video Clock PLL. 0 = Do not power down 1 = Power down
[2]	RW	1	REF_CLK_SEL	Crystal clock input type select. 0 = Single-ended input on XTI pin 1 = Differential signal required on crystal pins
[1]	RW	0	DIGITAL_PWR_DN	Gate digital clocks (sclk, vclk, clkx5). This bit can be configured to gate down clk5x or vclk only (see POWER_CTRL register). 0 = Do not gate 1 = Hold clocks in high state
[0]	RW	0	SLEEP	Put the chip in sleep mode. Gate the digital clocks and power down the analog circuitry. (Power down of some analog power domains can be masked when the SLEEP bit is asserted. See POWER_CTRL register.) 0 = Do not power down 1 = Power down

Host Register 2 **Address 0x001**

Bits	Type	Default	Name	Description
[2]	RW	0	PWR_DN_PLL_REG2	Powers down the regulator for the auxiliary clock PLL.
[1]	RW	0	PWR_DN_PLL_REG1	Powers down the regulator for the video clock PLL.
[0]	RW	0	PREFETCH_EN	Enables prefetch on reads. Prefetch is unnecessary unless the interface is operated many times faster than the typical maximum speed of 400 kHz. However, enabling prefetch can create problems when reading FIFOs. The prefetch operation can pop an entry from a FIFO, whether or not the transaction actually requests the byte. 0 = Disable 1 = Enable

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5.4 VIP Communications Host Registers

VIP Vendor ID **Address 0x000**

Bits	Type	Default	Name	Description
[15:0]	RO	0x14F1	VENDOR_ID	Conexant ID = 0x14F1

VIP Device ID **Address 0x002**

Bits	Type	Default	Name	Description
[15:0]	RO	0x837x or 0x836x	DEVICE_ID	Part ID. X denotes revision of chip.

VIP Subsystem ID **Address 0x004**

Bits	Type	Default	Name	Description
[15:0]	RO	0x0000	SUBSYS_ID	Identifies the board manufacturer

VIP Subsystem Vendor ID **Address 0x006**

Bits	Type	Default	Name	Description
[15:0]	RO	0x0000	SUBSYS_VEND_ID	Device ID of the subsystem

VIP Command **Address 0x008**

Bits	Type	Default	Name	Description
[15:3]	RZ	0x0000	RESERVED	
[2]	RW	0	XHOST_ON	A 1 indicates extended VIP capabilities. Host Interface does not support extended capabilities and hence a write to this state with a 1 has no effect.
[1:0]	RW	00	POWER_STATE	A read to this field shows the power mode in which the device is operating. Host Interface implements all the four power modes as described in VIP1.1 and VIP2. specification. Refer to section 1.6.6 for further details regarding these power modes.

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VIP Status **Address 0x00A**

Bits	Type	Default	Name	Description
[15:4]	RZ	0x0000	RESERVED	
[3:2]	RO	00	HOST_CAP	This indicates the Host Interface supports only 2 bit standard mode for Data on HAD lines.
[1]	RO	1	P2_SUPPORT	A 1 indicates support for P2 power mode.
[0]	R0	1	P1_SUPPORT	A 1 says Host Interface supports P1 power mode.

VIP Revision ID **Address 0x00C**

Bits	Type	Default	Name	Description
[15:0]	R0	0x0000	REV_ID	Revision of the chip

VIP Clock Status **Address 0x00E**

Bits	Type	Default	Name	Description
[15:5]	RZ	0x0000	PREFETCH_EN	Enable prefetch on reads. Prefetch is unnecessary unless the interface is operated many times faster than the typical max speed of 400 kHz. However, enabling prefetch can create problems when reading FIFOs. The prefetch operation can pop an entry from a FIFO, whether or not the transaction actually requests the byte.
[4]	RW	0	PWR_ON_PLL_REG2	Powers down the regulator for the auxiliary clock PLL.
[3]	RW	0	PWR_ON_PLL_REG1	Powers down the regulator for the video clock PLL.
[2]	RW	0	PWR_DN_AUX_PLL	Powers down AUX PLL.
[1]	RW	0	PWR_DN_VID_PLL	Powers down video PLL.
[0]	RW	0	REF_CLK_SEL	Selects between a differential crystal input versus a single-ended input. 0 = Digital buffer to support to support single-ended clock source 1 = Differential amplifier to support external crystal oscillator clock source

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5.5 Chip Configuration Space

Device ID Low Byte **Address 0x100**

Bits	Type	Default	Name	Description
[7:0]	RO	0x7x or 0x6x	DEVICE_ID_LOW	Device ID Lower Byte

Device ID High Byte **Address 0x101**

Bits	Type	Default	Name	Description
[7:0]	RO	0x83	DEVICE_ID_HIGH	Device ID Upper Byte

Miscellaneous Chip Control Configuration **Address 0x102**

Bits	Type	Default	Name	Description
[7:5]	RZ	00000	RESERVED	This bit should only be written with a logical 0.
[4]	RW	0	CHIP_ACFG_DIS	Auto-config disable of the following registers: 0 = Allow VID_PLL_INT, VID_PLL_FRAC, and AFE control fields to be automatically configured based on square pixel, video format, and input mode. 1 = Disable auto config With or without this bit set, the registers can always be written by software. The auto-config hardware only writes the registers when a change in format is detected.
[3]	RZ	0	RESERVED	
[2]	RW	0	DUAL_MODE_ADC2	Sets ADC2 to dual sampling mode. 0 = Normal mode 1 = Dual sampling mode
[1]	RW	0	CH_SEL_ADC2	ADC2 input select. This bit has no effect if the DUAL_MODE_ADC2 bit is set to 1. 0 = Analog input CH{2} 1 = Analog input CH{3}
[0]	RW, SC	0	SOFT_RST	Internal Reset 0 = Deassert reset 1 = Assert reset

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Video Input Control **Address 0x103**

Bits	Type	Default	Name	Description
[7:6]	RW	00	CH{3}_SOURCE	Selects input pin to CH{3} ADC. 00 = CVBS7/C3/Pr1 01 = CVBS8/C4/Pr2 10 and 11 = None
[5:4]	RW	00	CH{2}_SOURCE	Selects input pin to CH{2} ADC. 00 = CVBS4/Y4/Pb1 01 = CVBS5/C1/Pb2 10 = CVBS6/C2 11 = None
[3]	RZ	0	RESERVED	This bit should only be written with a logical 0.
[2:0]	RW	000	CH{1}_SOURCE	Selects input pin to CH{1} ADC 000 = CVBS1/Y1 001 = CVBS2/Y2 010 = CVBS3/Y3 011 = CVBS4/Y4/Pb1 100 = CVBS5/C1/Pb2 101 = CVBS6/C2 110 = CVBS7/C3/Pr1 111 = CVBS8/C4/Pr2

AFE Control 1 **Address 0x104**

Bits	Type	Default	Name	Description
[7]	RW	0	VGA_SEL_CH2	VGA gain select for CH2 0 = Video decoder drives VGA gain setting 1 = Audio decoder drives VGA gain setting
[6]	RW	0	VGA_SEL_CH1	VGA gain select for CH1 0 = Video decoder drives VGA gain setting 1 = Audio decoder drives VGA gain setting
[5]	RW	0	HALF_BW_CH3	When set, the CH3 anti-alias filter bandwidth is reduced to half.
[4]	RW	0	HALF_BW_CH2	When set, the CH2 anti-alias filter bandwidth is reduced to half.
[3]	RW	0	HALF_BW_CH1	When set, the CH1 anti-alias filter bandwidth is reduced to half.
[2]	RW	0	EN_12DB_CH3	Enables CH3 extra 12 dB gain 0 = Disable 1 = Enable
[1]	RW	0	EN_12DB_CH2	Enables CH2 extra 12 dB gain 0 = Disable 1 = Enable
[0]	RW	0	EN_12DB_CH1	Enables CH1 extra 12 dB gain 0 = Disable 1 = Enable

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AFE Control 2 **Address 0x105**

Bits	Type	Default	Name	Description
[7]	RW	1	CLAMP_EN_CH1	Enables (powers up) clamping for CH1.
[6]	RW	1	RESERVED	
[5]	RW	0	LUMA_IN_SEL	ADC input select for luma input path 0 = ADC 1 1 = ADC 2
[4]	RW	1	CHROMA_IN_SEL	ADC input select for chroma input path 0 = ADC 1 1 = ADC 2
[3]	RW	1	CLAMP_SEL_CH{3}	Clamp level select for CH{3} 0 = video decoder drives clamp level 1 = clamp level is fixed at 3'b111 (mid-code clamp). Use for chroma inputs.
[2]	RW	1	CLAMP_SEL_CH{2}	Clamp level select for CH{2} 0 = video decoder drives clamp level 1 = clamp level is fixed at 3'b111 (mid-code clamp). Use for chroma inputs.
[1]	RW	0	CLAMP_SEL_CH{1}	Clamp level select for CH{1} 0 = video decoder drives clamp level 1 = clamp level is fixed at 3'b111 (mid-code clamp). Use for chroma inputs.
[0]	RW	1	VGA_SEL_CH{3}	VGA gain select for CH{3} 0 = video decoder drives VGA gain setting 1 = audio decoder drives VGA gain setting

AFE Control 3 **Address 0x106**

Bits	Type	Default	Name	Description
[7]	RW	0	BYPASS_CH3	Bypass CH3 anti-alias filter when set.
[6]	RW	0	BYPASS_CH2	Bypass CH2 anti-alias filter when set.
[5]	RW	0	BYPASS_CH1	Bypass CH1 anti-alias filter when set.
[4]	RW	0	DROOP_COMP_CH3	Enables resistance boosting in CH3 input.
[3]	RW	0	DROOP_COMP_CH2	Enables resistance boosting in CH2 input.
[2]	RW	1	DROOP_COMP_CH1	Enables resistance boosting in CH1 input.
[1]	RW	0	CLAMP_EN_CH3	Enables (powers up) clamping for CH3. 0 = Disable 1 = Enable
[0]	RW	0	CLAMP_EN_CH2	Enables (powers up) clamping for CH2. 0 = Disable 1 = Enable

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AFE Control 4 **Address 0x107**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	This bit should only be written with a logical 0.
[3]	RW	0	IREF_SEL	Selects between on-chip (1) and external (0) resistor to generate reference current.
[2:0]	RW	111	RESERVED	

Video PLL Integer **Address 0x108**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x0F	VID_PLL_INT	Video PLL integer coefficient Valid values are 8–59 (decimal).

Video PLL Divider **Address 0x109**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x04	VID_PLL_POST	Video PLL post divide Valid values are 2–63 (decimal).

Aux PLL Integer **Address 0x10A**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x0A	AUX_PLL_INT	Auxiliary PLL integer coefficient Valid values are 8–59 (decimal).

Aux PLL Divider **Address 0x10B**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x10	AUX_PLL_POST	Auxiliary PLL post divide Valid values are 2–63 (decimal).

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Video PLL Fractional 1 **Address 0x10C**

Bits	Type	Default	Name	Description
[7:0]	RW	0xFE	VID_PLL_FRAC1	Lowest byte of the 25-bit fractional portion of the PLL multiplier

Video PLL Fractional 2 **Address 0x10D**

Bits	Type	Default	Name	Description
[7:0]	RW	0xE2	VID_PLL_FRAC2	Middle byte of the 25-bit fractional portion of the PLL multiplier

Video PLL Fractional 3 **Address 0x10E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x2B	VID_PLL_FRAC3	Highest byte of the 25-bit fractional portion of the PLL multiplier

Video PLL Fractional 4 **Address 0x10F**

Bits	Type	Default	Name	Description
[7:1]	RZ	0000000	RESERVED	
[0]	RW	0	VID_PLL_FRAC4	Highest bit of the 25-bit fractional portion of the PLL multiplier

Aux PLL Fractional 1 **Address 0x110**

Bits	Type	Default	Name	Description
[7:0]	RW	0x09	AUX_PLL_FRAC1	Lowest byte of the 25-bit fractional portion of the PLL multiplier

Aux PLL Fractional 2 **Address 0x111**

Bits	Type	Default	Name	Description
[7:0]	RW	0x07	AUX_PLL_FRAC2	Middle byte of the 25-bit fractional portion of the PLL multiplier

Aux PLL Fractional 3 **Address 0x112**

Bits	Type	Default	Name	Description
[7:0]	RW	0x98	AUX_PLL_FRAC3	Highest byte of the 25-bit fractional portion of the PLL multiplier

Aux PLL Fractional 4 **Address 0x113**

Bits	Type	Default	Name	Description
[7:1]	RZ	0000000	RESERVED	
[0]	RW	0	AUX_PLL_FRAC4	Highest bit of the 25-bit fractional portion of the PLL multiplier

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Pin Control 1 **Address 0x114**

Bits	Type	Default	Name	Description
[7]	RW	0	FIELD_OUT_EN	Output enable for FIELD/PRGM1 pin 0 = Disabled 1 = Enabled
[6]	RW	0	DVALID_OUT_EN	Output enable for DVALID/PRGM0 pin 0 = Disabled 1 = Enabled
[5]	RW	0	IR_TX_OUT_EN	Output enable for IR_TX_OUT pin 0 = Disabled 1 = Enabled
[4]	RW	0	IR_RX_OUT_EN	Output enable for IR_RX_OUT pin 0 = Disabled 1 = Enabled
[3]	RW	0	IRQN_OUT_EN	Output enable for IRQN_OUT pin 0 = Disabled 1 = Enabled
[2]	RW	0	CHIP_SEL_OUT_EN	Output enable for CHIP_SEL_OUT pin 0 = Disabled 1 = Enabled
[1]	RW	0	RESERVED	
[0]	RW	0	RESERVED	

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Pin Control 2 **Address 0x115**

Bits	Type	Default	Name	Description
[7]	RW	0	RESERVED	
[6]	RW	0	RESERVED	
[5]	RW	0	RESERVED	
[4]	RW	0	RESERVED	
[3]	RW	0	PIXCLK_OUT_EN	Output enable for PIXCLK pin 0 = Disabled 1 = Enabled
[2]	RW	0	VID_OUT_EN	Output enable for VID_DATA [7:0] pin 0 = Disabled 1 = Enabled
[1]	RW	0	VRESET_OUT_EN	Output enable for VRESET/PRGM3 pin 0 = Disabled 1 = Enabled
[0]	RW	0	HRESET_OUT_EN	Output enable for HRESET/PRGM2 pin 0 = Disabled 1 = Enabled

Pin Control 3 **Address 0x116**

Bits	Type	Default	Name	Description
[7:3]	RZ	0000	RESERVED	
[2]	RW	0	PLL_CLK_OUT_EN	Output enable for PLL_CLK pin 0 = Disabled 1 = Enabled
[1:0]	RW	00	RESERVED	

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Pin Control 4 **Address 0x117**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4]	RW	0	IR_IRQ_STAT	Infrared Remote Interrupt status 0 = interrupt is not active 1 = interrupt is active
[3]	RW	0	RESERVED	
[2]	RW	0	VID_IRQ_STAT	Video Interrupt status 0 = interrupt is not active 1 = interrupt is active
[1]	RW	0	IRQ_N_POLAR	Polarity of IRQ_N output 0 = IRQ_N is active low 1 = IRQ_N is active high
[0]	RZ	0	RESERVED	

Pin Control 5 **Address 0x118**

Bits	Type	Default	Name	Description
[7:4]	RW	0x00	RESERVED	
[3:2]	RW	00	VID_CTRL_SPD	Controls drive strength of PRGM{0:2} pads. 00 = Medium 01 = Slow 1x = Fast
[1:0]	RW	00	VID_OUT_SPD	Controls drive strength of PIXCLK and VID_DATA pads. 00 = Medium 01 = Slow 1x = Fast

Pin Control 6 **Address 0x119**

Bits	Type	Default	Name	Description
[7:2]	RZ	000000	RESERVED	
[1:0]	RW	00	GEN_OUT_SPD	Controls drive strength of IR_TX, IR_RX, IRQ_N, PRGM{3}/ HCTL, SER_CLK/HAD0, SER_DATA/HAD1. 00 = Medium 01 = Slow 1x = Fast

0x11A—RESERVED (DEFAULT 0x00)

Manufacturing Test

0x11C—RESERVED (DEFAULT 0x00)

Manufacturing Test

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Pin Configuration 2 **Address 0x11D**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	IRQN_OUT_SEL	Selects which signal to output on the IRQ_N/PRGM4 pin. 0000 = IRQ_N/PRGM4 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED
[3:0]	RW	0000	CHIPSEL_OUT_SEL	Selects which internal state is output on the CHIP_SEL/ VIPCLK pin. The options are: 0000 = GPO[0] 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED

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Pin Configuration 3 **Address 0x11E**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	IR_TX_OUT_SEL	Selects which signal to output on the IR_TX/PRGM6 pin. 0000 = IR_TX/PRGM6 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED
[3:0]	RW	0000	IR_RX_OUT_SEL	Selects which signal to output on the IR_RX/PRGM5 pin if this pin is in the output mode. 0000 = GPO[2] 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED

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Pin Configuration 4 **Address 0x11F**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	FIELD/PRGM1_OUT_SEL	Selects which signal to output on the PRGM1 pin. 0000 = FIELD 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED
[3:0]	RW	0000	DVALID/PRGM0_OUT_SEL	Selects which signal to output on the PRGM0 pin. 0000 = DVALID 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED

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Pin Configuration 5 **Address 0x120**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	VRESET/HCTL/PRGM3_OUT_SEL	Selects which signal to output on the PRGM3 pin. 0000 = VRESET/HCTL/PRGM3 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED
[3:0]	RW	0000	HRESET/PRGM2_OUT_SEL	Selects which signal to output on the PRGM2 pin. 0000 = HRESET 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED

Pin Configuration 6 **Address 0x121**

Bits	Type	Default	Name	Description
[7:2]	RZ	000000	RESERVED	
[1]	RW	0	PIXCLK_OUT_SEL	Should only be written with a 0
[0]	RW	0	VID_DATA_OUT_SEL	Should only be written with a 0

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Pin Configuration 7 **Address 0x122**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	AUX_PLL_DOUT_SEL	Selects which signal to output on the PLL _CLK pin. 0000 = PLL_CLK/PRGM7 0001 = ACTIVE 0010 = VACTIVE 0011 = CBFLAG 0100 = VID_DATA_EXT[0] 0101 = VID_DATA_EXT[1] 0110 = GPO[0] 0111 = GPO[1] 1000 = GPO[2] 1001 = GPO[3] 1010 = IRQ_N/PRGM4 1011 = RESERVED 1100 = RESERVED 1101 = PLL_CLK/PRGM7 1110 = VRESET/HCTL/PRGM3 1111 = RESERVED However, this register field works in conjunction with the AUX_PLL_AOUT_SEL field that directly controls the mux built into the PLL output pad. The AUX_PLL_DOUT_SEL field has no effect except when the CLK_PAD_IN selection is made. This selection means that the pad output comes from the digital core, rather than the analog domain.
[3]	RZ	0	RESERVED	
[2:0]	RW	001	AUX_PLL_AOUT_SEL	Selects which signal to output on the PLL_CLK/PRGM7 pin when AUX PLL is selected in the AUX_PLL_DOUT_SEL register field. x00 = XTI x5 DLL 101 = Video PLL 001 = Auxiliary PLL x10 = XTI x11 = CLK_PAD_IN (bits selected by [7:4] above)

0x123—RESERVED (DEFAULT 0x00)

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Pin Configuration 9 **Address 0x124**

Bits	Type	Default	Name	Description
[7:4]	RW	1000	GPI1_IN_SEL	Selects the pin that is muxed to the internal GPI1 flop. 0000 = DVALID/PRGM0 0001 = FIELD/PRGM1 0010 = HRESET/PRGM2 0011 = VRESET/HCTL/PRGM3 0100 = IRQ_N/PRGM4 0101 = IR_TX/PRGM6 0110 = IR_RX/PRGM5 0111 = RESERVED 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = PLL_CLK/PRGM7
[3:0]	RW	0111	GPI0_IN_SEL	Selects the pin that is muxed to the internal GPI0 flop. 0000 = DVALID/PRGM0 0001 = FIELD/PRGM1 0010 = HRESET/PRGM2 0011 = VRESET/HCTL/PRGM3 0100 = IRQ_N/PRGM4 0101 = IR_TX/PRGM6 0110 = IR_RX/PRGM5 0111 = RESERVED 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = PLL_CLK/PRGM7

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Pin Configuration 10 **Address 0x125**

Bits	Type	Default	Name	Description
[7:4]	RW	1011	GPI3_IN_SEL	Selects the pin that is muxed to the internal GPI3 flop. 0000 = DVALID/PRGM0 0001 = FIELD/PRGM1 0010 = HRESET/PRGM2 0011 = VRESET/HCTL/PRGM3 0100 = IRQ_N/PRGM4 0101 = IR_TX/PRGM6 0110 = IR_RX/PRGM5 0111 = RESERVED 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = PLL_CLK/PRGM7
[3:0]	RW	0110	GPI2_IN_SEL	Selects the pin that is muxed to the internal GPI2 flop. 0000 = DVALID/PRGM0 0001 = FIELD/PRGM1 0010 = HRESET/PRGM2 0011 = VRESET/HCTL/PRGM3 0100 = IRQ_N/PRGM4 0101 = IR_TX/PRGM6 0110 = IR_RX/PRGM5 0111 = RESERVED 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = PLL_CLK/PRGM7

Pin Configuration 11 **Address 0x126**

Bits	Type	Default	Name	Description
[7:4]	RO		GPIO_IN	Data from pins selected by the GPIOx_IN_SEL register settings.
[3:0]	RW	0000	GPIO_OUT	Registers that hold data that may get sent to the pins selected by the pin configuration registers.

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Pin Configuration 12 **Address 0x127**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RW	0	SA_MCLK_SEL	Selects alternate post-divider for internal SA_MCLK. The serial audio master clock is sent to the audio decoder for use in generating the bit and word clocks. 0 = Use AUX_PLL_POST value to derive SA_MCLK. 1 = PLL_CLK is divided by the alternate post-divider programmed in the SA_MCLK_DIV value.
[5:0]	RW	000000	SA_MCLK_DIV	Controls the generation of alternate serial audio master clock (PLL_CLK) post-divider when SA_MCLK_SEL is enabled. 0 or 1 = Bypass divider. PLL_CLK = Output of AUX_PLL_CLK VCO prior to the post-divider. 2–63 = Divide output of AUX_PLL_CLK VCO by the value in this field.

Video Count Low **Address 0x128**

Bits	Type	Default	Name	Description
[7:0]	RW	0xF8	VID_COUNT_LOW	Least significant byte of the expected count (minus 1 and times 8) for 8x PLL clock when the number of audio clocks is counted as reflected in AUD_COUNT.

Video Count Mid **Address 0x129**

Bits	Type	Default	Name	Description
[7:0]	RW	0x93	VID_COUNT_MID	Middle byte of the expected count (minus 1 and times 8) for 8x PLL clock when the number of audio clocks is counted as reflected in AUD_COUNT.

Video Count High **Address 0x12A**

Bits	Type	Default	Name	Description
[7:0]	RW	0x11	VID_COUNT_HIGH	Most significant byte of the expected count (minus 1 and times 8) for 8x PLL clock when the number of audio clocks is counted as reflected in AUD_COUNT.

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Audio Lock **Address 0x12B**

Bits	Type	Default	Name	Description
[7:1]	RW	1010000	RESERVED	This bit should only be written with a logical zero.
[0]	RW	0	EN_AV_LOCK	Enable locking of auxiliary PLL to video pixel rate.

Audio Count Low **Address 0x12C**

Bits	Type	Default	Name	Description
[7:0]	RW	0xFF	AUD_COUNT_LOW	Least significant byte of the number of audio sample-rate clocks, minus 1, to count before examining VID_COUNT

Audio Count Mid **Address 0x12D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x5F	AUD_COUNT_MID	Middle byte of the number of audio sample-rate clocks to count, minus 1, before examining VID_COUNT

Audio Lock 2 **Address 0x12E**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:4]	RW		AUD_LOCK_FREQ_SHIFT	The gain applied to the frequency error (difference in actual vs. expected counts) before passing to the loop filter. This is in addition to a default scaling that occurs. There is a default left or right shift depending on the length of time over which the sample is collected, as indicated by the VID_COUNT field.
[3:0]	RW	0x00	AUD_COUNT_HIGH	Upper 4 bits of the number of audio sample-rate clocks to count minus 1, before examining VID_COUNT.

Audio Lock 3 **Address 0x12F**

Bits	Type	Default	Name	Description
[7:4]	RW	0x01	AUD_LOCK_KI_MULT	The gain applied to the indirect error path of the loop filter through an unsigned multiply. this is used to lock the AUX PLL to the video pixel rate.
[3:0]	RW	0x01	AUD_LOCK_FREQ_SHIFT AUD_LOCK_KD_MULT	The gain applied to the direct error path of the loop filter through an unsigned multiply. This is used to lock the AUX PLL to the video pixel rate.

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Power Control 1 **Address 0x130**

Bits	Type	Default	Name	Description
[7]	RW	0	PWR_DN_CH3	Powers down Channel 3 VGA/filter circuitry. 0 = Do not power down Channel 3 1 = Power down Channel 3
[6]	RW	0	PWR_DN_CH2	Powers down Channel 2 VGA/filter circuitry. 0 = Do not power down Channel 2 1 = Power down Channel 2
[5]	RW	0	PWR_DN_CH1	Powers down Channel 1 VGA/filter circuitry. 0 = Do not power down Channel 1 1 = Power down Channel 1
[4]	RW	0	PWR_DN_ADC2	Powers down ADC2 circuitry. 0 = Do not power down ADC2 1 = Power down ACD2
[3]	RW	0	PWR_DN_ADC1	Powers down ADC1 circuitry. 0 = Do not power down ADC1 1 = Power down ACD1
[2]	RW	0	PWR_DN_DLL2	Powers down DLL2 (5x clock) circuitry. 0 = Do not power down DLL2 1 = Power down DLL2
[1]	RW	0	PWR_DN_DLL1	Powers down DLL1 (5x clock) circuitry. 0 = Do not power down DLL1 1 = Power down DLL1
[0]	RW	0	PWR_DN_TUNING	Powers down filter tuning circuitry. 0 = Do not power down filter tuning 1 = Power down filter tuning

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Power Control 2 **Address 0x131**

Bits	Type	Default	Name	Description
[5]	RW	0	SCLK_GATE_MSK	SCLK and 12S_MCLK gate mask 0 = DIG_PWR_ON disables sample clock (SCLK) and I2S master clock (I2S_MCLK) 1 = Gating of SCLK and I2S_MCLK inhibited
[4]	RW	0	CLK5x_GATE_MSK	CLK5x gate mask 0 = DIG_PWR_ON disables high-speed audio clock (CLK5x) 1 = Gating of CLK5x inhibited
[3]	RW	0	VCLK_GATE_MSK	Video clock gate mask 0 = DIG_PWR_ON disables high-speed video clock (VCLK) 1 = Gating of VCLK inhibited
[2]	RW	0	SLEEP_PLL_MSK	PLL sleep mask 0 = SLEEP powers down PLLs 1 = Power down of PLL inhibited
[1]	RW	0	SLEEP_DLL_MSK	DLL sleep mask 0 = SLEEP powers down DLL (5x clock) circuitry 1 = Power down inhibited
[0]	RW	0	SLEEP_ANALOG_MSK	Analog subsystem sleep mask 0 = SLEEP powers down analog subsystem 1 = Power down of analog subsystem inhibited including DLL and PLLs

AFE Diagnostic Control 1 **Address 0x134**

Bits	Type	Default	Name	Description
[7:4]	RZ	00	RESERVED	
[3]	RW	0	VREF_CTRL_ADC	Digital control for ADC reference voltage. 0 = 1.60 V 1 = 1.20 V
[2:1]	RW	01	VREG_D[1:0]	Voltage Regulator Select. Controls what voltage the regulator targets to supply the digital core. 00 = 1.20 V 01 = 1.26 V 10 = 1.32 V 11 = 1.38 V
[0]	RW	0	FOUR_X_CLK_ADC	Chooses 4x or 5x DLL output 0 = 5x output 1 = 4x output

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AFE Diagnostic Control 2 **Address 0x135**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6:5]	RW	00	BIAS_CTRL_ADC[6:5]	Digital control for the reference buffer bias. 00 = 50 µA 01 = 62.5 µA 10 = 37.5 µA 11 = 75 µA
[4:3]	RW	11	BIAS_CTRL_ADC[4:3]	MSB comparator current. 00 = 12.5 µA 01 = 6.25 µA 10 = 25 µA 11 = 50 µA
[2]	RW	0	BIAS_CTRL_ADC[2]	Digital control for refp and refm 0 = 1.6 V, 0.8 V 1 = 1.5 V, 0.9 V
[1:0]	RW	00	BIAS_CTRL_ADC[1:0]	Digital control for ADC bias current. 00 = 50 µA 01 = 37.5 µA 10 = 62.5 µA 11 = 75 µA

AFE Diagnostic Control 3 **Address 0x136**

Bits	Type	Default	Name	Description
[7:4]	RZ	0x0	RESERVED	
[3:2]	RW	01	FILTER_BIAS[1:0]	Digital control for bias current multiplier. 00 = 0.5 01 = 1 10 = 1.5 11 = 2
[1:0]	RW	01	S2DIFF_BIAS[1:0]	Digital control for the single-ended to differential converter bias multiplier. 00 = 0.75 01 = 1 10 = 1.25 11 = 1.5

0x137—RESERVED (DEFAULT 0x00)

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AFE Diagnostic Control 5 **Address 0x13C**

Bits	Type	Default	Name	Description
[7:4]	RZ	0	RESERVED	
[3]	RW	0	TEST_MODE_CH1	Connects the differential analog signal at ADC1 input to pins VIN2 and VIN3. 0 = Do not connect 1 = Connect
[2]	RW	0	DISCONNECT_CH1	Disables the filter in CH1 test mode. 0 = Enable filter 1 = Disable filter
[1]	RW	0	CH_SEL_ADC1	ADC1 test mode 0 = Connects ADC1 to output of filter. 1 = Connects ADC1 to the output of first VGA stage.
[0]	RW	0	TUNE_FIL_RST	Reset filter tuning logic. When 1, filter tuning is reset. When set back to 0, filter will auto-tune itself, and after a few clocks, return to normal operation.

AFE Diagnostic Control 6 **Address 0x13D**

Bits	Type	Default	Name	Description
[7]	RW	0	FORCE_TUNING	Auto tuning code override 0 = Do not override 1 = Forces tuning code to value contained in TUNE_IN field.
[6:5]	RZ	00	RESERVED	
[4:0]	RW	00000	TUNE_IN[4:0]	Tuning code to be used when FORCE_TUNING is set. Overrides the value chosen by auto tuning.

AFE Diagnostic Control 7 **Address 0x13E**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5]	RO		TUNING_READY	Filter auto tuning status 0 = Not complete 1 = Filter tuning complete
[4:0]	RO		TUNE_OUT	The tuning code selected by the auto-tune algorithm.

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AFE Diagnostic Control 8 **Address 0x13F**

Bits	Type	Default	Name	Description
[7:2]	RZ	0x00	RESERVED	
[1]	RW	0	AUD_DUAL_FLAG_POL	Audio Decoder Dual Flag Polarity Polarity of dual_flag signal sent to audio decoder. 0 = Noninverted polarity 1 = Inverted polarity
[0]	RW	0	VID_DUAL_FLAG_POL	Video Decoder Dual Flag Polarity Polarity of dual_flag signal sent to video decoder. 0 = Noninverted polarity 1 = Inverted polarity

PLL Diagnostic Control 1 **Address 0x140**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x04	PLL_SPMP	PLL charge pump current

PLL Diagnostic Control 2 **Address 0x141**

Bits	Type	Default	Name	Description
[7]	RR	0	VID_PLL_UNLOCK	Video PLL unlock detection 0 = No unlock detected 1 = Unlock detected
[6]	RR	0	AUX_PLL_UNLOCK	Auxiliary PLL unlock detection 0 = No unlock detected 1 = Unlock detected
[5]	RO	0	VID_PLL_LOCK	Video PLL lock status 0 = Unlocked 1 = Locked
[4]	RO	0	AUX_PLL_LOCK	Auxiliary PLL lock status 0 = Unlocked 1 = Locked
[3]	RW	0	AUX_PLL_RST	Video PLL reset 0 = Do not reset 1 = Reset the auxiliary PLL
[2]	RW	0	VID_PLL_RST	Auxiliary PLL reset 0 = Do not reset 1 = Reset the auxiliary PLL
[1]	RW	0	AUX_PLL_DDS	Auxiliary PLL delta sigma fractional divide 0 = Enable 1 = Disable
[0]	RW	0	VID_PLL_DDS	Video PLL delta signal fractional divide 0 = Enable 1 = Disable

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0x144–0x14F—Test Registers
Manufacturing Use

0x158—RESERVED (DEFAULT 0x00)

DLL1 Diagnostic Control 2 **Address 0x159**

Bits	Type	Default	Name	Description
[7:6]	RW	00	COMP_GT_LOW	Lower 2 bits of COMP_GT Used in False Lock Detect: counts this many pulses in half period to determine pulse-swallow.
[5:3]	RW	100	CHPREF	Charge pump current. Bit2 = 50 μA Bit1 = 25 μA Bit0 = 12.5 μA Static is 6 μA
[2]	RW	0	DOWN_OVRD	Overrides the down command to PFD.
[1]	RW	0	UP_OVRD	Overrides the up command to PFD.
[0]	RW	1	FLD	False Lock Detect mode

DLL1 Diagnostic Control 3 **Address 0x15A**

Bits	Type	Default	Name	Description
[7]	RW	1	DLYS_LOW	Low bit of DLYS Adds delay in path of reference.
[6:4]	RW	110	DEPTH	Used in False Lock detect: increases stability of decisions in FLD. 111:x7 routes DLL output to test pad 110:x6 puts DLL in fast lock mode
[3:1]	RW	011	COMP_LT	Used in False Lock Detect: counts this many pulses in half period to determine up override.
[0]	RW	1	COMP_GT_HIGH	High bit of COMP_GT. Used in False Lock Detect: counts this many pulses in half period to determine pulse-swallow.

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DLL1 Diagnostic Control 4 **Address 0x15B**

Bits	Type	Default	Name	Description
[7]	RW	0	DLL1_BYPASS	Clock reference for DLL1 (ADC DLL) input from clock pad rather than crystal input. Overrides CLK_OUT_MODE.
[6:5]	RZ	00	RESERVED	
[4:1]	RW	0000	CURRSET	Changes current used in DLL.
[0]	RW	0	DLYS_HIGH	High bit of DLYS. Adds delay in path of reference.

DLL2 Diagnostic Control 1 **Address 0x15C**

Bits	Type	Default	Name	Description
[7:0]	RZ	0x00	RESERVED	

DLL2 Diagnostic Control 2 **Address 0x15D**

Bits	Type	Default	Name	Description
[7:6]	RW	00	COMP_GT_LOW	Used in False Lock Detect: counts this many pulses in half period to determine pulse-swallow.
[5:3]	RW	100	CHPREF	Charge pump current. Bit2 = 50 μA Bit1 = 25 μA Bit0 = 12.5 μA Static is 6 μA
[2]	RW	0	DOWN_OVRD	Overrides the down command to PFD.
[1]	RW	0	UP_OVRD	Overrides the up command to PFD.
[0]	RW	1	FLD	False Lock Detect mode.

DLL2 Diagnostic Control 3 **Address 0x15E**

Bits	Type	Default	Name	Description
[7]	RW	1	DLYS_LOW	Low bit of DLYS Adds delay in path of reference.
[6:4]	RW	110	DEPTH	Used in False Lock detect: increases stability of decisions in FLD. 111:x7 routes DLL output to test pad 110:x6 puts DLL in fast lock mode
[3:1]	RW	011	COMP_LT	Used in False Lock Detect: counts this many pulses in half period to determine up override.
[0]	RW	1	COMP_GT_HIGH	High bit of COMP_GT. Used in False Lock Detect: counts this many pulses in half period to determine pulse-swallow.

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DLL2 Diagnostic Control 4 **Address 0x15F**

Bits	Type	Default	Name	Description
[7:6]	RW	0	DLL2_BYPASS	Clock reference for DLL2 (Audio Decoder DLL) input from clock pad rather than crystal input. Overrides CLK_OUT_MODE.
[6:5]	RZ	00	RESERVED	
[4]	RW			Control for DLL2 (Audio Decoder DLL).
[3:1]			CURRSET	Changes current used in DLL
[0]	RW	0	DLLYS_HIGH	High bit of DLYS Adds delay in path of reference.

IR Control 1 **Address 0x200**

Bits	Type	Default	Name	Description
[7]	RW	0	TFE	Transmit FIFO Enable 0 = Disable and reset transmit FIFO to all 0s 1 = Enable transmit FIFO
[6]	RW	0	RFE	Receive FIFO Enable 0 = Disable and reset receive FIFO to all 0s 1 = Enable receive FIFO
[5]	RW	0	MOD	Transmit Modulation Enable 0 = Disable transmit carrier modulation, transmit data as simple logic levels 1 = Enable transmit carrier modulation, transmit a mark as a burst of ir_tx_data pin transitions, and a space as the absence of transitions Programming the carrier polarity bit determines whether ones or 0s are encoded into marks/high or spaces/low
[4]	RW	0	DMD	Receive Demodulation Enable 0 = Disable receive carrier demodulation, receive data as simple logic levels 1 = Enable receive carrier demodulation, detect a mark as a series of RX pin transitions, and a space as the absence of transitions Programming the carrier polarity bit determines whether marks/high or spaces/low are decoded as ones or 0s
[3:2]	RW	00	EDG	Receive Edge Detect Control 00 = Disabled 01 = Falling edges trigger RX filter/pulse timer start/stop 10 = Rising edges trigger RX filter/pulse timer start/stop 11 = Either edge trigger RX filter/pulse timer start/stop The RX low pass filter and pulse width timer starts/ends a pulse duration measurement each time the programmed edge on the demodulated input is detected
[1:0]	RW	00	WIN	Next Predicted Receive Carrier Edge Window Limits 00 = Next carrier edge predicted to be 16 RX clocks –3/+3 01 = Next carrier edge predicted to be 16 RX clocks –4/+3 10 = Next carrier edge predicted to be 16 RX clocks –3/+4 11 = Next carrier edge predicted to be 16 RX clocks –4/+4 Once the first rising-edge within a carrier burst is detected, each subsequent rising-edge should occur 16 RX clock cycles later, plus or minus the programmed limits above, transitions out of this range are not detected.

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IR Control 2 **Address 0x201**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RW	0	R	Receive FIFO load on Timer Overflow Disable 0 = Load Rx FIFO with 1's and Rx_data_Ih level on timer overflow; 1 = Do Not load Rx FIFO on timer overflow. Shut off when noise occurs but must be turned back on when a real transmission starts.
[5]	RW	0	LBM	Loop Back Mode 0 = Transmit and receive operation functions normally through the IR port's pins. 1 = The output of the transmit modulation logic is fed into the input of the receive demodulation logic internal to the IR port. Transmit pin continues to reflect transmit data, receive pin is ignored by the IR receive logic.
[4]	RW	0	CPL	Carrier Polarity (Transmitter Only) 0 = If mod/demodulation enabled, 1s are transmitted and received as series of carrier transitions (mark), 0s are transmitted and received as the absence of a carrier or no transitions (space). If mod/demodulation disabled, ones transmitted/received as logic high, 0s as logic low, and the ir_tx_data pin is driven low when idle. 1 = If mod/demodulation enabled, ones transmitted and received as the absence of a carrier or no transitions (space), 0s transmitted and received as a series of carrier transitions (mark). If mod/demodulation disabled, ones transmitted/received as logic low, 0s as logic high, and the ir_tx_data pin is driven high when idle. Note(s): Receive carrier polarity can be changed by software. No hardware support for this.
[3]	RW	0	TIC	Transmitter Interrupt Control 0 = Transmit FIFO service interrupt/DMA request asserted when TX FIFO is half full or less, negated when TX FIFO is more than half full 1 = Transmit FIFO service interrupt/DMA request asserted after transmitter becomes idle, negated when transmitter becomes busy. See status register below for a description of this interrupt request.
[2]	RW	0	RIC	Receiver Interrupt Control 0 = Receive FIFO service interrupt/DMA request asserted when RX FIFO is half full or greater, negated when RX FIFO is less than half full. 1 = Receive FIFO service interrupt/DMA request asserted when RX FIFO is not empty, negated when RX FIFO is empty. See the status register for a description of this interrupt request.

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IR Control 2 (continued) **Address 0x201**

Bits	Type	Default	Name	Description
[1]	RW	0	TXE	Transmitter Enable 0 = Disable transmitter 1 = Enable transmitter
[0]	RW	0	RXE	Receiver Enable 0 = Disable receiver 1 = Enable receiver

IR TX Clock Divider Low **Address 0x204**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	TCD_LOW	Transmit Clock Divider 16-bit value used by the transmit clock down counter as a modulus value to generate the transmit clock for the modulator and TX pulse width timer. Transmit clock counter reloaded any time this register is written. A value of 0x00 is not permitted for the TCD

IR TX Clock Divider High **Address 0x205**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	TCD_HIGH	Transmit Clock Divider 16-bit value used by the transmit clock down counter as a modulus value to generate the transmit clock for the modulator and TX pulse width timer. Transmit clock counter reloaded any time this register is written. A value of 0x00 is not permitted for the TCD.

IR RX Clock Divider Low **Address 0x208**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	RCD_LOW	Receive Clock Divider 16-bit value used by the receive clock down counter as a modulus value to generate the receive clock for the demodulator and RX pulse width timer. Receive clock counter reloaded any time this register is written. A value of 0x00 is not permitted for the RCD.

IR RX Clock Divider High **Address 0x209**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	RCD_HIGH	Receive Clock Divider 16-bit value used by the receive clock down counter as a modulus value to generate the receive clock for the demodulator and RX pulse width timer. Receive clock counter reloaded any time this register is written. A value of 0x00 is not permitted for the RCD.

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IR TX Carrier Duty Cycle **Address 0x20C**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3:0]	RW	0000	CDC	Transmit Carrier Duty Cycle 0000 = 1 TX clock high and 15 TX clocks low 0001 = 2 TX clocks high and 14 TX clocks low 0010 = 3 TX clocks high and 13 TX clocks low ... 1101 = 14 TX clocks high and 2 TX clocks low 1110 = 15 TX clocks high and 1 TX clock low 1111 = 16 TX clocks high and 0 TX clocks low

IR Status **Address 0x210**

Bits	Type	Default	Name	Description
[7:6]	RW	00	RESERVED	
[5]	R	0	TSR	Transmit FIFO Service Request 0 = If TIC=0 in IR_CNTL_REG, transmit FIFO is more than half full. If TIC=1, transmitter is busy. 1 = IF TIC=0, transmit FIFO is half full or less. If TIC=1, transmitter is idle. Generate an irq request if the TSE mask bit is set in the IR_IRQEN_REG.
[4]	R	0	RSR	Receive FIFO Service Request 0 = If RIC=0 in IR_CNTL_REG, receive FIFO is less than half full. If RIC=1, receive FIFO is empty. 1 = IF RIC=0, receive FIFO is half full or more. If RIC=1, receive FIFO is not empty. Generate an irq request if the RSE mask bit is set in the IR_IRQEN_REG.
[3]	R	0	TBY	Transmitter Busy (noninterruptible) 0 = Transmitter is idle 1 = Transmitter is busy
[2]	R	0	RBY	Receiver Busy (noninterruptible) 0 = Receiver is idle 1 = Receiver is busy
[1]	R	0	ROR	Receive FIFO Overrun 0 = Receive FIFO contains one or more empty entries or is full but has not experienced an overrun 1 = Receive FIFO has experienced an overrun, generate an irq request if the ROE mask bit is set in the IR_IRQEN_REG Note(s): When an overrun occurs, data within the FIFO remains intact, and any new data from the RX pulse width counter is lost until the FIFO once again contains one or more empty entries.

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IR Status (continued) **Address 0x210**

Bits	Type	Default	Name	Description
[0]	R	0	RTO	Receive Pulse Width Timer Time-out 0 = Receive pulse width counter has not reached its limit 1 = Receive pulse width counter has reached its limit (contains all ones), generate an irq request if the RTE mask bit is set in the ir_irq Note(s): Cleared by disabling RXE (Rx enable) bit of the IR_CNTRL_REG

IR Interrupt Enable **Address 0x214**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5]	RW	0	TSE	Transmit FIFO Service Request Interrupt Enable 0 = Transmit FIFO/Idle interrupt disabled 1 = Transmit FIFO/Idle interrupt enabled
[4]	RW	0	RSE	Receive FIFO Service Request Interrupt Enable 0 = Receive FIFO interrupt disabled 1 = Receive FIFO interrupt enabled
[3:2]	RZ	00	RESERVED	
[1]	RW	0	ROE	Receive FIFO Overrun Interrupt Enable 0 = Receive FIFO overrun interrupt disabled 1 = Receive FIFO overrun interrupt enabled
[0]	R	0	RTE	Receive Pulse Width Timer Time-out Interrupt Enable 0 = Receive pulse width timer time-out interrupt disabled 1 = Receive pulse width timer time-out interrupt enabled

IR Low-Pass Filter Low **Address 0x218**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	LPF_LOW	Low Pass Filter Modulus 16-bit value used as a modulus value to filter out pulses below a minimum width. Filter counter is reloaded with modulus each time the programmed edge is encountered. Counter decrements using the host bus clock, if the next edge is seen before the counter reaches 0, the pulse measurement is discarded. If the counter reaches 0 it retains this value until the next edge is seen. Whenever the counter contains a 0, pulse measurements are saved to the RX FIFO. A value of 0x0000 disables the filter function, and values 0x0001 through 0x0004 are not permitted.

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IR Low Pass Filter High **Address 0x215**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	LPF_HIGH	Low Pass Filter Modulus 16-bit value is used as a modulus value to filter out pulses below a minimum width. Filter counter is reloaded with modulus each time programmed edge is encountered. Counter decrements using the host bus clock, if next edge seen before counter reaches 0, pulse measurement is discarded. If counter reaches 0 it retains this value until the next edge is seen. Whenever the counter contains a 0, pulse measurements are saved to the RX FIFO. A value of 0x0000 disables the filter function, and values 0x0001 through 0x0004 are not permitted.

IR FIFO Low **Address 0x23C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	RX/TX_FIFO_LOW	Transmit/Receive Pulse Width Count/Measurement Value Read: Bottom entry of the receive FIFO Write: Top entry of the receive FIFO

IR FIFO High **Address 0x23D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	RX/TX_FIFO_HIGH	Transmit/Receive Pulse Width Count/Measurement Value Read: Bottom entry of the receive FIFO Write: Top entry of the receive FIFO

IR FIFO Level **Address 0x23E**

Bits	Type	Default	Name	Description
[7:2]	RZ	000000	RESERVED	
[1]	RO		RXNDV	Receive Next Data Valid (read-only) 0 = No more data in the RX FIFO 1 = One or more entries of valid data remain in RX FIFO
[0]	RW	0	RX/TX_LVL	Transmit/Receive Pin Level Read: Value of demodulated input at end of RX pulse width measurement Write: Value to send to modulator for TX pulse width count output

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5.6 Video Decoder Core

These registers are used to configure the basic mode of the video decoder. In general, the configuration controlled by these registers is static based on the desired application.

This section also includes interrupt management for the video decoder core.

Video Mode Control 1 **Address 0x400**

Bits	Type	Default	Name	Description
[7]	RW, PW	0	AFD_NTSC_SEL	This bit is used by the Auto Format Detect block to differentiate between NTSC-M and NTSC-J. 0 = NTSC-M 1 = NTSC-J
[6]	RW, PW	0	AFD_PAL_SEL	This bit is used by the Auto Format Detect block to differentiate between PAL-N and PAL-B,D,G,H,I. 0 = PAL-BDGHI 1 = PAL-N
[5]	RW, PW	0	ACFG_DIS	Disable autoconfig of registers addressed 0x470 to 0x47F based on format. 0 = Enable 1 = Disable
[4]	RW, PW	0	SQ_PIXEL	Square-pixel mode
[3:0]	RW, PW	0000	VID_FMT_SEL	Manual video format select value. This value is used to force the video decoder into a certain video format when it is non-0. 0000 = AUTO-DETECT 0001 = NTSC-M 0010 = NTSC-J 0011 = NTSC-4.43 0100 = PAL-BDGHI 0101 = PAL-M 0110 = PAL-N 0111 = PAL-NC 1000 = PAL-60 1100 = SECAM

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Video Mode Control 2 **Address 0x401**

Bits	Type	Default	Name	Description
[7]	RW	1	WCEN	White crush enable
[6]	RW	1	CAGCEN	Chroma AGC enable 0 = Enable 1 = Disable
[5]	RW	1	CKILLEN	Chroma killer enable 0 = Enable 1 = Disable
[4]	RW	1	AUTO_SC_LOCK	Auto chroma subcarrier lock speed select 0 = Manual mode. Lock speed is determined by man_sc_fast_lock 1 = Auto Mode When unlocked, chose fast lock speed. When locked, choose slow speed.
[3]	RW	0	MAN_SC_FAST_LOCK	Manual chroma subcarrier lock speed select. 1 = Fast lock speed This bit is a don't-care if the AUTO_SC_LOCK bit is set.
[2:1]	RW	00	INPUT_MODE	Signal Input Format 00 = CVBS 01 = Y/C 11 = Y/Pb/Pr
[0]	RW	0	AFD_ACQUIRE	By setting to 1 and then 0, forces the auto-format-detect state machine to re-evaluate the incoming video format and update AFD_FMT_STAT accordingly. 0 = The auto-detect state machine operates normally. 1 = The auto-detect state machine soft reset. The auto-detect state machine is forced back to the INIT state, and held there until the bit is cleared.

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Video Mode Control 3 **Address 0x402**

Bits	Type	Default	Name	Description
[5:4]	RW	00	CKILL_MODE	Color Kill Mode. Defines how luma output is generated when color kill asserted: 0 = Chroma output is forced to 0, and luma output is generated from normal comb filter operation (default) 1 = Chroma output is forced to 0, entire chroma band is notched from luma output. The comb filter is forced into notch mode 1 (see COMB_NOTCH_MODE field) 2 = Black and White mode. Chroma output is forced to 0, and entire composite signal is treated as luma. The comb filter is forced into notch mode 3 (see COMB_NOTCH_MODE field)
[3:2]	RW	10	COMB_NOTCH_MODE	Controls behavior Y/C separation when adaptive comb filter selects notch (bandpass) filter output rather than combed output. 0 = Disable notch filter. Comb only 1 = Notch data is interpreted as chroma 2 = Notch data is split (50/50) between luma and chroma (default) 3 = Notch data is interpreted as luma (black and white mode)
[1]	SC	0	CLR_LOCK_STAT	Clear HLOCK, VLOCK, and clock status bits
[0]	RW	0	FAST_LOCK_MD	Active-high fast lock algorithm select. This register selects between a standard and a fast vertical locking algorithm. This has two effects: The fast locking algorithm (FAST_LOCK_MD=1) locks onto the first vertical sync that it encounters, regardless of its position. The normal vertical locking algorithm (FAST_LOCK_MD=0) looks for a sync within an expected window. If no sync appears during the next expected window, it locks onto the first subsequent incoming vertical sync. The fast locking algorithm bypasses the 8 field hysteresis that is built into the field detection logic. In this mode as soon as the even/odd field is detected, the field signal reflects the status. When this is disabled the field detection must be stable for 8 consecutive fields before the field signal reflects the change.

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Video Mode Control 4 **Address 0x403**

Bits	Type	Default	Name	Description
[5]	RW	0	AFD_PAL60_DIS	Disable the auto-detection of PAL-60 formats. 0 = PAL-60 can be detected and discriminate from NTSC-4.43 based on phase alternation. 1 = Any 525-line 4.43 format is assumed to be NTSC-4.43.
[4]	RW	0	AFD_FORCE_SECAM	Force SECAM format when 625 lines are detected. 0 = The auto-detect algorithm proceeds normally. 1 = SECAM is chosen when a 625-line format is detected.
[3]	RW	0	AFD_FORCE_PALNC	Force PAL_Nc format when 625 lines are detected. 0 = The auto-detect algorithm proceeds normally. 1 = PAL-Nc is chosen when a 625-line format is detected according to the AFD_PAL_SEL bit.
[2]	RW	0	AFD_FORCE_PAL	Force PAL_BG format when 625 lines are detected. 0 = The auto-detect algorithm proceeds normally. 1 = PAL-BG/PAL-N is chosen when a 625-line format is detected.
[1:0]	RW	00	AFD_PALM SEL	Select PAL-M format when 525-lines and 3.58 carrier is detected. 00 = NTSC will be detected according to the AFD_NTSC_SEL bit. 01 = PAL-M format is chosen when 525 lines and a 3.58 carrier is detected 10 = Enable algorithm to dynamically detect between NTSC-M and PAL-M.

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Video Out Control 1 **Address 0x404**

Bits	Type	Default	Name	Description
[7]	RW	0	BLUE_FIELD_EN	Enable generation of blue field on output when decoder loses lock. 0 = Disable 1 = Enable
[6]	RW	0	BLUE_FIELD_ACT	Activate blue field on output regardless of BLUE_FIELD_EN register.
[5]	RW	1	TASKBIT_VAL	Task bit value in VIP 2 mode.
[4]	RW	1	ANC_DATA_EN	Enable Ancillary Data Insertion for BT.656 or VIP modes. 0 = Disable 1 = Enable
[3]	RW	0	VBIHACTRAW_EN	Enables raw data output during the horizontal active region of the vertical blanking interval 0 = Disable 1 = Enable
[2]	RW	0	MODE10B	Selects either 8-bit or 10-bit output for 4:2:2 Luma and Chroma output. 0 = Luma and Chroma Output are rounded to 8 bits 1 = Luma and Chroma Output have 10 bits of resolution
[1:0]	RW	01	OUT_MODE	Selects video output format 00 = SPI-coded video Synchronous Pixel Interface (SPI) 01 = ITU-R BT.656 control codes 10 = VIP 1.1 control codes 11 = VIP 2 control codes

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Video Out Control 2 **Address 0x405**

Bits	Type	Default	Name	Description
[7:6]	RW	00	CLK_GATING	Select pixel clock gating scheme 0X = No gating 10 = Gate with VALID output 11 = Gate with logical AND of VALID and ACTIVE outputs
[5]	RW	1	CLK_INVERT	When set, the pixel clock output is inverted.
[4]	RW	0	HSFMT	Selects width of HRESET_N 0 = Nominal width 1 = One pixel clock (VOF_PIXCLK) pulse wide
[3]	RW	0	VALIDFMT	VALID signal format 0 = Valid indicates nonscaled pixels 1 = Valid is logical AND of nominal VALID and ACTIVE, where ACTIVE is controlled by ACTFMT register.
[2]	RW	1	ACTFMT	Active signal format 0 = Active is composite active 1 = Active is horizontal active
[1]	RW	0	SWAPRAW	Switch the positioning of the raw samples between the luma and chroma data paths 0 = Even samples on chroma; odd samples on luma 1 = Odd samples on chroma; even samples on luma
[0]	RW	1	CLAMPRAW_EN	Enable clamping of raw ADC samples to 1-254.75 when video output format mode uses control codes 0 = Disable 1 = Enable

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Video Out Control 3 **Address 0x406**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4]	RW	0	VIPCLAMP_EN	Clamp luma and chroma data in VIP modes (i.e., when OUT_MODE[1]=1) to 1-254.75. Affects all output bytes except control codes, raw data, and ancillary data fields. 0 = Disable 1 = Enable
[3]	RW	0	VIPBLANK_EN	Enable substitution of blanking data during horizontal and vertical blanking intervals during VIP modes (i.e., when OUT_MODE[1]=1) 0 = Disable 1 = Enable
[2]	RW	0	VIP_OPT_AL	VIP optional active line enable. In VIP modes, the transition of the V-bit from 1 to 0 is determined by either the VBLANK register or V656BLANK register. 0 = VBLANK 1 = V656BLANK
[1]	RW	0	IDID0_SOURCE	Source of IDID0 byte in VIP ancillary data 0 = IDID0 register 1 = Line Count from VBI Slicer
[0]	RW	0	DCMODE	Determines the format of the data count field in ancillary data in 8-bit mode (MODE10B=0) 0 = Data Count is number of blocks of 4 UDWs, with padding 1 = Data Count is number UDWs

Video Out Control 4 **Address 0x407**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	POLAR	When bit is set, invert polarity of output Bit [0] = VRESET/PRGM3 Bit [1] = HRESET/PRGM2 Bit [2] = ACTIVE Bit [3] = FIELD/PRGM1 Bit [4] = CBFLAG Bit [5] = VACTIVE Bit [6] = DVALID/PRGM0

Ancillary IDID-0 **Address 0x408**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	IDID0[9:2]_LOW	Value for IDID0 byte in VIP ancillary data. ([9:2] are used in 8-bit mode.)

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Ancillary IDID-1 **Address 0x409**

Bits	Type	Default	Name	Description
[9:0]	RW	0x00	IDID1[9:2]_LOW	Value for IDID1 byte in VIP ancillary data. ([9:2] are used in 8-bit mode.)

Ancillary IDID-0/1 **Address 0x40A**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3:2]	RW	00	IDID1[1:0]_HIGH	Value for IDID1 byte in VIP ancillary data. ([1:0] are used in 10-bit mode.)
[1:0]	RW	00	IDID0[1:0]_HIGH	Value for IDID0 byte in VIP ancillary data. ([1:0] are used in 10-bit mode.)

Copy Protection Status **Address 0x40C**

Bits	Type	Default	Name	Description
[7]	RO	0	MV_TYPE2_PAIR	Macrovision Type 2 pair detected
[6]	RO	0	MV_T3CS	A 1 indicates the presence of type 3 of the color stripe process. A one here always triggers 1 in the MV_CS bit.
[5]	RO	0	MV_CS	Macrovision Color Striping Detected
[4]	RO	0	MV_PSP	Macrovision Pseudo Sync Pulses detected
[3:2]	RZ	00	RESERVED	
[1:0]	RO	00	MV_CDAT	Macrovision Copy Control Bits as described in the MacroVision spec. This an encoding of the same information that is contained in MV_CS, MV_T3CS, and MV_PSP.

General Status 1 **Address 0x40D**

Bits	Type	Default	Name	Description
[7]	RO	0	VSYNC	Vertical sync
[6]	RO	0	SRC_FIFO_UFLOW	Sample Rate Converter FIFO Underflow
[5]	RO	0	SRC_FIFO_OFLOW	Sample Rate Converter FIFO Overflow
[4]	RO	0	FIELD	Field status (even/odd)
[3:0]	RO	0001	AFD_FMT_STAT	Currently detected Format

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General Status 2 **Address 0x40E**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RO	0	SPECIAL_PLAY_N	Active-low special play mode (fast forward, rewind, pulse, or slow motion). This is used to disable certain algorithms when not in a normal play mode. Special play mode is assumed wen the detected vsync falls outside of a narrow 2-line expected window.
[5]	RO	0	VPRES	Active-high video present. Indication of the presence of a reasonable video signal, one that we can lock onto horizontally or both horizontally and vertically. If vpres_vert_en = 0, then vpres is dependent upon the location of the last 32 hsync pulses relative to their expected location. If vpres_vert_en = 1, then vpres is dependent upon both the location of the last 16 vsync pulses and the last 32 hsync pulses relative to their expected locations.
[4]	RO	0	AGC_LOCK	VGA lock status
[3]	RO	0	CSC_LOCK	Color Subcarrier lock status
[2]	RO	0	VLOCK	Vertical lock status
[1]	RO	0	SRC_LOCK	Sample Rate Converter lock Status
[0]	RO	0	HLOCK	Horizontal lock status

Interrupt Status 1 **Address 0x410**

Bits	Type	Default	Name	Description
[7]	RR	0	END_VBI_ODD_STAT	The end of the VBI region of an odd field sets this bit.
[6]	RR	0	FMT_CHANGE_STAT	A change in the detected video format sets this bit.
[5]	RR	0	VSYNC_TRAIL_STAT	The falling edge of the detected vsync sets this bit.
[4]	RR	0	HLOCK_CHANGE_STAT	A change in the horizontal lock status sets this bit.
[3]	RR	0	VLOCK_CHANGE_STAT	A change in the vertical lock status sets this bit.
[2]	RR	0	CSC_LOCK_CHANGE_STAT	A change in the Color Subcarrier Lock status sets this bit.
[1]	RR	0	SRC_FIFO_UFLOW_STAT	The detection of a SRC FIFO Underflow sets this bit.
[0]	RR	0	SRC_FIFO_OFLOW_STAT	The detection of a SRC FIFO Overflow sets this bit.

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Interrupt Status 2 **Address 0x411**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RR	0	WSS_DAT_AVAIL_STAT	VBI FIFO for Wide-Screen-Signaling has data (not empty).
[5]	RR	0	GS2_DAT_AVAIL_STAT	VBI FIFO for Gemstar 2X has data (not empty).
[4]	RR	0	GS1_DAT_AVAIL_STAT	VBI FIFO for Gemstar 1X has data (not empty).
[3]	RR	0	CC_DAT_AVAIL_STAT	VBI FIFO for Closed Caption has data (not empty).
[2]	RR	0	VPRES_CHANGE_STAT	A change in the vpres (video present) status bit sets this bit.
[1]	RR	0	MV_CHANGE_STAT	A change in the mv_cdat field sets this bit.
[0]	RR	0	END_VBI_EVEN_STAT	The end of the VBI region of an even field sets this bit.

Interrupt Mask 1 **Address 0x412**

Bits	Type	Default	Name	Description
[7]	RW	1	END_VBI_ODD_MSK	When set, END_VBI_ODD_STAT is masked from generating an interrupt.
[6]	RW	1	FMT_CHANGE_MSK	When set, FMT_CHANGE_STAT is masked from generating an interrupt.
[5]	RW	1	VSYNC_TRAIL_MSK	When set, VSYNC_TRAIL_STAT is masked from generating an interrupt.
[4]	RW	1	HLOCK_CHANGE_MSK	When set, HLOCK_CHANGE_STAT is masked from generating an interrupt.
[3]	RW	1	VLOCK_CHANGE_MSK	When set, VLOCK_CHANGE_STAT is masked from generating an interrupt.
[2]	RW	1	CSC_LOCK_CHANGE_MSK	When set, CSC_LOCK_CHANGE_STAT is masked from generating an interrupt.
[1]	RW	1	SRC_FIFO_UFLOW_MSK	When set, SRC_FIFO_UFLOW_STAT is masked from generating an interrupt.
[0]	RW	1	SRC_FIFO_OFLOW_MSK	When set, SRC_FIFO_OFLOW_STAT is masked from generating an interrupt.

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Interrupt Mask 2 **Address 0x413**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RR	0	WSS_DAT_AVAIL_MSK	When set, WSS_DAT_AVAIL_STAT is masked from generating an interrupt.
[5]	RR	0	GS2_DAT_AVAIL_MSK	When set, GS2_DAT_AVAIL_STAT from generating an interrupt.
[4]	RR	0	GS1_DAT_AVAIL_MSK	When set, GS1_DAT_AVAIL_STAT from generating an interrupt.
[3]	RR	0	CC_DAT_AVAIL_MSK	When set, CC_DAT_AVAIL_STAT from generating an interrupt.
[2]	RW	1	VPRES_CHANGE_MSK	When set, VPRES_CHANGE_STAT is masked from generating an interrupt.
[1]	RW	1	MV_CHANGE_MSK	When set, MV_CHANGE_STAT is masked from generating an interrupt.
[0]	RW	1	END_VBI_EVEN_MSK	When set, END_VBI_EVEN_STAT is masked from generating an interrupt.

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5.6.1 Basic User Settings

The following registers are for dynamic user control of basic video parameters such as scaling, brightness, contrast, hue, and saturation.

Brightness **Address 0x414**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	BRIGHT	Brightness offset. This value is effectively an offset that is added to the luma signal to produce a brighter output. In 8-bit output mode, one least significant bit change adds or subtracts 0.5. In 10-bit output mode, one least significant bit change adds or subtracts 2.

Contrast **Address 0x415**

Bits	Type	Default	Name	Description
[7:0]	RW	0x80	CNTRST	Contrast multiply value. This value is a 1.7 number that is multiplied by the luma level to produce an adjusted luma signal. The resulting range of the contrast multiplication factor is 0– 1.996. A 1-bit change causes a 0.78% difference of the original signal.

Luma Control **Address 0x416**

Bits	Type	Default	Name	Description
[7:6]	RW	00	LUMA_CORE_SEL	Luma coring threshold select. This value determines the cutoff threshold for the luma coring logic. 00 = no coring 01 = coring threshold set to ±16 10 = coring threshold set to ±32 11 = coring threshold set to ±64 As a result, any pixel value between the selected threshold limits will result in 0.
[5:4]	RW	00	RANGE	Selects the allowed luma output range. This allows the user to select between three possible output ranges. 00 = range: 64–1016 Nominal 656 range with excursions allowed up to 1016. 01 = range: 4–1016 Nominal 656 range with excursions allowed up to 1016 and down to 4. 1x = range: 0–1023 Full-range.
[3]	RZ	0	RESERVED	
[2]	RW	0	PEAK_EN	Peaking enable 0 = Disable 1 = Enable
[1:0]	RW	00	PEAK_SEL	Select for peaking filter response. This value selects from the four available peaking filter responses. 00 = +2.0 dB response @ center freq 01 = +3.5 dB response @ center freq 10 = +5.0 dB response @ center freq 11 = +6.0 dB response @ center freq

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Horizontal Scaling Low **Address 0x418**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	HSCALE_LOW	Least significant byte of Horizontal Scaling Ratio (hscale = (scaling ratio–1) x 2^{20}).

Horizontal Scaling Mid **Address 0x419**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	HSCALE_MID	Middle significant byte of Horizontal Scaling Ratio (hscale = (scaling ratio–1) x 2^{20}).

Horizontal Scaling High **Address 0x41A**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	HSCALE_HIGH	Most significant byte of Horizontal Scaling Ratio (hscale = (scaling ratio–1) x 2^{20}).

Horizontal Scaling Control **Address 0x41B**

Bits	Type	Default	Name	Description
[7:2]	RZ	00000	RESERVED	
[1:0]	RW	00	HFILT	Low pass filter select. This is used in the luma low pass filter block to determine which of the three filters or the auto-mode should be used. 00 = Auto Mode 01 = CIF 10 = QCIF 11 = ICON

Vertical Scaling Low **Address 0x41C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VSCALE_LOW	Least significant byte of Vertical Scaling Ratio (vsf = 2^{16} – (scaling ratio – 1) x 2^{9})

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Vertical Scaling High **Address 0x41D**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4:0]	RW	0x00	VSCALE_HIGH	Most significant byte of Vertical Scaling Ratio (vsf = 2^{16} – (scaling ratio – 1) x 2^{9})

Vertical Scaling Control **Address 0x41E**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3]	RW	0	VS_INTRLACE	VS Interlace Format. The initial output phase must alternate if the scaled images are to be interlaced. 0 = Noninterlace VS 1 = Interlace VS
[2:0]	RW	000	VFILT	These bits control the number of taps in the Vertical Scaling Filter. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure the needed data does not overflow the internal FIFO. 000 = 2-tap interpolation (available at all resolutions) 001 = 3-tap interpolation (available if scaling to less than 385 horizontal active pixels) 010 = 4-tap interpolation (available if scaling to less than 193 horizontal active pixels) 011 = 5-tap interpolation (available if scaling to less than 193 horizontal active pixels)

Vertical Line Control **Address 0x41F**

Bits	Type	Default	Name	Description
[7:1]	RZ	0000000	RESERVED	
[0]	RW	0	LINE_AVG_DIS	PAL line averaging disable. 0 = PAL line averaging enabled. Adjacent lines are averaged together to produce the output lines. 1 = PAL line averaging disabled

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Saturation U **Address 0x420**

Bits	Type	Default	Name	Description
[7:0]	RW	0x80	USAT	Saturation adjust for U chroma

Decimal	Hex	Percent of Original
255	0xFF	199.22
254	0xFE	198.44
. . .	. . .	. . .
129	0x81	100.78
128	0x80	100.00
127	0x7F	99.22
. . .	. . .	. . .
1	0x01	0.78
0	0x00	0.00

Saturation V **Address 0x421**

Bits	Type	Default	Name	Description
[7:0]	RW	0x80	VSAT	Saturation adjust for V chroma

Decimal	Hex	Percent of Original
255	0xFF	199.22
254	0xFE	198.44
. . .	. . .	. . .
129	0x81	100.78
128	0x80	100.00
127	0x7F	99.22
. . .	. . .	. . .
1	0x01	0.78
0	0x00	0.00

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Hue **Address 0x422**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	HUE	Hue adjust. A 1-bit change causes the subcarrier phase to rotate in increments of 0.35 degrees with a range of –45 degrees to +45 degrees. Hue adjust is supported for NTSC and PAL, but not SECAM.

Chroma Control **Address 0x423**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4:2]	RW	000	CHR_DELAY	Chroma delay. A signed number representing the number of pixel the chroma is delayed relative to the luma. A value of 0 matches the luma to chroma. 110 = –2 111 = –1 000 = 0 001 = +1 010 = +2 All others = 0 delay
[1:0]	RW	00	C_CORE_SEL	Chroma coring select. 000 = No coring 01 = ±7 10 = ±15 11 = ±31

5.6.2 VBI Slicer Configuration

The following registers are for the purpose of configuring the VBI format slicing and output. This includes the ability to configure three custom VBI formats through the VBI_CUSTx_CFG registers. The default configuration for VBI_CUST1_CFG is Closed Caption 525, VBI_CUST2_CFG is WSS625, and VBI_CUST3_CFG is WST525, System C.

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VBI Line Control 1 **Address 0x424**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE1	1st VBI line data type First VBI line as defined by VOFFSET. The mode consists of 4 bits as listed below. The most significant nibble is used for the odd field and the least significant nibble is used for the even field. 525 line modes: 0000 = no VBI data slicing 0001 = WST525-B 0010 = WST525-C (NABTS) 0011 = WST525-D (Moji) 0100 = WSS525 0101 = VITC525 0110 = CC525 0111 = Gemstar 1x 1000 = Gemstar 2x 1001 = Custom VBI1 1010 = Custom VBI2 1011 = Custom VBI3 625 line modes: 0000 = no VBI data slicing 0001 = WST625-B 0010 = WST625-A 0011 = RESERVED 0100 = WSS625 0101 = VITC625 0110 = CC625 0111 = VPS 1000 = RESERVED 1001 = Custom VBI1 1010 = Custom VBI2 1011 = Custom VBI3

VBI Line Control 2 **Address 0x425**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE2	2nd VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

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VBI Line Control 3 **Address 0x426**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE3	3rd VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 4 **Address 0x427**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE4	4th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 5 **Address 0x428**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE5	2nd VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 6 **Address 0x429**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE6	6th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 7 **Address 0x42A**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE7	7th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 8 **Address 0x42B**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE8	8th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 9 **Address 0x42C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE9	9th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

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VBI Line Control 10 **Address 0x42D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE10	10th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 11 **Address 0x42E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE11	11th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 12 **Address 0x42F**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE12	12th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 13 **Address 0x430**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE13	13th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 14 **Address 0x431**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE14	14th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 15 **Address 0x432**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE15	15th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Line Control 16 **Address 0x433**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE16	16th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

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VBI Line Control 17 **Address 0x434**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI_MD_LINE17	17th VBI line data type. Valid programmed values are the same as in VBI LINE CONTROL 1 register.

VBI Alternate Frame Code Search Mode **Address 0x438**

Bits	Type	Default	Name	Description
[7:1]	RZ	0000000	RESERVED	
[0]	RW	0	FC_SEARCH_MODE	Frame code search mode. Allows dynamic search from frame code: 0 = Frame code match is declared only if frame code (start code, data run-in) is found at expected bit position 1 = Frame code match is declared upon discovering the first bit sequence that matches the expected pattern. Only applies for common frame code lengths of 3, 8, 12,16 and 24.

VBI Alternate Frame Code Type **Address 0x439**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	FC_ALT2_TYPE	When this field matches the VBIMODE setting for a particular line, the FC_ALT2 frame code is used instead of the default frame code associated with a given autoconfig mode. This allows using an alternate frame code for any given autoconfig mode.
[3:0]	RW	0000	FC_ALT1_TYPE	When this field matches the VBIMODE setting for a particular line, the FC_ALT1 frame code is used instead of the default frame code associated with a given autoconfig mode. This allows using an alternate frame code for any given autoconfig mode.

VBI Alternate 1 Frame Code **Address 0x43A**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	FC_ALT1	Alternate frame code used when VBIMODE matches FC_ALT1_TYPE.

VBI Alternate 2 Frame Code **Address 0x43B**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	FC_ALT2	Alternate frame code used when VBIMODE matches FC_ALT2_TYPE.

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VBI Miscellaneous Config 1 **Address 0x43C**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5]	RW	0	MOJI_PACK_DIS	Moji packing disable. 0 = WST525, system D formats cause the decoder to extract the first 6 bits for the first byte packet. The subsequent bit stream is packed into standard byte packets. 1 = The WST 525, system D bit stream is packed into byte packets in a normal fashion.
[4]	RW	0	VPS_DEC_DIS	VPS biphase decode disable. 0 = VPS formats are decoded based on a two-bit biphase pattern. 1 = Raw slice bits are transmitted
[3:2]	RW	01	CRI_MARG_SCALE	Clock run-in margin scale. Used to loosen or tighten lock criteria for clock run-in. 00 = Divide default timing margin by 2 01 = Use default timing margin 10 = Multiply default timing margin by 2 11 = Multiply default timing margin by 4
[1]	RW	1	EDGE_RESYNC_EN	Enable dynamic timing resynchronization based on edge detection. 0 = Sample point timing is determined by initial edge synchronization during clock run-in. 1 = Sample point timing is re-synchronized upon detecting any edge during data pattern.
[0]	RW	0	ADAPT_SLICE_DIS	Disable adaptive slice level 0 = Slice level comes from averaging points in the clock run-in. 1 = Slice level is set to pre-determined level based on mode.

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TTX Packet Address 1 **Address 0x43D**

Bits	Type	Default	Name	Description
[7:0]	RW	0000	TTX_PKTADRL_LB	Low byte of Teletext packet address lower limit for packet filtering purposes. Enabled when VBIx_TTX_MODE = 1.

TTX Packet Address 2 **Address 0x43E**

Bits	Type	Default	Name	Description
[7:4]	RW	1111	TTX_PKTADRU_LN	Low nibble of Teletext packet address upper limit for packet filtering purposes. Enabled when VBIx_TTX_MODE = 1.
[3:0]	RW	0000	TTX_PKTADRL_HN	High nibble of Teletext packet address lower limit for packet filtering purposes. Enabled when VBIx_TTX_MODE = 1.

TTX Packet Address 3 **Address 0x43F**

Bits	Type	Default	Name	Description
[7:0]	RW	0xFF	TTX_PKTADRU_HB	High byte of Teletext packet address upper limit for packet filtering purposes. Enabled when VBIx_TTX_MODE = 1.

VBI 1 and 2 SDID **Address 0x440**

Bits	Type	Default	Name	Description
[7:4]	RW	0100	VBI2_SDID	SDID to use when VBI_CUST2 data type is selected.
[3:0]	RW	0110	VBI1_SDID	SDID to use when VBI_CUST1 data type is selected.

VBI 3 SDID **Address 0x441**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3:0]	RW	0010	VBI3_SDID	SDID to use when VBI_CUST3 data type is selected.

VBI FIFO Reset **Address 0x442**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3]	RW	0	WSS_FIFO_RST	When = 1, reset WSS payload FIFO
[2]	RW	0	GS2_FIFO_RST	When = 1, reset Gemstar2x payload FIFO
[1]	RW	0	GS1_FIFO_RST	When = 1, reset Gemstar1x payload FIFO
[0]	RW	0	CC_FIFO_RST	When = 1, reset Closed Caption/XDS payload FIFO

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VBI Hamming **Address 0x443**

Bits	Type	Default	Name	Description
[7:4]	RZ	0000	RESERVED	
[3:0]	RW	0000	HAMMING_TYPE	When this field matches the VBIMODE setting for a particular line, hamming comparison is enabled for that type. Leave this field at 0x0 to disable the feature. When enabled, the least-significant four bits of the framing code are used for hamming comparison.

Closed Caption Status **Address 0x444**

Bits	Type	Default	Name	Description
[7:0]	RO	0x00	CC_STAT	Generic payload status format: Bit 7 – PARERR 0 – No parity error detected 1 – Parity error detected Bit 6 – FF 0 – FIFO not full 1 – FIFO full Bit 5 – DA 0 – FIFO is empty 1 – One or more bytes available for read Bit 4 – CX/XDS 0 – CC byte (odd field) 1 – XDS byte (even field) Bits 3–2 – RESERVED Bits 1–0 – BYTE_NUM BYTE_NUM describes byte number within a field. For payloads larger than four, the number will wrap. 00 – byte 1 01 – byte 2 02 – byte 3 03 – byte 4

Closed Caption Data **Address 0x445**

Bits	Type	Default	Name	Description
[7:0]	RO,PR	0x00	CC_FIFO_DAT	CC/XDS payload data. Data pointer advanced after reading this byte.

GEMSTAR 1x Status **Address 0x446**

Bits	Type	Default	Name	Description
[7:0]	RO	0x00	GS1_STAT	See description of CC_STAT byte

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GEMSTAR 1x Data **Address 0x447**

Bits	Type	Default	Name	Description
[7:0]	RO,PR	0x00	GS1_FIFO_DAT	Gemstar 1x payload data. Data pointer advanced after reading this byte.

GEMSTAR 2x Status **Address 0x448**

Bits	Type	Default	Name	Description
[7:0]	RO	0x00	GS2_STAT	See description of CC_STAT byte

GEMSTAR 2x Data **Address 0x449**

Bits	Type	Default	Name	Description
[7:0]	RO,PR	0x00	GS2_FIFO_DAT	Gemstar 2x payload data. Data pointer advanced after reading this byte.

WSS Status **Address 0x44A**

Bits	Type	Default	Name	Description
[7:0]	RO	0x00	WSS_STAT	See description of CC_STAT byte (PARERR will be held at 0).

WSS Data **Address 0x44B**

Bits	Type	Default	Name	Description
[7:0]	RO,PR	0x00	WSS_FIFO_DAT	Wide Screen Signaling payload data. Data pointer advanced after reading this byte.

VBI Custom 1 Horizontal Delay **Address 0x44C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x7E	VBI1_HDELAY	Delay from internal hreset signal to start of clock run-in in number of pixel clock cycles. VBI1_HDELAY = (hdelay (μs) x pixel_rate (MHz)) – 13

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VBI Custom 1 Bit Increment **Address 0x44D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x99	VBI1_BITINC_LOW	Least significant byte of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase encoding modes, this sample rate should be set to six times the effective bit rate. VBI1_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

VBI Custom 1 Slice Distance **Address 0x44E**

Bits	Type	Default	Name	Description
[7:4]	RW	0x1	VBI1_SLICE_DIST	Slice level sample distance. Controls how often samples are taken for the adaptive slice level routine. Distance is defined in terms of 1/8 or a bit period time, where the bit period is defined by BITINC. The parameter describes the number of points where samples are NOT taken. Therefore, to take one sample every four points, put three in this field.
[3:0]	RW	0x0	VBI1_BITINC_HIGH	Most significant nibble of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase encoding modes, this sample rate should be set to six times the effective bit rate. VBI1_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

VBI Custom 1 Clock Run-in Window **Address 0x44F**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6:0]	RW	0x2C	VBI1_CRWIN	Specifies the time window during which edge detection (positive and negative) is inhibited. This window is based on the clock run-in frequency. Avoids spurious edges from being detected. VBI1_CRWIN = 4 x pixel_rate x clock_runin_half_period x wr; Where wr = window ratio, portion of cycle to inhibit detection

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VBI Custom 1 Frame Code Low **Address 0x450**

Bits	Type	Default	Name	Description
[7:0]	RW	0x01	VBI1_FRAME_CODE_LOW	Least significant byte of start code bit pattern in transmission order

VBI Custom 1 Frame Code Mid **Address 0x451**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI1_FRAME_CODE_MID	Middle byte of start code bit pattern in transmission order

VBI Custom 1 Frame Code High **Address 0x452**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI1_FRAME_CODE_HIGH	Most significant byte of start code bit pattern in transmission order

VBI Custom 1 Frame Code Length **Address 0x453**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4:0]	RW	0x03	VBI1_FC_LENGTH	Number of start bits (or frame code bits)

VBI Custom 1 Clock Run-in Period **Address 0x454**

Bits	Type	Default	Name	Description
[7:0]	RW	0x0D	VBI1_CRI_TIME	Expected time period of clock run-in period in terms of halves of the bit period specified in VBI1_BITINC. The algorithm detects the number of edges specified in VBI1_CRI_LENGTH and compares the elapsed time with this parameter. If the result is within VBI1_CRI_MARGIN of this parameter, then the waveform is decoded.

VBI Custom 1 Clock Run-in Margin and Length **Address 0x455**

Bits	Type	Default	Name	Description
[7:4]	RW	0x4	VBI1_CRI_LENGTH	Number of clock run-in edges expected in the CRI period. This does not include the edge that transitions into the frame start code, and this is an N-1 parameter. For example, in a Teletext waveform with 16 bit periods and 16 edges, program 0xF in this register. For closed caption with 6.5 bit periods, but 13 edges, program 0xC
[3:0]	RW	0x4	VBI1_CRI_MARGIN	This field specifies the margin around VBI1_CRI_TIME in which the measured time of the clock run-in period can fall. See VBI1_CRI_TIME. This is in units of eights of the bit period defined by VBI1_BITINC.

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VBI Custom 1 Payload Length **Address 0x456**

Bits	Type	Default	Name	Description
[7:0]	RW	0x08	VBI1_PAYLD_LENGTH	Number of data bits to be captured, divided by two. If N is the number of bits in the payload, program this register with N/2.

VBI Custom 1 Miscellaneous **Address 0x457**

Bits	Type	Default	Name	Description
[7]	RW	0	VBI1_HAM_EN	Enable hamming comparison for framing comparison when this bit is set. When set VBI1_FRAME_CODE[3:0] are used for hamming comparison.
[6:4]	RW	010	VBI1_FIFO_MODE	Determines which payload FIFO is loaded. 000 = Don't load to payload FIFO 001 = Load to Gemstar 1x FIFO 010 = Load to CC FIFO 011 = Load to WSS FIFO 100 = Load to Gemstar 2x FIFO
[3:0]	RW	0x6	VBI1_FORMAT_TYPE	Specifies basic VBI decoding model. Find the standard format which most closely matches the intended format, and program this field to match the type field encoding specified in the VBI_LINE_CTRLx registers. Special operating modes are enabled based on the format type as described below: 0000 = RESERVED 0101, 1010, 0011 = Teletext – enable packet address filter 0011 = Enable Moji style byte alignment – first six bits go into separate byte packet. 525-line modes only. 0100 = Wide-screen signaling – assume signal includes single sync pulse, and no frame code. 525-line mode only. 0100 = Wide-screen signaling – implement WSS625 style biphase decoding. 625-line mode only. 0101 = VITC – assume sync pulses every 8 bits 0110, 0111, 1000 = Closed caption – assume 50 IRE signal amplitude 1001 = VPS – implement VPS style biphase decoding

VBI Custom 2 Horizontal Delay **Address 0x458**

Bits	Type	Default	Name	Description
[7:0]	RW	0x77	VBI2_HDELAY	Delay from internal hreset signal to start of clock run-in in number pixel clock cycles. VBI2_HDELAY = (hdelay(uS) x pixel_rate (MHz)) - 13

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VBI Custom 2 Bit Increment **Address 0x459**

Bits	Type	Default	Name	Description
[7:0]	RW	0x88	VBI2_BITINC_LOW	Least significant byte of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase encoding modes, this sample rate should be set to six times the effective bit rate. VBI2_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

VBI Custom 2 Slice Distance **Address 0x45A**

Bits	Type	Default	Name	Description
[7:4]	RW	0x0	VBI2_SLICE_DIST	Slice level sample distance. Controls how often samples are taken for the adaptive slice level routine. Distance is defined in terms of 1/8 or a bit period time, where the bit period is defined by BITINC. The parameter describes the number of points where samples are NOT taken. Therefore, to take one sample every four points, put three in this field.
[3:0]	RW	0x0	VBI2_BITINC_HIGH	Most significant nibble of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase encoding modes, this sample rate should be set to six times the effective bit rate. VBI2_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

VBI Custom 2 Clock Run-In Window **Address 0x45B**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6:0]	RW	0x54	VBI2_CRWIN	Specifies the time window during which edge detection (positive and negative) is inhibited. This window is based on the clock run-in frequency. Avoids spurious edges from being detected. VBI2_CRWIN = 4 x pixel_rate x clock_runin_half_period x wr; Where wr = window ratio, portion of cycle to inhibit detection

VBI Custom 2 Frame Code Low **Address 0x45C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI2_FRAME_CODE_LOW	Least significant byte of start code bit pattern in transmission order

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VBI Custom 2 Frame Code Mid **Address 0x45D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI2_FRAME_CODE_MID	Middle byte of start code bit pattern in transmission order

VBI Custom 2 Frame Code High **Address 0x45E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI2_FRAME_CODE_HIGH	Most significant byte of start code bit pattern in transmission order

VBI Custom 2 Frame Code Length **Address 0x45F**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4:0]	RW	0x00	VBI2_FC_LENGTH	Number of start bits (or frame code bits)

VBI Custom 2 Clock Run-in Period **Address 0x460**

Bits	Type	Default	Name	Description
[7:0]	RW	0x02	VBI2_CRI_TIME	Expected time period of clock run-in period in terms of halves of the bit period specified in VBI2_BITINC. The algorithm detects the number of edges specified in VBI2_CRI_LENGTH and compares the elapsed time with this parameter. If the result is within VBI2_CRI_MARGIN of this parameter, then the waveform is decoded.

VBI Custom 2 Clock Run-in Margin and Length **Address 0x461**

Bits	Type	Default	Name	Description
[7:4]	RW	0x4	VBI2_CRI_LENGTH	Number of clock run-in edges expected in the CRI period. This does not include the edge that transitions into the frame start code, and this is an N-1 parameter. For example, in a Teletext waveform with 16 bit periods and 16 edges, program 0xF in this register. For closed caption with 6.5 bit periods, but 13 edges, program 0xC
[3:0]	RW	0x4	VBI2_CRI_MARGIN	This field specifies the margin around VBI1_CRI_TIME in which the measured time of the clock run-in period can fall. See VBI1_CRI_TIME. This is in units of eights of the bit period defined by VBI1_BITINC.

VBI Custom 2 Payload Length **Address 0x462**

Bits	Type	Default	Name	Description
[7:0]	RW	0x0A	VBI2_PAYLD_LENGTH	Number of data bits to be captured, divided by two. If N is the number of bits in the payload, program this register with N/2.

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VBI Custom 2 Miscellaneous **Address 0x463**

Bits	Type	Default	Name	Description
[7]	RW	0	VBI2_HAM_EN	Enable hamming comparison for framing comparison when this bit is set. When set VBI2_FRAME_CODE[3:0] are used for hamming comparison.
[6:4]	RW	010	VBI2_FIFO_MODE	Determines which payload FIFO is loaded. 000 = Don't load to payload FIFO 001 = Load to Gemstar 1x FIFO 010 = Load to CC FIFO 011 = Load to WSS FIFO 100 = Load to Gemstar 2x FIFO
[3:0]	RW	0x6	VBI2_FORMAT_TYPE	Specifies basic VBI decoding model. Find the standard format which most closely matches the intended format, and program this field to match the type field encoding specified in the VBI_LINE_CTRLx registers. Special operating modes are enabled based on the format type as described below: 0000 = RESERVED 0101, 1010, 0011 = Teletext – enable packet address filter 0011 = Enable Moji style byte alignment – first six bits go into separate byte packet. 525-line modes only. 0100 = Wide-screen signaling – assume signal includes single sync pulse, and no frame code. 525-line mode only. 0100 = Wide-screen signaling – implement WSS625 style biphase decoding. 625-line mode only. 0101 = VITC – assume sync pulses every 8 bits 0110, 0111, 1000 = Closed caption – assume 50 IRE signal amplitude 1001 = VPS – implement VPS style biphase decoding

VBI Custom 3 Horizontal Delay **Address 0x464**

Bits	Type	Default	Name	Description
[7:0]	RW	0x6E	VBI3_HDELAY	Delay from internal hreset signal to start of clock run-in in number pixel clock cycles. VBI3_HDELAY = (hdelay(uS) x pixel_rate (MHz)) - 13

VBI Custom 3 Bit Increment **Address 0x465**

Bits	Type	Default	Name	Description
[7:0]	RW	0xCA	VBI3_BITINC_LOW	Least significant byte of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase endcoding modes, this sample rate should be set to six times the effective bit rate. VBI3_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

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VBI Custom 3 Slice Distance **Address 0x466**

Bits	Type	Default	Name	Description
[7:4]	RW	0x3	VBI3_SLICE_DIST	Slice level sample distance. Controls how often samples are taken for the adaptive slice level routine. Distance is defined in terms of 1/8 or a bit period time, where the bit period is defined by BITINC. The parameter describes the number of points where samples are NOT taken. Therefore, to take one sample every four points, put three in this field.
[3:0]	RW	0x6	VBI3_BITINC_HIGH	Most significant nibble of the value used to increment a 14-bit counter that measures the bit sample rate. A bit is sampled when the 14-bit counter rolls over. The bit sample rate defines the rate at which the waveform is sampled during the payload. For biphase endcoding modes, this sample rate should be set to six times the effective bit rate. VBI3_BITINC = 2^{14} / ((4 x pixel_rate) / bit_sample_rate)

VBI Custom 3 Clock Run-in Window **Address 0x467**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6:0]	RW	0x06	VBI3_CRWIN	Specifies the time window during which edge detection (positive and negative) is inhibited. This window is based on the clock run-in frequency. Avoids spurious edges from being detected. VBI3_CRWIN = 4 x pixel_rate x clock_runin_half_period x wr; Where wr = window ratio, portion of cycle to inhibit detection

VBI Custom 3 Frame Code Low **Address 0x468**

Bits	Type	Default	Name	Description
[7:0]	RW	0xE7	VBI3_FRAME_CODE_LOW	Least significant byte of start code bit pattern in transmission order

VBI Custom 3 Frame Code Mid **Address 0x469**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI3_FRAME_CODE_MID	Middle byte of start code bit pattern in transmission order

VBI Custom 3 Frame Code High **Address 0x46A**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	VBI3_FRAME_CODE_HIGH	Most significant byte of start code bit pattern in transmission order

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VBI Custom 3 Frame Code Length **Address 0x46B**

Bits	Type	Default	Name	Description
[7:5]	RZ	000	RESERVED	
[4:0]	RW	0x08	VBI3_FC_LENGTH	Number of start bits (or frame code bits)

VBI Custom 3 Clock Run-in Period **Address 0x46C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x20	VBI3_CRI_TIME	Expected time period of clock run-in period in terms of halves of the bit period specified in VBI3_BITINC. The algorithm detects the number of edges specified in VBI3_CRI_LENGTH and compares the elapsed time with this parameter. If the result is within VBI3_CRI_MARGIN of this parameter, then the waveform is decoded.

VBI Custom 3 Clock Run-in Margin and Length **Address 0x46D**

Bits	Type	Default	Name	Description
[7:4]	RW	0xF	VBI3_CRI_LENGTH	Number of clock run-in edges expected in the CRI period. This does not include the edge that transitions into the frame start code, and this is an N-1 parameter. For example, in a Teletext waveform with 16 bit periods and 16 edges, program 0xF in this register. For closed caption with 6.5 bit periods, but 13 edges, program 0xC
[3:0]	RW	0x6	VBI3_CRI_MARGIN	This field specifies the margin around VBI3_CRI_TIME in which the measured time of the clock run-in period can fall. See VBI3_CRI_TIME. This is in units of eights of the bit period defined by VBI1_BITINC.

VBI Custom 3 Payload Length **Address 0x46E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x84	VBI3_PAYLD_LENGTH	Number of data bits to be captured, divided by two. If N is the number of bits in the payload, program this register with N/2.

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VBI Custom 3 Miscellaneous **Address 0x46F**

Bits	Type	Default	Name	Description
[7]	RW	0	VBI3_HAM_EN	Enable hamming comparison for framing comparison when this bit is set. When set VBI3_FRAME_CODE[3:0] are used for hamming comparison.
[6:4]	RW	000	VBI3_FIFO_MODE	Determines which payload FIFO is loaded. 000 = Don't load to payload FIFO 001 = Load to Gemstar 1x FIFO 010 = Load to CC FIFO 011 = Load to WSS FIFO 100 = Load to Gemstar 2x FIFO
[3:0]	RW	0x2	VBI3_FORMAT_TYPE	Specifies basic VBI decoding model. Find the standard format which most closely matches the intended format, and program this field to match the type field encoding specified in the VBI_LINE_CTRLx registers. Special operating modes are enabled based on the format type as described below: 0000 = RESERVED 0101, 1010, 0011 = Teletext – enable packet address filter 0011 = Enable Moji style byte alignment – first six bits go into separate byte packet. 525-line modes only. 0100 = Wide-screen signaling – assume signal includes single sync pulse, and no frame code. 525-line mode only. 0100 = Wide-screen signaling – implement WSS625 style biphase decoding. 625-line mode only. 0101 = VITC – assume sync pulses every 8 bits 0110, 0111, 1000 = Closed caption – assume 50 IRE signal amplitude 1001 = VPS – implement VPS style biphase decoding

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5.6.3 Autoconfiguration Parameters

The user can write the following registers, or allow them to be set automatically based on either the specified or detected video format. The user can also let the hardware configure these registers based on the video format, and overwrite selected parameters to customize the mode.

If the ACFG_DIS bit (MODE_CTRL) is left cleared, the hardware will set these registers when either of the following happens.

- The user specifies a specific mode by writing the VID_FMT_SEL (MODE_CTRL) field.
- The user specifies the auto-detect mode in the VID_FMT_SEL (MOD_CTRL) field, and the auto-detect hardware detects a mode change.

When the ACFG_DIS bit is set, the hardware will never modify the values written by the programmer to these registers.

Horizontal Blanking Delay Low **Address 0x470**

Bits	Type	Default	Name	Description
[7:0]	RW	0x7A	HBLANK_CNT_LOW	Lower 8-bits of horizontal blanking delay. It is number of pixels between the leading edge of hsync and the start of active video.

Horizontal Blanking Delay High **Address 0x471**

Bits	Type	Default	Name	Description
[7:4]	RW	0000	HACTIVE_CNT_LOW	Lower nibble of horizontal active region duration. It is the number of scaled pixels in the horizontal active and horizontal blanking region of the line.
[3:2]	RZ	00	RESERVED	
[1:0]	RW	00	HBLANK_CNT_HIGH	Upper six bits of horizontal active region. It is number of scaled pixels in the horizontal active and horizontal blanking region of the line.

Horizontal Active High **Address 0x472**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x2D	HACTIVE_CNT_HIGH	Upper 6 bits of horizontal active region. It is number of pixels in the active region of the line.

Burst Gate Delay **Address 0x473**

Bits	Type	Default	Name	Description
[7:0]	RW	0x5A	BGDEL_CNT	Burst gate delay. This value is used to generate the window during which the color burst is sampled. It is the delay, in pixel clocks, between the leading edge of hsync and the center of the 4-pixel wide burst accumulate window.

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Vertical Blanking Delay Low **Address 0x474**

Bits	Type	Default	Name	Description
[7:0]	RW	0x14	VBLANK_CNT_LOW	Lower 8-bits of vertical blanking delay.

Vertical Blanking Delay High **Address 0x475**

Bits	Type	Default	Name	Description
[7:4]	RW	0111	VACTIVE_CNT_LOW	Lower nibble of vertical active region duration. It is the number of half lines in the vertical active region. This register is only valid when the reg override bit is set.
[3:2]	RZ	00	RESERVED	
[1:0]	RW	00	VBLANK_CNT_HIGH	Upper two bits of vertical blanking delay.

Vertical Active High **Address 0x476**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x1E	VACTIVE_CNT_HIGH	Upper six bits of vertical active duration. It is number of half lines in the vertical active region. This register is only valid when the reg override bit is set.

Vertical Blanking Delay **Address 0x477**

Bits	Type	Default	Name	Description
[7:0]	RW	0x20	V656BLANK_CNT	Vertical blanking for 656 output. Determines the timing of the internal v656blank signal. It allows us to control the v-bit transition in the 656 output independently of the vblank signal seen by the rest of the chip. The counter starts 12 half-lines before the expected trailing edge of vreset. Thus it must = vblank_cnt + 0x04 to have vbank and v656blank line up.

SRC Decimation Ratio Low **Address 0x478**

Bits	Type	Default	Name	Description
[7:0]	RW	0x1F	SRC_DECIM_RATIO_LOW	Lower byte of sample rate converter decimation ratio. Default phase increment: SRC_DECIM_RATIO = 256 x Fin/Fpix Where Fin = ADC sampling frequency, Fpix = pixel rate (should be consistent with square_pixel setting).

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SRC Decimation Ratio High **Address 0x479**

Bits	Type	Default	Name	Description
[7:2]	RZ	000000	RESERVED	
[1:0]	RW	0x2	SRC_DECIM_RATIO_HIGH	Two most significant bits of sample rate converter decimation ratio. Default phase increment: SRC_DECIM_RATIO = 256 x Fin/Fpix Where Fin = ADC sampling frequency, Fpix = pixel rate (should be consistent with square_pixel setting).

Comb Filter Bandwidth Select **Address 0x47A**

Bits	Type	Default	Name	Description
[7:6]	RW	01	LUMA_LPF_SEL	Selects luma low-pass filter bandwidth: 00 = low (~600 kHz) 01 = medium (~1 MHz) 10 = high (~1.5 MHz) 11 = RESERVED
[5:4]	RW	01	UV_LPF_SEL	Selects U/V low-pass filter bandwidth: 00 = low (~600 kHz) 01 = medium (~1 MHz) 10 = high (~1.5 MHz) 11 = RESERVED
[3:0]	RZ	0x0	RESERVED	

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Comb Filter Enable **Address 0x47B**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RW	1	CCOMB_3LN_EN	Enables the adaptation algorithm to choose the 3-line chroma comb. 0 = Disable 1 = Enable
[5]	RW	1	CCOMB_2LN_EN	Enables the adaptation algorithm to choose the 2-line chroma comb. 0 = Disable 1 = Enable
[4]	RW	0	RESERVED	
[3]	RZ	0	RESERVED	
[2]	RW	1	LCOMB_3LN_EN	Enables the adaptation algorithm to choose the 3-line luma comb. 0 = Disable 1 = Enable
[1]	RW	1	LCOMB_2LN_EN	Enables the adaptation algorithm to choose the 2-line luma comb. 0 = Disable 1 = Enable
[0]	RW	0	RESERVED	

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Subcarrier Step Size Low **Address 0x47C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x1F	SC_STEP_LOW	Lower byte of the chroma subcarrier DTO step size value. Chroma subcarrier DTO step size, $F_{sc}/F_{pix} \times 2_{21}$ where F_{sc} = subcarrier frequency, and F_{pix} = pixel rate. However, the pixel rate used in this calculation should be based on the exact pixel rate that is defined in the src_decim_ration field of the SRC_COMB_CFG register above: $F_{pix} = 256/src\_decim\_ration \times F_{in}$. Note: This does not imply that the effective pixel rate is only as accurate as this equation. This equation just determines the initial pixel rate, which will then be fine-tuned to achieve the exact ratio. However, the initial subcarrier frequency must be based on the initial pixel rate.

Subcarrier Step Size Mid **Address 0x47D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x7C	SC_STEP_MID	Middle byte of the chroma subcarrier DTO step size value. Chroma subcarrier DTO step size, $F_{sc}/F_{pix} \times 2_{21}$ where F_{sc} = subcarrier frequency, and F_{pix} = pixel rate. However, the pixel rate used in this calculation should be based on the exact pixel rate that is defined in the src_decim_ration field of the SRC_COMB_CFG register above: $F_{pix} = 256/src\_decim\_ration \times F_{in}$. Note: This does not imply that the effective pixel rate is only as accurate as this equation. This equation just determines the initial pixel rate, which will then be fine-tuned to achieve the exact ratio. However, the initial subcarrier frequency must be based on the initial pixel rate.

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Subcarrier Step Size High **Address 0x47E**

Bits	Type	Default	Name	Description
[7:4]	RZ	0x0	RESERVED	
[3:0]	RW	0x8	SC_STEP_HIGH	Upper nibble of the chroma subcarrier DTO step size value. Chroma subcarrier DTO step size, $F_{sc}/F_{pix} \times 2_{21}$ where F_{sc} = subcarrier frequency, and F_{pix} = pixel rate. However, the pixel rate used in this calculation should be based on the exact pixel rate that is defined in the src_decim_ration field of the SRC_COMB_CFG register above: $F_{pix} = 256/src\_decim\_ration \times F_{in}$. Note: This does not imply that the effective pixel rate is only as accurate as this equation. This equation just determines the initial pixel rate, which will then be fine-tuned to achieve the exact ratio. However, the initial subcarrier frequency must be based on the initial pixel rate.

VBI Offset **Address 0x47F**

Bits	Type	Default	Name	Description
[7:5]	RZ	0x0	RESERVED	
[4:0]	RW	0x00	VBI_OFFSET	The offset in lines from vreset to enable the VBI Slicer to capture data.

Field Count Low **Address 0x480**

Bits	Type	Default	Name	Description
[7:0]	RW,PW	0x00	FIELD_COUNT_LOW	Lower byte of the count value. Counts fields continuously, and wraps around when it reaches the max count of 0x3FF. It is reset to 0 by writing to either byte.

Field Count High **Address 0x481**

Bits	Type	Default	Name	Description
[1:0]	RW,PW	00	FIELD_COUNT_HIGH	Upper two bits of the count value. Counts fields continuously, and wraps around when it reaches the max count of 0x3FF. It is reset to 0 by writing to either byte.

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5.6.4 Diagnostic Registers

Registers addresses, 0x484 to 0x4AF, are intended for engineering diagnostics and performance fine-tuning only. In general, it is not intended that the user should need to access these registers.

Temporal Decimation **Address 0x484**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x00	TEMPDEC	This signal is the control for the temporal decimation logic. This value is the number of fields or frames to discard out of 50 (625/50) or 60 (525/60). This value should not exceed 60 for a 60 Hz system or 50 for a 50 Hz system.

Miscellaneous Timing Control **Address 0x485**

Bits	Type	Default	Name	Description
[7]	RW	0	VPRES_VERT_EN	Enable for the vertical portion of the video present logic. 1 = VPRES status bit reflects when the video is both locked vertically and horizontally. 0 = VPRES reflects the horizontal locking only.
[6:4]	RZ	000	RESERVED	
[3]	RW	0	HR32	This bit controls the width of the HRESET output. 0 = HRESET is 64 clocks wide 1 = HRESET is 32 clocks wide
[2]	RW	0	TDALGN	Aligns start of decimation with even or odd field. 0 = Start on odd field 1 = Start on even field
[1]	RW	0	TDFIELD	This signal is an indication of whether the temporal decimation is done on a frame (0) or field (1) basis.
[0]	RZ	00	RESERVED	

0x486—Test Register (DEFAULT 0x00)

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Video Detect Configuration **Address 0x487**

Bits	Type	Default	Name	Description
[7:6]	RW	01	DEBOUNCE_COUNT	Number of consecutive fields of detected video format stability required before switching video formats. This period is provided to help prevent erroneous switching due to noise or other short- term errors. 00 = 2 consecutive fields of stability 01 = 4 consecutive fields of stability 10 = 8 consecutive fields of stability 11 = 16 consecutive fields of stability
[5:4]	RW	00	VT_LINE_CNT_HYST	Number of consecutive fields with approximately 525/2 or 625/2 lines before changing the detected line count. 00 = 2 consecutive fields with approximately 525/2 or 625/2 lines 01 = 4 consecutive fields with approximately 525/2 or 625/2 lines 10 = 8 consecutive fields with approximately 525/2 or 625/2 lines 11 = 16 consecutive fields with approximately 525/2 or 625/2 lines
[3:0]	RZ	0	RESERVED	

VGA Gain Control **Address 0x488**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x20	VGA_GAIN	R/W register for VGA gain (can be written when vga_auto_en = 0)

AGC Gain Control Low **Address 0x489**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	AGC_GAIN_LOW	Lower byte of the 12 bit value for AGC digital gain (can be written when agc_auto_en = 0)

AGC Gain Control High **Address 0x48A**

Bits	Type	Default	Name	Description
[7:4]	RZ	0x0	RESERVED	
[3:0]	RW	0x1	AGC_GAIN_HIGH	Upper nibble of the 12 bit value for AGC digital gain (can be written when agc_auto_en = 0)

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Digital Front-End Control **Address 0x48B**

Bits	Type	Default	Name	Description
[7]	RW	1	CLAMP_AUTO_EN	Analog clamp setting is tied to VGA gain
[6]	RW	1	AGC_AUTO_EN	AGC enable 0 = freeze/manual 1 = auto mode
[5]	RW	1	VGA_CRUSH_EN	ADC overflow protection enable (decreases VGA_SYNC if ADC overflows)
[4]	RW	1	VGA_AUTO_EN	VGA enable 0 = freeze/manual 1 = auto mode
[3]	RW	1	VBI_GATE_EN	Enable gating of back porch updates during vertical blanking interval.
[2:0]	RW	000	CLAMP_LEVEL	Analog clamp setting (if CLAMP_AUTO_EN = 0)

VGA Sync Control **Address 0x48C**

Bits	Type	Default	Name	Description
[7:0]	RW	0xDC	VGA_SYNC	Sync pulse height out of ADC

VGA Track Range **Address 0x48D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x40	VGA_TRACK_RANGE	Minimum error of sync height before losing VGA lock

VGA Acquire Range **Address 0x48E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x10	VGA_ACQUIRE_RANGE	Maximum error of sync height before declaring VGA lock.

DFE Control **Address 0x490**

Bits	Type	Default	Name	Description
[7:6]	RW	10	SYNC_LOOP_GAIN	Sync level detect control loop gain = $2^n/4$
[5:4]	RZ	00	RESERVED	
[3:2]	RW	10	AGC_LOOP_GAIN	AGC control loop gain = $2^n/4$
[1:0]	RW	10	DCC_LOOP_GAIN	Backporch clamp control loop gain = $2^n/4$

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Backporch Loop Gain **Address 0x491**

Bits	Type	Default	Name	Description
[5:2]	RZ	0000	RESERVED	
[1:0]	RW	10	BP_LOOP_GAIN	Backporch level detect control loop gain = $2^n/4$

DFT Threshold **Address 0x492**

Bits	Type	Default	Name	Description
[7:0]	RW	0x3F	DFT_THRESHOLD	Correlator threshold for SC detect (threshold = 256 x setting).

Backporch Percent **Address 0x493**

Bits	Type	Default	Name	Description
[7:0]	RW	0xCD	BP_PERCENT	Percent of line expected to be used above or equal to backporch threshold. Used in sync slicing algorithm for initial sync location.

PLL Offset Low **Address 0x494**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	PLL_MAX_OFFSET_LOW	Least significant byte of video PLL maximum adjustment offset = 2^9 x PLL_MAX_OFFSET

PLL Offset High **Address 0x495**

Bits	Type	Default	Name	Description
[7:0]	RW	0x03	PLL_MAX_OFFSET_HIGH	Most significant byte of video PLL maximum adjustment offset = 2^9 x PLL_MAX_OFFSET

PLL Indirect Loop Gain **Address 0x496**

Bits	Type	Default	Name	Description
[7:0]	RW	0x1F	PLL_KI	PLL control loop indirect gain = $1/2^{(n+11)}$

PLL Direct Loop Gain **Address 0x497**

Bits	Type	Default	Name	Description
[7:0]	RW	0x16	PLL_KD	PLL control loop indirect gain = $1/2^n$

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Horizontal Tracking Loop Indirect Gain **Address 0x498**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:4]	RW	10	HTL_KD	Horizontal tracking loop indirect gain = $1/2^n$
[3:2]	RZ	00	RESERVED	
[1:0]	RW	10	HTL_KI	Horizontal tracking loop indirect gain = $1/2^n$

Luma Comb Error Limit Max **Address 0x49C**

Bits	Type	Default	Name	Description
[7:0]	RW	0x14	LCOMB_ERR_LIMIT	Maximum comb error before falling back to complementary filter mode.

Luma Comb Threshold **Address 0x49D**

Bits	Type	Default	Name	Description
[7:0]	RW	0x00	LUMA_THRESHOLD	Minimum chroma amplitude before using luma comb filter.

Chroma Comb Error Limit Max **Address 0x49E**

Bits	Type	Default	Name	Description
[7:0]	RW	0x50	CCOMB_ERR_LIMIT	Maximum comb error before falling back to notch filter mode.

Luma Comb Error Limit Max **Address 0x49F**

Bits	Type	Default	Name	Description
[7:0]	RW	0x20	COMB_PHASE_LIMIT	Comb filter is enabled when the burst phase difference between adjacent lines is measured to be less than this limit. The phase difference is measured by taking the burst phase of the current line and subtracting it from the phase of a vertically aligned burst sample points in the previous lines, allowing for the expected phase shift. Lack of alignment shows that there is too much horizontal jitter to enable comb filter.

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White Crush Increment **Address 0x4A0**

Bits	Type	Default	Name	Description
[7:6]	RZ	00	RESERVED	
[5:0]	RW	0x0F	SYNC_TIP_INC	White crush increment value. This value is the step amount that the sync height can be increased by the white crush logic on any single adjustment.

White Crush Decrement **Address 0x4A1**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6:1]	RW	000000	SYNC_TIP_REDUCE	White crush decrement value. This value is the step amount that the sync height can be decreased by the white crush logic on any single adjustment.
[0]	RZ	0	RESERVED	

White Crush Comparison Point **Address 0x4A2**

Bits	Type	Default	Name	Description
[7]	RZ	0	RESERVED	
[6]	RW	0	WTW_EN	Active-high enable for the white crush whiter-than-white peak threshold. 0 = 100 IRE peak threshold 1 = 110 IRD peak threshold
[5]	RW	0	CRUSH_FREQ	White crush adjust frequency. This bit is used to determine whether to perform the white crush adjustments on a field or frame basis. 0 = field rate 1 = frame rate
[4]	RW	0	MAJ_SEL_EN	Enables adaptive majority select logic
[3:2]	RW	11	MAJ_SEL	White crush majority comparison point select bits. This value is the intensity threshold that the white crush logic compares each pixel to in order to determine if the majority of the image is too dark. 00 = ¾ maximum luma 01 = ½ maximum luma 10 = ¼ maximum luma 11 = Automatic
[1:0]	RZ	00	RESERVED	

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5.6.5 Soft Reset Control

The soft reset control register allows the reset of the video decoder for diagnostic or recovery purposes. Each module can be reset individually through use of the mask bits. When set to one, a mask bit will disable the reset of the particular module. Therefore, by masking all modules except one, only one module is reset. The default is that the master reset, VD_SOFT_RST, resets the whole video decoder core.

Writes to this register are broken up into bytes; therefore, the reset behavior will depend on the byte order. For example, if several mask bits are set along with the VD_SOFT_RST bit, and the programmer wants to clear both mask bits and the reset at the same time, writing byte 0x4A4 will clear the mask bits in the lower byte before the reset is cleared. The result will be that for a brief time the reset will be asserted, but not masked, to some modules. In general, the order to follow is:

1. Write mask bits
2. Set VD_SOFT_RST bit to assert reset
3. Clear VD_SOFT_RST bit
4. Make any changes to mask bits for the next soft reset assertion

Soft Reset Mask 1 **Address 0x4A4**

Bits	Type	Default	Name	Description
[7]	RW	0	VBI_RST_MSK	Masks soft reset for the VBI slicer module
[6]	RW	0	SCALE_RST_MSK	Masks soft reset for the Scaling module
[5]	RW	0	CHROMA_RST_MSK	Masks soft reset for the Chroma Datapath module
[4]	RW	0	LUMA_RST_MSK	Masks soft reset for the Luma Datapath module
[3]	RW	0	VTG_RST_MSK	Masks soft reset for the Video Timing Generator module
[2]	RW	0	YCSEP_RST_MSK	Masks soft reset for the Y/C separation module
[1]	RW	0	SRC_RST_MSK	Masks soft reset for the Sample Rate Converter module
[0]	RW	0	DFE_RST_MSK	Masks soft reset for the Digital Front End module

Soft Reset Mask 2 **Address 0x4A5**

Bits	Type	Default	Name	Description
[7]	RW	0	VD_SOFT_RST	Video decoder soft reset. Resets video decoder core per the mask bits for each module.
[6:3]	RW	0000	RESERVED	
[2]	RW	0	REG_RST_MSK	Masks soft reset for the Register module
[1]	RW	0	VOF_RST_MSK	Masks soft reset for the Video Output Formatter module
[0]	RW	0	MVDET_RST_MSK	Masks soft reset for the Macrovision Detect module

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Version ID **Address 0x4B4**

Bits	Type	Default	Name	Description
[7:0]	RO	0x02	REV_ID	Revision ID. The initial value is set to 0x01. This refers to the revision of the video decoder core only, and should not be confused with the chip-level revision ID.

Miscellaneous Diagnostic Control **Address 0x4B8**

Bits	Type	Default	Name	Description
[0]	RW	10	APL_DETECT_ENA	Enables detection of video pattern with one white line surrounded by black lines. The adaptive tallithim does not handle this situation well, without enabling this detection. 0 = This special case is not detected. The white line will be combed with the black line, reducing the luminance of the white line. 1 = Forces the Y/C separation algorithm into notch mode upon detecting white lines surrounded by black.

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5.7 Auto Configuration Defaults

Tables 5-4and 5-5 show how a subset of registers should be configured based on the video format and pixel rate. If the VID_FMT_SEL field is set to auto mode, autoconfig logic will set the registers to the specified values according to the SQ_PIXEL bit and detected video format from the Video Timing Generation module. If not set to auto mode, the autoconfig logic will set the register to the specified values according to the SQ_PIXEL bit and VID_FMT_SEL field whenever a write access is done to that byte of the MODE_CTRL register. If the ACFG_DIS bit is set, autoconfig will be disabled altogether.

Table 5-4. Autoconfig Values for BT.656 Pixel Timing

	NTSC-4.43	NTSC-J	NTSC-M	PAL-BDGHI	PAL-N	PAL-NC	SECAM	PAL-60	PAL-M	SECAM-60
vblank[9:0]	10'h014	10'h014	10'h014	10'h022	10'h022	10'h022	10'h022	10'h014	10'h014	10'h014
v656blank[7:0]	8'h20	8'h20	8'h20	8'h2E	8'h2E	8'h2E	8'h2E	8'h20	8'h20	8'h20
vactive[9:0]	10'h1E7	10'h1E7	10'h1E7	10'h240	10'h240	10'h240	10'h240	10'h1E7	10'h1E7	10'h1E7
hblank[9:0]	10'h07A	10'h07A	10'h07A	10'h084	10'h084	10'h084	10'h084	10'h07A	10'h07A	10'h07A
hactive[9:0]	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0	10'h2D0
bgdel[7:0]	8'h5A	8'h5A	8'h5A	8'h5B	8'h5B	8'h5B	8'h5B	8'h5F	8'h5F	8'h5F
bpf_sel[1:0]	2'b01	2'b00	2'b00	2'b01	2'b01	2'b00	2'b11	2'b01	2'b00	2'b11
comb_err_limit[7:0]	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50
src_decim_ratio[9:0]	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F	10'h11F
sc_step[19:0]	20'h9E8A6	20'h80000	20'h80000	20'h9E8A6	20'h9E8A6	20'h8016F	20'h9AC4A	20'h9E8A6	20'h80000	20'h9AC4A
vbi_voffset[4:0]	5'h0A	5'h0A	5'h0A	5'h06	5'h06	5'h06	5'h06	5'h0A	5'h0A	5'h0A

GENERAL NOTE: Gray columns indicate 625-line standards.

Table 5-5. Autoconfiguration Values for Square Pixel Timing

	NTSC-4.43	NTSC-J	NTSC-M	PAL-BDGHI	PAL-N	PAL-NC	SECAM	PAL-60	PAL-M	SECAM-60
vblank[9:0]	10'h016	10'h016	10'h016	10'h022	10'h01A	10'h022	10'h022	10'h016	10'h016	10'h016
v656blank[7:0]	8'h22	8'h22	8'h22	8'h2E	8'h26	8'h2E	8'h2E	8'h22	8'h22	8'h22
vactive[9:0]	10'h1E0	10'h1E0	10'h1E0	10'h240	10'h240	10'h240	10'h240	10'h1E0	10'h1E0	10'h1E0
hblank[9:0]	10'h078	10'h078	10'h078	10'h09B	10'h08E	10'h09B	10'h09B	10'h078	10'h078	10'h078
hactive[9:0]	10'h280	10'h280	10'h280	10'h300	10'h300	10'h300	10'h300	10'h280	10'h280	10'h280
bgdel[7:0]	8'h51	8'h51	8'h51	8'h63	8'h63	8'h63	8'h63	8'h57	8'h57	8'h57
bpf_sel[1:0]	2'b01	2'b00	2'b00	2'b01	2'b01	2'b00	2'b11	2'b01	2'b00	2'b11
comb_err_limit[7:0]	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50	8'h50
src_decim_ratio[9:0]	10'h155	10'h155	10'h155	10'h0F1	10'h0F1	10'h0F1	10'h0F1	10'h155	10'h155	10'h155
sc_step[19:0]	20'h9E8A6	20'h80000	20'h80000	20'h9E8A6	20'h9E8A6	20'h8016F	20'h9AC4A	20'h9E8A6	20'h80000	20'h9AC4A
vbi_voffset[4:0]	5'h0A	5'h0A	5'h0A	5'h06	5'h06	5'h06	5'h06	5'h0A	5'h0A	5'h0A

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6 Electrical/Mechanical

6.1 DC Electrical Parameters

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to VSS)	—	—	—	4.6	V
VDDO (measured to VSSO)	—	—	—	4.6	V
VDD (measured to VSS)	—	—	—	1.7	V
Voltage on any signal pin (see note below)	—	VSSO – 0.5	—	VDDO + 0.5	V
Analog Input Voltage	—	–1.0	—	4.6	V
Storage Temperature	Ts	–65		+150	ºC
Junction Temperature	Tj	—	—	+125	ºC
Peak Reflow Temperature	Tvsol	—	—	260	ºC

GENERAL NOTES:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V, or drops below ground by more than 0.5 V can induce destructive latchup.

Table 6-2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Analog Power Supply	VAA	3.135	3.3	3.465	V
Digital Core Power Supply	VDD	1.140	1.2	1.31	V
Digital I/O Power Supply	VDDO	3.135	3.3	3.465	V
Analog Input CVBS or Luma Amplitude Range (AC coupling required)	Yin	0.5	1.0	2.0	Vp-p
Analog Input Chroma Amplitude Range (AC coupling required)	Cin	0.5	1.0	2.0	Vp-p
Sound IF Audio Amplitude Range (AC coupling required)	SIFin	0.1	1.0	2.0	Vp-p
Ambient Operating Temperature	Ta	0	—	70	ºC

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Table 6-3. Signal Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0	—	VDDO + 0.5	V
Input Low Voltage	VIL	–0.5	—	0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (1 MHz, 2.4 V)	Ci		7		pF
Crystal Inputs (XTI, XTO)					
Input Low Voltage	VIL	–0.5	—	0.4	V
Input High Voltage	VIH	2.4	—	VDDO + 0.5	V
Digital Outputs					
Output Voltage High (IOH = -400 µA)	VOH	2.4	—	VDDO	V
Output Voltage Low (IOL = 4 mA)	VOL	0.0	—	0.4	V
Three-State Current	IOZ	—	—	10	µA
Analog Input Capacitance	Ca		5		pF

6.2 AC Electrical Parameters

Table 6-4. Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
XTI / XTO					
Crystal Cycle Time	1	34.919	34.921	34.922	ns
High Time	2		17.460		ns
Low Time	3		17.460		ns
ITU-R BT.656 Operation					
PIXCLK Frequency	4	—	27.0	—	MHz
NTSC Square Pixel Operation					
PIXCLK Frequency	4	—	24.54	—	MHz
PAL/SECAM Square Pixel Operation					
PIXCLK Frequency	4	—	29.50	—	MHz
PIXCLK Duty Cycle	5	45	—	55	%
PIXCLK to Data Delay (see note 1)	6	—	—	5	ns
VIPCLK Input Frequency	7	25	—	33	MHz
PLL_CLK Frequency		8.192		54	MHz
PLL_CLK Duty Cycle		45		55	%

GENERAL NOTE: Data delay value is measured relative to the rising edge of PIXCLK but note that PIXCLK can be inverted for systems requiring data to output relative to the falling edge of PIXCLK.

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Table 6-5. Control Signal Timing

Parameter	Symbol	Min	Typ	Max	Units
VIP Host Port					
Data to VIPCLK Setup	8	5	—	—	ns
Data to VIPCLK Hold	9	0	—	—	ns
Video Timing/Indicator (VRESET, HRESET, FIELD, DVALID, ACTIVE, CBFLAG)					
PIXCLK to Timing/Indicator Delay	10	0	0.5	2	ns
RESET_N Low Time		350	—	—	µs

Figure 6-1. Video Interface Timing Diagrams

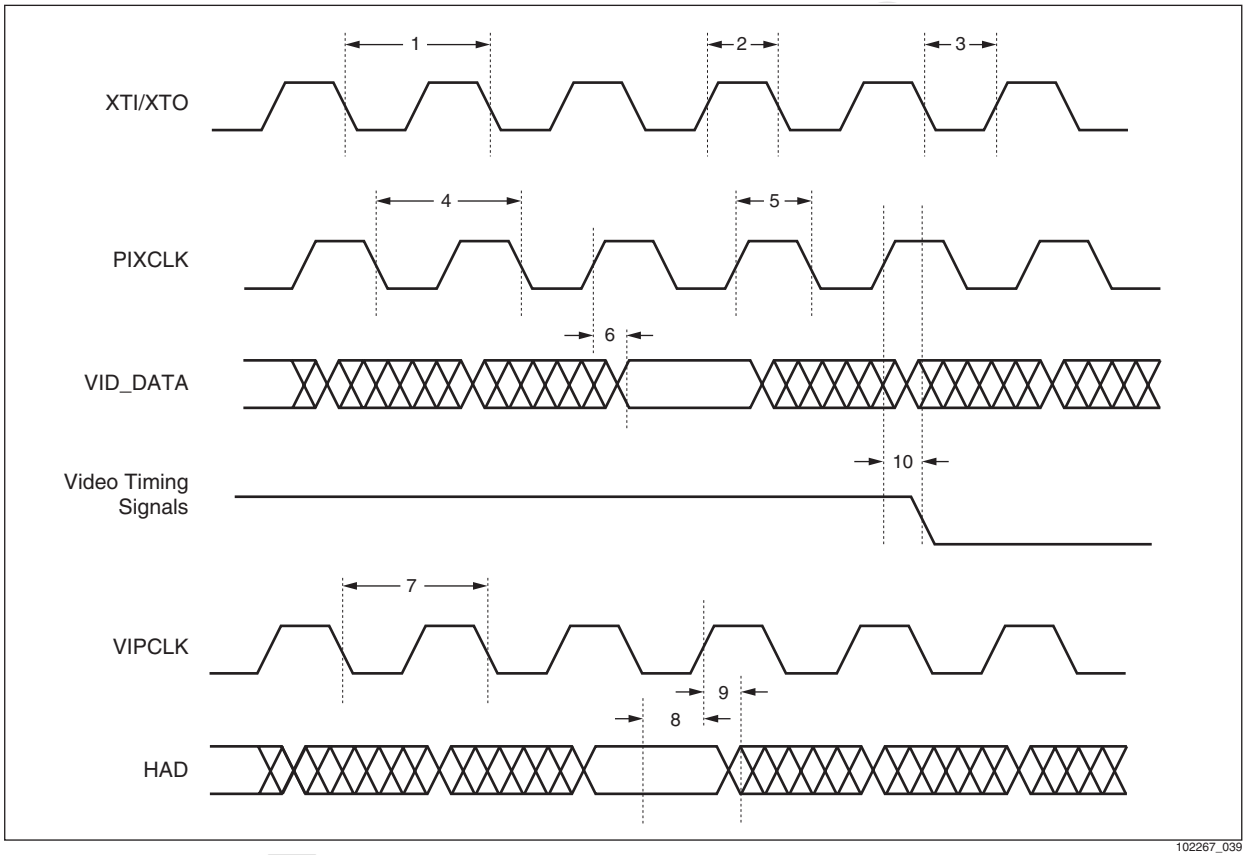

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Table 6-6. Power Supply Currents

Parameter	Symbol	Min	Typ	Max	Units
ITU-R BT.656 Mode					
Analog Current	IAA	—	105	115	mA
Digital Core Current	IDD	—	140	170	mA
Digital I/O Current	IDDO	—	20	50	mA
NTSC Square Pixel Mode					
Analog Current	IAA	—	105	115	mA
Digital Core Current	IDD	—	120	160	mA
Digital I/O Current	IDDO	—	10	47	mA
PAL/SECAM Square Pixel Mode					
Analog Current	IAA	—	105	115	mA
Digital Core Current	IDD	—	150	200	mA
Digital I/O Current	IDDO	—	25	60	mA
SLEEP Mode					
Analog Current	IAA	—	6	10	mA
Digital Core Current	IDD	—	2	11	mA
Digital I/O Current	IDDO	—	0	2	mA

GENERAL NOTE:
1. Typical values represent VAA, VDDO = 3.3 V and VDD = 1.2 V.
2. Maximum values represent VAA, VDDO = 3.465 V and VDD = 1.26 V.

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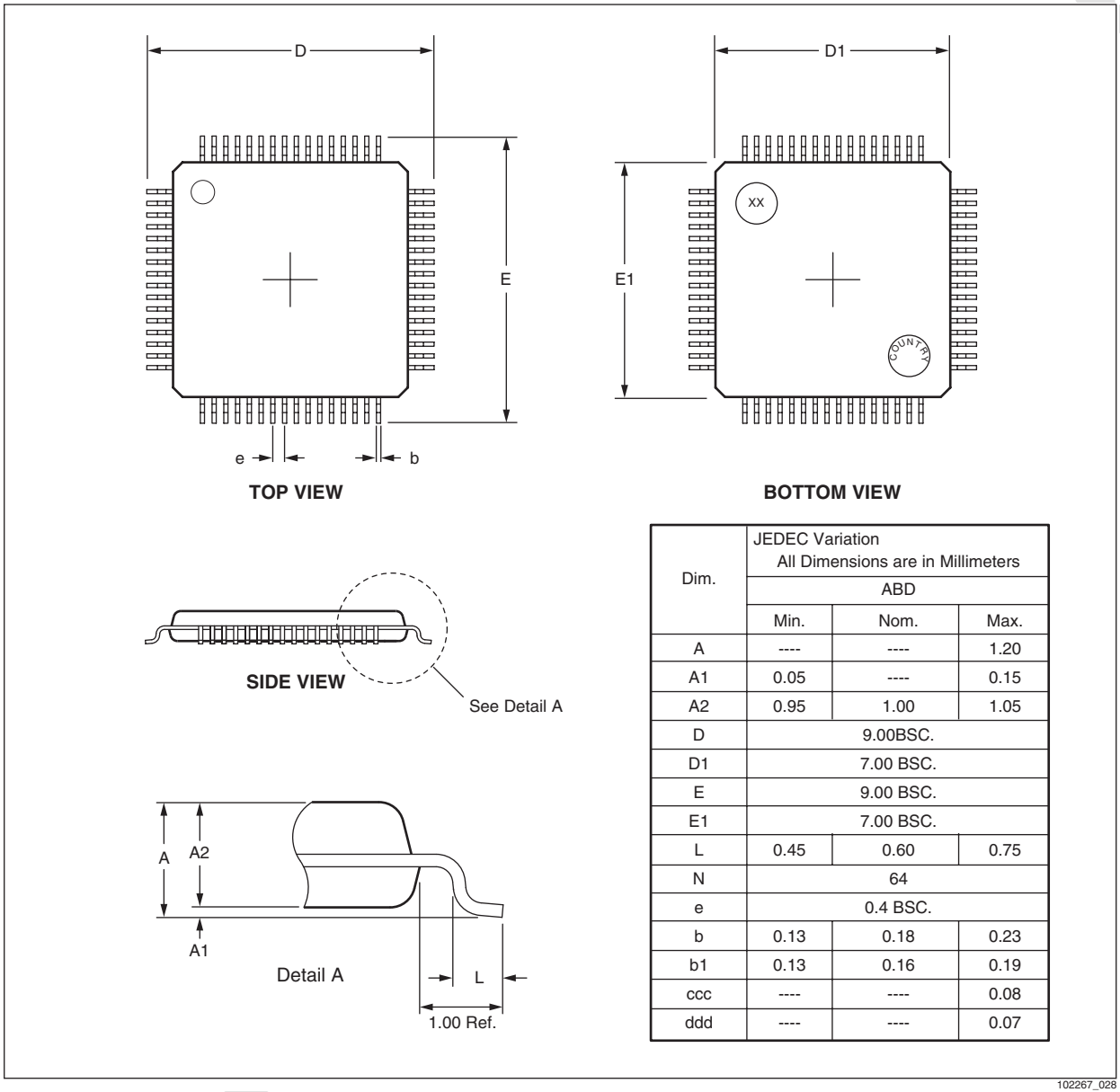
6.3 Mechanical

Figure 6-2. 64-Pin TQFP



Dim.	JEDEC Variation All Dimensions are in Millimeters		
	ABD		
	Min.	Nom.	Max.
A	----	----	1.20
A1	0.05	----	0.15
A2	0.95	1.00	1.05
D		9.00BSC.	
D1		7.00 BSC.	
E		9.00 BSC.	
E1		7.00 BSC.	
L	0.45	0.60	0.75
N		64	
e		0.4 BSC.	
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
ccc	----	----	0.08
ddd	----	----	0.07

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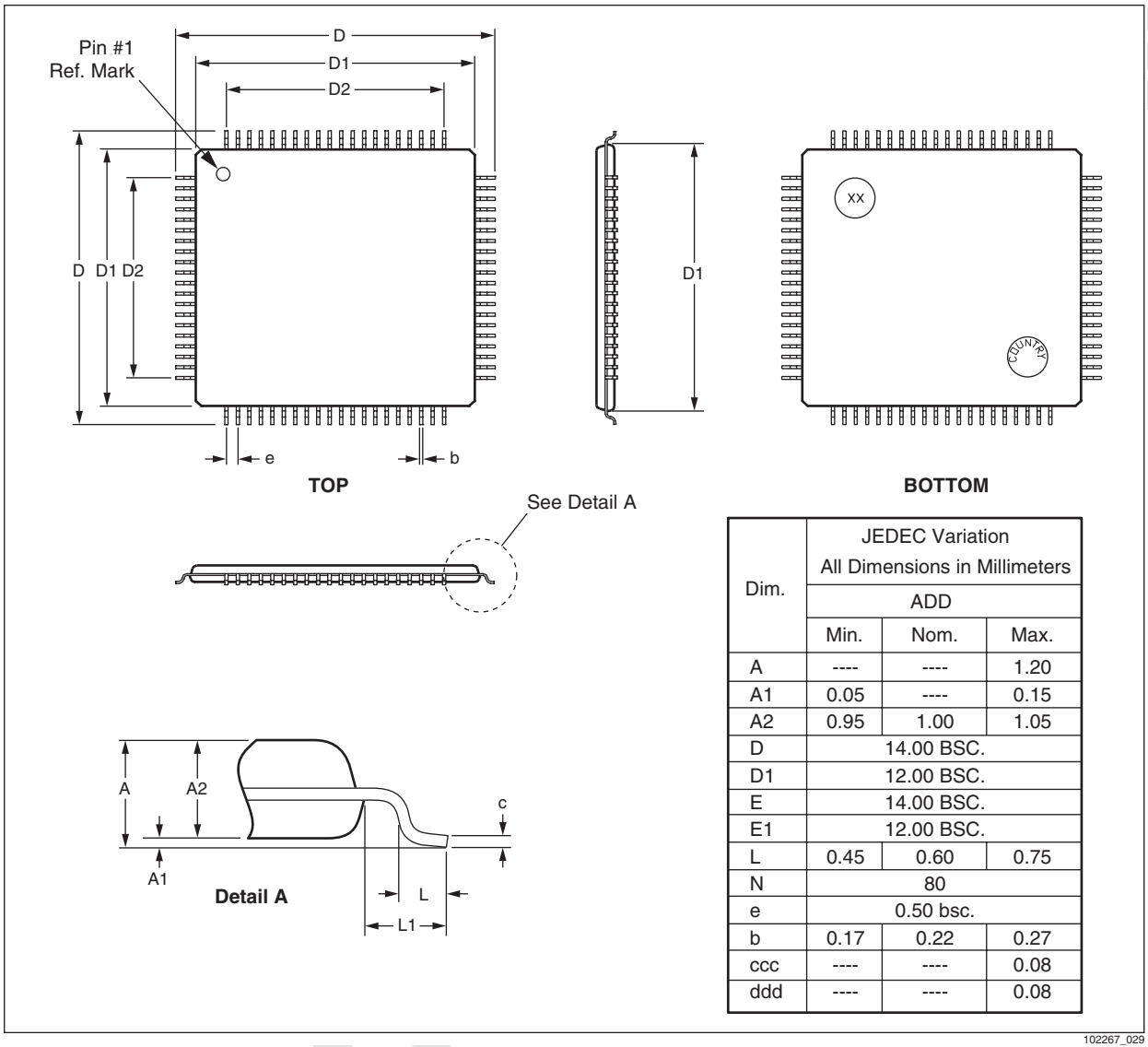
Figure 6-3. 80-Pin TQFP



Dim.	JEDEC Variation All Dimensions in Millimeters		
	ADD		
	Min.	Nom.	Max.
A	----	----	1.20
A1	0.05	----	0.15
A2	0.95	1.00	1.05
D		14.00 BSC.	
D1		12.00 BSC.	
E		14.00 BSC.	
E1		12.00 BSC.	
L	0.45	0.60	0.75
N		80	
e		0.50 bsc.	
b	0.17	0.22	0.27
ccc	----	----	0.08
ddd	----	----	0.08

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General Information:
U.S. and Canada: (888) 855-4562
International: (732) 345-7500
Headquarters – Red Bank
100 Schulz Drive
Red Bank, NJ 07701

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